MADHA
Expertise | Empathy | Excellence
ENGINEERING COLLEGE

Department of

Electronics & Communiction Engineering

QUESTION BANK

EC3451 -

LINEAR INTEGRATED CIRCUITS

IV SEMESTER

Regulation – 2021

MADHA ENGINEERING COLLEGE

DEPT. OF ELECTRONICS & COMMUNICATION ENGG.

SEM / YEAR : IV Sem / II Year Branch : E.C.E

EC3451 LINEAR INTEGRATED CIRCUITS

SYLLABUS

UNIT I :BASICS OF OPERATIONAL AMPLIFIERS 9

Current mirror and current sources, Current sources as active loads, Voltage sources, Voltage References, BJT Differential amplifier with active loads, Basic information about op-amps – Ideal Operational Amplifier - General operational amplifier stages -and internal circuit diagrams of IC 741, DC and AC performance characteristics, slew rate, Open and closed loop configurations.JFET operational amplifiers-LF155 and TL082

UNIT II APPLICATIONS OF OPERATIONAL AMPLIFIERS 9

Sign Changer, Scale Changer, Phase Shift Circuits, Voltage Follower, V-to-I and I-to-V converters, adder, subtractor, Instrumentation amplifier, Integrator, Differentiator, Logarithmic amplifier, Antilogarithmic amplifier, Comparators, Schmitt trigger, Precision rectifier, peak detector, clipper and clamper, Low-pass, high-pass and band-pass Butterworth filters.

UNIT III ANALOG MULTIPLIER AND PLL 9

Analog Multiplier using Emitter Coupled Transistor Pair - Gilbert Multiplier cell – Variable transconductance technique, analog multiplier ICs and their applications, Operation of the basic PLL, Closed loop analysis, Voltage controlled oscillator, Monolithic PLL IC 565, application of PLL for AM detection, FM detection, FSK modulation and demodulation and Frequency synthesizing and clock synchronization.

UNIT IV ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS 9

Analog and Digital Data Conversions, D/A converter – specifications - weighted resistor type, R-2R Ladder type, Voltage Mode and Current-Mode R-2R Ladder types - switches for D/A converters, high speed sample-and-hold circuits, A/D Converters – specifications - Flash type - Successive Approximation type - Single Slope type – Dual Slope type - A/D Converter using Voltage-to-Time Conversion - Over-sampling A/D Converters, sigma-delta converters.

UNIT V WAVEFORM GENERATORS AND SPECIAL FUNCTION ICS 9

Sine-wave generators, Multivibrators and Triangular wave generator, Saw-tooth wave generator, ICL8038 function generator, Timer IC 555, IC Voltage regulators – Three terminal fixed and adjustable voltage regulators - IC 723 general purpose regulator - Monolithic switching regulator,LowDrop-Out(LDO) Regulators- Switched capacitor filter IC MF10, Frequency to Voltage and Voltage to Frequency converters, Audio Power amplifier, Video Amplifier, Isolation Amplifier, Opto-couplers and fibre optic IC.

TEXT BOOKS:

1. D.Roy Choudhry, Shail Jain, “Linear Integrated Circuits”, New Age International Pvt. Ltd., 2018.
2. Sergio Franco, “Design with Operational Amplifiers and Analog Integrated Circuits”, 4th Edition, Tata Mc Graw-Hill, 2007.

REFERENCES:

1. Ramakant A. Gayakwad, “OP-AMP and Linear ICs”, 4th Edition, Prentice Hall / Pearson Edu, 2015.
2. Robert F.Coughlin, Frederick F.Driscoll, “Operational Amplifiers and Linear Integrated Circuits”, Sixth Edition, PHI, 2001.
3. B.S.Sonde, “System design using Integrated Circuits” , 2nd Edition, New Age Pub, 2001
4. Gray and Meyer, “Analysis and Design of Analog Integrated Circuits”, Wiley International, 2009.
5. William D.Stanley, “Operational Amplifiers with Linear Integrated Circuits”, Pearson Education, 2004.
6. S.Salivahanan & V.S. Kanchana Bhaskaran, “Linear Integrated Circuits”, TMH, 2016.

UNIT-I BASICS OF OPERATIONAL AMPLIFIERS

PART-A

1. State the significance of current mirror circuit **[April/May 2019]**

   A current mirror circuit is designed to copy a current through one active device by controlling the current in another active device of a circuit keeping the output current constant regardless of loading. The current mirrors are used to provide bias currents and active loads to circuits

2. Mention the application of LF155 **[April/May 2019]**
   - Precision high speed integrators
   - Fast D/A and A/D converters
   - High impedance buffers
   - Wideband low noise low drift amplifiers

3. Define differential mode gain **[Nov/Dec 2018]**

   It is the change in the difference between the two outputs divided by the change in the difference between the two inputs.

4. Enumerate any two blocks associated with op-amp schematic. **[April/May 2018]**

   Differential amplifier

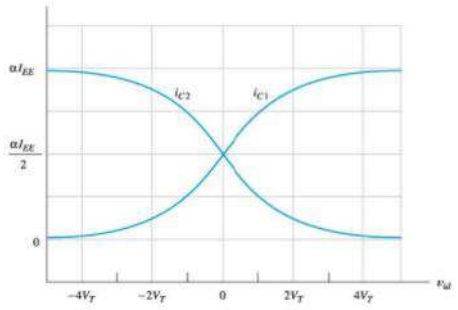
   Differential amplifier is to provide high gain to difference mode signal and cancel the common mode signal**.**

   Level translator

   As the op-amp is used to operate down to d.c no coupling capacitor is used. Because of direct coupling ,the d.c level rises from stage to stage. This increase in d.c level tends to shift the operating point of the next stage. This in turn limits the output swing and may distort the output signal. Therefore it becomes essential that the quiescent voltage of one stage is shifted before it is applied to the next stage.

5. What are the two methods can be used to produce voltage sources? **[April/May 2018]**
   - Using temperature compensation
   - Using avalanche diode.

6. Draw the dc transfer characteristics of a BJT differential amplifier and define differential mode input voltage **[Nov/Dec 2017]**



7. Write down the characteristics of ideal operational amplifier? **[Nov/Dec 2018] [April/May 2017][April/May 16]**

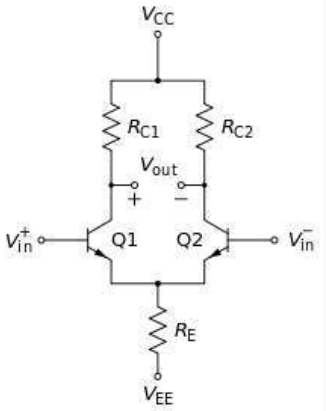
Open loop voltage gain, (AOL) = ∞
Input impedance (Ri) = ∞
Output impedance (Ro) = 0
Bandwidth (BW) = ∞
Zero offset Vo = 0, when V1 = V2 = 0

8. Why is the current mirror circuit used in differential amplifier stages? **[April/May 2017]**

The current mirror is a special case of constant current bias and the current mirror bias requires of constant current bias and therefore can be used to set up currents in differential amplifier stages

9. Draw the Internal Block diagram of Op – Amp (IC 741) **[Nov/Dec 2016]**

10. Draw the circuit diagram of a symmetrical emitter coupled differential amplifier. **[Nov/Dec 2016]**



11. Differentiate the ideal and practical characteristics of an op-amp **[May/June 2016]**

Characteristics	Ideal	Practical
Open loop voltage gain	∞	High
Input impedance (Ri)	∞	High
Output impedance (Ro)	0	Low
Bandwidth (BW)	∞	High
Zero offset	Vo = 0, when V1 = V2 = 0	Non zero

12. An operational amplifier has a slew rate of 4v/μs .Determine the maximum frequency of operation to produce distortion less output swing of 12V **[April/May 16]**

Frequency f = slewrate(SR) / 2ΠVm

= 4 / (2* Π*12)

= 0.013 Hz

13. What is the cause for slew rate and how it can be made faster? **[April/May 2015]**

There is a capacitor within or outside an op-amp to prevent oscillation. It is this capacitor which prevents the output voltage from responding immediately to a fast changing input .The slew rate can be made faster by having a higher current or a small compensating capacitor

14. Define input bias current and input offset current of an operational amplifier **[Nov/Dec 2015]**

Input bias current is the average value of the base current entering in to the i/p terminals of an opamp.Its typical value is 500nA

Input offset current is the algebraic difference between the current into the inverting and non-inverting terminals is referred to as input offset current I_{io}. Mathematically it is represented as

$I_{io} = |I_{B+} - I_{B-}|$

Where IB+ is the current into the non-inverting input terminals.

IB- is the current into the inverting input terminals.

15. Mention two advantages of active load over passive load in an operational amplifier **[Nov/Dec 2015]**

- Larger gain
- Larger Bandwidth

16. A differential amplifier has a differential voltage gain of 2000 and a common mode gain of 0.2.Determine the CMRR in dB **[April/May 2015]**

Given common mode gain A_{cm}=0.2

Difference mode gain A_{dm}=2000

CMRR= A_{dm}/ A_{cm}= 2000/0.2 =10000=10log10000=80dB

17. Define Slew rate and what causes slew rate? **[April/May 2015]**

The slew rate of an op amp or any amplifier circuit is the rate of change in the output voltage caused by a step change on the input.

There is usually a capacitor within or outside an op-amp to prevent oscillation. It is this capacitor which prevents the output voltage from responding immediately to a fast changing input

18. Define CMRR of an operational amplifier? **[May/June 2013]**

The common mode rejection ratio (CMRR) can be defined as the ratio of differential gain to common mode gain.

CMRR = |Ad/Ac|

19. Define integrated circuit.

An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors inductors and capacitors

20. What are the advantages of integrated circuits over discrete components?

i. Miniaturization and hence increased equipment density.
ii. Cost reduction due to batch processing.
iii. Increased system reliability due to the elimination of soldered joints.
iv. Improved functional performance.
v. Matched devices.
vi. Increased operating speeds.
vii. Reduction in power consumption

21. What are the disadvantages of integrated circuits?

- Inductors can’t be fabricated
- IC’s function at fairly low voltage
- They can handle only limited amount of power.
- It can’t withstand for rough handling and excessive heat

22. What is meant by monolithic IC

A monolithic integrated circuit (IC) is an electronic circuit that is built on a single semiconductor base material or single chip

23. What is current mirror?

The circuit in which the output current is forced to equal the input current is called as current mirror circuit. The current mirror makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively

independent of the collector voltage. In this the output current is a reflection or mirror of the reference current.

24. What are the two requirements to be met for a good current source?

A good current source must meet two requirements:

1. Output current I_O should not depend on β;
2. Output Resistance (RO) of the current source should be very high;

25. List the various methods of realizing high input resistance in a differential amplifier.

The various methods of realizing high input resistance in a differential amplifier circuits are

(i) Use of Darlington pair
(ii) Use of FET
(iii) Use of swamping resistors.

26. What is active load? Where it is used and why?

In circuit design, an active load is a circuit component made up of active devices, such as transistors, intended to present a high small-signal impedance yet not requiring a large DC voltage drop, as would occur if a large resistor were used instead. Such large AC load impedances may be desirable, for example, to increase the AC gain of some types of amplifier.

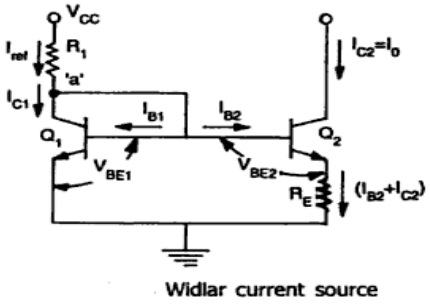
Most commonly the active load is the output part of a current mirror and is represented in an idealized manner as a current source. Usually, it is only a constant-current resistor that is a part of the whole current source including a constant voltage source as well

27. Explain the limitation of current mirror circuits?

For low value of current source, the value of resistance R should be high which can't be fabricated economically in an Ic circuits.Widlar current source is suitable for low value.

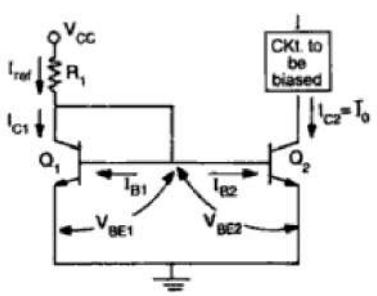
28. Draw the circuit of a Widlar current source and write the exp for its output current. (May 2007)

Ic1 = (β/β+1) Iref
Iref = VCC –VBE / R1 For β>>1,
Ic1 = Iref

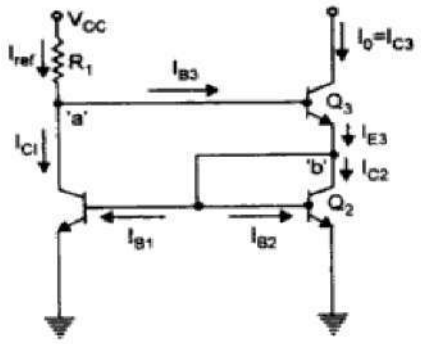


Widlar current source

29. Draw the basic current mirror circuit.



30. Draw the Wilson current source.



31. Define Thermal Drift.

The change in bias current ,offset voltage and offset voltage for each degree Celsius change in temperature .The offset current drift is expressed in A/^{o}c and offset voltage drift in V/ ^{o}c

32. What is an operational amplifier?

The operational amplifier is a multi-terminal device, which is quite complex internally. An operational amplifier is a direct coupled high gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and an output stage. An operational amplifier is available as a single integrated circuit package. It is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for computing such mathematical functions.

33. What are the AC characteristics of an op-amp?

- Frequency response
- Slew rate

34. What are the DC characteristics of an op-amp? Give the typical values for an IC741?

1. Input bias current: 500 nA
2. Input offset current: 200 nA
3. Input offset voltage: 6mV
4. Thermal drift

35. When does the op-amp behave as a switch?

When op-amp is operating in open loop mode it acts as a switch. Consider two signals V1 and V2 applied at both inverting and non-inverting terminal respectively. Since the gain of the op-amp is infinite, the output V0 is either at its positive saturation voltage (+Vsat) or negative saturation voltage (-Vsat) as V1 > V2 or V2 – V1 respectively. Therefore amplifier acts as a switch.

36. In response to square wave input, the output of an op-amp changed from –3V to +3V over a time interval of 0.25μs. Determine the slew rate of the op-amp.

Slew rate = dvc/dt / max
= ΔVo/Δt
= 6V / 0.25μS
= 1.5 V/μS

37. Define supply voltage rejection ratio (SVRR)

The change in OPAMP's input offset voltage due to variations in supply voltage is called the supply voltage rejection ratio. It is also called Power Supply Rejection Ratio (PSRR) or Power Supply Sensitivity (PSS)

38. Define input offset voltage

The input offset voltage is a parameter defining the differential DC voltage required between the inputs of an amplifier, especially an operational amplifier (op-amp), to make the output zero

39. Define Frequency Response

Frequency response is the quantitative measure of the output spectrum of a system or device in response to a stimulus, and is used to characterize the dynamics of the system. It is a measure of magnitude and phase of the output as a function of frequency, in comparison to the input.

40. Define unity gain bandwidth of a Op-Amp

The GBWP (Gain Band Width Product) of an operational amplifier is 1 MHz, it means that the gain of the device falls to unity at 1 MHz. Hence, when the device is wired for unity gain, it will work up to 1 MHz (GBWP = gain × bandwidth, therefore if BW = 1 MHz, then gain = 1) without excessively distorting the signal.

41. Why IC 741 is not used for high frequency applications?

IC741 has a low slew rate because of the predominance of capacitance present in the circuit at higher frequencies. As frequency increases the output gets distorted due to limited slew rate.

42. Why do we use R_{comp} resistor?

R_{comp} is used to compensate for input bias current,which is added between non inverting input terminal of op-amp and ground.

43. What is the gain cross over and phase cross over frequencies?

The gain crossover frequency, wgc, is the frequency where the amplittude ratio is 1, or when log modulus is equal to 0.

The phase crossover frequency, wpc , is the frequency where phase shift is equal to -180o.

44. State loading effect?

Load effect is a power supply specification (also known as load regulation) that describes how well the power supply can maintain its steady-state output setting when the load changes

45. What are the applications of current sources?

The Current sources are used as the emitter resistance in differential amplifier to increase CMRR and as an active load to provide high a.c resistance without disturbing the d.c. conditions.

46. State the various blocks of IC op-amp

- Input stage
- Intermediate stage
- Level shifting stage
- Output stage

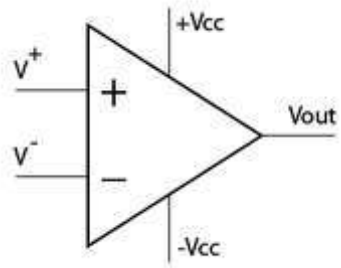
47. Why frequency compensation is required?

The op-amp with single break frequency is inherently stable. Practically op-amp has more than one break frequencies. It is necessary to provide compensation so that only one break over frequency exist duo to which phase shift of op-amp cannot increase beyond -90^o .Hence there is no chance that op-amp phase shift becomes -135^o and phase margin always remains more than $+45^o$.Hence op-amp becomes inherently stable.

48. List the methods used to provide external frequency compensation.

- Dominant pole compensation
- pole zero compensation
- Feed forward compensation

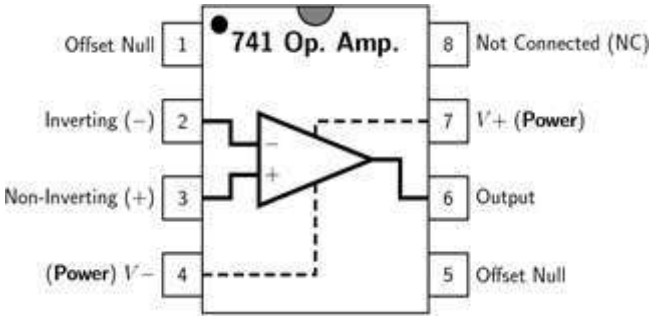
49. Draw the op-amp symbol and state its important terminals.



Important terminals are

- Inverting input
- Non inverting input
- Positive supply
- Negative supply
- output

50. Draw the pin diagram of IC741



51. Why op-amp in open loop is not used for most of the applications?

The open loop gain of op-amp is very large and hence the output saturates at supply voltage which are of the order of few volts. Thus linear operation of op-amp is possible only for very small range of input voltage of the order of few millivolts.This is not sufficient for most of the practical applications. Hence op-amp in open loop is not used for most of the applications

52. Define current mirror with magnification.

A current mirror circuit in which the ratio of the biasing currents in two transistors are fixed , is called current mirror with magnification.

.

PART –B&C

1. (i) Draw the transfer characteristics of an operational amplifier and explain its linear and non linear operations. (8) **[Nov/Dec 2017] [Nov/Dec 2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 55]

(ii) Discuss the operation of BJT differential amplifier with active loads.(5) **[Nov/Dec 2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 77]

2. (i) Present the inverting and non inverting amplifier circuits of an op-amp in closed loop configuration. Derive the expressions for the closed loop gain in these circuits. (9) **[Nov/Dec 2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 43]

(ii) Define slew rate. In what way does it possess impact on the performance of an op-amp circuit (4) **[Nov/Dec 2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 123]

3. Discuss about the principle of operation of differential amplifier using BJT. **[April/May 2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 53]

4. Explain about Ideal Op-Amp in detail with suitable diagrams. **[April/May 2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 41]

5. With a neat diagram Explain the input side of the internal circuit diagram of IC741 **[Nov/Dec2015] [Nov/Dec 2017]**

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 96]

6. (i) What is the input and output voltage and current offsets? How are they compensated? **[April/May 2017]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 108]

(ii) With neat diagram derive the AC performance close loop characteristics of Op-Amp to discuss on the circuit Bandwidth, Frequency response and slew rate **[April/May 2017]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 111]

7. i) With a schematic diagram,explain the effect of R_E on CMRR in differential amplifier **[April/May 2016]**

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 63].

ii) Discuss about the methods to improve CMRR **[April/May 2016]**

8. (i) With simple schematic of differential amplifier explain the function of Operational Amplifier (8) **[April/May 2015]**

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 63]

(ii) Briefly Explain about constant current source(8) **[April/May2015]**

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 73]

9. (i) Briefly explain the techniques used for frequency compensation (12) **[April/May2015]**

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 135]

(ii) How do the open loop gain and the closed loop gain of an op-amp differ? (4) **[April/May2015]**

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 225]

10. What is the need for frequency compensation in an OPAMP? With a suitable illustration, explain the pole-zero frequency compensation technique. **[Nov/dec 15][April/May 2017]**

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 135]

11. Explain different voltage reference circuit in detail

[Ref .S.Salivahanan & V S Kanchana Baskaran, "Linear Integrated Circuits (Second Edition)", Page 60]

12. Explain different voltage sources in detail

[Ref .S.Salivahanan & V S Kanchana Baskaran, "Linear Integrated Circuits (Second Edition)", Page 57]

13. Draw the circuit of basic current mirror and explain its operation. Also discuss about how current ratio can be improved in the basic current mirror.Sketch the improved circuit and explain

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 73]

14. (i) Define and explain slew rate. What is full power bandwidth? Also explain the method adopted to improve slew rate

[Ref .Roy Choudhry, Shail B.Jain, “Linear Integrated Circuits (Second Edition)”, Page 140]

(ii) Define output off set voltage. Explain methods to nullify offset voltage

[Ref .Roy Choudhry, Shail B.Jain, “Linear Integrated Circuits (Second Edition)”, Page 123]

[Ref .Roy Choudhry, Shail B.Jain, “Linear Integrated Circuits (Second Edition)”, Page 71]

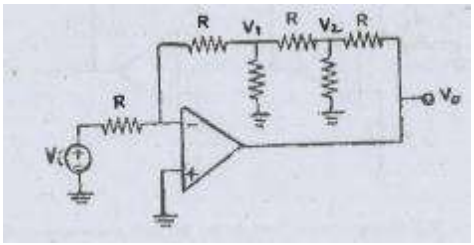
15. Explain in detail wilson current source and widlar current source and derive necessary equations

[Ref .Roy Choudhry, Shail B.Jain, “Linear Integrated Circuits (Second Edition)”, Page 75]

UNIT II- APPLICATIONS OF OPERATIONAL AMPLIFIERS

Part-A

1. Find the gain V_o/V_i of the circuit **[April/May 2019]**



Applying KCL at inverting terminal

$$\frac{0-V_1}{R} = \frac{V_i-0}{R}$$

V_1=-V_i

Applying KCL at node 1

$$\frac{0-V_1}{R} = \frac{V_1}{R} + \frac{V_1-V_2}{R}$$

$$V_2 = -3v$$

Applying KCL at node 2

$$\frac{V_1-V_2}{R} = \frac{V_2}{R} + \frac{V_2-V_0}{R}$$

$$8V_i = -V_0$$

$$\frac{V_0}{V_i} = -8$$

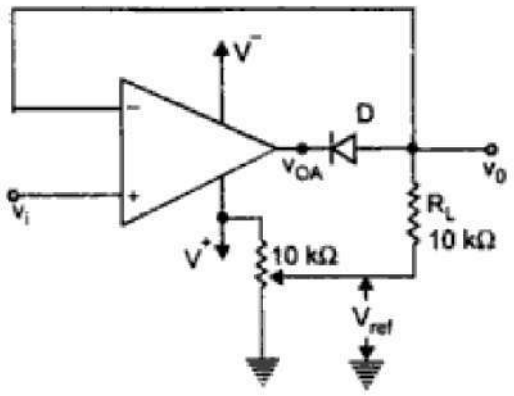
2. How does a zero crossing detector work **[April/May 2019]**

Zero crossing detector is one type of voltage comparator used to detect a sine waveform transition from positive and negative that coincides when the input crosses the zero voltage condition

3. How does operational amplifier work as an integrator **[Nov/Dec 2018]**

By replacing this feedback resistance with a capacitor we now have an RC Network connected across the operational amplifiers feedback path producing another type of operational amplifier circuit called an Op-amp Integrator

4. Draw the circuit of clipper using op-amp **[Nov/Dec 2018]**



5. What is the function of a phase shift circuit? **[April/May 2018]**

A phase shifter circuit is one that shifts the relative phase of an input AC signal

6. Write the other name for clipper circuit. **[April/May 2018]**

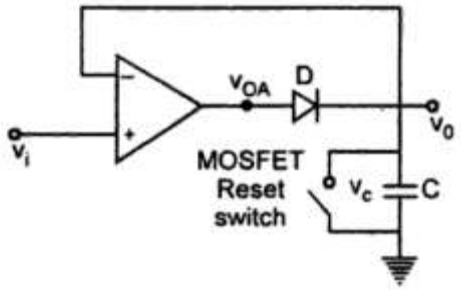
Other name of clipper circuit is limiter circuit

7. State the limitations of an ideal integrator. **[Nov/Dec 2017]**

- Bandwidth is very small and used for only small range of input frequencies.

- For dc input (f = 0), reactance of capacitance, Xc is infinite. Because of this op-amp goes into open loop configuration. In open loop configuration the gain is infinite and hence the small input offset voltages are also amplified and appears at output as error

8. How will you realize a peak detector using a precision rectifier? **[Nov/Dec 2017]**



9. What is the need for converting a first order filter into a second order filter?

[April/May 2017]

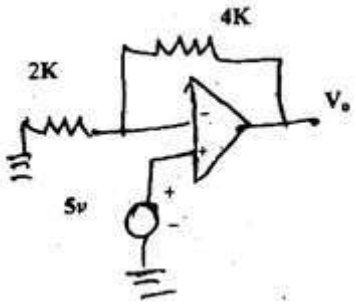
A first order active filter has one pole which is defined by a capacitor/resistor pair. A second order filter has two capacitors and resistors. This gives the filters frequency response a steeper slope as it transitions from pass band to stop band

10. How is the current characteristic of a PN junction employed in a Log amplifier?

[April/May 2017]

The voltage across the diode will be always proportional to the log of the current through it and when a diode is placed in the feedback path of an op-amp in inverting mode, the output voltage will be proportional to the negative log of the input current. Since the input current is proportional to the input voltage, we can say that the output voltage will be proportional to the negative log of the input voltage

11. For the op-amp shown in figure determine the voltage gain **[Nov/Dec 2016]**

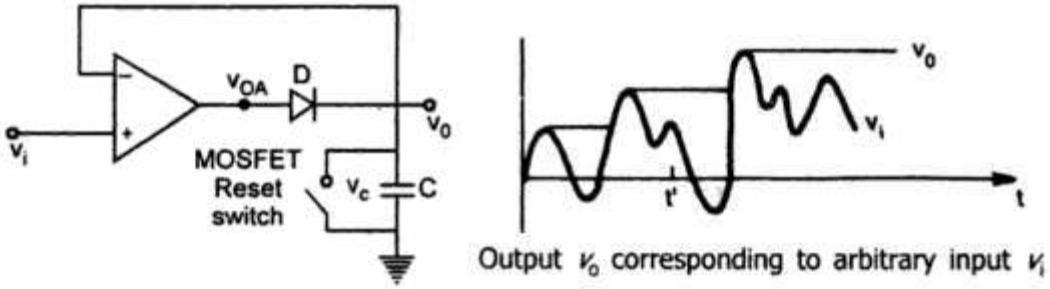


The given circuit is inverting amplifier

For inverting amplifier voltage gain $= -\frac{R_f}{R_i}$

$$= -\frac{4k}{2k} = -2$$

12. Draw the circuit diagram of a peak detector with waveforms. **[Nov/Dec 2016]**



13. Give any four applications of comparators. **[May/June 2016]**
    - Zero crossing detector
    - Window detector
    - Time marker generator
    - Phase meter
14. What is hysteresis and mention the purpose of hysteresis in a comparator?

[April/May 2015]

Hysteresis is the time-based dependence of a system's output on present and past inputs. The dependence arises because the history affects the value of an internal state. To predict its future outputs, either its internal state or its history must be known.

In comparator hysteresis has the effect of separating the up-going and down-going switching points so that, once a transition has started, the input must undergo a significant reversal before the reverse transition can occur.

15. What is the difference between normal rectifier and precision rectifier?

[April/May 2015]

A simple rectifier circuit uses a diode. The input voltage has to exceed the turn-on voltage (0.6V for ordinary Si diode) before rectification is achieved.

A precision rectifier is an active circuit using an opamp and a diode in the feedback loop. This overcomes the turn-on "knee" voltage

16. Plot the transfer characteristics of the circuit shown in figure 2 .The op-amp saturates at +/-12V **[Nov/Dec 2015]**

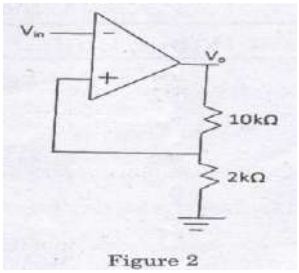
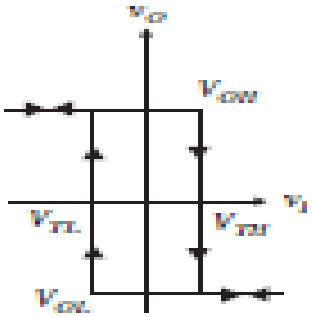


Figure 2



17. Determine the output voltage for the circuit shown in figure 1 when
    (a) Vin=-2V
    (b) Vin=3V **[Nov/Dec 2015]**

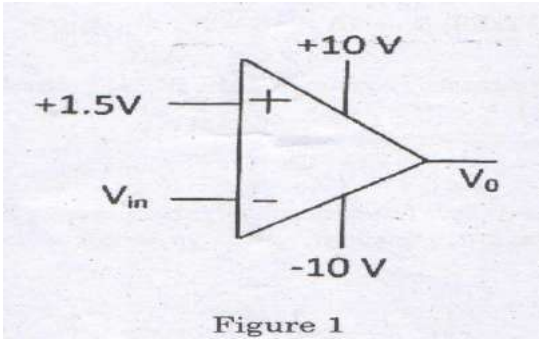


Figure 1

This is basic comparator circuit

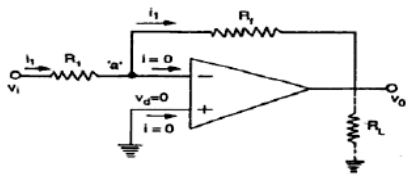
when Vin=-2V then Vo=10V

When Vin =3V then Vo=-10V

18. Define inverting amplifier and draw the circuit?

The input v_{in} is given to the second pin of op-amp through the input resistanceR_1 the feedback resistor R_f connects the output and input pin and the output is always reversed or inverted.

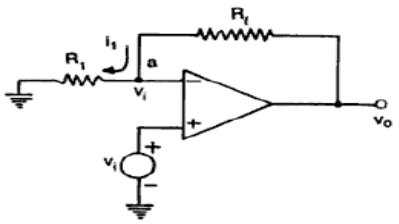
$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1}$$



(a) Inverting amplifier

19. Define non-inverting amplifier and draw the circuit?

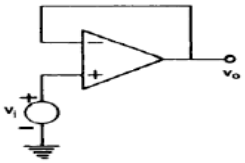
The input v_{in} is given to the non-inverting terminal pin 3 of op-amp.The input resistor R1 & the feedback resistor R_f are connected to the inverting input only ,the input pin and the output is always same phase.



(a) Non-inverting amplifier

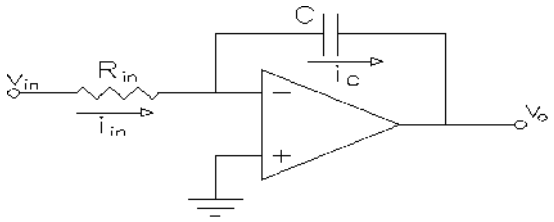
20. What is meant by voltage follower?

In the non-inverting amplifier, if R_f=0 and R1=∞ then the modified circuit is called voltage follower or unity gain amplifier.



Voltage follower

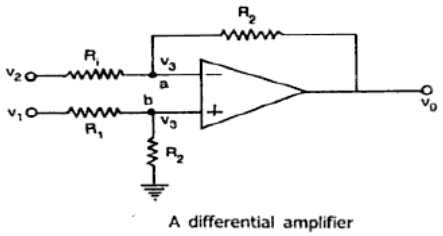
21. Draw the circuit diagram of an op-amp integrator. Mention its applications.



Application:

1. It is generally used in analog computer and analog to digital converter.
2. It also used in wave shaping circuits

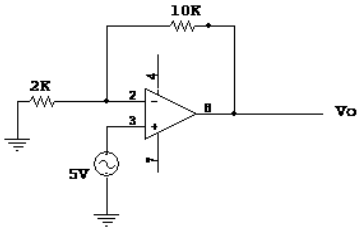
22. Draw the circuit diagram of an op-amp differential amplifier. Mention its o/p equation.



A differential amplifier

$$v_o = \frac{R_2}{R_1}(v_1 - v_2)$$

23. For the op-amp shown in figure, determine the voltage gain.



Vo / Vin = 1+Rf / R1

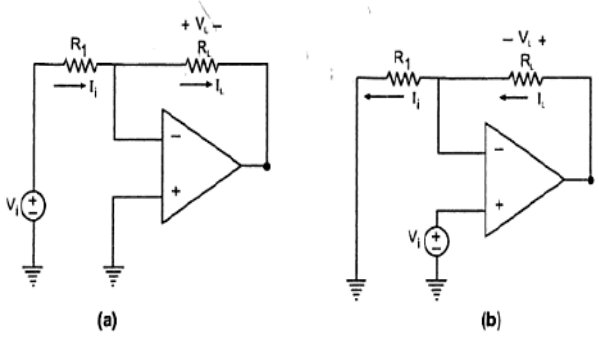
= 1+ 10K / 2K

= 6

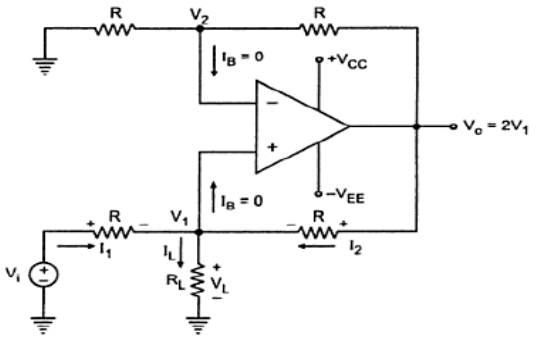
24. Explain the voltage to current convertor

Voltage to current convertor converts an input signal voltage to a proportional output current. According to the connection of load there are two types of voltage to current convertor

1. Floating type
2. Grounded type

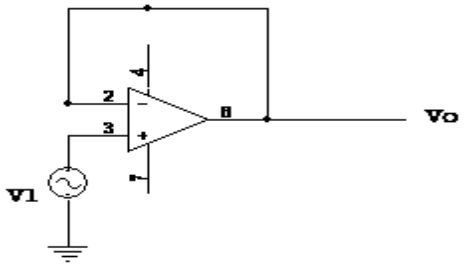


Floating load V-I converters



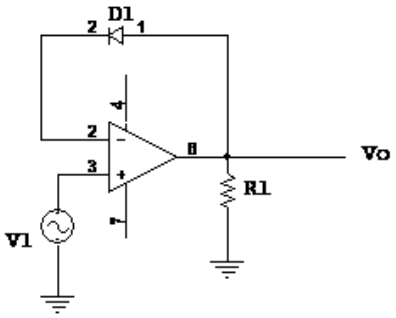
Voltage to current converter with grounded load

25. Draw the circuit of a voltage follower using op-amp and prove that its gain is exactly equal to unity.



Vo / Vin = 1+Rf / R1; Vo / Vin = 1+ 0; Vo / Vin = 1.

26. An ac signal has got a magnitude of 0.1 volt peak to peak. Suggest a suitable half wave rectifier for this signal.



27. Derive the expression for voltage gain of an inverting operational amplifier?

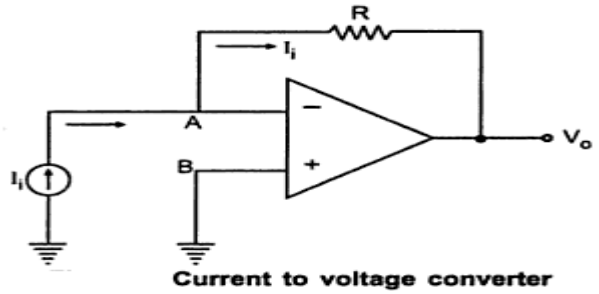
ACL = Vo/Vi = -Rf / R1

28. Mention two linear and two non- linear operations performed by an operational amplifier?

Linear operations: Adder, Subtractor, Voltage to current converter, Current to voltage converter, Instrumentation amplifier, Analog computation, and Power amplifier.

Non-linear operations: Rectifier, Peak detector, Clipper, Clamper, Sample and hold circuits, Log and antilog amplifier and Multiplier.

29. Draw the circuit of current to voltage convertor?



Current to voltage converter

30. Mention two application of Schmitt trigger?

- For eliminating comparator chatter.
- In ON/ OFF controller.
- Square wave generation

31. Mention the characteristics of Instrumentation amplifier?

- High gain
- High CMRR
- High gain stability
- Low dc offset
- Low output impedance
- Low power loss
- High input impedance

32. State the disadvantages of passive filters?

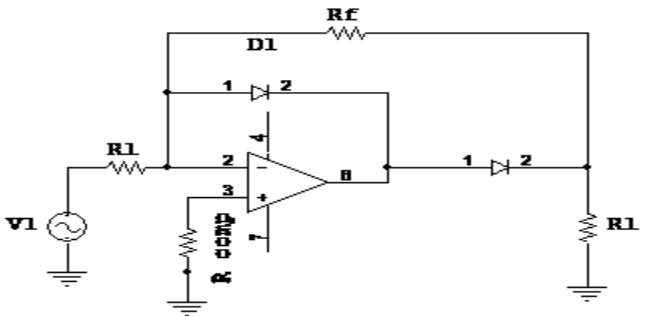
At audio frequencies inductors becomes problematic, as the inductors become large, heavy and expensive. For low frequency application, more number of turns of wire must be used which in turn adds to the series resistance degrading inductors performance.

33. What is Precision rectifier?

It is a rectifier circuit which utilities precision diode instead of usual diodes for rectification purpose in order to operate them for cut-in voltages in the order of microvolt.

34. Define precision half wave rectifier with diagram?

It is defined as a circuit, which utilizes two precision diodes instead of usual diodes for rectification purpose in order to operate them for, cut in voltages in the order of micro volts.



35. What are the main drawbacks of ideal differentiator?

At high frequency, differentiators may become unstable and break into oscillation. The input impedance i.e. (1/ωC1) decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

36. What are the steps to be followed while designing a good differentiator?

Choose f_a equal to highest frequency of the input signal. Assume a practical value of C1 (<1μF) and then calculate Rf.

Choose $f_b=10f_a$ (Say). Now calculate the values of R1 and C1.

R1C1 = RfCf.

37. What are the main drawbacks of ideal integrator circuit?

At low frequencies such as dc ($\omega \approx 0$) the gain becomes infinite.

When the op-amp saturates i.e. the capacitor is fully charged it behaves like an open circuit.

38. Give the output voltage when V_i is positive and negative in a precision diode.

When Vi is positive, diode D1 conducts causing V0 to negative by one diode drop (Vr =0.6v). Hence, diode D2 is reverse biased. The output voltage V0 is zero.

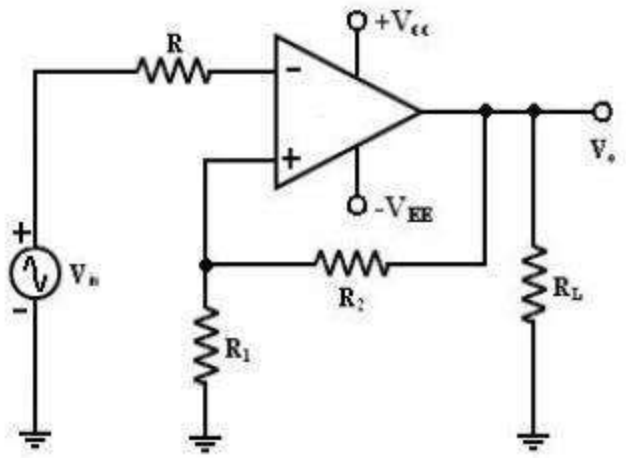
When Vi is negative ie Vi < 0, diode D2 conducts D1 is off. The negative input Vi forces the op-amp circuit VON positive and causes D2 to conduct. Output V_o becomes positive.

39. Give an application of an Inverting Amplifier.

1.Sign Changer

2. Scale changer

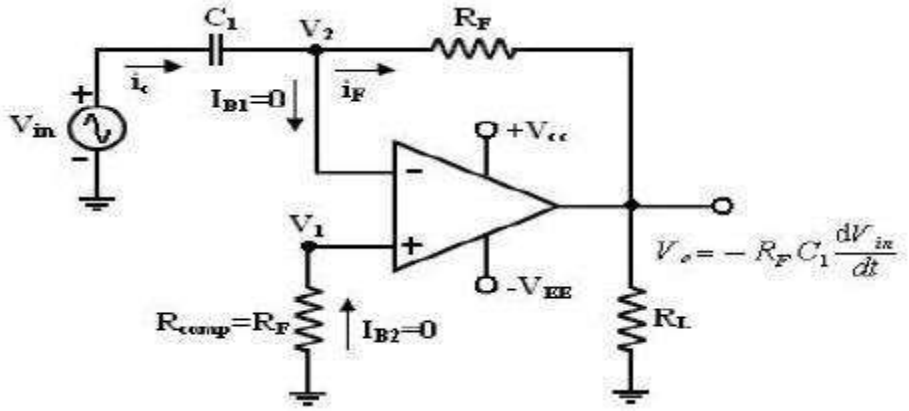
40. Draw the circuit diagram of a schmitt trigger



41. What is a filter?

Filter is a frequency selective circuit that passes signal of specified band of frequencies and attenuates the signals of frequencies outside the band

42. Draw the circuit diagram of differentiators and give its output equation

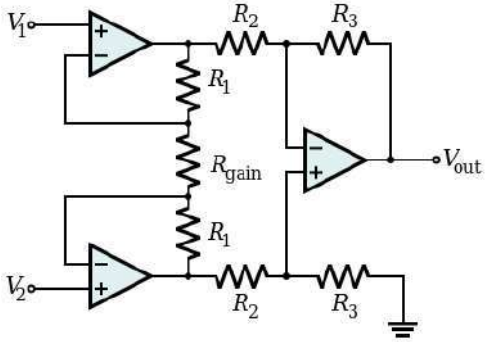


43. State the applications of V-I converter
    - Low voltage d.c voltmeter
    - Low voltage a.c voltmeter
    - Diode tester
    - Zener diode tester
44. State the applications of current to voltage converter
    - Photodiode detector
    - PhotoFET detector
45. List the applications of differentiator circuit.
    - In the wave shaping circuits
    - To detect high frequency components in the input.
    - As a rate of change detector in the FM demodulator
46. List various applications of comparator.
    - Zero crossing detector
    - Window detector
    - Level detector
47. What is a zero crossing detector?

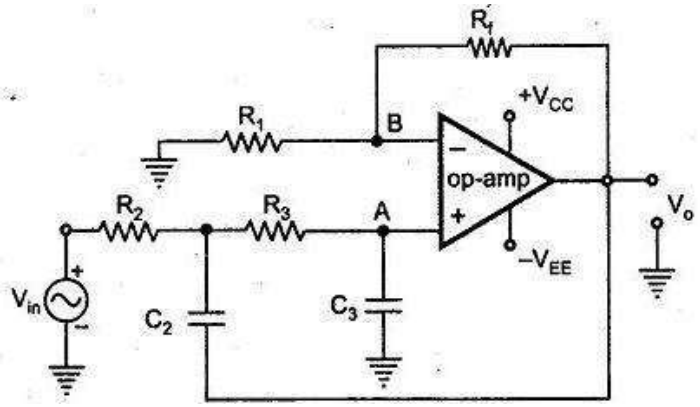
    A circuit which detects the crossing of zero level by the input signal is called a zero crossing detector. An op-amp comparator is used as a zero crossing detector.
48. When inverting amplifier is called phase inverter?

    When the gain of inverting amplifier is unity and is used to change the phase of the input to produce the output then it is called phase inverter.
49. State any four applications of instrumentation amplifier,
    - Temperature controller
    - Data acquisition system
    - Light intensity meter
    - Analog weight scale
50. Why temperature compensation is required for log amplifiers?

    The reverse saturation current I_o for the diode changes with temperature and it doubles for every ten degree celicius rise in the temperature. Similarly the emitter saturation current varies significantly from one transistor to other and also with temperature. Hence it is very difficult to set the term V_{ref} for the circuit. The term V_T which is KT also changes with temperature, which appears in the final equations. Hence temperature affects the performance and accuracy of the basic logarithmic amplifier circuit. Hence it is must to provide some sort of temperature compensation to reduce the errors.
51. Draw the circuit diagram of 3 op-amp instrumentation amplifier.



52. Draw the circuit diagram of second order active low pass Butterworth filter



PART –B&C

1. (i) With suitable circuit diagram ,explain the operating principle of an instrumentation amplifier and derive its gain.(7) **[Nov/Dec 2018]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 141]
   (ii) Design a second order butterworth low-pass filter having upper cut-off frequency of 2.1961 kHz (6) **[Nov/Dec 2018]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 269]
2. (i) Design a clipper circuit for a clipping level of +0.83V,given an input sine wave signal of 0.3V peak. Assume the gain of the amplifier is 9 and it has an input resistance of 2.2k-ohm connected.(5) **[Nov/Dec 2018]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 151]
   (ii) Draw the operational diagram and explain the working principle of antilogarithmic amplifier and Schmitt trigger.(8) **[Nov/Dec 2018]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 157]
3. i) Describe about voltage follower circuit.(7) **[April/May 2018]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 49]
   ii) Write short notes on subtractor circuit(6) **[April/May 2018]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 137]
4. With a neat diagram Explain about V-I conveter. **[April/May 2018]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 146]
5. (i) For performing differentiation in an operational amplifier, integrator is preferred to differentiator-Explain **[Nov/Dec 2017]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 168]
   (ii) What is instrumentation amplifier? Draw a system whose gain is controlled by a variable resistance **[Nov/Dec 2017]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 141 &142]
6. Explain the operation of differentiator and integrator with relevant waveforms and equations **[April/May 2017]**
7. (i) Design a differentiator to produce an output of 6 V when the input changes by 2V in 40 micro seconds. (5) **[Nov/Dec 2018]**
   [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 170]
   (ii) Write short notes on Clipper and clamper circuits(8) **[April /May 2017]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 151]
8. With a neat block diagram explain the stages for developing the signal analysis circuits required for an instrumentation module of say a vibration sensor data using

instrumentation amplifier, waveshaper, and comparator for ADC using OPAMP and required components

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 141]

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 186]

9. i) Draw the circuit of a second order Butterworth active low pass filter and derive its transfer function. **[April/May 2016]**

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 293]

ii) Design a second order active low pass filter for a cut-off frequency of 1 KHz. **[April/May 2016]**

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 293]

10. Explain the working of 3 op-amp Instrumentation amplifier? **[April/May 2018][[April/May2016]**

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 161]

11. i) Briefly explain the working principle of Schmitt trigger.

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 237]

ii) Design a wide band pass filter having f_L=400 Hz f_H=2kHz and pass band gain of 4.Find the value of Q of the filter **[April/May 2015]**

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 306]

12. With a circuit diagram discuss the following applications of op-amp.
    a. Voltage to current converter.
    b. Precision rectifier.

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 166 &169]

13. Explain the working of Log amplifier and antilog amplifier? [May/June 14]

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 178]

14. (i) Explain the operation of current to voltage converter

[Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 147]

(ii) Differentiate between low pass ,high pass ,band pass and band reject filter.Sketch the frequency plot

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 263]

15. With neat diagram derive the expression for transfer function of a narrow band pass filter and find the resonant frequency factor and Bandwidth

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 272]

UNIT – III-ANALOG MULTIPLIER AND PLL

PART-A

1. What is Gilbert multiplier cell? **[April/May 2018] [April/May 2019]**

   A circuit which uses emitter couples pair in series with cross coupled emitter coupled pairs is called Gilbert Cell.

2. List the basic building blocks of PLL. **[April/May 2019]**
   - Phase detector
   - Low pass filter
   - Error amplifier
   - Voltage controlled Oscillator

3. Mention the significance of Gilbert multiplier Cell. **[Nov/Dec 2018]**

   The Gilbert cell mixer or Gilbert cell multiplier is a form of RF mixer circuit that is widely used in integrated circuits. Not only does the Gilbert cell mixer lend itself to integrated circuit technology, but it is able to provide a high level of performance. Gilbert cells are often referred to as four-quadrant multipliers

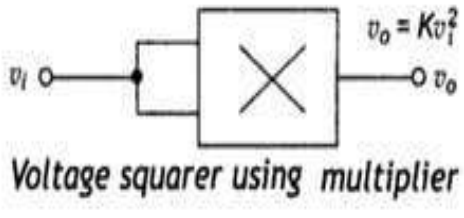
4. State various applications of phase locked loop. **[Nov/Dec 2018]**
   - Frequency multiplication and division
   - Frequency translation.
   - AM detection.
   - FM demodulation

4. (a) State any two terminologies associated with multiplier characteristics **[April/May 2018]**
   - Two Quadrant
   - Four Quadrant

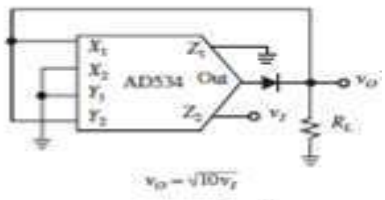
5. Define capture range of a PLL? **[Nov/Dec 2017]**

   The range of frequency over which the PLL can acquire lock with an input signal is called capture range. The PLL cannot acquire a signal outside the capture range, but once captured, it will hold on till the signal frequency goes beyond the lock-in range, larger capture range is required.

6. How are square root and squarer of a signal obtained with multiplier Circuit ? **[April/May 2015] [April/May 2017]**



Voltage squarer using multiplier



Square root circuit using multiplier

7. How is frequency stability obtained in a PLL by use of a VCO? **[April/May 2017]**

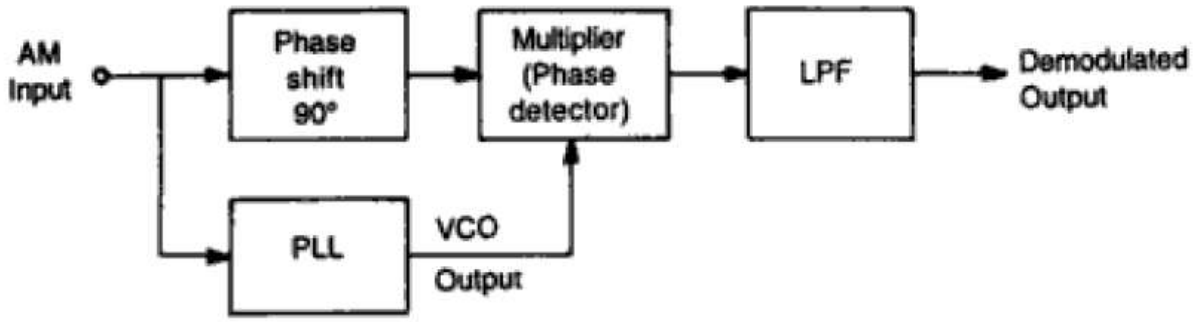
   A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillation can be controlled by an externally applied voltage. It provides the linear relationship between the applied voltage and the oscillation frequency.

   VCO is a free running multivibrator and operates at a set of frequency fo called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage Vc to an appropriate terminal of the IC.The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator

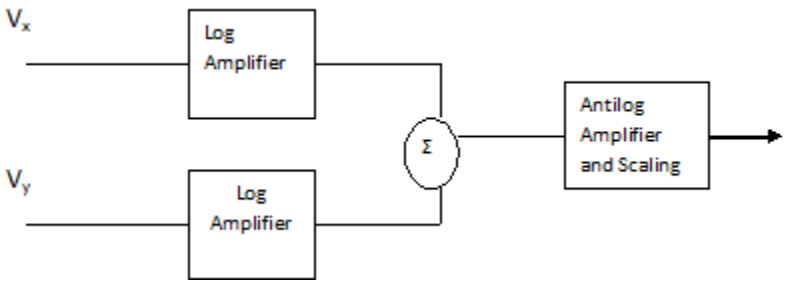
8. What is a four-quadrant multiplier? **[Nov/Dec 2016]**

It is a multiplier circuit with two inputs being both positive and both negative, then the multiplier is called as four-quadrant multiplier

9. Draw the block diagram of PLL for AM detection? **[April/May 2016]**



10. Calculate the lock range and the capture range of the PLL.
    Lock in range Δf_L= +/- 7.8 f_o/ V
    $f_o$is free running frequency
    Capture range = +/- = $[\Delta f_L/ (2*\pi*R*C)]^{1/2}$
11. The lock range of a certain general purpose PLL with a free running frequency of 50MHz is specified to be +/- 10% what is its lock range?
    Lock in range Δf_L= +/- 7.8 f_o/ V
12. What are the essential building blocks of a PLL?
    The essential building blocks of PLL are
    - Phase detector
    - Low pass filter
    - Amplifier
    - Voltage Controlled Oscillator
13. What is a two quadrant multiplier?
    It is a multiplier one input must be held positive and other can change to positive or negative it is called two quadrant multiplier.
14. What is compander?
    The signal is compressed at the transmitter and expanded at the receiver. This is called as companding. The combination of a compressor and expander is called a compander.
15. State why the phase detector output in a PLL should be followed by a low pass filter?
    The phase detector is basically a multiplier and produces the sum (f_s+f_o) and the difference (f_s-f_o) components at its output. The high frequency component is removed by the low pass filter and the difference frequency component is applied as control voltage v_c to VCO.
16. Draw the block diagram of a multiplier using log and antilog amplifiers.



17. What is frequency synthesizer?

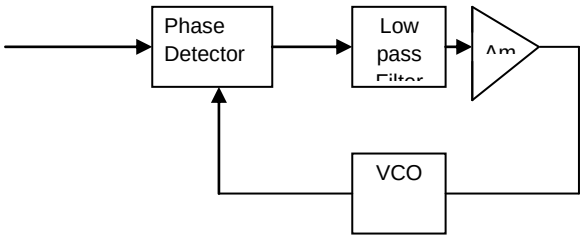
    Frequency synthesizer is a circuit here each frequency is selected by closing the desired program switches to program a particular frequency output.

    Period = Tsum + T

18. Define PLL

    A phase locked loop is a closed loop system designed to lock the output frequency and phase to the frequency and phase of an input signal

19. Draw the basic block diagram of PLL?



20. What is amplitude modulation?

    It is the process of amplitude of carrier wave varies in accordance with the instantaneous value of the amplitude of message signal.

21. Define voltage to frequency conversion factor kv?

    It is given as

    $K_v = \Delta f_o / \Delta v_c$

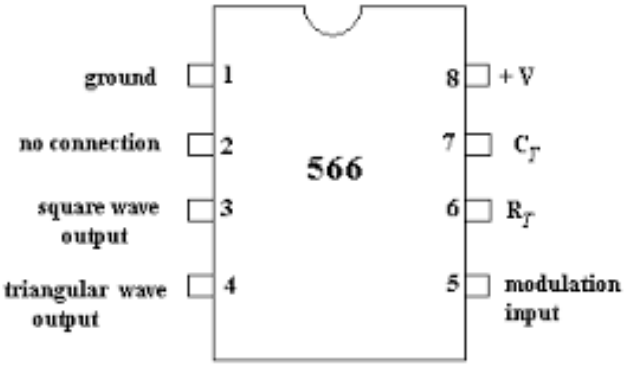
    Here $K_{v\ is}$ the modulation voltage required to produce the frequency shift $\Delta f_o$for a VCO.

22. What is a voltage-controlled oscillator?

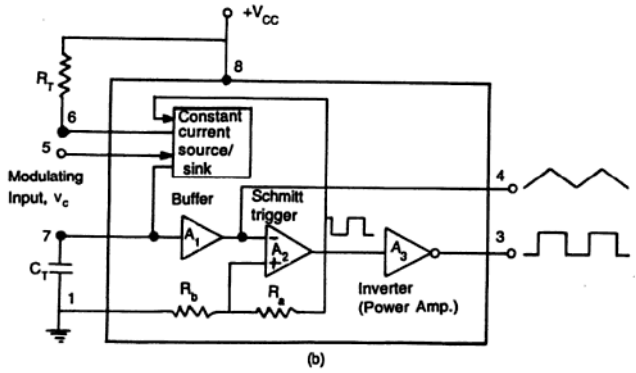
    A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillation can be controlled by an externally applied voltage. It provides the linear relationship between the applied voltage and the oscillation frequency.

    VCO is a free running multivibrator and operates at a set of frequency fo called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage Vc to an appropriate terminal of the IC.The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator".

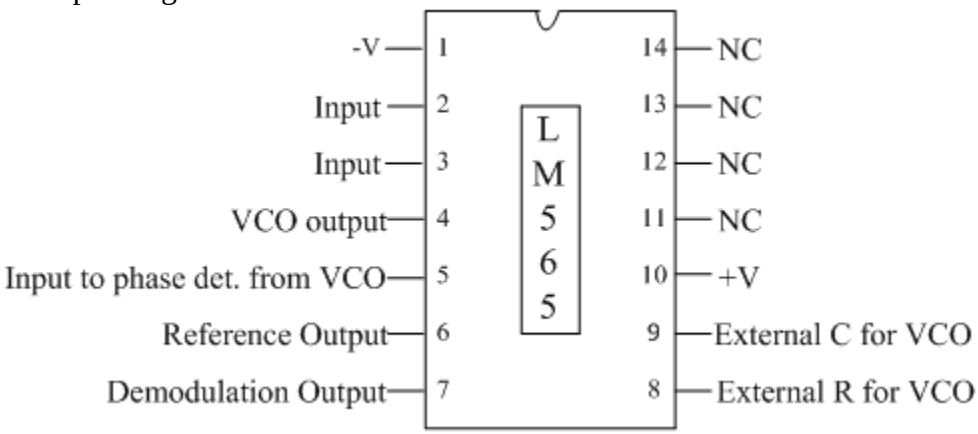
23. Draw the pin diagram of 566 VCO



24. Draw the block diagram of 566 VCO



25. Draw the pin diagram of 565 PLL.



26. How VCO different from oscillators?

An oscillator is a circuit that generates the frequency output of fixed frequency.On the other hand a voltage controlled oscillator (VCO) is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage.

27. When an amplifier is also called an error amplifier?

An amplifier also called an error amplifier in control theory, which accepts the signal X_d and yields the output signal X_0=a.Xd, where a is the forward gain of the amplifier is called the open-loop gain of the circuit.

28. What are the merits of companding?

- The compression process reduces the dynamic range of the signal before it is transmitted.
- Companding preserves the signal to noise ratio of the original signal and avoids non linear distortion of the signal when the input amplitude is large.
- It also reduces buzz, bias and low level audio tones caused by mild interference.

29. List the applications of OTA:

OTA can be used in

- programmable gain voltage amplifier
- sample and hold circuits
- voltage controlled state variable filter
- current controlled relaxation oscillator

30. Mention some areas where PLL is widely used.

Radar synchronization
Satellite communication systems
Air borne navigational systems
FM communication systems

31. Define lock-in range of a PLL.

The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. It is expressed as a percentage of the VCO free running frequency.

32. Define free running mode.

In a PLL if the error control voltage is zero then the PLL is said to be operated in free running mode and its output frequency is called its center frequency f_0.

33. What are the advantages of variable transconductance technique?

The advantages of variable transconductance technique are:

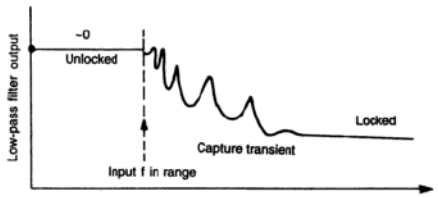
1) Simple to integrate into monolithic chip
2) Provides very good accuracy.
3) Very cheap hence economical.
4) Provides four quadrant operations.
5) It provides high speed of operation which is 2 to 3 times more than the logarithmic method.
6) Reduced error at least by 10 times.

34. With reference to a VCO, define voltage to frequency conversion factor Kv.

Voltage to frequency conversion factor Kv is defind as $Kv=\Delta fo/\ \Delta vc$

Here Δvc is the modulation voltage required to produce the frequency shift of Δfo for a VCO

35. Draw the relation between the capture ranges and lock range in a PLL.



36. Mention two applications of analog multiplier

- Variable-gain amplifier
- Ring modulator
- Product detector
- Frequency mixer

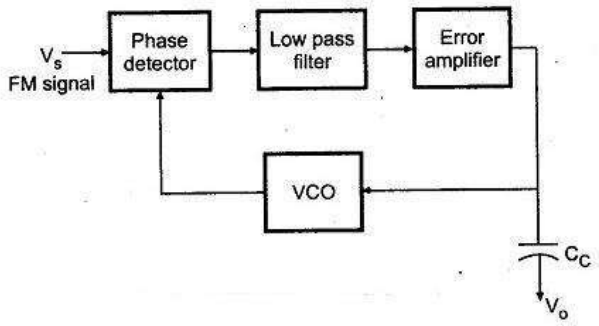
37. VCO is called as V-F converter why?

A voltage-controlled oscillator or VCO is an electronic oscillator whose oscillation frequency is controlled by a voltage input ie the change in input voltage results in change in output frequency hence it is called as V-F converter

38. Define FSK

Frequency shift keying is a digital modulation technique in which the frequency of carrier signal is varied in accordance with the amplitude of digital modulating signal

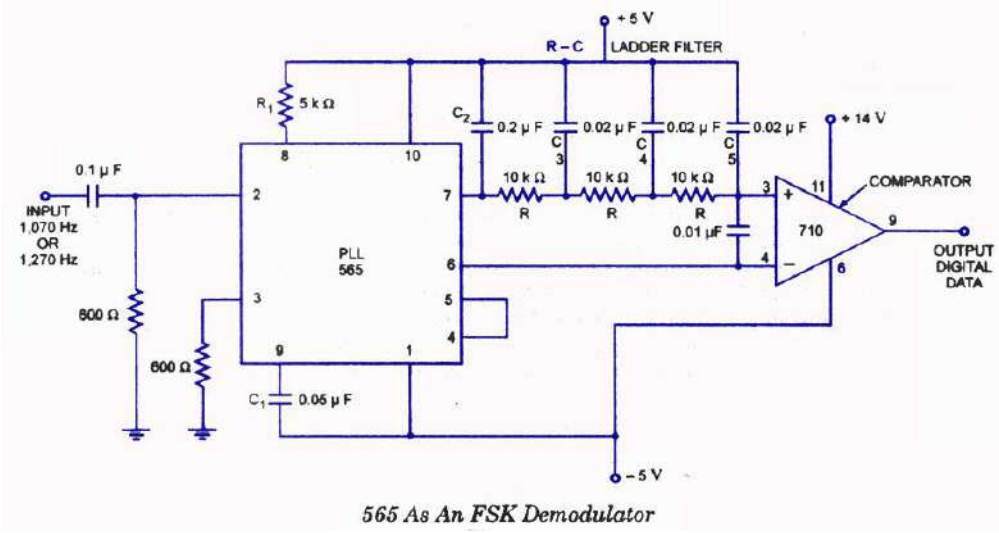
39. Draw the block diagram of PLL for FM detection



40. What is the need for frequency synthesizer

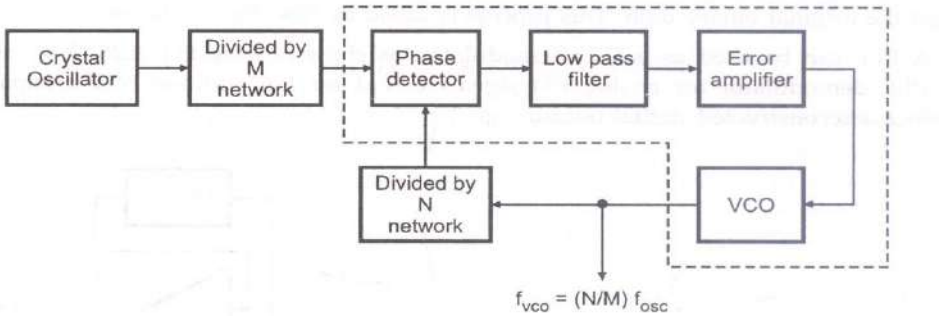
A frequency synthesizer is an electronic system for generating any of a range of frequencies from a single fixed time base or oscillator. They are found in many modern devices, including radio receivers, mobile telephones, radiotelephones, walkie-talkies, CB radios, satellite receivers, GPS systems, etc

41. Draw the block diagram of PLL for FSK demodulation



565 As An FSK Demodulator

42. Draw the block diagram of PLL for frequency synthesizing



43. List the performance parameters of multiplier

- Accuracy
- Linearity
- Bandwidth
- Feed through voltage
- Scale factor
- Quadrant

44. State the various techniques used for multiplier.

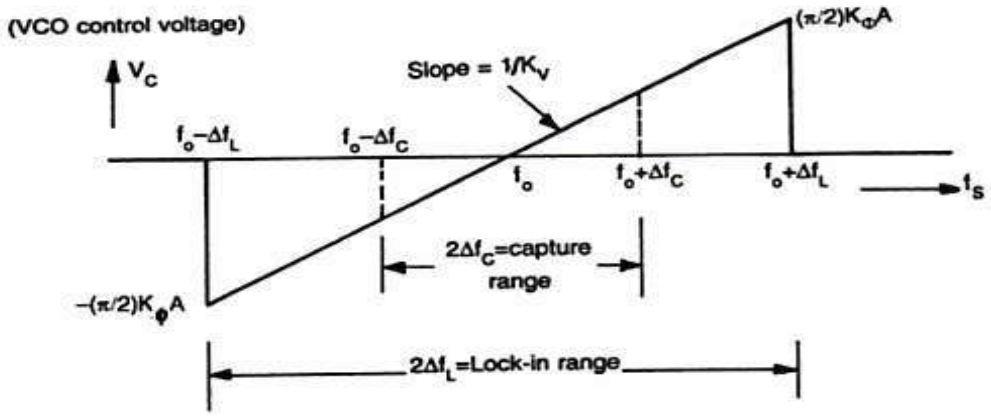
- Logarithmic summing technique
- Quarter square technique
- Pulse width modulation
- Variable transconductance technique
- Triangle averaging technique

45. What are the limitations of logarithmic summing technique?

- Poor accuracy
- One quadrant operation
- Temperature instability

46. State the two multiplier ICs
    - AD533
    - AD534
47. Mention the applications of AD533
    - Function generator
    - Peak detection
    - RMS computation
    - Phase detection
    - Automatic gain control
    - Square and square root extractor
48. Mention the applications of AD534
    - Multiplier
    - Divider
    - High quality analog signal processing
    - Square and square root extractor
    - Differential ratio and percentage computation
    - Accurate voltage controlled oscillators and filters
49. What is pull in time?

    From the application of the input signal ,the total time taken by the PLL to establish a lock is called pull in time.
50. Which parameter decides the pull in time
    - Initial Frequency and phase difference between two signals
    - Overall loop gain
    - Bandwidth of low pass filter.
51. Draw the relation between the capture range and lock range of PLL



PLL lock-in range and capture range

PART – B&C

1. (i) Explain in detail the operation of a basic phase locked loop. (5)

[Nov/Dec 2018]

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 327]

(ii) How are PLLs applied for frequency synthesizing and FM detection.(8)

[Nov/Dec 2018]

Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 343]

2. A PLL has a free running frequency of 400 kHz and the band width of the low pass filter is 8kHz.Will the loop tend to acquire lock for an input signal of 550 kHz? Explain in this case ,assume that the phase detector produces sum and difference frequency components. **[Nov/Dec 2018] [Nov/Dec 2017]**
3. (i) Obtain the expression for free running frequency of voltage controlled oscillator.(6) **[Nov/Dec 2018]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 334]
   (ii) Design an analog multiplier employing an emitter coupled transistor pair. (7) **[Nov/Dec 2018]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 342]
4. Discuss briefly about analog multiplier ICs **[April/May 2018]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 159]
5. Discuss in detail about VCO using suitable diagram. **[April/May 2018]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 334]

6. With neat diagram explain the design of (i) Frequency Synthesizer (ii) Frequency Division circuit using PLL IC 565 **[April/May 2017]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 342]
7. (i) Discuss the principle of operation of NE 565 PLL circuit **[Nov/Dec 2016]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 337]
   (ii) How can PLL be modeled as a frequency multiplier? **[Nov/Dec 2016]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 342
8. Explain the Application of PLL as AM detection,FM detection and FSK demodulation **[April/May 2016]**
   [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 375]
9. Explain the basic blocks of PLL and determine expressions for lock in range and capture range **[April/May 2015]**
   [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 353& 370]
10. i) With neat simplified internal diagram explain the working principle of Operational Transconductance Amplifier(OTA) **[April/May2015]**
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 210]
    ii) Explain the application of VCO for FM generation **[April /May15]**
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 225]
11. With suitable block diagram explain the operation of 566 voltage controlled oscillator. Also derive an expression for the frequency of the output waveform generated
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 363]
12. Explain the working principle of four quadrant variable form transconductance multiplier **[May/June 2016]**
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 210]
13. Draw the analog multiplier IC and explain its features and Explain the application of analog multiplier IC **[April/May 2015]**
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 183]
14. i)Explain Analog Multiplier using Emitter Coupled Transistor Pair
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 183]
    ii)Explain Gilbert Multiplier cell in detail
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 183]
15. Explain the application of PLL for
    i. Frequency synthesizing
    ii. Clock synchronization
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 342]

UNIT -IV - **ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS**

PART A:

1. Define settling time **[April/May 2019]**

   It is the time the converter takes for the output to settle within a specified band +/-(1/2)LSB

2. What is the largest value of output voltage from an 8 bit DAC that produces 1.0V for a digital input of 00110010 **[April/May 2019]**

   5.10V

3. Differentiate between direct type and integrating type in ADC converters. **[Nov/Dec 2018]**

   Direct type ADCs compare a given analog signal with the internally generated equivalent signal.

   Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to linear function of time or frequency and then to a digital code.

4. What is the need of sample and hold circuit. **[Nov/Dec 20178]**

   For accurate analog and digital conversion the analog input voltage should be held constant during the conversion cycle. The input voltage is kept constant during conversion time using sample and hold circuit.

5. Define Sampling. **[April/May 2018]**

   The process of converting analog signals into discrete time signals is called sampling.

6. Write the name of the switches used in MOS transistors. **[April/May 2018]**

   - Totem pole MOSFET switch
   - CMOS inverter switch

7. How is the classification of A/D converters carried out based on their operational features? **[Nov/Dec 2017]**

   A/D converter are classified into two groups according to their conversion

   (i) Direct type ADC
   (ii) Integrating type ADC

   Direct Type ADC

   (i) Flash Type converter
   (ii) Counter type converter
   (iii) Tracking or servo converter
   (iv) Successive approximation type converter

   Integrating type ADC

   (i) Charge balancing ADC
   (ii) Dual slope ADC

8. Find the number of resistors required for an 8 bit weighted resistor D/A converter. Consider the smallest resistance is R and obtain those resistance values. **[Nov/Dec 2017]**

   The No of Resistors required =8

   The resistance values are $2^1R,2^2R,2^3R,2^4R,2^5R,2^6R,2^7R,2^8R$

9. Why are Scottky diodes used in sample and hold circuits? **[April/May 2017]**

Schottky diodes can be used in diode-bridge based sample and hold circuits. When compared to regular p-n junction based diode bridges, Schottky diodes can offer advantages. A forward-biased Schottky diode does not have any minority carrier charge storage. This allows them to switch more quickly than regular diodes, resulting in lower transition time from the sample to the hold step. The absence of minority carrier charge storage also results in a lower hold step or sampling error, resulting in a more accurate sample at the output

10. What are the advantages of inverted R-2R (current type) ladder D/A converter over R-2R (voltage type) D/A converter? **[Nov/Dec 2016]**

In R-2R ladder type DAC current flowing in the resistors changes as the input data changes. More power dissipation causes heating which in turn creates non-linearity in DAC.This problem can be avoided in inverted R-2R ladder type as the current divides equally at each node.

11. What is the need for electronic switches in D/A converter? **[Nov/Dec 2016]**

The Switches which connects the digital binary input to the nodes of a D/A converter is an electronic switch

12. A 12 bit D/A converter has a resolution of 20mv/LSB.Find the full scale output voltage. **[May/June 2016]**

$$\text{Re}\,solution = \frac{V_{oFS}}{2^n - 1}$$

Where, V_{oFS} is the full scale output voltage

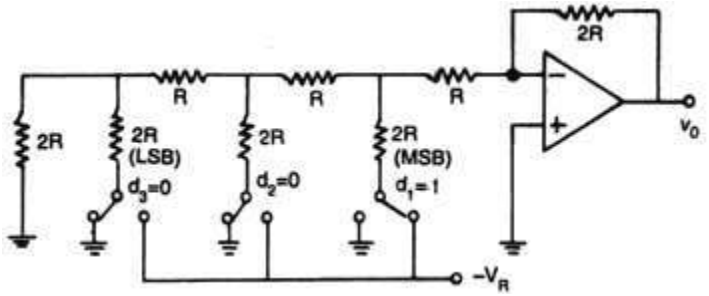
n is the number of bits

$$V_{oFS} = \text{Re}\,solution * (2^n - 1)$$

$$V_{oFS} = 20 * 10^{-3} * (2^{12} - 1)$$

$$V_{oFS} = 81.9V$$

13. Draw the binary ladder network of DAC, If the value of the smaller resistance is 10K.What is the value of other resistance? **[May/June 2016]**



The value of other resistance=2R=20 Kohm

14. Determine the number of comparators and resistors required for 8 bit flash type ADC **[Nov/Dec2015]**

No Of comparators required is $=2^8-1=255$

15. Mention two advantages of R-2R ladder type DAC when compared to weighted resistor type DAC **[Nov/Dec 2015]**

- Only two resistor values are used in R-2R ladder type.
- It does not need as precision resistors as Binary weighted DACs.
- It is cheap and easy to manufacture.

16. What would be produced by a DAC whose output ranges is 0 to 10V and whose input binary number is 10111100(for a 8 bit DAC)? **[April/May 2015]**

V_o=10V(1x(1/2)+0x(1/2)^2+1x(1/2)^3+1x(1/2)^4+1x(1/2)^5+1x(1/2)^6+0x(1/2)^7+0x(1/2)^8)

V_o=7.34V

17. What is over sampling? **[April/May 2015]**

The technique of increasing the apparent sampling frequency of a digital signal by repeating each digit a number of times, in order to facilitate the subsequent filtering of unwanted noise.

In signal processing, oversampling is the process of sampling a signal with a sampling frequency significantly higher than the Nyquist rate. Theoretically a bandwidth-limited signal can be perfectly reconstructed if sampled above the Nyquist rate, which is twice the highest frequency in the signal. Oversampling improves resolution, reduces noise and helps avoid aliasing and phase distortion by relaxing anti-aliasing filter performance requirements.

18. State the reason for keeping the integrating time in the dual slope analog to digital converter equal to that of mains supply period.

The dual slope ADC integrates the input signal for a fixed time, hence it provides excellent noise rejection of ac signals whose periods are integral multiples of the integration time Ti. Thus as noise superimposed on the input signal such as 50Hz power link pick-up will be averaged during the input integration time. So choose clock period T, so that 2^nT is an exact integral multiple of the line period (1/50) second = 20 ms.

19. Which is the fastest A/D converter? Give reason.

Parallel comparator A/D is the fastest and most expansive comparator.

Because it consists of a resistive divider network, 8 op-amp comparators and a 8 line to 3 line encoder.

20. A 12 bit D/A converter have resolution of 30 mV/ LSB. Find the full scale output voltage.

Vo = Vfs/2

Vfs = 2xVo

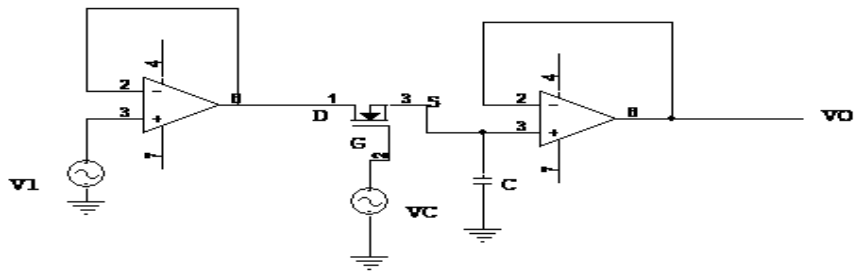
= 2x30 = 60 mv.

21. Calculate the number of comparators required for realizing a 4 bit flash A/D converter.

Numbers of comparators required are $2^n - 1$

$2^4 - 1 = 16 - 1 = 15$.

22. Draw a sample and hold circuit.



23. Define resolution of a D/A converter?

The resolution of a DAC is defined as the smallest change in voltage, which may be produced at the output or input of the converter.

24. How many comparators are required to build n –bit flash type A/D converter?

Comparator required to build n –bit flash type A/D converter is $2^n - 1$

Where n is the desired number of bits.

25. Define monotonicity with respect to D/A converter?

A DAC is said to be monotonic if the analog output increases or remains the same as the digital input increases. This results in the output always being single – valued.

26. Why is R-2R ladder network DAC better than weighted resistor DAC?

Wide ranges of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC.

i. Easier to build accurately as only two precision metal film resistors are required.
ii. Number of bits can be expanded by adding more sections of same R-2R values.
iii. In inverted R-2R ladder DAC, node voltages remain constant with changing input binary words. This avoids any slowdown effects by stray capacitances.

27. Which type of ADC is used in all digital voltmeter?

Dual slope ADC converters are particularly suitable for accurate measurement of slowly varying signals, such as digital panel meters and multimeters.

28. What do you mean by delta modulation?

Delta modulation is a method of information transmission with the help of pulses. It is one type of digital modulation and it determines the increase or decrease of the signal sample with respect to previous sample. And encodes this rise or fall of amplitude by 1 bit.

29. List the application of sample and Hold circuits?

i. It is used in ADC.
ii. It is used in digital interfacing
iii. It is used in pulse modulation system
iv. It is used in analog demultiplexer

30. Mention the types of DAC techniques?

ii. Weighted resistance
iii. Inverted R-2R ladder
iv. Multiplying.

31. Define the resolution of DAC?

Resolution of DAC is defined as the change in the output voltage corresponding to the change of one bit in the digital input.

32. Explain in brief stability of a converter:

The performance of converter changes with temperature age & power supply variation . So all the relevant parameters such as offset, gain, linearity error& monotonicity must be specified over the full temperature & power supply ranges to have better stability performances.

33. What is meant by linearity?

The linearity of an ADC/DAC is an important measure of its accuracy & tells us how close the converter output is to its ideal transfer characteristics. The linearity error is usually expressed as a fraction of LSB increment or percentage of full-scale voltage. A good converter exhibits a linearity error of less than ±½LSB.

34. What is monotonic DAC?

A monotonic DAC is one whose analog output increases for an increase in digital input.

35. What is multiplying DAC?

A digital to analog converter which uses a varying reference voltage VR is called a multiplying DAC (MDAC). If the reference voltage of a DAC, VR is a sine wave given by:

$$V(t) = V_{in} \text{ Cos } 2\pi ft;$$

$$\text{Then, } V_o(t) = V_{om} \text{ Cos } (2\pi ft + 180^o)$$

36. What is a sample and hold circuit? Where it is used?

A sample and hold circuit is one which samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is mainly used in digital interfacing, analog to digital systems, and pulse code modulation systems.

37. Define sample period and hold period.

The time during which the voltage across the capacitor in sample and hold circuit is equal to the input voltage is called sample period. The time period during which the voltage across the capacitor is held constant is called hold period.

38. Define accuracy of converter.

Absolute accuracy:

It is the maximum deviation between the actual converter output & the ideal converter output.

Relative accuracy:

It is the maximum deviation after gain & offset errors have been removed. The accuracy of a converter is also specified in form of LSB increments or % of full scale voltage.

39. What output voltage would be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is 0110 for a 4 bit DAC.

Given $V_{o\ FS} = 10V$

$$Resolution = \frac{10}{10^4 - 1} = 0.6667\ V$$

The output voltage at 0110=0.6667*6=4V

40. What is the main drawback of dual slope ADC?

The conversion time of dual slope ADC is high .This is the main drawback of dual slope ADC.

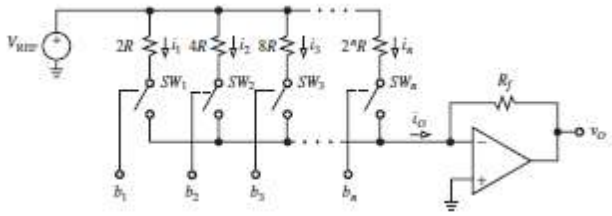
41. Draw the binary ladder network of DAC .If the value of the smaller resistance is 10K what is the value of the other resistance

42. A 12 bit D/A converter has resolution of 20mV/LSB.Find the full scale output voltage **[April/May 16]**

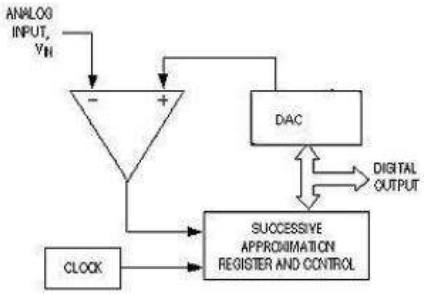
Given resolution = 20mV/LSB

Full scale output voltage =Resolution(10^{12}-1)=20*10^{-3} (10^{12}-1)

43. Draw the weighted resistor network of DAC[APRIL/MAY 16]



44. Draw the functional diagram of the successive approximation ADC



44. Define voltage droop.

The leakage current causes voltage of the capacitor to drop down.This is referred to as droop.

45. What are current driven DACs?

The DAC in which the problem of radioed emitter is solved by using equal value current sinks and exploiting the current scaling capability of the inverter R-2R ladder to obtain binary weighted contributions to the output is known as current driven DAC

46. What are the specifications of D/A converter?

- Accuracy
- Resolution
- Offset
- Linearity error
- Conversion time
- Monotonicity

47. Define conversion time of DAC

It is the time required for conversion of analog signal into its digital equivalent.

48. What is linear error?

The linear error is defined as the amount by which the actual output differs from ideal straight line output characteristics of DAC

49. Define Offset error.

Offset error is defined as the nonzero level of the output voltage when all inputs are zero.

50. Compare single slope ADC and dual slope ADC

Sl.No	Single slope ADC	Dual slope ADC
1.	Resolution is low	Resolution is high
2.	Does not use integrator	It uses integrator
3.	Accuracy is low	Accuracy is high
4.	Less immune to temperature variations	More immune to temperature variations
5.	More sensitive to input voltage variations	Less sensitive to input voltage variations

PART –B&C

1. (i) Describe the operational feature of R-2R ladder type D/A converter.(7) **[Nov/Dec2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 352]

(ii) Discuss various switches employed for D/A converters.(6) **[Nov/Dec2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 351]

2. (i) With a neat block diagram, explain the operation of flash and successive approximation type A/D converter. (10) **[Nov/Dec2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 358]

(ii) What is oversampling? Give examples of oversampling converter. (3) **[Nov/Dec2018]**

3. (i) For a 4 bit R-2R ladder D/A converter assume that the full scale voltage is 16V.Calculate the step change in output voltage on input varying from 0111 to 1111(8) **[Nov/Dec2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 357]

(ii) Explain sigma delta converters in detail

4. Enumerate the specifications of D/A converter. **[April/May 2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 366]

5. Describe in detail about the single slope type AC with neat sketch. **[April/May 2018]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 363]
6. Describe the operation of dual slope and successive approximation type ADC .What are the advantages of dual slope ADC **[April/May 2017]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 358]

7. (i) What is meant by resolution ,offset error in ADC **[April/May 2017]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 366]
8. (ii) Discuss on the single slope type ADC **[April/May 2017]**
   [Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 363]
9. (i) Explain the successive approximation type A/D converter **[April/May 2016]**
   [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 396]
   (ii) Narrate the functions of Analog switches **[April/May 2016]**
   [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 383]

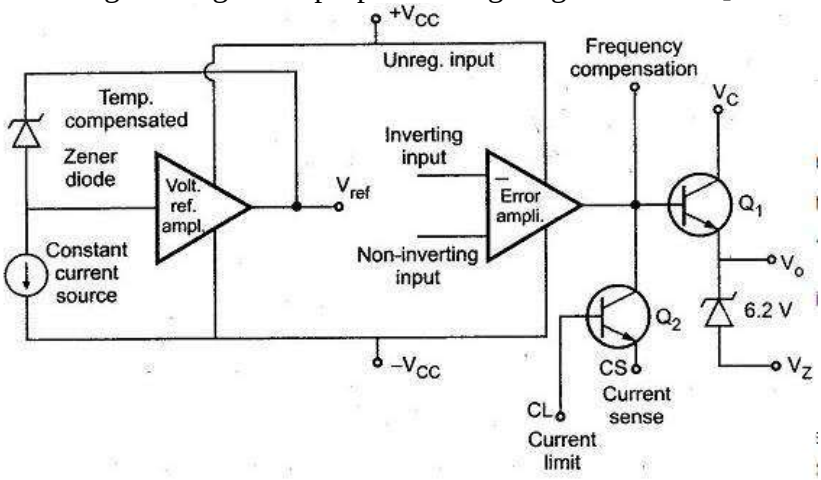
10. How are A/D converters categorized? **[April/May 2017]**
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 393]
    (ii) Write Short Note on high speed sample and hold circuits(6)
    [April/May 2015] [April/May 16]
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 176]
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 397]
11. (i) Explain voltage mode and current mode operations of R-2R ladder type DAC[Nov/Dec 10]
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 386]
    (ii) Explain over sampling type analog to digital converters
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 176]
12. Draw the block diagram and explain the working of
    (i) Charge Balancing VFCS (8)
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 225]
    (ii) Voltage to Time converter (8)
    [May/June 13]
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 225]
13. Explain the following type DAC with suitable diagrams
    (i) Binary weighted resistor DAC (6)
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 382]
    (ii) R-2R Ladder DAC (5)
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 385]
    (iii) Inverted R-2R ladder DAC (5)
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 386]
14. (i) Explain the following type of electronic switches used in D/A converter with suitable diagrams
    1.Totem pole MOSFET switch (4)
    2.CMOS inverter as a switch (4)
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 384]
    (ii) Compare Flash type ,Dual slope and successive approximation ADC in terms of parameters like speed ,accuracy, resolution ,input hold time(8)
    [May/June 12]
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 393]
15. With a neat block diagram explain the working of three bit flash type analog to digital converter
    [Ref .Roy Choudhry, Shail B.Jain, "Linear Integrated Circuits (Second Edition)", Page 393]

UNIT-V-WAVEFORM GENERATORS AND SPECIAL FUNCTION ICs

PART A:

1. What are the types of multivibrators **[April/May 2019]**
   - Monostable multivibrator
   - Astable multivibrator
   - Bistable multivibrator
2. State the function of Opto coupler **[April/May 2019]**

   An opto-isolator (also called an optocoupler, photocoupler, or optical isolator) is an electronic component that transfers electrical signals between two isolated circuits by using light.Opto-isolators prevent high voltages from affecting the system receiving the signal.
2. List the various applications of multivibrators. **[Nov/Dec 2018]**
   - Pulse width modulation
   - Frequency doublers
   - Linear Ramp generator
   - Missing pulse detector
   - Square wave generator
   - Voltage controlled oscillator
   - FSK generator
3. Draw the circuit diagram of general purpose voltage regulator. **[Nov/Dec 2018]**



4. Name some LC oscillator circuits **[April/May 2018]**
   - Hartley Oscillator
   - Colpitts oscillator
5. Define Line regulation. **[April/May 2018]**

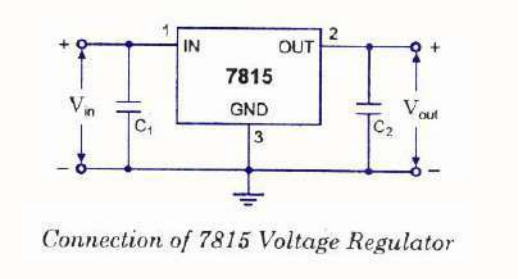
   The line regulation is defined as the change in the regulated output load voltage for a specified range of the line voltage .It specifies the effect of changes in the source voltage on the regulator performance.

   Line regulation is also defined as the percentage change in the output voltage for a change in the input voltage. It is expressed in millivolts or as a percentage of the output voltage.
6. Define current transfer ratio of an opto coupler **[Nov/Dec 2017]**

   The current transfer ratio (CTR) is a parameter similar to the DC current amplification ratio of a transistor (hFE) and is expressed as a percentage indicating the ratio of the output current (IC) to the input current (IF).

   CTR(%)=(IC/IF) x 100

7. Draw a fixed voltage regulator circuit and state its operation **[Nov/Dec 2017]**



Connection of 7815 Voltage Regulator

8. What is a voltage regulator? **[April/May 2017]**

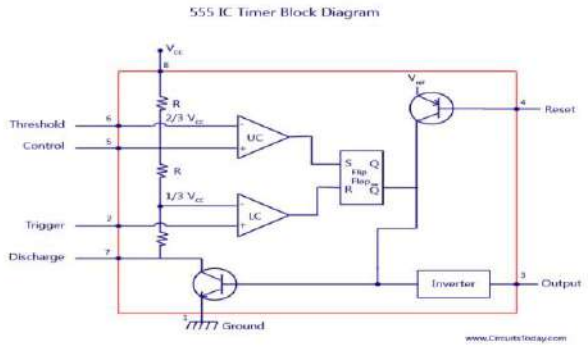
A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature, and ac line voltage variations.

9. Distinguish the principle of linear regulator and a switched mode power supply. **[April/May 2017]**

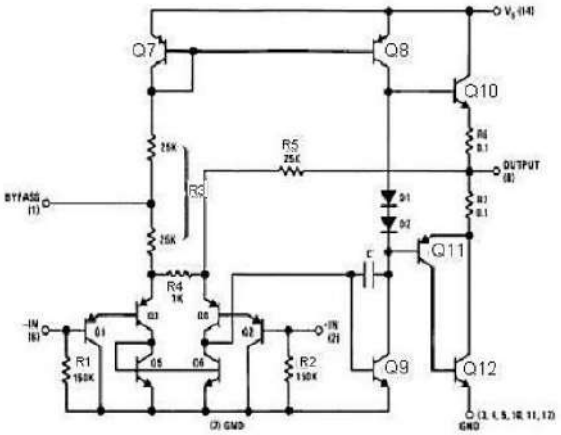
As its name suggests, a linear regulator is one where a linear component (such as a resistive load) is used to regulate the output. It is also sometimes called a series regulator because the control elements are arranged in series between the input and output.

A switching regulator is a voltage regulator that uses a switching element to transform the incoming power supply into a pulsed voltage, which is then smoothed using capacitors, inductors, and other elements.

10. Draw the block schematic of IC 555 timer. **[Nov/Dec 2016]**



11. Draw the internal circuit for audio power amplifier **[April/May 2016]**



12. What is the function of a voltage regulator? Name few IC voltage regulators. **[Nov/Dec 2016]**

The function of voltage regulator is to provide a stable dc voltage for powering other electronic circuits. A voltage regulator should be capable of providing substantial output current.

Some IC voltage regulator is 78 XX/79 XX series and 723 general purpose regulators

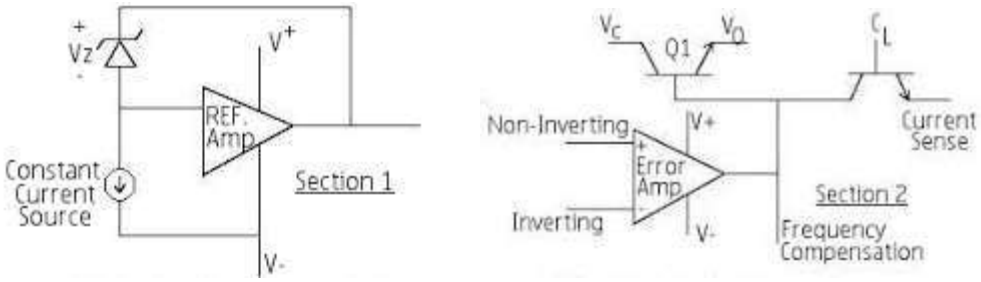
13. What is the purpose of connecting a capacitor at the input and the output side of an IC voltage regulator? **[Nov/Dec 2015]**

    A capacitor connected between the input terminal and ground cancels the inductive effects due to long distribution leads. The output capacitor improves the transient response.

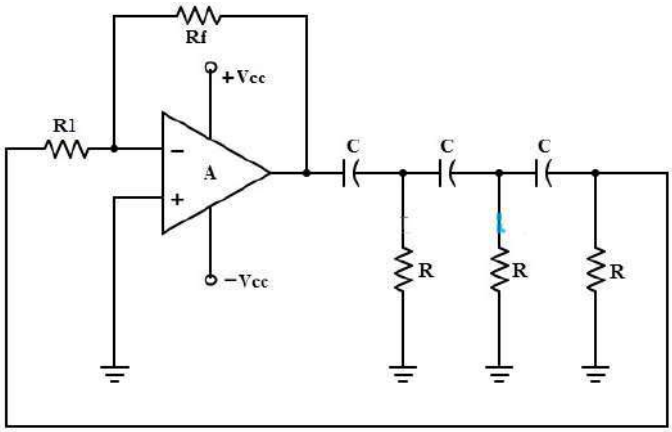
14. Mention two applications of frequency to voltage converter **[Nov/Dec 2015]**
    - Frequency to voltage converter in tachometers.
    - Frequency difference measurement

15. State the two conditions for oscillation. **[April/May 2015]**
    - The loop gain is equal to unity in absolute magnitude, that is, $|\beta A| = 1$ and
    - The phase shift around the loop is zero or an integer multiple of 2π:

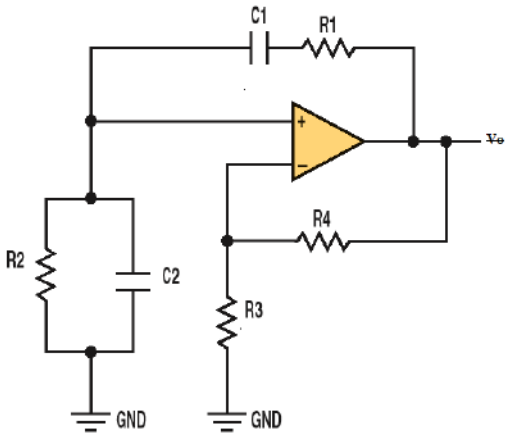
16. Draw the functional block diagram of 723 regulator. **[April/May 2015]**



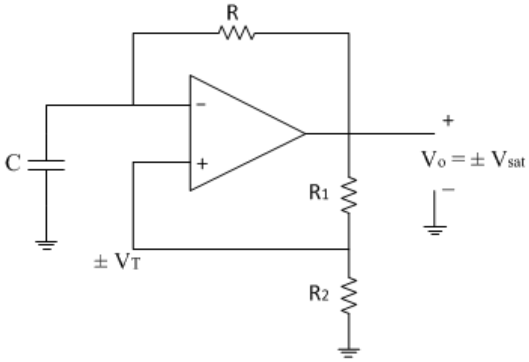
17. Draw the circuit diagram of RC phase shift oscillator



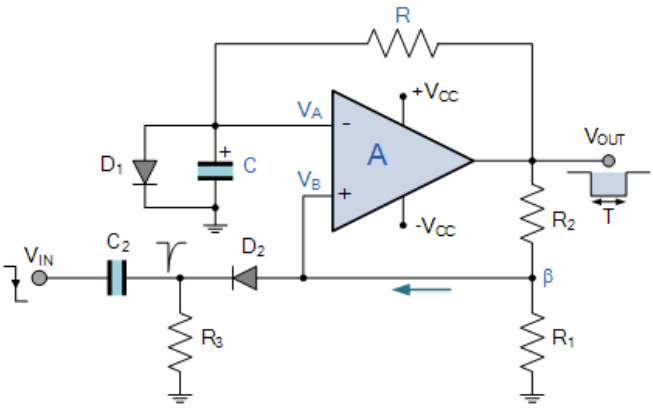
18. Draw the circuit diagram of wien bridge oscillator



19. Draw the circuit diagram of astable multivibrator using op-amp



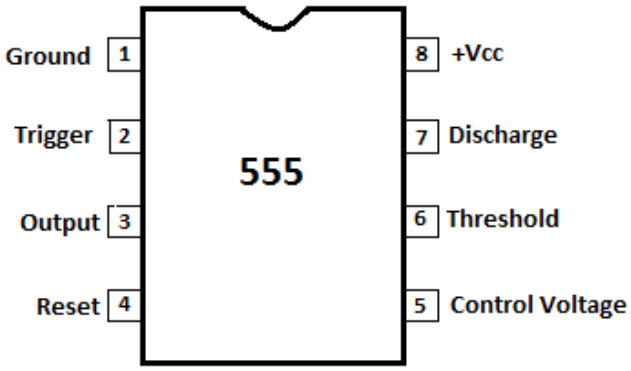
20. Draw the circuit diagram of monostable multivibrator using op-amp



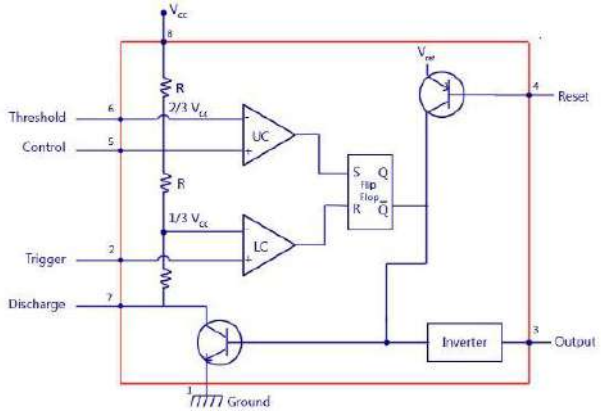
21. Which are the basic elements of IC555 timer

- A relaxation oscillator
- R-S flip-flop
- Two comparators
- discharge transistor

22. Draw the pin diagram of 555 timer



23. Draw the block diagram of 555 timer



24. Mention some applications of 555 timer:
    - Oscillator
    - Pulse generator
    - Ramp and square wave generator
    - Mono-shot multivibrator
    - Burglar alarm
    - Traffic light control.
25. List the applications of 555 timer in monostable mode of operation:
    - Missing pulse detector
    - Linear ramp generator
    - Frequency divider
    - Pulse width modulation.
26. List the applications of 555 timer in Astable mode of operation:
    - FSK generator
    - Pulse-position modulator
27. Give the classification of voltage regulators:
    - Series / Linear regulators
    - Switching regulators.
28. What is a linear voltage regulator?

    Series or linear regulator uses a power transistor connected in series between the unregulated dc input and the load and it conducts in the linear region. The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor.
29. What is a switching regulator?

    Switching regulators are those which operate the power transistor as a high frequency on/off switch, so that the power transistor does not conduct current continuously. This gives improved efficiency over series regulators.
30. What is the purpose of having input and output capacitors in three terminal IC regulators?

    A capacitor connected between the input terminal and ground cancels the inductive effects due to long distribution leads. The output capacitor improves the transient response.
31. Define load regulation.

    Load regulation is defined as the change in output voltage for a change in load current. It is expressed in millivolts or as a percentage of the output voltage.
32. What is meant by current limiting?

    Current limiting refers to the ability of a regulator to prevent the load current from increasing above a preset value.
33. Give the drawbacks of linear regulators:
    - The input step down transformer is bulky and expensive because of low line frequency.
    - Because of low line frequency, large values of filter capacitors are required to decrease the ripple.
    - Efficiency is reduced due to the continuous power dissipation by the transistor as it operates in the linear region.
34. What is the advantage of switching regulators?
    - Greater efficiency is achieved as the power transistor is made to operate as low impedance switch. Power transmitted across the transistor is in discrete pulses rather than as a steady current flow.
    - By using suitable switching loss reduction technique, the switching frequency can be increased so as to reduce the size and weight of the inductors and capacitors.

35. What is an opto-coupler IC? Give examples.

Opto-coupler IC is a combined package of a photo-emitting device and a photo sensing device.

Examples for opto-coupler circuit : LED and a photo diode,
LED and photo transistor,
LED and Darlington.

Examples for opto-coupler IC : MCT 2F , MCT 2E

36. Mention the advantages of opto-couplers:
    - Better isolation between the two stages.
    - Impedance problem between the stages is eliminated.
    - Wide frequency response.
    - Easily interfaced with digital circuit.
    - Compact and light weight.
    - Problems such as noise, transients, contact bounce are eliminated.
37. What is an isolation amplifier?

An isolation amplifier is an amplifier that offers electrical isolation between its input and output terminals.

38. What is the need for isolation amplifiers?

The isolation amplifier is required when the common mode voltages exist between instrument ground and signal ground. Such voltages allow ground loop cements to circulate in the absence of isolation amplifier. This causes noisy operation, destruction of instrument and measurement errors. To avoid this isolation amplifiers are needed.

39. What is the need for a tuned amplifier?

In radio or TV receivers, it is necessary to select a particular channel among all other available channels. Hence some sort of frequency selective circuit is needed that will allow us to amplify the frequency band required and reject all the other unwanted signals and this function is provided by a tuned amplifier.

40. Give the classification of tuned amplifier:

(i) Small signal tuned amplifier
    - Single tuned
    - Double tuned
    - Stagger tuned

(ii) Large signal tuned amplifier.

41. Why is the monostable multivibrator circuit called time delay circuit and gating circuit?

Monostable multivibrator circuit called time delay circuit because it generates a fast transition at a predetermined time T after the application of input trigger. It is called as a gating circuit because it generates rectangular waveform at a definite time and could be used as gate parts of a system.

42. Why there is no phase shift provided in the feedback network in Wein-Bridge oscillator?

In Wein-bridge oscillator, the feedback signal is connected to the (+) input terminal so that, the op-amp is working as a non-inverting amplifier, which produces 0 degree or 360 degree phase shift.. Therefore the feedback network need not provide any phase shift.

43. Give the formula for period of oscillations in an op-amp astable circuit.

The formula for period of oscillations in an op-amp astable circuit is $T =$

$$2RC \ln\left[1 + \frac{2R_2}{R_1}\right]$$

44. Define duty cycle for a periodic pulse waveform.

The duty cycle of the output pulse waveform is given by

$$d\% = \frac{T_C}{T} * 100 = \frac{R_A + R_B}{R_A + 2R_B} * 100$$

45. What is meant by thermal shutdown applied to voltage regulators?

Due to overheating , the series pass element of regulator may get damaged. To avoid this, thermal shutdown is provided. In this protection scheme, the junction temperature of the series pass element is sensed. By sensing this, its power dissipation is reduced by using certain circuit till its temperature drops to a lower safe value.

46. What are the three waveforms generated by ICL8038?
    - Sine wave
    - Square wave
    - triangular Wave
47. List the characteristics of optocoupler

(i) Current Transfer Ratio:
(ii) Isolation voltage between input & output:
(iii) Response Time:
(iv) Common mode Rejection:

48. What is the advantage of switching regulators?

Switching regulators are highly efficient and able to step up (boost), step down (buck), and invert voltages with ease

Switching regulators are efficient because the series element is either fully conducting or switched off because it dissipates almost no power. Switching regulators are able to generate output voltages that are higher than the input voltage or of opposite polarity, unlike linear regulators.

49. What are the basic elements of voltage regulator circuit?
    - Voltage reference
    - Error amplifier
    - Feedback Network
    - Active Element
50. Name the various protection circuits used for the voltage regulators.
    - Constant current limiting
    - Foldback current limiting
    - Over voltage protection
    - Thermal protection
51. State the applications of IC LM 380
    - Audio amplifier
    - High gain audio amplifier
    - Phone amplifier
    - Intercom systems

PART B&C:

1. Explain the working principle and salient features of triangular wave generator and saw tooth wave generator. **[April/May 2018]** **[Nov/Dec 2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 220]
[Ref .S.Salivahanan &V S Kanchana Bhaskaram=n, "Linear Integrated Circuits (Second Edition)", Page 335]

2. (i) State the significant difference between fixed and adjustable voltage regulators. **[Nov/Dec 2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 241]

(ii) Design a wave generator using 555 timer for a frequency of 110Hz and 80% duty cycle.Assume C=0.16μF. (7) **[Nov/Dec 2018]**

[Ref .Roy Choudhry, ShailB.Jain, "Linear Integrated Circuits (Fourth Edition)", Page 322]

3. Discuss briefly about opto-couplers. **[April/May 2018]**

[Ref .S.Salivahanan &V S Kanchana Bhaskaram=n, “Linear Integrated Circuits (Second Edition)”, Page 542]

4. (i) With neat diagram explain the operation of an astable and monostable multivibrators **[Nov/Dec 2017]**

   [Ref .Roy Choudhry, ShailB.Jain, “Linear Integrated Circuits (Fourth Edition)”, Page 216 &318]

   (ii) Draw the functional diagram and connection diagram of a low voltage regulator and explain **[Nov/Dec 2017]**

   [Ref .Roy Choudhry, ShailB.Jain, “Linear Integrated Circuits (Fourth Edition)”, Page 241]

5. Answer any two of the following **[April/May 2017]**

   (iii) Switched capacitor filters

   [Ref .Roy Choudhry, ShailB.Jain, “Linear Integrated Circuits (Fourth Edition)”, Page 288]

   (iv) Audio power amplifier

   [Ref .Roy Choudhry, ShailB.Jain, “Linear Integrated Circuits (Fourth Edition)”, Page 322]

   (v) Opto coupler

   [Ref .Roy Choudhry, ShailB.Jain, “Linear Integrated Circuits (Fourth Edition)”, Page 322]

6. With neat diagram explain IC723 general purpose voltage regulator[May/June 14] **[April/May 16]**

   [Ref .Roy Choudhry, Shail B.Jain, “Linear Integrated Circuits (Second Edition)”, Page 272]

7. Explain Sawtooth waveform generator and LM 380Audio amplifier in detail **[April/May 16]**

   [Ref .Roy Choudhry, Shail B.Jain, “Linear Integrated Circuits (Second Edition)”, Page 247]

8. Describe the working of a astable multivibrator using 555 timer[Nov/Dec 11] **[April/May 16]**

   [Ref .Roy Choudhry, Shail B.Jain, “Linear Integrated Circuits (Second Edition)”, Page 345]

9. Explain in detail Voltage to frequency and frequency to voltage converter [May/June 14]

   . Sergio Franco, “Design with Operational Amplifiers and Analog Integrated Circuits”, 3rd Edition page 520

10. (i)Design a phase shift oscillate at 100Hz **(May/June 15)**

    [Ref .Roy Choudhry, Shail B.Jain, “Linear Integrated Circuits (Second Edition)”, Page 250]

    (ii) Describe monostable multivibrator with necessary diagrams and derive for ON time and recovery time **[May/June 15]**

    [Ref .Roy Choudhry, Shail B.Jain, “Linear Integrated Circuits (Second Edition)”, Page 337]

11. (i)Briefly describe about monolithic switching regulators **[April/May 15]**

    [Ref .Roy Choudhry, Shail B.Jain, “Linear Integrated Circuits (Second Edition)”, Page 255]

    (ii)Draw the schematic of ICL 8038 function generator and discuss its features (8) **[April/May 15]**

    [Ref .Roy Choudhry, Shail B.Jain, “Linear Integrated Circuits (Second Edition)”, Page 225]

12. Describe the working of a Astable multivibrator using op-amp [Nov/Dec 14]

    [Ref .Roy Choudhry, Shail B.Jain, “Linear Integrated Circuits (Second Edition)”, Page 241]

13. Describe the working of a monostable multivibrator using 555 timer[Nov/Dec 13]

    [Ref .Roy Choudhry, Shail B.Jain, “Linear Integrated Circuits (Second Edition)”, Page 337]

14. Explain Video amplifier and opto-couplers

    [Ref .S.Salivahanan &V S Kanchana Bhaskaram=n, “Linear Integrated Circuits (Second Edition)”, Page 542]

15. Explain the following in detail
    i. Switched capacitor filter
    ii. Isolation amplifier

[Ref .S.Salivahanan &V S Kanchana Bhaskaram=n, “Linear Integrated Circuits (Second Edition)”, Page 547]

UNIT I

BASICS OF OPERATIONAL AMPLIFIERS

Contents

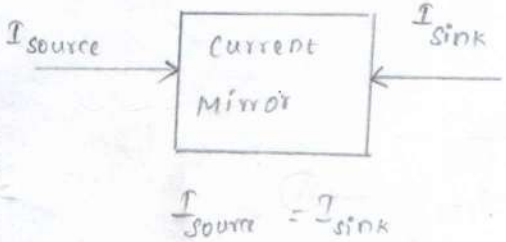
- Current mirror and current sources,
- Current sources as active loads
- Voltage sources, Voltage References,
- BJT Differential amplifier with active loads,
- Basic information about op-amps
- Ideal Operational Amplifier
- General operational amplifier stages -and internal circuit diagrams of IC 741
- DC and AC performance characteristics,
- slew rate
- Open and closed loop configurations.

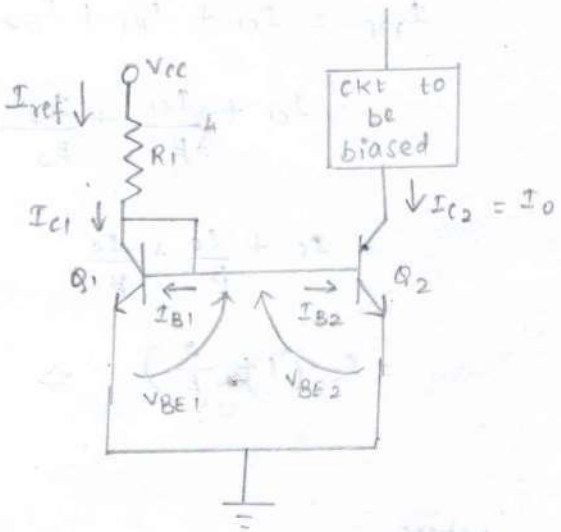
EC6404 - LINEAR INTEGRATED CIRCUITS

UNIT - 1 BASICS OF OPERATIONAL AMPLIFIERS

Current Mirror :

The Circuit in which the output current is forced to equal the input current is called as current mirror circuit. In a current mirror circuit, the output current is the mirror image of input current.





Circuit Operation :

Since the base and emitter of Q_1 & Q_2 are tied together, they have same V_{BE}. The transistor Q_1 is connected as a diode by shorting its collector to base. Since Q_1 & Q_2 are identical transistors, The emitter current of Q_1 is approximately equal to I_{ref}. Hence, $I_{C2} = I_o \simeq I_{ref}$. Since the output current (I_o) is mirror of I_{ref}, the above circuit is called as current mirror circuit.

Analysis :

WKT,

$$I_{C1} = \alpha_F I_{ES} e^{V_{BE1}/V_T} \quad -(1)$$

$$I_{C2} = \alpha_F I_{ES} e^{V_{BE2}/V_T} \quad -(2)$$

Divide ② by ①,

$$\frac{I_{C2}}{I_{C1}} = e^{(V_{BE2} - V_{BE1})/V_T} \quad -③$$

Since $V_{BE1} = V_{BE2}$, $I_{C2} = I_{C1} = I_C = I_O$ and also since both the transistors are identical, $\beta_1 = \beta_2 = \beta$.

Applying KCL at collector of Q_1,

$$I_{ref} = I_{C1} + I_{B1} + I_{B2}$$

$$= I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2}$$

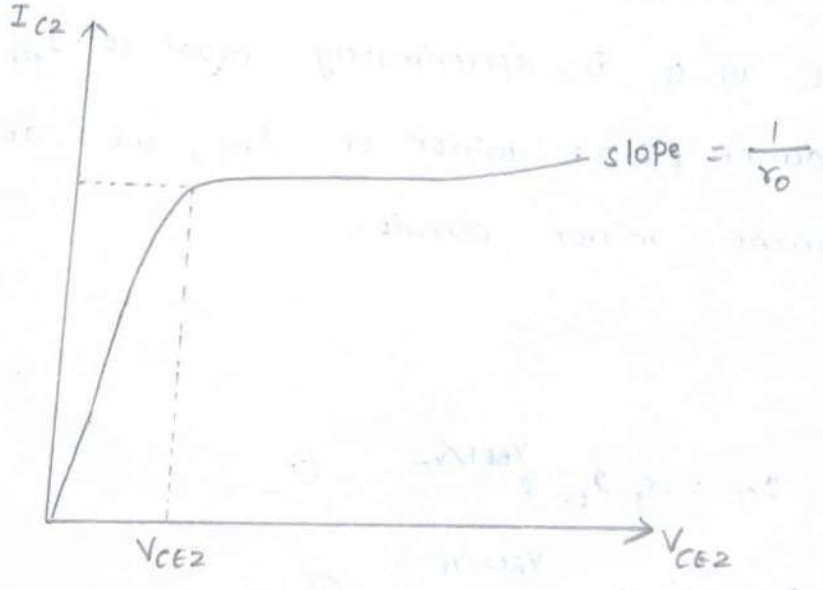
$$= I_C + \frac{I_C}{\beta} + \frac{I_C}{\beta}$$

$$= I_C \left(1 + \frac{2}{\beta}\right) \Rightarrow \boxed{I_C = \left(\frac{\beta}{2+\beta}\right) I_{ref}} \quad -④$$

where,

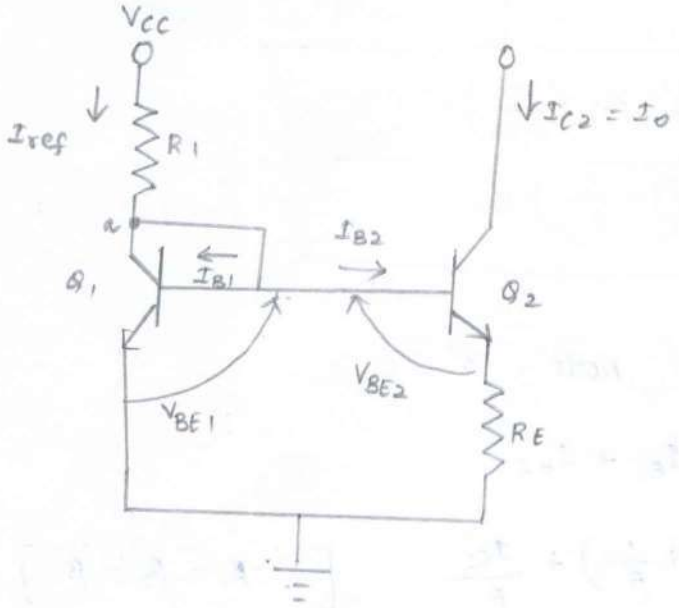
$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \simeq \frac{V_{CC}}{R_1} \quad [\text{since } V_{BE} = 0.7 \text{ which is small}]$$

In eqn ④, $\beta >> 1$ hence $\left(\frac{\beta}{2+\beta}\right) \simeq 1$ ∴ Output current (I_C) is equal to reference current (I_{ref}).



Widlar Current Sources :

In OP-AMP's, low input current is required. Hence, input stages is biased at very low current of order 5 μA. such low magnitude current can be obtained by widlar current sources.



Due to emitter resistance at Q_2, $V_{BE2} < V_{BE1}$ and hence $I_o < I_{C1}$.

Analysis :

$$\frac{I_{C1}}{I_{C2}} = e^{(V_{BE1} - V_{BE2})/V_T} \quad \text{—①}$$

Taking Natural logarithm on both sides,

$$\frac{V_{BE1} - V_{BE2}}{V_T} = \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$\therefore V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) \quad \text{—②}$$

Applying KVL at base-emitter loop,

$$V_{BE1} = V_{BE2} + (I_{B2} + I_{C2}) R_E$$

The above eqn can be rewritten as,

$$V_{BE1} - V_{BE2} = \left(\frac{1}{\beta} + 1\right) I_{C2} R_E \quad \text{— (3)}$$

From (2) & (3),

$$\left(\frac{1}{\beta} + 1\right) I_{C2} R_E = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$\boxed{R_E = \frac{V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)}{\left(1 + \frac{1}{\beta}\right) I_{C2}}}$$

Applying KCL at node 'a'.

$$I_{ref} = I_{C1} + I_{B1} + I_{B2}$$

$$= I_{C1}\left(1 + \frac{1}{\beta}\right) + \frac{I_{C2}}{\beta} \qquad \left[\because \beta_1 = \beta_2 = \beta\right]$$

In widlar current source, $I_{C2} << I_{C1}$ $\therefore$ $\frac{I_{C2}}{\beta}$ is neglected.

$$I_{ref} = I_{C1}\left(1 + \frac{1}{\beta}\right)$$

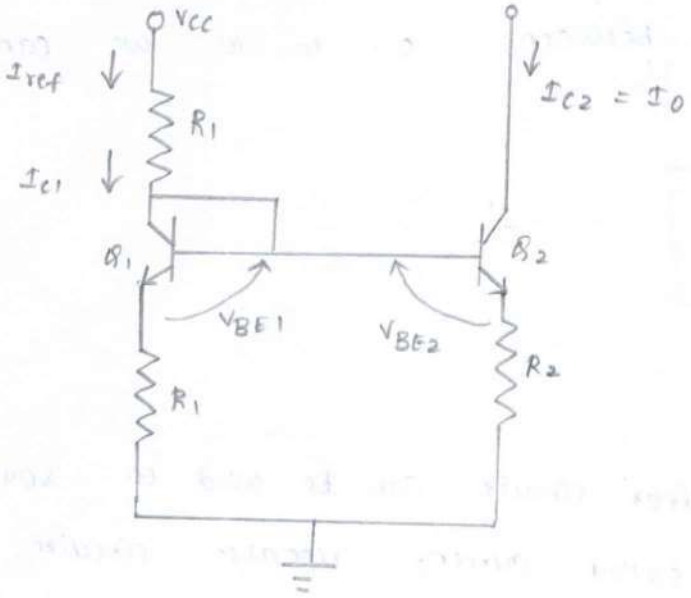
$$\boxed{I_{C1} = \left(\frac{\beta}{\beta + 1}\right) I_{ref}}$$

where $I_{ref} = \dfrac{V_{CC} - V_{BE}}{R_1}$

when $\beta >> 1$, $I_{C1} \simeq I_{ref}$.

Current Mirror With Magnifrcation :

Current mirror with magnification is the improved version of widlar circuit. sometimes it is necessary to have a circuit in which ratio of biasing currents in two transistors is required to be fixed, it is done by current mirror circuit with magnification.



Analysis :

Applying KVL at base-emitter loop,

$$V_{BE2} - V_{BE1} = I_{C1} R_1 - I_{C2} R_2 \quad [\text{neglect base current}] \quad -②$$

WKT,

$$V_{BE2} - V_{BE1} = V_T \ln\left(\frac{I_{C2}}{I_{C1}}\right) \quad -①$$

From ① & ②

$$I_{C1} R_1 - I_{C2} R_2 = V_T \ln\left(\frac{I_{C2}}{I_{C1}}\right)$$

$$\frac{I_{C2}}{I_{C1}} \frac{R_2}{R_1} = 1 - \frac{V_T}{I_{C1} R_1} \ln\left(\frac{I_{C2}}{I_{C1}}\right)$$

$$\frac{I_{C2}}{I_{C1}} = \frac{R_1}{R_2}\left(1 - \frac{V_T}{I_{C1} R_1} \ln\left(\frac{I_{C2}}{I_{C1}}\right)\right)$$

when $\frac{I_{C2}}{I_{C1}}$ lies between 0.1 to 10, we can assume that

$$\boxed{\frac{I_{C2}}{I_{C1}} \simeq \frac{R_1}{R_2}}$$

Current Repeaters :

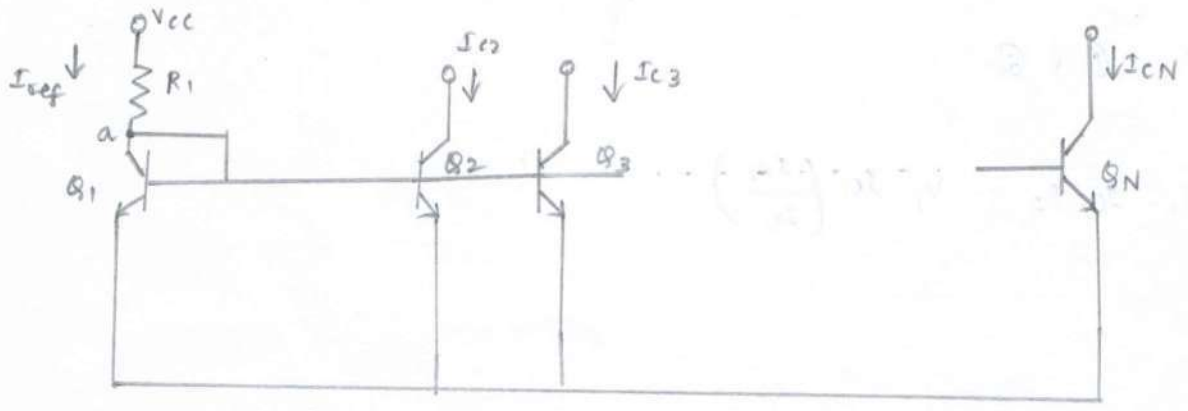
A current mirror circuit can be used to source current to more than one load is called current repeater circuits.

$$I_{ref} = I_C + I_B + N I_B$$

$$= I_C + \frac{(1+N)}{\beta} I_C$$

$$\boxed{I_{ref} = I_C \left(1 + \frac{(1+N)}{\beta}\right)}$$ where, 'N' is no of stages (transistors)

$$\therefore I_C = I_{ref} \left(\frac{\beta}{\beta+1+N}\right)$$



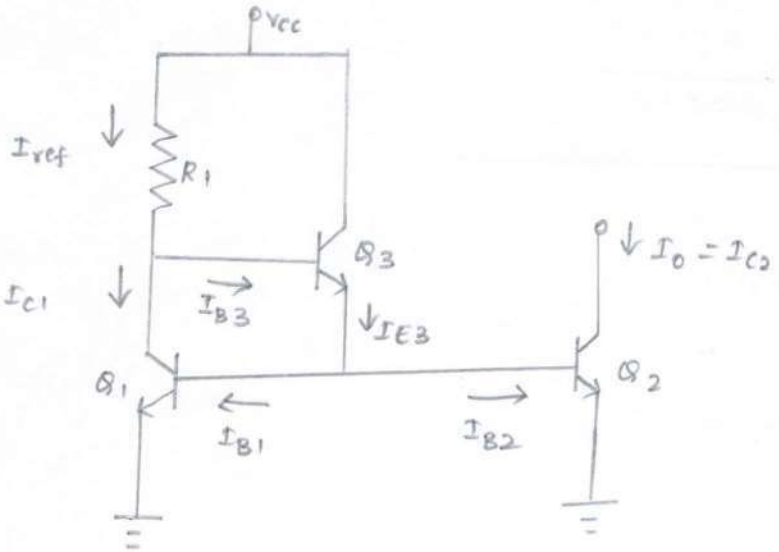
Improved Current Source with gain :

A good current source should meet the following two requirements

(i) Output current (I_o) should be independent of β.

(ii) Output resistance should be very high.

In differential amplifiers, high output resistance is required to reduce common-mode gain. To obtain high voltage gain, large output resistance is required. Improved current source with gain circuit shows that the output current is independent of β.



Analysis :

Applying KCL at node 'a',

$$I_{ref} = I_{C1} + I_{B3}$$

$$= I_{C1} + \frac{I_{E3}}{1+\beta}$$

$$= I_{C2} + \frac{I_{E3}}{1+\beta} \quad [\because I_{C1} = I_{C2} = I_o]$$

And also,

$$I_{E3} = I_{B1} + I_{B2}$$

$$= 2I_B \quad [\because Q_1, Q_2 \text{ are identical}]$$

$$\therefore I_{ref} = I_{C1} + \frac{2I_B}{1+\beta}$$

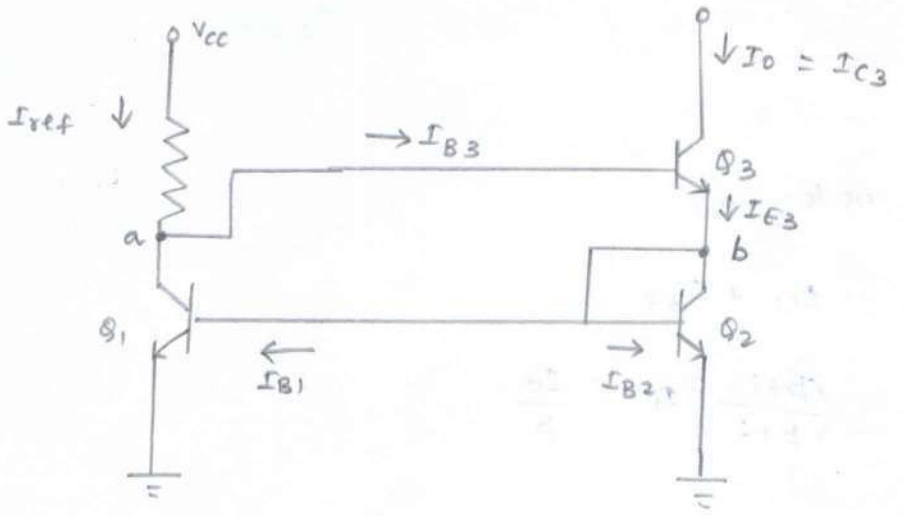
$$= I_C + \frac{2I_C}{\beta(1+\beta)}$$

$$= I_C \left(1 + \frac{2}{\beta(1+\beta)}\right)$$

$$\boxed{I_O = I_C = I_{ref}\left[\frac{\beta(1+\beta)}{\beta^2+\beta+2}\right]}$$

Wilson Current Source :

To increase output resistance, an emitter resistance is placed in both Q_1 & Q_2 transistors (or) by creating feedback path.



Since $V_{BE1} = V_{BE2}$, $I_{C1} = I_{C2}$ & $I_{B1} = I_{B2} = I_B$

Applying KCL at node 'b',

$$I_{E3} = 2I_B + I_{C2}$$

$$I_{E3} = \frac{2I_{C2}}{\beta} + I_{C2}$$

$$= I_{C2}\left(\frac{2}{\beta} + 1\right) \quad -①$$

Also,

$$I_{E3} = I_{C3} + I_{B3}$$

$$= I_{C3}\left(1 + \frac{1}{\beta}\right) \quad -②$$

equating ① & ②

$$I_{C3}\left(1 + \frac{1}{\beta}\right) = I_{C2}\left(\frac{2}{\beta} + 1\right)$$

$$\therefore I_{C3} = I_O = I_{C2}\left(\frac{2+\beta}{1+\beta}\right) \quad -③$$

since $I_{C1} = I_{C2}$,

$$\boxed{I_O = I_{C1}\left(\frac{2+\beta}{1+\beta}\right)}$$

Applying KCL at node 'a',

$$I_{ref} = I_{C1} + I_{B3}$$

$$= \left(\frac{\beta+1}{\beta+2}\right) I_O + \frac{I_O}{\beta}$$

$$= I_O\left[\frac{\beta^2+2\beta+2}{\beta^2+2\beta}\right]$$

$$\boxed{I_O = \left[\frac{\beta^2+2\beta}{\beta^2+2\beta+2}\right] I_{ref}}$$

where, $I_{ref} = \dfrac{V_{CC} - 2V_{BE}}{R_1}$

$$\boxed{I_O - I_{ref} = \frac{2}{\beta^2+2\beta+2} I_{ref}}$$

Voltage References :

A voltage reference circuit is basically used to provide a constant D.C voltage which acts as a reference for other circuits. The basic requirements of any voltage reference circuits are accuracy and stability with temperature and time. Temperature coefficient is the important characteristics of voltage reference.

$$\text{Temperature Coefficient} = \frac{\Delta V_o}{\Delta T} \text{ mV/°C (or) } \mu\text{V/°C}.$$

In percentage form it is expressed as,

$$\%\ TC = 100 \left[\frac{\Delta V_o / V_o}{\Delta T} \right] \%/^{\circ}C.$$

Performance Parameters

① Line Regulation :

$$= \frac{\Delta V_o}{\Delta V_i}$$

$$\%\ \text{line regulation} = 100 \left[\frac{\Delta V_o / V_o}{\Delta V_i} \right] \text{ mV/V}$$

② Load Regulation :

$$= \frac{\Delta V_o}{\Delta I_L}$$

$$\%\ \text{load regulation} = 100 \left[\frac{\Delta V_o / V_o}{\Delta I_L} \right] \%/\text{mA}$$

③ Long-term Stability :-

The ability of a circuit to maintain the output voltage constant with respect to time is called long-term stability.

④ Ripple Rejection Ratio :-

$$= 20 \log_{10} \left(\frac{V_{ri}}{V_{ro}} \right)$$

V_{ri} = input ripple magnitude

V_{ro} = Output ripple magnitude

Voltage Reference Circuit Using Avalanche Diode Reference :-

The supply voltage provides bias to Q_1 and d.c current for biasing of D_A, D_1, D_2. The base voltage V_B is the sum of V_A, V_{D1} & V_{D2}.

Applying KVL through V_{BE1}, R_2, V_{BE1} & V_B,

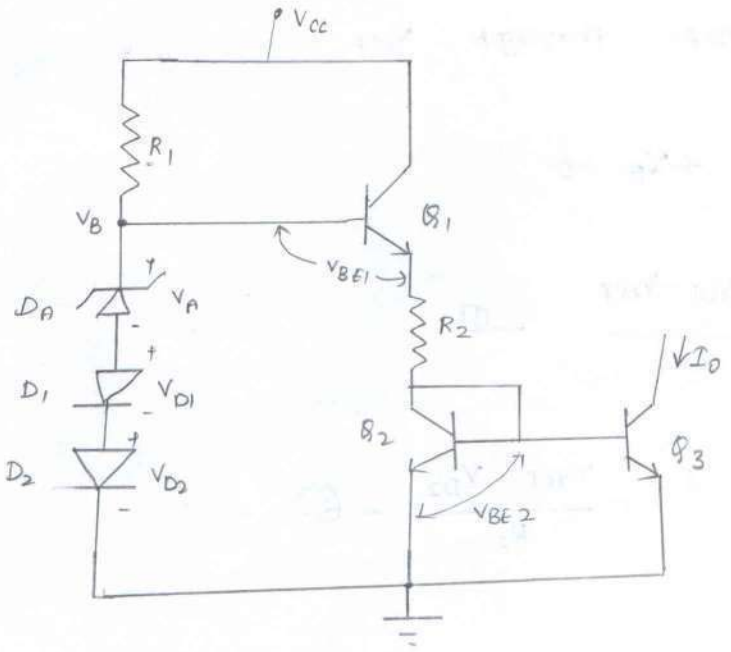
Drop across $R_2 = V_B - V_{BE1} - V_{BE2}$

but $V_B = V_A + V_{D1} + V_{D2}$

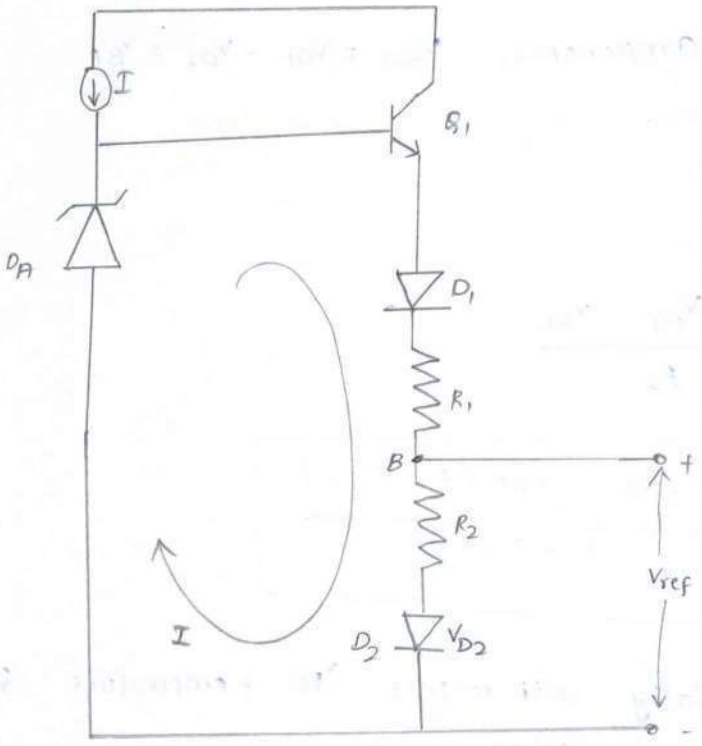
Since $V_{D1} = V_{D2} = V_{BE1} = V_{BE2}$ drop across R_2 is equal to drop across V_A. Due to current mirror, the Output current is equal to current through R_2,

$$I_0 = \frac{\text{drop across } R_2}{R_2} = \frac{V_A}{R_2}$$

By adding two diodes in series with R_2, zero temperature Coefficient can be achieved.



Voltage Reference Circuit using temperature Compensation :-



Diodes D_1, D_2 are conventional diodes and D_A is avalanche diode. The Diode D_A is supplied with current source I and it provides base voltage V_B to Q_1.

Applying KVL to two loops through V_{ref}

$$-V_{BE1} - V_{D1} - IR_1 - V_{ref} + V_B = 0$$

$$\therefore I = \frac{V_B - V_{BE1} - V_{D1} - V_{ref}}{R_1} \quad -①$$

$$-I_{R2} - V_{D2} + V_{ref} = 0 \quad \therefore I = \frac{V_{ref} - V_{D2}}{R_2} \quad -②$$

Equating ① & ②

$$\frac{V_B - V_{BE1} - V_{D1} - V_{ref}}{R_1} = \frac{V_{ref} - V_{D2}}{R_2} \quad -③$$

with matched components, $V_{BE1} = V_{D1} = V_{D2} = V_{BE}$

$\therefore$ Eqn ③ becomes,

$$\frac{V_B - 2V_{BE} - V_{ref}}{R_1} = \frac{V_{ref} - V_{BE}}{R_2}$$

$$\therefore \boxed{V_{ref} = \frac{R_2 V_B + V_{BE}(R_1 - 2R_2)}{R_1 + R_2}}$$

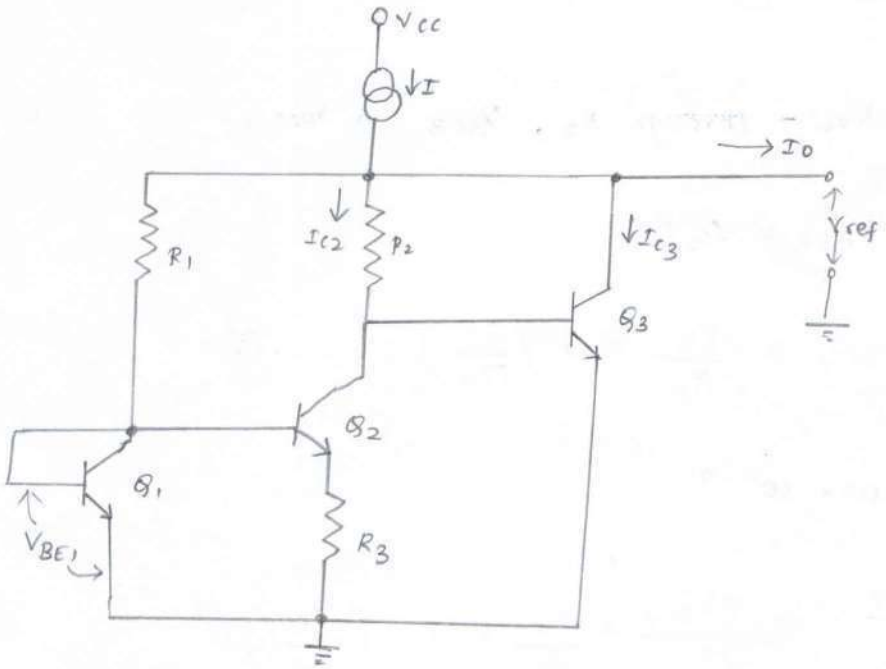
Diff V_B & V_{BE} partially with respect to temperature & for zero temperature coefficient, $\frac{\partial V_{ref}}{\partial T} = 0$

$$\therefore 0 = \left(\frac{R_2}{R_1+R_2}\right)\frac{\partial V_B}{\partial T} + \frac{(R_1 - 2R_2)}{R_1+R_2}\frac{\partial V_{BE}}{\partial T}$$

$$\therefore \boxed{\frac{\partial V_B/\partial T}{\partial V_{BE}/\partial T} = \frac{2R_2 - R_1}{R_2}}$$

Bandgap voltage Reference :

Using avalanche diode reference circuits is not possible for low supply voltage circuits. Hence, bandgap reference circuits are used.



$$\frac{I_{C1}}{I_{C2}} = e^{(V_{BE1}-V_{BE2})/V_T}$$

$$\ln\left(\frac{I_{C1}}{I_{C2}}\right) = \frac{V_{BE1} - V_{BE2}}{V_T}$$

$$\therefore V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$\boxed{V_{R3} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)} \quad -① \quad \left[\because V_{BE1} - V_{BE2} = \Delta V_{BE} = V_{R3}\right]$$

Neglecting base current of Q_2

$$I_{C2} = R_3$$

$$I_{R3} = \frac{V_{R3}}{R_3} = \frac{V_T \ln\left(I_{C1}/I_{C2}\right)}{R_3}$$

$$\boxed{I_{R3} = \frac{V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)}{R_3}} \quad \text{— (2)}$$

Applying KVL through R_2, V_{BE3} & V_{REF},

$$V_{ref} = V_{BE3} + I_{C2} R_2$$

$$V_{ref} = V_{BE3} + \frac{R_2}{R_3} V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) \quad \text{— (3)}$$

diff (3) w.r to T

$$TC = \frac{\partial V_{ref}}{\partial T} = \frac{\partial V_{BE3}}{\partial T} + \frac{R_2}{R_3} k \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$TC(V_{BE}) = \frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (V_{G0} + 3V_T)}{T}$$ where V_{G0} is bandgap voltage at absolute zero temperature

$$\therefore TC(V_{BE}) = -\left[\frac{V_{G0} - V_{BE}}{T} + 3k\right]$$

$$TC(V_{BE3}) = -\frac{R_2}{R_3} k \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$-\frac{V_{G0} - V_{BE}}{T} + 3k = \frac{R_2}{R_3} k \ln\left(\frac{I_{C1}}{I_{C2}}\right) \quad \text{— (4)}$$

Multiply by 'T' on both sides in (4) & assume $V_T = kT$ we have

$$V_{BE} = V_{G0} + 3V_T - \frac{R_2}{R_3} V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

sub above in (3)

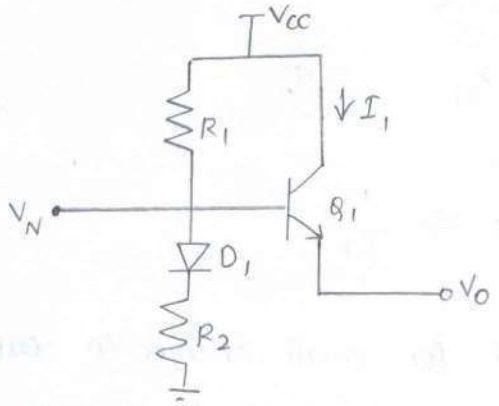
$$\boxed{V_{ref} = V_{G0} + 3V_T}$$

Voltage Sources

The voltage source circuit is dual of constant current source. A voltage source produces an output voltage which is independent of load driven by voltage source. There are two methods to produce voltage source namely,

* using amplifier with feedback
* using Impedance transformation property of transistor.

(i) Common-collector (or) voltage follower voltage source :

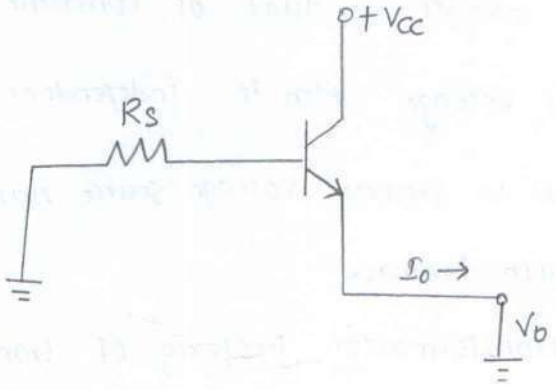


This circuit is suitable for differential gain stage in op-amp. The low output impedance of common-collector stage simulates low impedance voltage-source with output voltage (V_O) is given by,

$$V_O = \left(\frac{R_2}{R_1+R_2}\right)V_{CC}$$

The diode 'D_1' is used for offsetting the effect of DC value across V_{BE} and for compensating temperature of V_{BE} drop of Q_1.

(ii) Voltage Source Circuit Using Impedance Transformation :



The voltage source (V_s) drives the base of transistor through R_s and output is taken across the emitter.

$$R_o = \frac{dV_o}{dI_o} = \left(\frac{R_s}{\beta+1}\right) + r_{eb} \quad \text{—①}$$

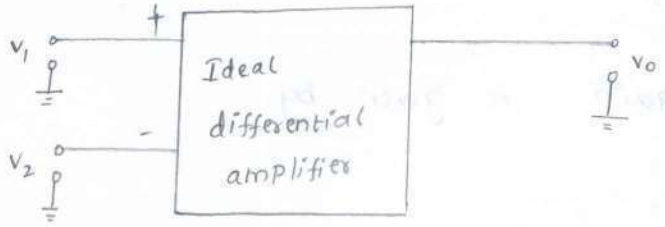
when $\beta > 100$, $R_s \Rightarrow \frac{R_s}{\beta+1}$

Eqn ① is applicable only for small changes in output current. The load regulation parameter indicates the change in V_o resulting from large changes in output current I_o. Reduction in V_o occurs as I_o goes from no-load to full-load.

Differential Amplifiers

Introduction :

Differential amplifier amplifies the difference between two input voltage signals.



let V_1 & V_2 are two input signals while V_o is single ended output. In ideal differential amplifier, the output voltage (V_o) is proportional to the difference between two input signals. (ie) $V_o \propto (V_1 - V_2)$ —①

Differential Gain (Ad) :

From ①,

$$V_o = A_d (V_1 - V_2)$$

where 'A_d' is differential gain.

$$\boxed{A_d = \frac{V_o}{V_d}}$$

Differential gain is expressed in decibel (dB) as

$$\boxed{A_d = 20 \log_{10} (A_d)}$$

Common Mode Gain (A_c) :

When two input voltages are equal, the output voltage must be zero. The common mode signal is the average level of two input signals.

$$V_c = \frac{V_1 + V_2}{2}$$

Common mode gain is given by

$$V_o = A_c V_c$$

The total output of any differential amplifier is

$$\boxed{V_o = A_d V_d + A_c V_c}$$

Common Mode Rejection Ratio (CMRR) :

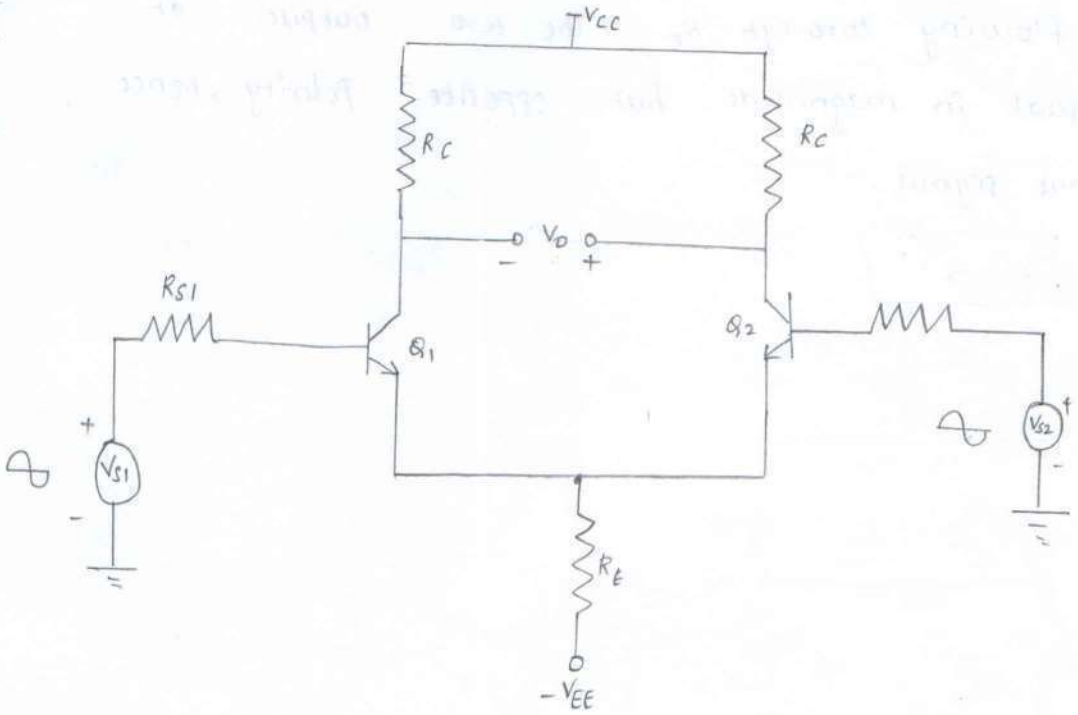
The ability of a differential amplifier to reject common mode signal is called as common mode rejection ratio. It is the ratio of differential voltage gain to common mode gain

$$CMRR = \rho = \left| \frac{A_d}{A_c} \right|$$

Features of Differential Amplifier :

* High differential voltage gain
* Low Common Mode gain
* High CMRR
* Large Bandwidth

Working Principle of Differential Amplifier :



BJT differential amplifier uses emitter biased circuit with two identical transistors. The base B_1 of Q_1 is connected to input 1 which is V_{S1} while base B_2 of Q_2 is connected to input 2 which is V_{S2}. The balanced output is taken from collectors of two transistors. this amplifier is called as emitter coupled differential amplifier.

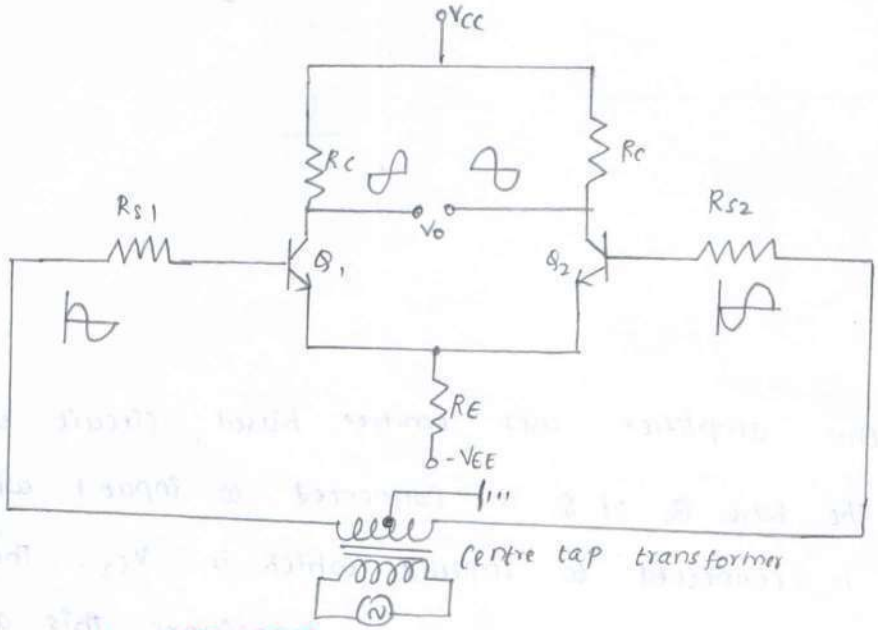
Differential Mode Operation :

The two input signals are different from each other.

let us assume that the two inputs are equal in magnitude but 180° out of Phase. This Phase shift can be obtained by using centre-tap transformer. With a positive going signal on Q_1 produces an amplified negative going signal. Due to positive going signal, Current through R_E increases and hence a positive going wave is Produced across R_E.

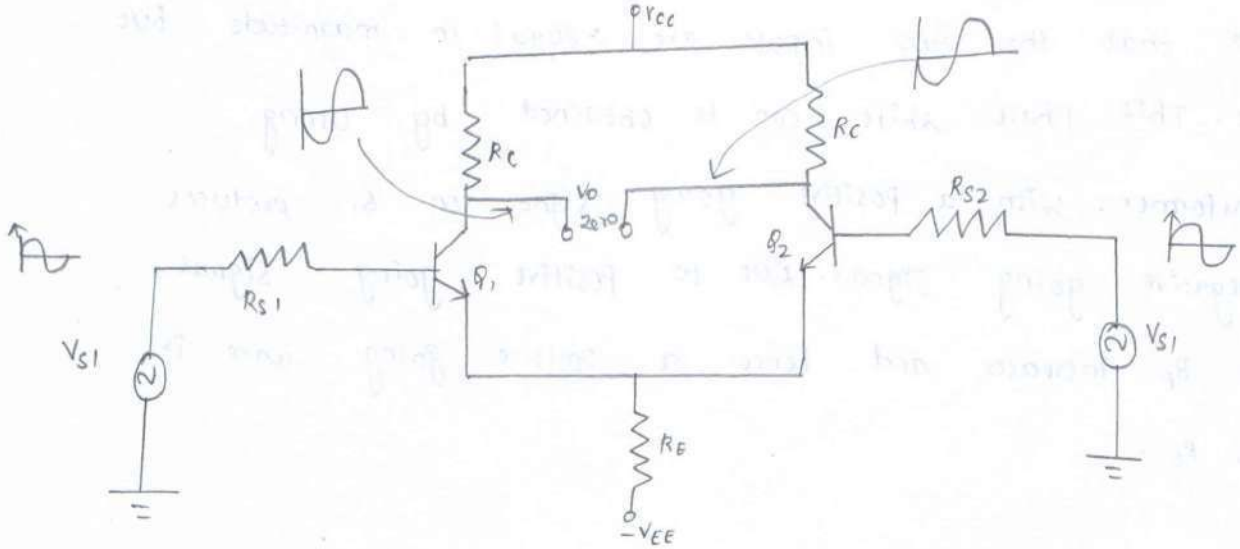
Due to negative going signal on Q_2, an amplified positive going signal is produced at collector of Q_2. Hence there is no A.C. signal current flowing through R_E. The two outputs at the collector are equal in magnitude but opposite polarity, hence 'V_o' is twice of input signal.

$$V_o = 2V_i$$



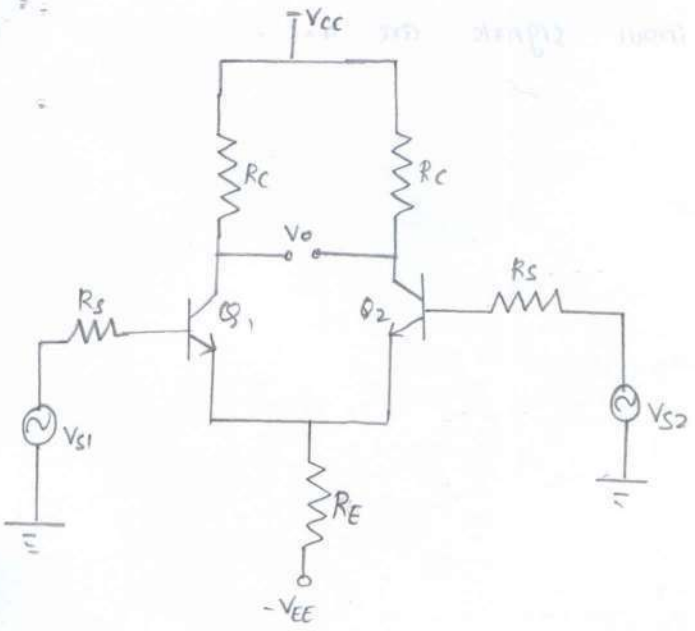
Common Mode Operation :

In this mode, the two input signals are equal in magnitude & phase. Here R_E carries a signal current and provides negative feedback. The output voltage in common mode operation is almost zero. In ideal case, it should be zero.

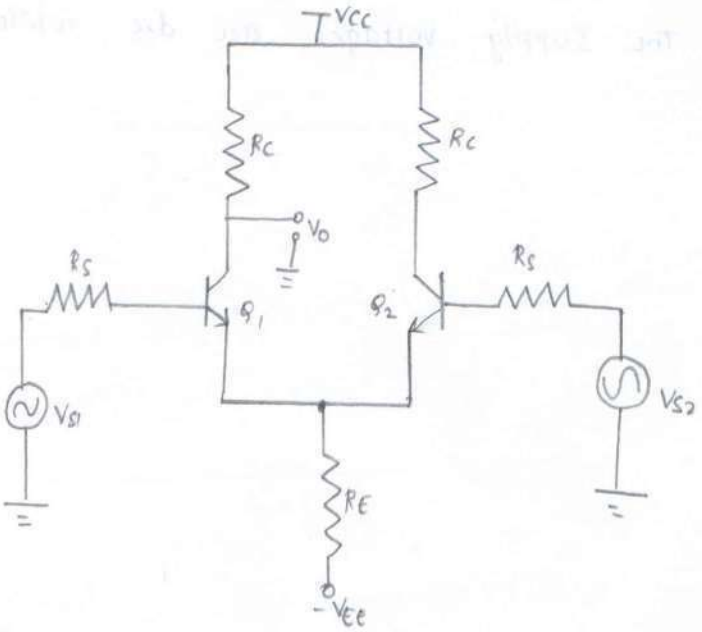


Types Of Differential Amplifier

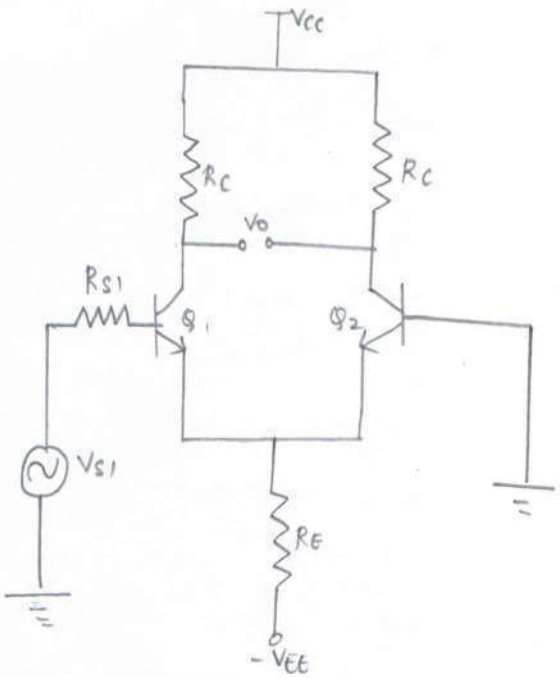
Dual input balanced output



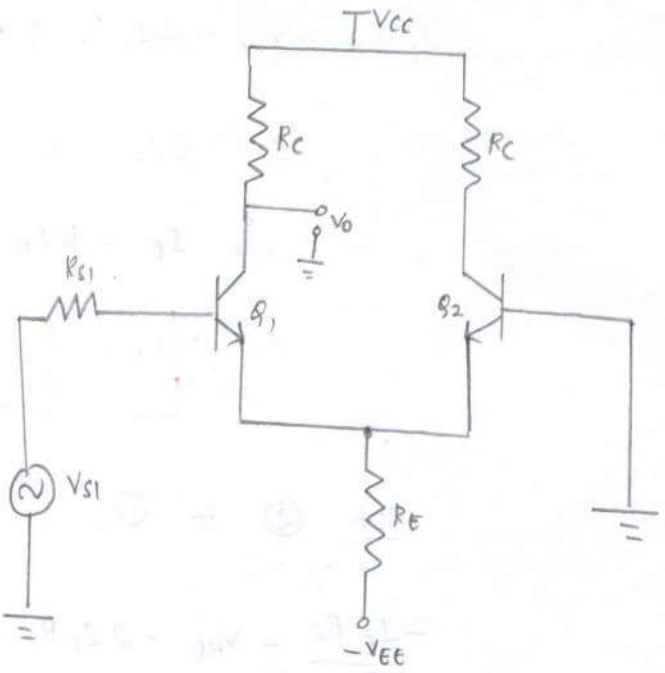
Dual input unbalanced Output



Single input balanced Output

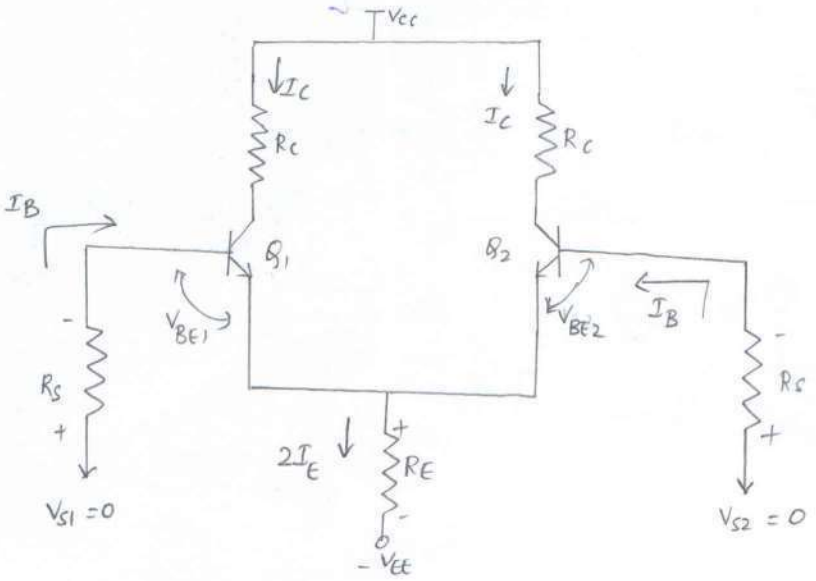


Single input unbalanced Output



D.C Analysis Of Differential Amplifier :

To obtain D.C analysis, two identical transistors are used. The supply voltages are d.c while input signals are a.c.



Apply KVL to base-emitter loop of Q_1,

$$-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad \text{—(1)}$$

$$I_C = \beta I_B \quad \& \quad I_C \simeq I_E$$

$$\therefore I_E = \beta I_B$$

$$\therefore \boxed{I_B = \frac{I_E}{\beta}} \quad \text{—(2)}$$

Sub (2) in (1),

$$-\frac{I_E R_S}{\beta} - V_{BE} - 2I_E R_E + V_{EE} = 0$$

$$\therefore I_E \left[-\frac{R_S}{\beta} - 2R_E \right] + V_{EE} - V_{BE} = 0$$

$$\therefore \boxed{I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E}} \quad \text{—(3)}$$

where, V_{BE} = 0.6 – 0.7V for silicon
0.2V for Germanium.

Generally $\frac{R_s}{\beta} << 2R_E$

$$\therefore I_E = \frac{V_{EE} - V_{BE}}{2R_E}$$

Since $I_E = I_C = I_{CQ}$ we get

$$I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E}$$

V_{CE} is given by,

$$V_{CE} = V_C - V_E$$
$$= (V_{CC} - I_C R_C) - (-V_{BE})$$

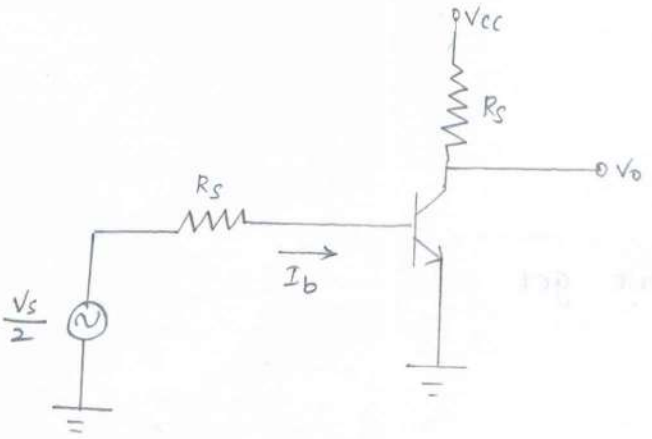
$$V_{CE} = V_{CC} - I_C R_C + V_{BE}$$

Since $V_{CE} = V_{CEQ}$ we get

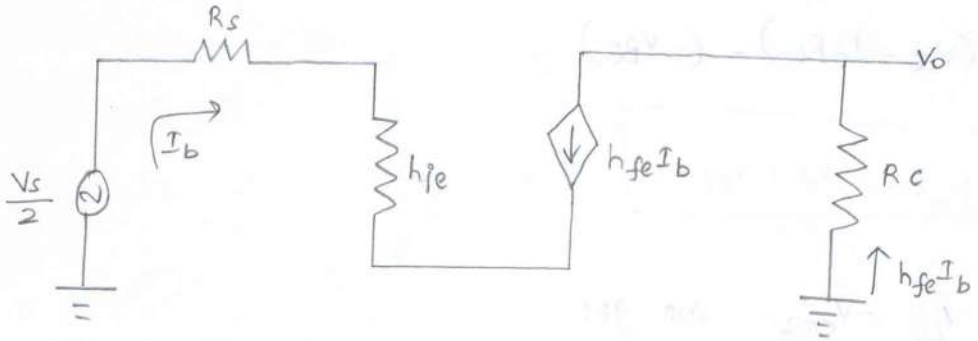
$$V_{CEQ} = V_{CC} - I_C R_C + V_{BE}$$

A.C Analysis Of Differential Amplifier :

(i) Differential Gain (Ad) :



As the two transistors are matched, the a.c equivalent circuit for differential amplifier can be analysed by considering only one transistor. This is called as half-circuit analysis.



Applying KVL to input loop,

$$-I_b R_s - I_b h_{ie} + \frac{V_s}{2} = 0$$

$$\therefore\ -I_b (R_s + h_{ie}) = -\frac{V_s}{2}$$

$$\therefore\ \boxed{I_b = \frac{V_s}{2(R_s + h_{ie})}} \quad -(1)$$

Applying KVL to output loop,

$$V_o = -h_{fe} I_b R_c \quad \text{— (2)}$$

Sub (1) in (2)

$$V_o = -h_{fe} R_c \frac{V_s}{2(R_s + h_{ie})}$$

$$\frac{V_o}{V_s} = \frac{-h_{fe} R_c}{2(R_s + h_{ie})}$$

The magnitude of differential gain is given by,

$$A_d = \frac{V_o}{V_s} = \frac{h_{fe} R_c}{2(R_s + h_{ie})}$$

This differential gain is for balanced output but, for unbalanced output, the gain is twice that of gain of balanced output.

$$\therefore A_d = 2 \times \frac{h_{fe} R_c}{2(R_s + h_{ie})}$$

$$A_d = \frac{h_{fe} R_c}{(R_s + h_{ie})}$$

ii) Common Mode Gain :

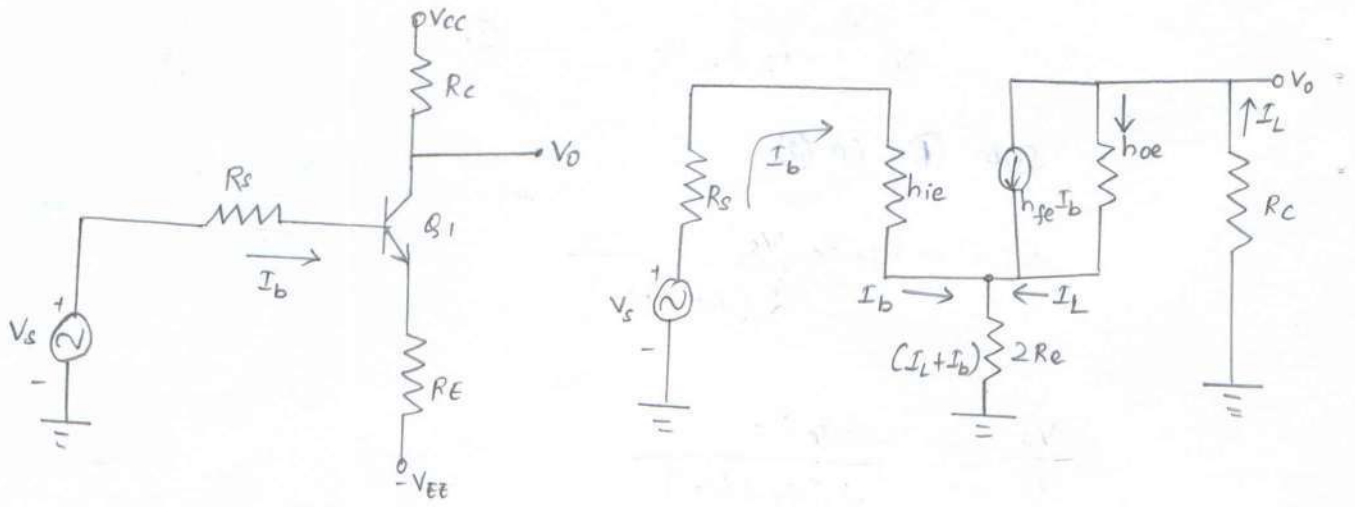
$$V_c = \frac{V_1 + V_2}{2} = \frac{V_s + V_s}{2} = V_s$$

The Output is expressed as,

$$V_o = A_c V_s$$

$$\therefore A_c = \frac{V_o}{V_s}$$

Now $I_{E1} = I_{E2} = I_E$, hence total current flowing through R_E is $2I_E$.



Applying KVL at input side,

$$-I_b R_S - I_b h_{ie} - 2R_E (I_L + I_b) + V_S = 0$$

$$\therefore V_S = I_b (R_S + h_{ie} + 2R_E) + I_L (2R_E) \quad -(1)$$

while $V_O = -I_L R_C$.

Applying KVL at output side,

$$\frac{-(I_L - h_{fe} I_b)}{h_{oe}} - 2R_E (I_L + I_b) - I_L R_C = 0$$

$$I_b \left[\frac{h_{fe}}{h_{oe}} - 2R_E \right] = I_L \left[\frac{1}{h_{oe}} + 2R_E + R_C \right]$$

$$\therefore \frac{I_L}{I_b} = \frac{h_{fe} - 2R_E h_{oe}}{\left[1 + h_{oe} (2R_E + R_C) \right]} \quad -(2)$$

Sub (2) in (1) in the place of I_b

$$V_S = \frac{I_L\left[1+h_{oe}(2R_E+R_C)\right](R_S+h_{ie}+2R_E)}{h_{fe}-2R_E h_{oe}} + I_L(2R_E)$$

$$\frac{V_S}{I_L} = \frac{\left[1+h_{oe}(2R_E+R_C)\right](R_S+h_{ie}+2R_E)}{h_{fe}-2R_E h_{oe}} + 2R_E$$

calculate LCM,

$$\frac{V_S}{I_L} = \frac{2R_E(1+h_{fe}) + R_S(1+h_{oe}2R_E) + h_{ie}(1+2R_E h_{oe}) + h_{oe}R_C\left[2R_E+R_S+h_{ie}\right]}{h_{fe}-2R_E h_{oe}}$$

Neglecting $h_{oe}R_C$ terms,

$$\frac{V_S}{I_L} = \frac{2R_E(1+h_{fe}) + (R_S+h_{ie})(1+2R_E h_{oe})}{h_{fe}-2R_E h_{oe}}$$

Sub I_L in V_O

$$V_O = \frac{-V_S(h_{fe}-2R_E h_{oe})R_C}{2R_E(1+h_{fe}) + (R_S+h_{ie})(1+2R_E h_{oe})}$$

$$A_C = \frac{V_O}{V_S} = \frac{-h_{fe}R_C}{R_S+h_{ie}+2R_E(1+h_{fe})}$$

iii) CMRR :

$$CMRR = \left|\frac{A_d}{A_C}\right|$$

$$= \frac{R_S+h_{ie}+2R_E(1+h_{fe})}{(R_S+h_{ie})}$$

(iv) Input Resistance :

Input Resistance R_i is given by

$$R_i = 2(R_s + h_{ie})$$

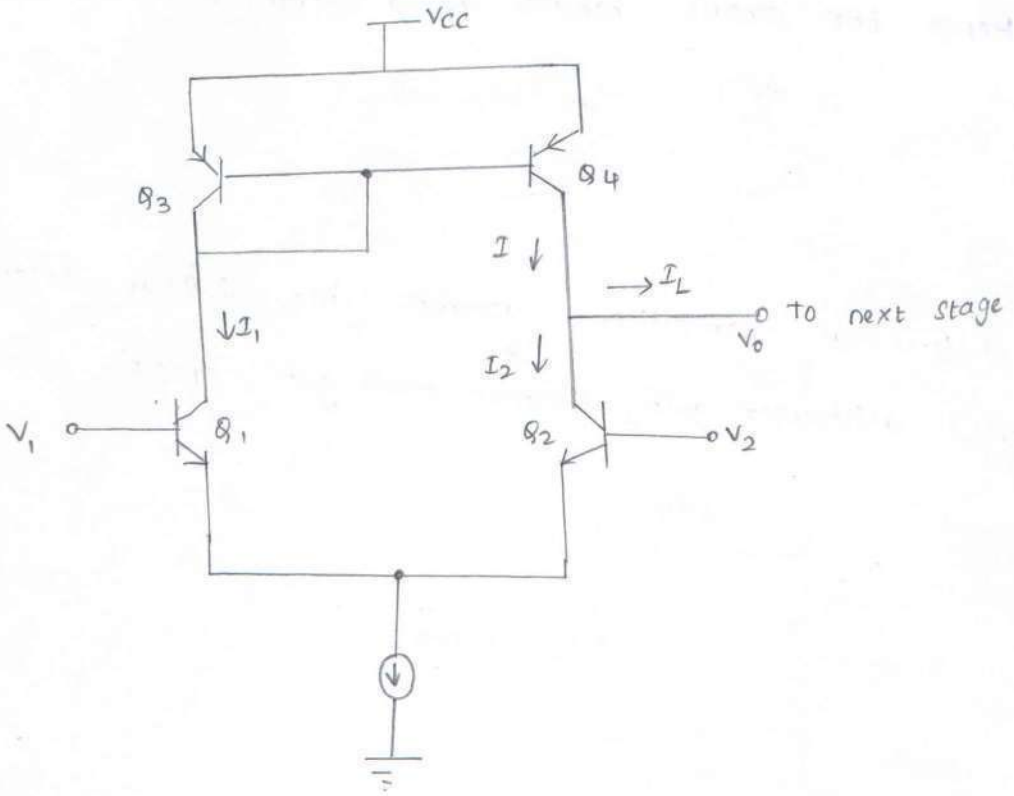
(v) Output Impedance :

It is the equivalent resistance between one of the Output terminals with respect to ground.

$$R_o = R_c$$

Differential Amplifier with active loads :

The open circuit voltage gain should be as large as Possible by cascading gain stages. But this method increases Phase shift. Another alternative way is to use large Collector resistance. But increasing R_C increases chip area and increases Power supply required for maintaining given quiescent collector current. To overcome these drawbacks, a current Source is placed as a load to differential amplifier.



The current mirror uses PnP transistors Q_3 & Q_4. The Constant current (I_Q) may also be Obtained from a current mirror. Since Q_1 & Q_2 are identical transistors,

$$I_1 = I_2 = \frac{I_Q}{2}$$ where I_B is neglected.

Since Q_3 & Q_4 forms a current mirror

$$I_1 = I_2 = I$$

The load current is calculated by

$$I_L = I - I_2 = 0$$

$$= I_1 - I_2$$

$$= g_m V_1 - g_m V_2$$

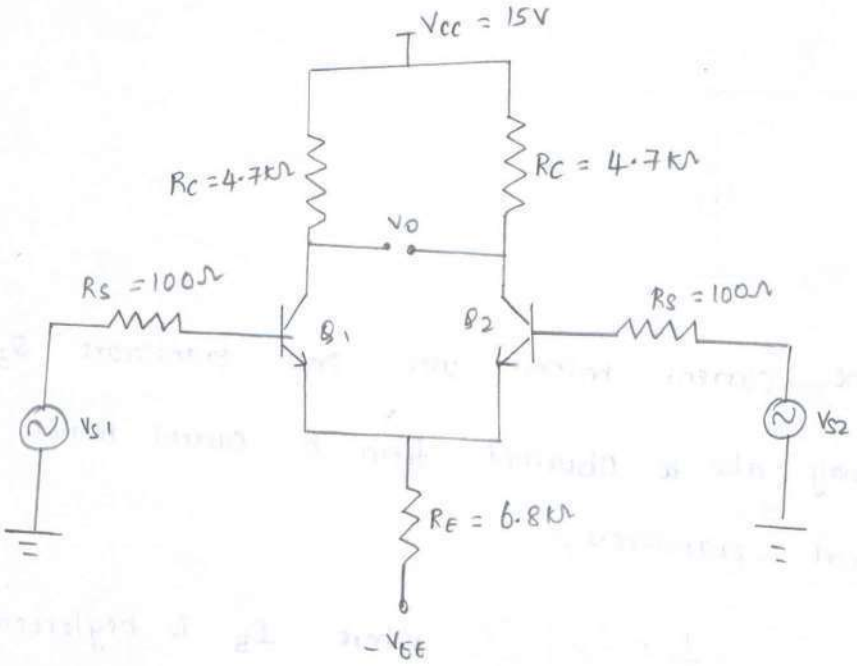
$$= g_m (V_1 - V_2)$$

$$\boxed{I = g_m V_d}$$

Hence the circuit behaves as a transconductance amplifier

PROBLEMS

1) For the given differential amplifier assume $h_{ie} = 2.8\,k\Omega$. Calculate operating point values, differential gain, common mode gain, CMRR.



Solution :

As the transistors are silicon,

$$V_{BE} = 0.7V$$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_S}{\beta}}$$

given $\beta = h_{fe} = 100$

$$\therefore I_E = \frac{15 - 0.7}{2 \times 6.8 \times 10^3 + \frac{100}{100}}$$

$$I_E = 1.051 mA$$

Here $I_C = I_E = I_{CQ}$

$$\therefore \boxed{I_{CQ} = 1.051 mA}$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C$$

$$= 15 + 0.7 - (1.051 \times 10^{-3} \times 4.7 \times 10^3)$$

$$\boxed{V_{CE} = 10.758 V}$$

Differential gain $A_d = \frac{h_{fe} R_C}{R_S + h_{ie}} = \frac{100 \times 4.7 \times 10^3}{100 + 2.8 \times 10^3}$

$$\boxed{A_d = 162.068}$$

Common Mode gain $A_c = \frac{h_{fe} R_C}{2R_E(1 + h_{fe}) + R_S + h_{ie}} = \frac{100 \times 4.7 \times 10^3}{2 \times 6.8 \times 10^3 (1 + 100) + 100 + 2.8 \times 10^3}$

$$\boxed{A_c = 0.3414}$$

$$CMRR = \frac{A_d}{A_c} = \frac{162.068}{0.3414}$$

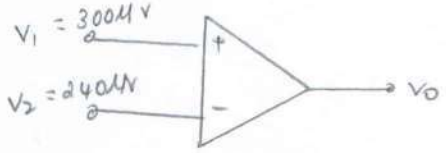
$$\boxed{CMRR = 474.652}$$

In dB, $CMRR = 20 \log (474.652)$

$$\boxed{CMRR = 53.52 \text{ dB}}$$

2) Determine the output voltage of differential amplifier for an input 300μV & 240μV. Ad is given as 5000. Calculate Ac for CMRR of 10^5.

Solution :



WKT,

$$CMRR = \frac{A_d}{A_c}$$

$$10^5 = \frac{5000}{A_c}$$

$$\boxed{A_c = 0.05}$$

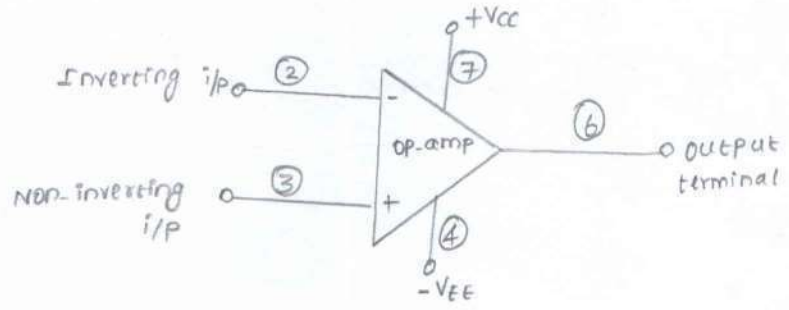
The output voltage is given by

$$V_o = A_d V_d + A_c V_c$$

$$= 5000 \times 60 + 0.05 \times 270$$

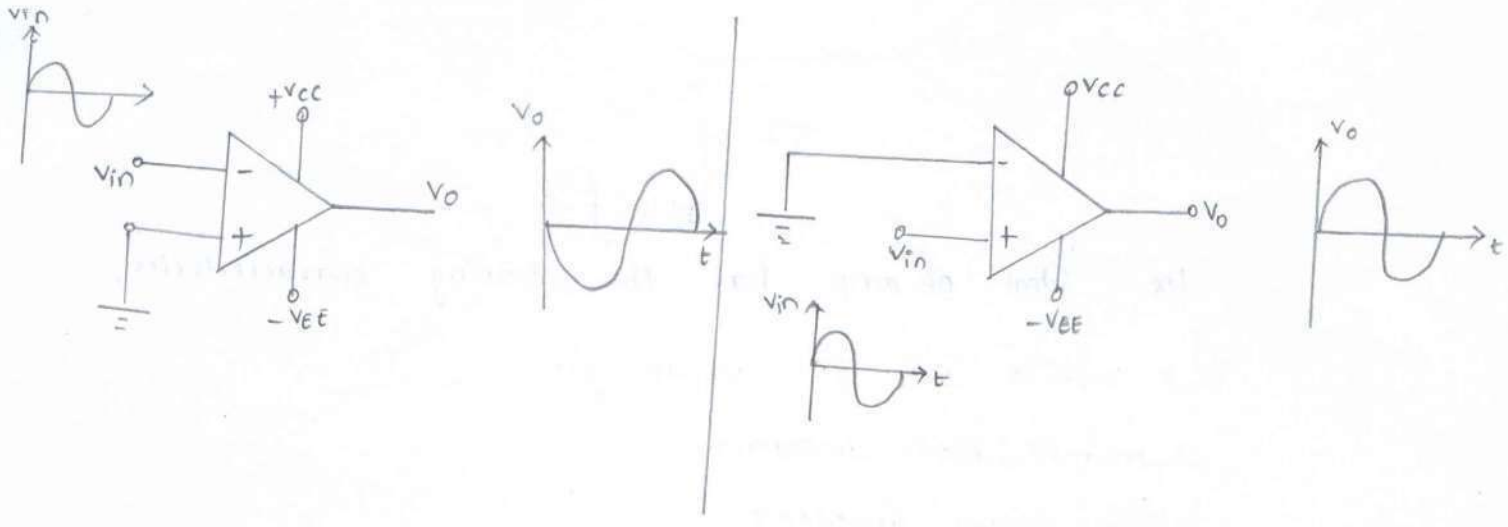
$$\boxed{V_o = 300.01 \text{ mV}}$$

Basic Information about OP-AMP :



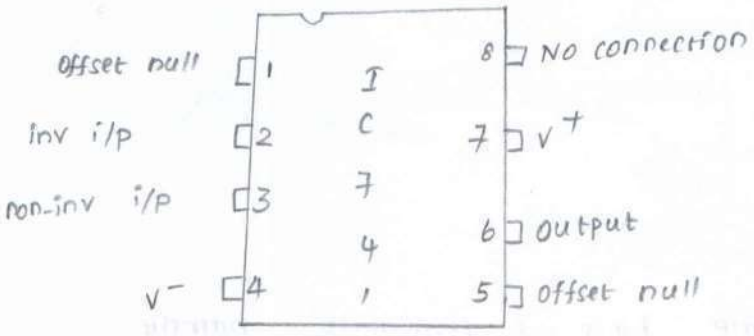
The OP-AMP have 5-terminals namely,

* Positive supply voltage terminal ($+V_{cc}$)
* Negative supply voltage terminal ($-V_{EE}$)
* Output terminal
* Inverting input terminal
* Non-inverting input terminal.



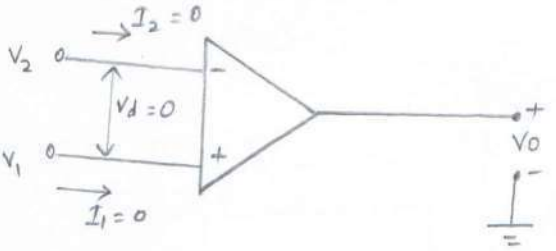
The OP-amp works on dual supply. A dual supply consist of two supply voltages both d.c, whose middle point is generally the ground terminal. If the two voltages V_{cc} & $-V_{EE}$ are same, it is called balanced power supply. If the two voltages are different, it is called unbalanced power supply.

Pin Diagram of IC741 :



Ideal operational Amplifier :

The ideal OP-amp is basically an amplifier which amplifies the difference between two input signals.



The ideal OP-amp has the following characteristics,

* Infinite open loop voltage gain
* Infinite input impedance
* zero output impedance
* Infinite Bandwidth
* zero Offset voltage
* Infinite slew rate

Slew rate :

Slew rate is defined as maximum rate of change of output voltage with respect to time.

$$\text{Slew rate} = S = \left.\frac{dV_o}{dt}\right|_{\text{maximum}}$$

Power Supply Rejection Ratio :

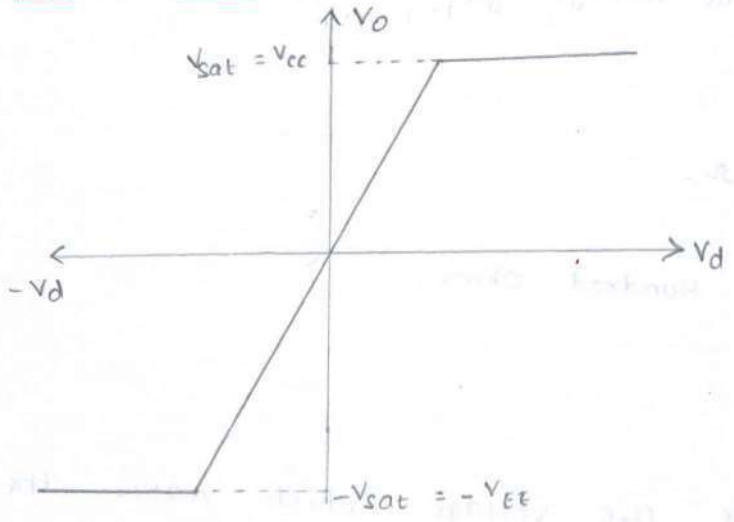
It is the ratio of change in input offset voltage due to change in supply voltage.

$$PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{cc}}\right|_{V_{EE} = \text{constant}}$$

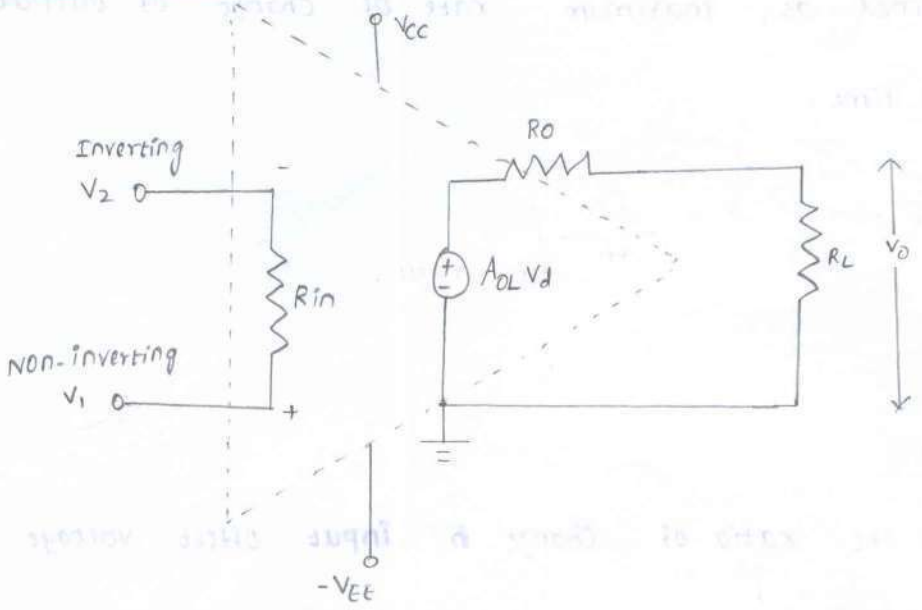
For a fixed V_{cc},

$$PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{EE}}\right|_{V_{cc} = \text{constant}}$$

Ideal voltage Transfer Curve :



Equivalent Circuit of OP-Amp :



$$V_o = A_{OL} V_d$$

$$\boxed{V_o = A_{OL} (V_1 - V_2)}$$

The output voltage is directly proportional to V_d. The voltage source $A_{OL} V_d$ is the thevenin's equivalent voltage source while R_o is thevenin's equivalent resistance.

Practical OP-Amp characteristics :

(i) Open loop gain :- It is the voltage gain of op-amp when no feedback is applied.

(ii) Input impedance :- $> 1 M\Omega$.

(iii) Output impedance :- Few Hundred Ohms.

(iv) Bandwidth :- very small

(v) Input offset voltage :- The D.C voltage which makes the output voltage zero, when other terminals are grounded is called as input offset voltage.

(vi) Input bias current :- when the two transistors of differential amplifier are not biased correctly, they conduct a small d.c current which is called as input bias current.

$$I_b = \frac{|I_{b1}| + |I_{b2}|}{2}$$

(vii) Input offset current :-

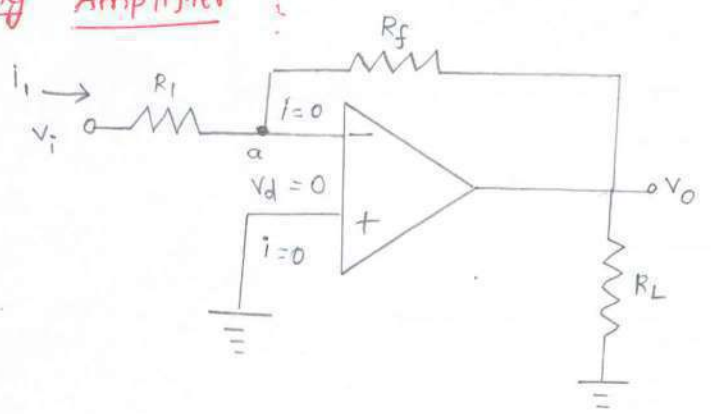
$$I_b = |I_{b1} - I_{b2}|$$

(viii) Thermal drift :- The effect of change in temperature on input offset voltage is called as thermal drift. It is also called as input offset voltage drift.

$$\text{Input offset voltage drift} = \frac{\Delta V_{ios}}{\Delta T} \quad \mu V/^{\circ}C.$$

The Inverting Amplifier

(i



The output voltage (V_o) is fed back to the inverting input terminal through $R_f - R_1$ network where R_f is feedback resistor. Assume ideal case of op-amp, as $V_d = 0$ node 'a' is at ground potential and current i_1 through R_1 is

$$i_1 = \frac{V_i}{R_1}$$

The output voltage is,

$$V_o = -i_1 R_f$$

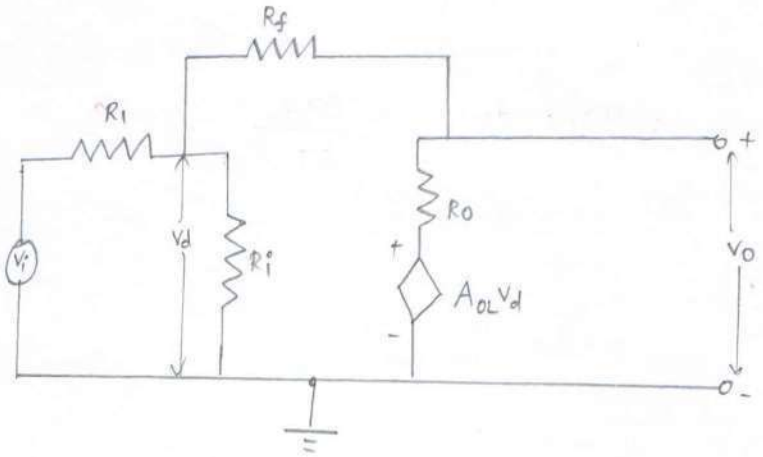
$$= -V_i \frac{R_f}{R_1}$$

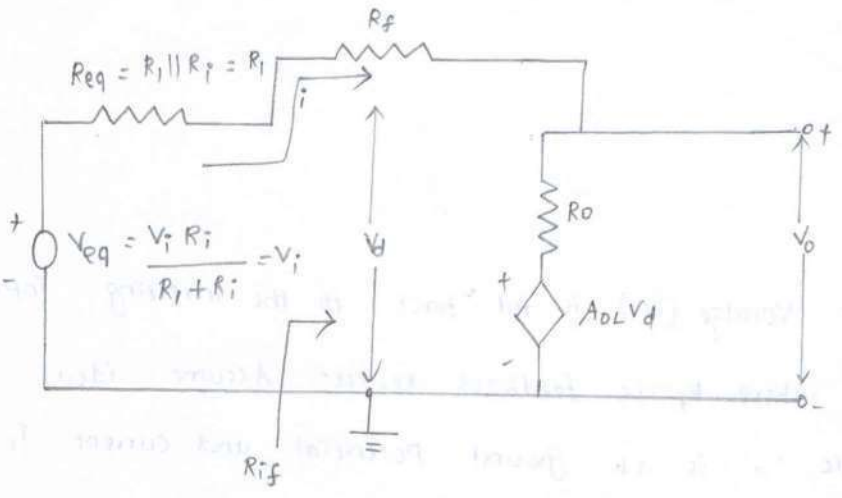
Hence the gain of inverting amplifier (closed loop gain) is

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

Practical Inverting Amplifier :

For practical OP-Amp, the expression for closed loop voltage gain should be calculated using low frequency model.





from the output loop,

$$V_o = iR_o + A_{OL} V_d \Rightarrow V_d = \frac{V_o - iR_o}{A_{OL}} \quad -(1)$$

and

$$V_d + iR_f + V_o = 0 \quad -(2)$$

$$V_d = -iR_f - V_o$$

Sub ① in ②

$$\frac{V_o - iR_o}{A_{OL}} + iR_f + V_o = 0$$

$$V_o(1+A_{OL}) + i(R_f A_{OL} - R_o) = 0$$

$$V_o(1+A_{OL}) = i(R_o - A_{OL}R_f) \quad -③$$

Apply KVL,

$$V_i = i(R_1 + R_f) + V_o \quad -④$$

Sub 'i' from ③ in ④

$$A_{CL} = \frac{V_o}{V_i} = \frac{R_o - A_{OL}R_f}{R_o + R_f + R_1(1+A_{OL})}$$

if $A_{OL} >> 1$, then $A_{OL}R_1 >> R_o + R_f$

$$\therefore A_{CL} = -\frac{R_f}{R_1}$$

It can be seen that,

$$R_{if} = \frac{V_d}{i}$$

Apply KVL in figure (2),

$$V_d + i(R_f + R_o) + A_{OL}V_d = 0 \Rightarrow V_d(1+A_{OL}) = -i(R_f + R_o)$$

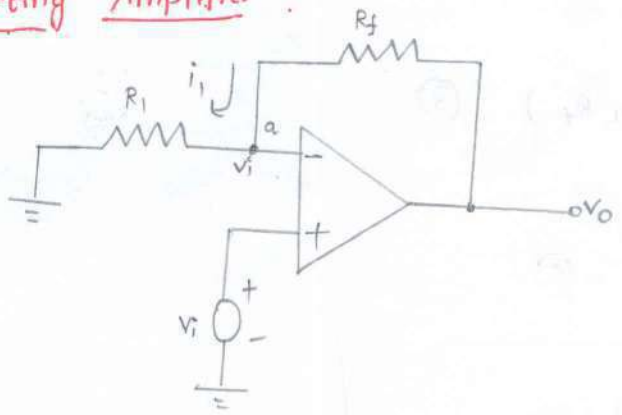
$$\frac{V_d}{i} = \frac{R_f + R_o}{1+A_{OL}}$$

$$\therefore R_{if} = \frac{R_o + R_f}{1+A_{OL}}$$

The output resistance is given by,

$$R_{of} = \frac{R_o(R_1 + R_f)}{R_o + R_f + R_1(1+A_{OL})}$$

Non-Inverting Amplifier :



As the differential voltage (V_d) at the input terminal of op-Amp is zero. Now R_f and R_1 forms a potential divider. Hence,

$$V_i = \left(\frac{V_o}{R_1 + R_f}\right) R_1$$

Since no current flows into op-amp,

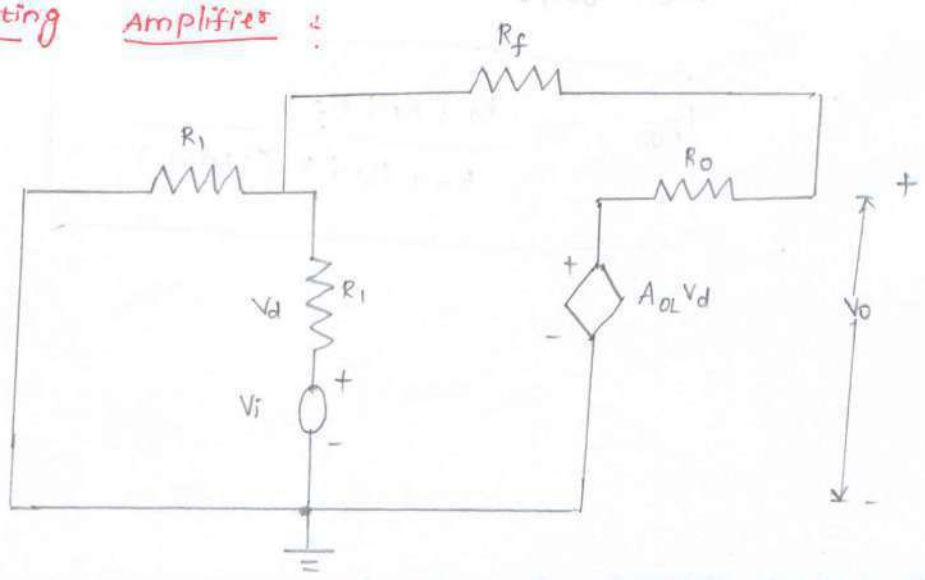
$$\frac{V_o}{V_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}$$

The voltage gain is given by

$$\boxed{A_{CL} = 1 + \frac{R_f}{R_1}}$$

The gain can be adjusted to unity (or) more by proper selection of R_f & R_1.

Practical Non-inverting Amplifier :



Writing KCL at input node,

$$(V_i - V_d)Y_1 + V_d Y_i + (V_i - V_d - V_o)Y_f = 0 \quad \text{---(1)}$$

$$\Rightarrow -(Y_1 + Y_i + Y_f)V_d + (Y_1 + Y_f)V_i = Y_f V_o \quad \text{---(1a)}$$

Writing KCL at output node,

$$(V_i - V_d - V_o)Y_f + (A_{OL} V_d - V_o)Y_o = 0 \quad \text{---(2)}$$

$$-(Y_f - A_{OL} Y_o)V_d + Y_f V_i = (Y_f + Y_o)V_o \quad \text{---(2a)}$$

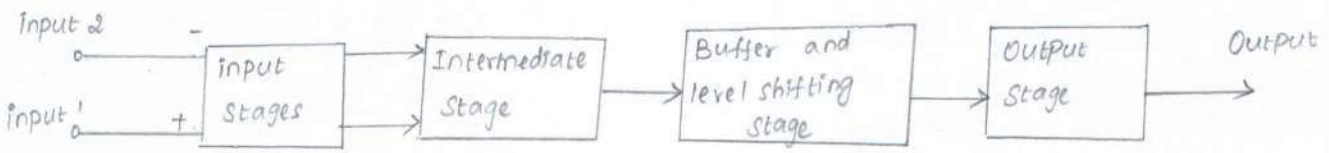
From (1) & (2a),

$$A_{CL} = \frac{A_{OL} Y_o (Y_1 + Y_f)}{A_{OL} Y_o Y_f}$$

$$= \frac{Y_1 + Y_f}{Y_f} = 1 + \frac{Y_1}{Y_f}$$

$$\therefore A_{CL} = 1 + \frac{R_f}{R_1}$$

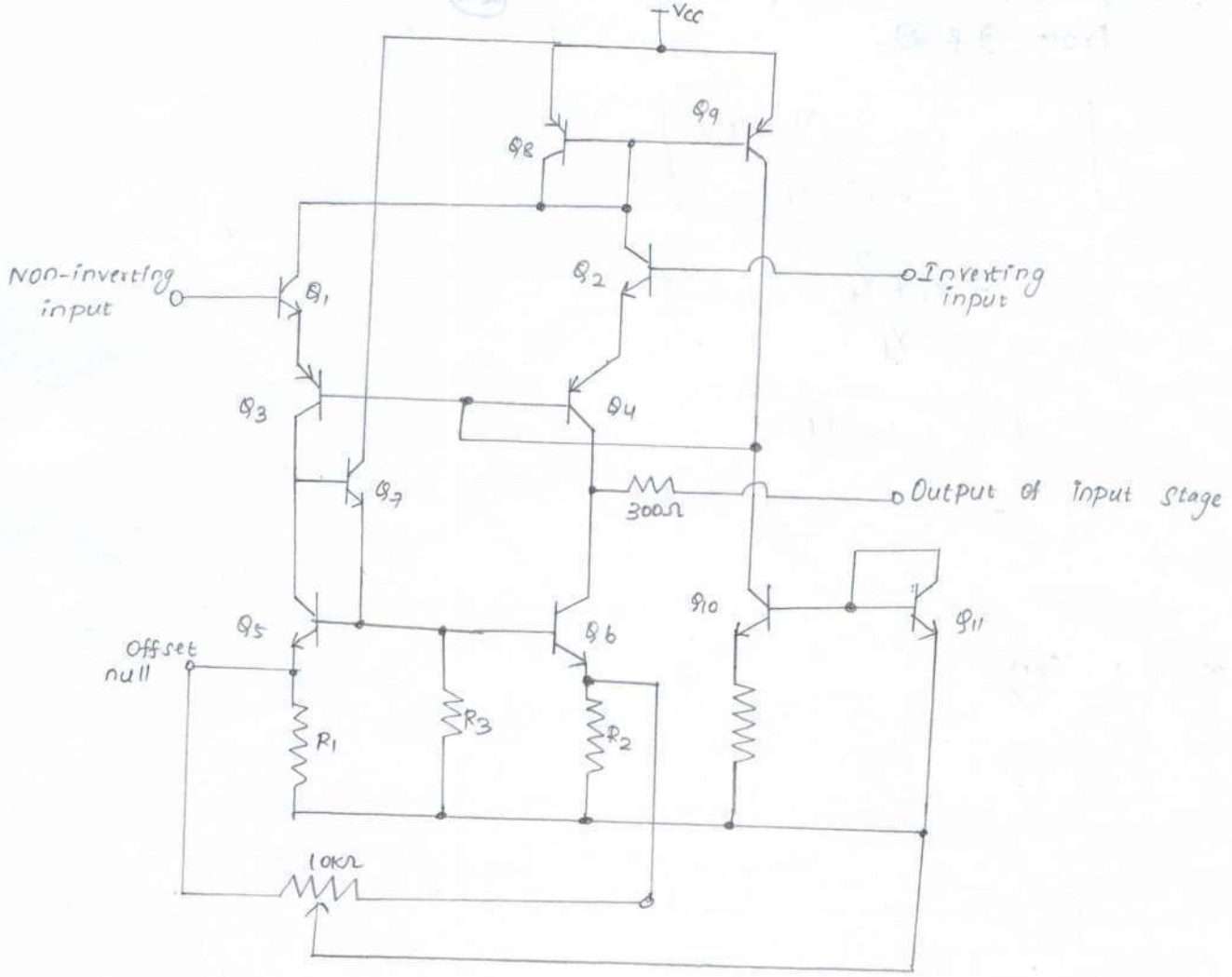
General op-Amp Stages :



Input stage :

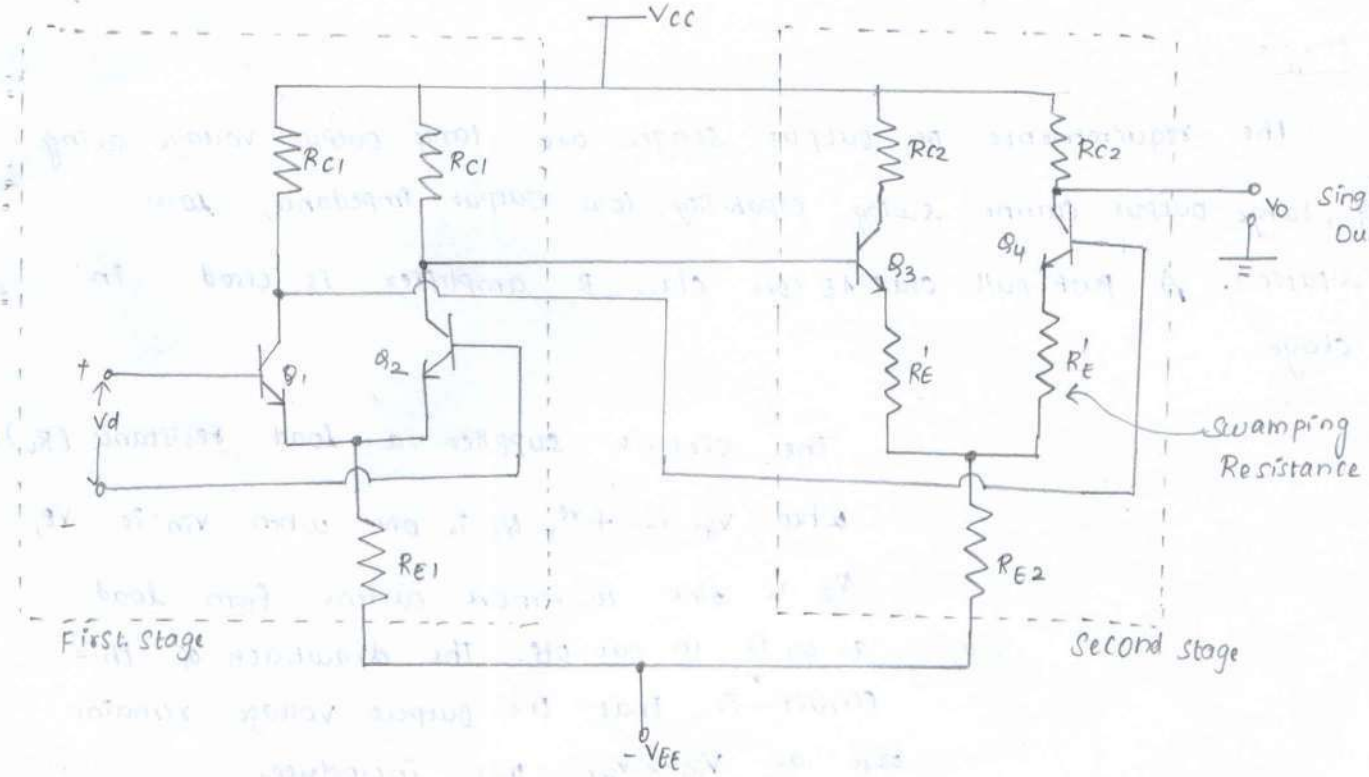
The basic requirements of input stages of op-amp are high voltage gain, high input impedance, two input terminals, small input offset voltage and high CMRR. The dual input, balanced output differential amplifier satisfies all the requirements of input stages of an op-amp.

The transistors Q_3 and Q_4 are part of input of differential amplifier to increase maximum signal input capacity. The constant current source is provided by Q_9 and Q_{10} to Q_3 & Q_4. The resistors R_1, R_2 and R_3 along with transistors Q_5 & Q_6 form a controlled current source. The 10KΩ potentiometer is connected between offset null which is used to control the emitter currents of Q_5 and Q_6. The transistors Q_4 and Q_6 form the complementary symmetry amplifier.



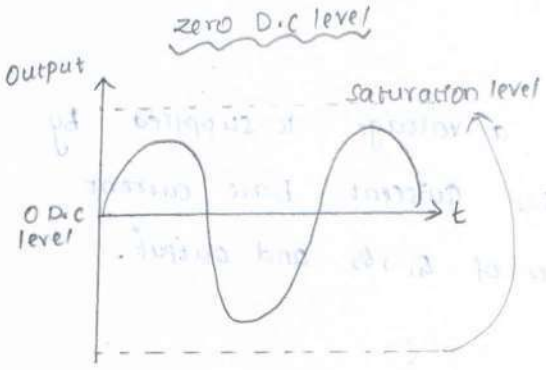
Intermediate Stage :

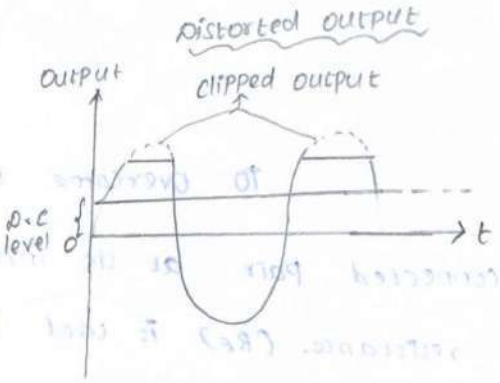
The Output of input stage drives the next stage which is an intermediate stage. Here dual input unbalanced output differential amplifier is used. The main function of intermediate stage is to provide an additional voltage gain. Multistage amplifiers are used to provide additional gain.

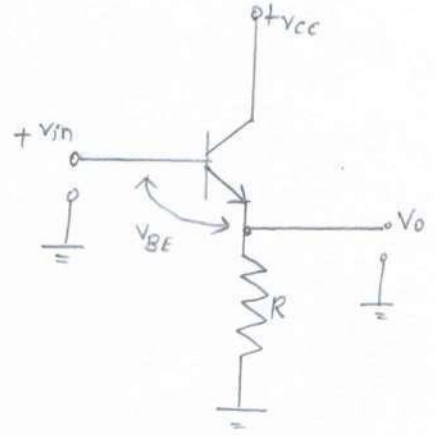


Level shifting stage :

The level shifter stage brings the d.c level down to ground Potential, when no signal is applied at input terminals. Due to the presence of d.c level, the output gets distorted and it limits the maximum output voltage swing.





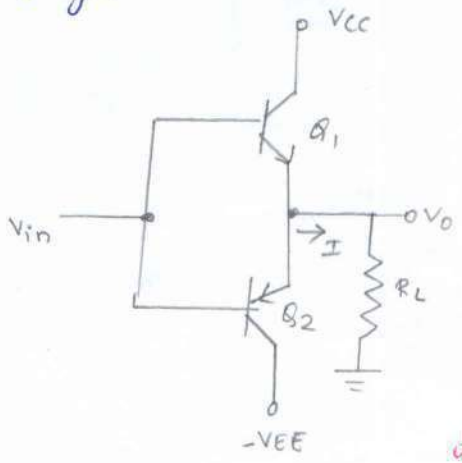


The level shifter circuit is basically an emitter follower. The amount of shift obtained is equal to V_{BE} which is almost 0.7v. If V_{in} is ↑ and V_o is ↓ then

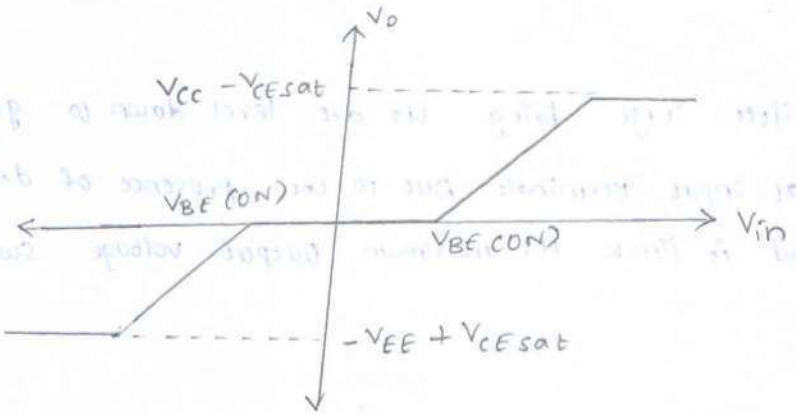
$$V_o = V_{in} - V_{BE}$$

Output stage :

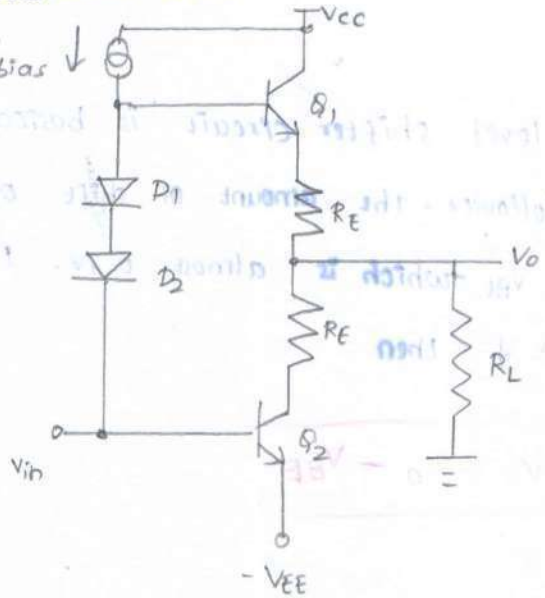
The requirements of output stages are large output voltage swing capability, large output current swing capability, low output impedance, low power dissipation. A push-pull class AB (or) class B amplifier is used in output stage.



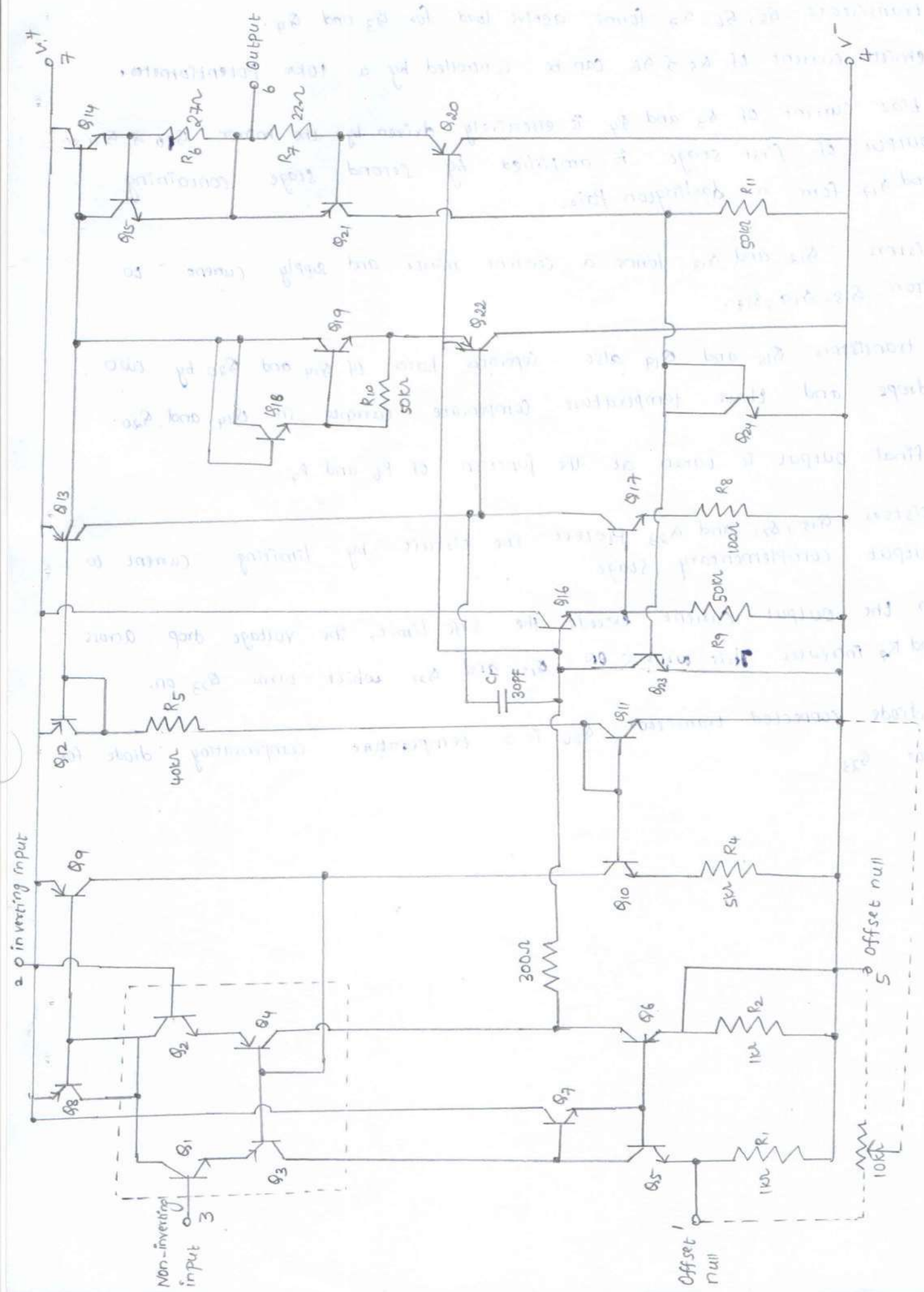
The circuit supplies a load resistance (R_L). When V_{in} is $+^{ve}$, Q_1 is ON when V_{in} is $-^{ve}$, Q_2 is sink to remove current from load as Q_1 is in cut-off. The drawback of this circuit is that the output voltage remains zero as $V_{in} < V_{BE}$. This introduces Cross-over distortion at the output.



To overcome this drawback, a voltage is supplied by a diode connected pair at the input. To stabilize quiscent base current the small resistance (R_E) is used between emitter of Q_1, Q_2 and output.



Internal Circuit Diagram Of IC741:



* The input differential amplifiers consist of transistors $Q_1 - Q_3$ & $Q_2 - Q_4$. $Q_1 Q_3$ & $Q_2 Q_4$ are in cascode (CE-CB) configuration.

* The transistors Q_5, Q_6, Q_7 forms active load for Q_3 and Q_4.

* The emitter current of Q_5 & Q_6 can be controlled by a 10kΩ potentiometer.

* The bias current of Q_3 and Q_4 is effectively driven by the mirror Q_{10} & Q_{11}. The output of first stage is amplified by second stage containing Q_{16} and Q_{17} forms a darlington pair.

* Transistors Q_{12} and Q_{13} forms a current mirror and supply current to transistors Q_{18}, Q_{19}, Q_{17}.

* The transistors Q_{18} and Q_{19} also seperates bases of Q_{14} and Q_{20} by two diode drops and thus temperature compensate currents in Q_{14} and Q_{20}.

* The final output is taken at the junction of R_6 and R_7.

* Transistors Q_{15}, Q_{21} and Q_{23} Protect the circuit by limiting current to the output complementary stage.

* When the output current exceeds the safe limit, the voltage drop across R_6 and R_7 increases. This turns on Q_{15} and Q_{21} which turns Q_{23} on.

* The diode connected transistor Q_{24} is a temperature compensating diode for transistor Q_{23}.

Slew Rate :

The slew rate is defined as maximum rate of change of output voltage with respect to time. Let the input voltage V_s is purely sinusoidal hence the output voltage is also purely sinusoidal.

$$V_s = V_m \sin \omega t$$

$$V_o = V_m \sin \omega t$$

$$\frac{dV_o}{dt} = V_m (\omega \cos \omega t)$$

$\frac{dV_o}{dt}$ is maximum hence $\cos \omega t \simeq 1$

$$\therefore S = \left(\frac{dV_o}{dt}\right)_{max} = \omega V_m$$

$$\boxed{S = 2\pi f V_m \quad V/sec}$$

This equation is called as slew rate equation. The maximum signal frequency from above equation can be written as,

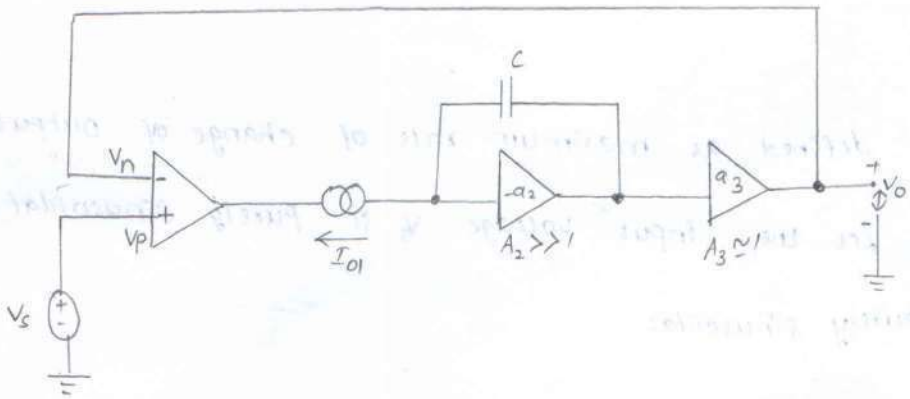
$$\boxed{f_m = \frac{S}{2\pi V_m}}$$

This frequency is called as full-power bandwidth of op-amp.

Methods for Improving Slew Rate :

The slew rate can also be given by

$$S = \frac{I_{max}}{C}$$



when input overdrives the input stage then $I_{max} = \pm I_{01(sat)}$ which are saturation current levels of the input stage. The saturation of input stage limits the slew rate because in saturation region, the rate at which capacitor 'C' can charge/discharge.

$$I_{01(sat)} = C \frac{dV_{02}}{dt}$$

$$\frac{dV_{02}}{dt} = \frac{I_{01(sat)}}{C}$$

Now the gain of third stage $a_3 \simeq 1$. hence $V_o = V_{02}$

$$\left.\frac{dV_o}{dt}\right|_{max} = \frac{dV_{02}}{dt} = \frac{I_{01(sat)}}{C}$$

$$\therefore \boxed{S = \frac{I_{01(sat)}}{C}}$$

The input stage is a transconductance amplifier hence,

Output current = g_m (differential input)

$$I_{01} = g_{m1}(V_p - V_n)$$

$$V_{02} = Z_c g_{m1}(V_p - V_n)$$

Since $a_3 \simeq 1$

$$V_{o2} = V_o$$

$$V_o = z_c g_{m1} (V_p - V_n)$$

$$V_o = \left[\frac{1}{j\omega C}\right] g_{m1} (V_p - V_n) \qquad \left[\because z_c = x_c = \frac{-j}{\omega c}\right]$$

$$\text{Op-amp gain} = \frac{|V_o|}{|V_p - V_n|}$$

$$|a| = \frac{|V_o|}{|V_p - V_n|} = \frac{g_{m1}}{\omega C} = \frac{g_{m1}}{2\pi f C}$$

The gain bandwidth product of op-amp is given by

$$f_t = |a| f$$

$$f_t = \frac{g_{m1}}{2\pi C}$$

$$\therefore \boxed{C = \frac{g_{m1}}{2\pi f_t}}$$

Sub C in slew rate equation,

$$\boxed{S = \frac{2\pi f_{o1(sat)} f_t}{g_{m1}}}$$

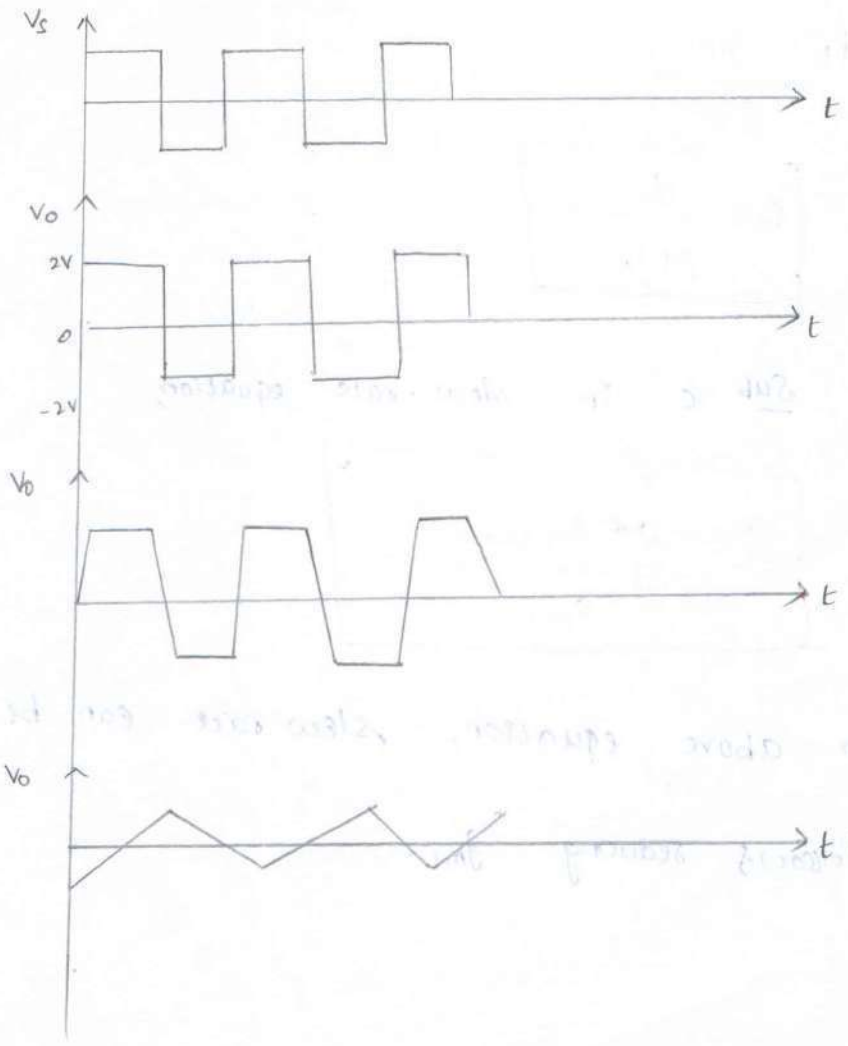
From above equation, slew rate can be increased by increasing f_t, $f_{o1(sat)}$ & reducing g_{m1}.

* Increasing f_t : ↑ value of gain-bandwidth Product, ↑ slew rate. To ↑ f_t, capacitor must be reduced. Frequency compensation methods can be done to increase f_t.

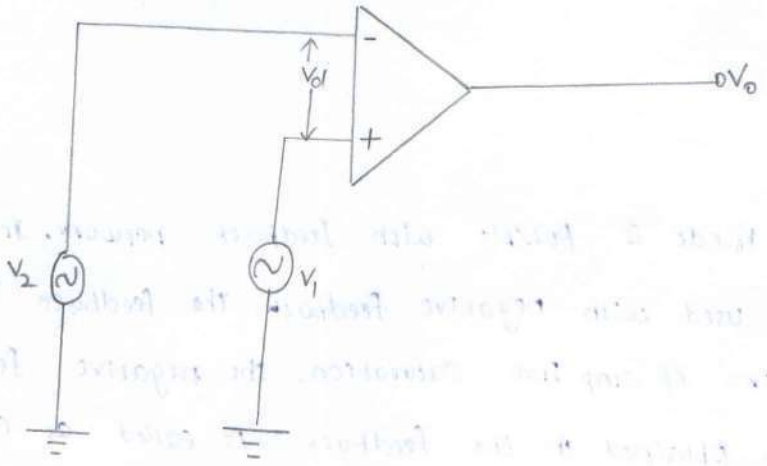
* Increasing $I_{O1(sat)}$: To ↑ $I_{O1(sat)}$ without affecting g_{m1}, an alternative path for charging and discharging of capacitance should be provided. It is possible by using additional input transistor pair.

* Reducing g_{m1} :

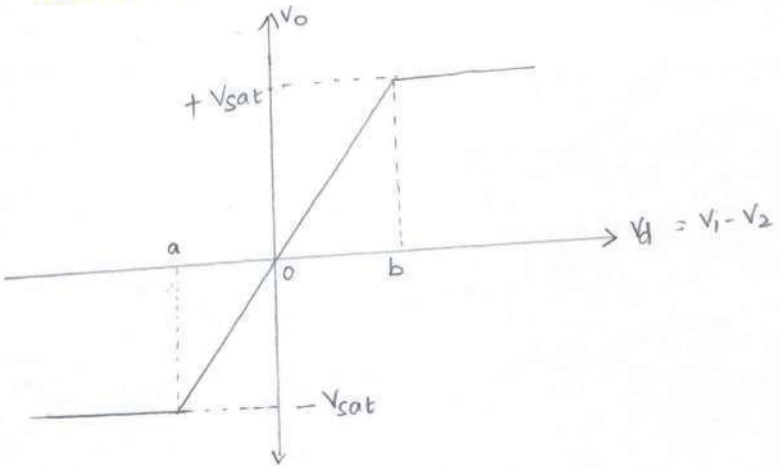
By using emitter degeneration technique, transconductance can be reduced. Another method is to use FET differential pair at input instedd of BJT.



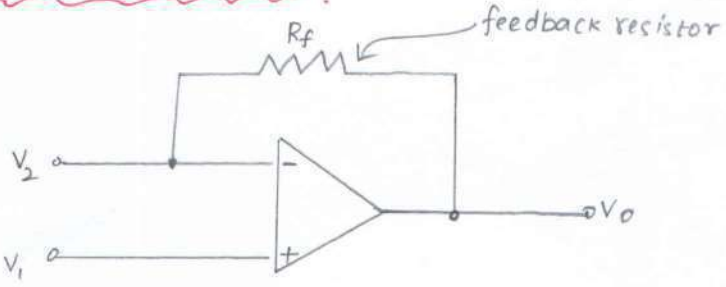
Open-loop Configuration of OP-Amp :



The D.C supply voltages applied to op-amp are V_{CC} & $-V_{EE}$ and the output varies linearly only between V_{CC} and $-V_{EE}$. Since the gain is very large in open loop condition, the output voltage V_o is either at positive saturation voltage ($+V_{sat}$) or negative saturation voltage ($-V_{sat}$). Thus a small noise voltage present at input also gets amplified due to high frequency open-loop gain and op-amp gets saturated. Hence, op-amp does not work as a linear small signal amplifier in open loop mode. Open loop op-amps are used in voltage comparator, zero crossing detector etc.



Closed loop Configuration of op-amp :



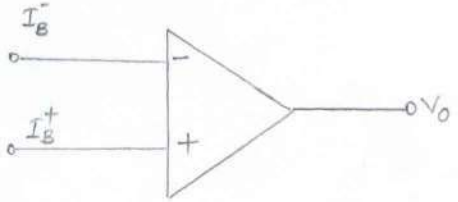
The closed loop mode is possible with feedback network. In linear applications, the op-amp is always used with negative feedback. The feedback helps to control gain which otherwise drives op-amp into saturation. The negative feedback is done by adding a resistor. The gain obtained in the feedback is called as closed loop gain. The closed loop gain is much less than the open loop gain because of feedback resistance. The advantages of using negative feedback are it increases bandwidth, input resistance and reduces distortion, output-resistance.

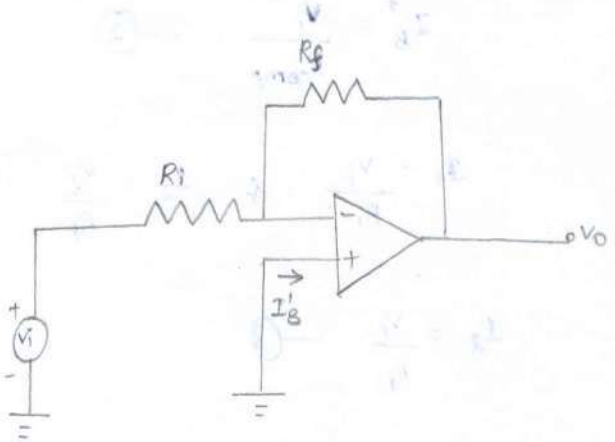
DC characteristics of OP-AMP :

An ideal OP-amp draws no current from source. But in practical cases, it won't work. The various non-ideal dc characteristics of op-amp are

* Input bias current
* Input offset current
* Input offset voltage
* thermal Drift.

* Input bias current :



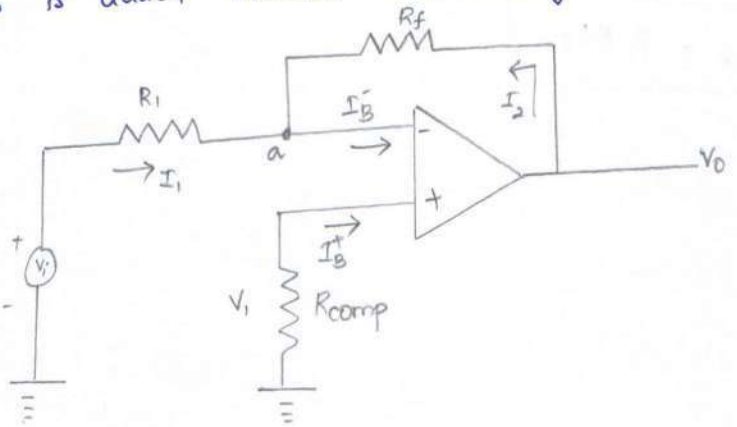


$$I_B = \frac{I_B^+ + I_B^-}{2}$$

If the input voltage V_i is set to zero volt, the output voltage V_o should be also zero volt. But some offset occurs which is given by,

$$V_o = (I_B^-) R_f .$$

TO overcome the effect of bias current, a compensation resistor R_{comp} is added between noninverting input terminal and ground.



Applying KVL,

$$-V_1 + 0 + V_2 - V_o = 0$$

$$\therefore V_o = V_2 - V_1 \quad \text{—(1)}$$

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and output V_o will be zero. Hence,

$$V_1 = I_B^{\uparrow} R_{comp}$$

$$I_B^{\uparrow} = \frac{V_1}{R_{comp}} \quad \text{—(2)}$$

$$I_1 = \frac{V_1}{R_1} \quad \& \quad I_2 = \frac{V_2}{R_f} \quad \text{since} \quad V_1 = V_2,$$

$$I_2 = \frac{V_1}{R_f} \quad \text{—(3)}$$

Applying KCL at node 'a',

$$I_B^{-} = I_2 + I_1$$

$$= \frac{V_1}{R_f} + \frac{V_1}{R_1} = \frac{V_1 (R_1 + R_f)}{R_1 R_f}$$

Assume $I_B^{\uparrow} = I_B^{-}$

$$\therefore \frac{V_1 (R_1 + R_f)}{R_1 R_f} = \frac{V_1}{R_{comp}}$$

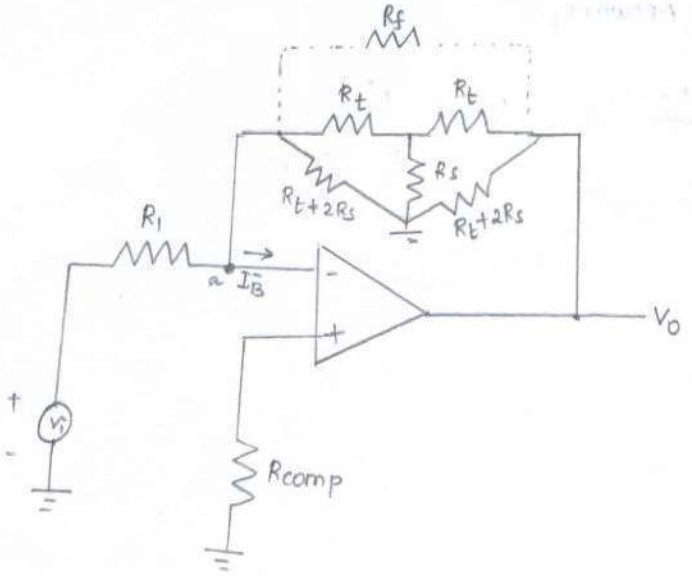
$$\therefore \boxed{R_{comp} = R_1 \parallel R_f}$$

* Input Offset Current :

The small difference between I_B^+ and I_B^- is called as Input offset current.

$$|I_{os}| = I_B^+ - I_B^-$$

Offset current for BJT is 200nA and FET it is 10pA.



Applying KCL at node 'a',

$$I_2 = (I_B^- - I_1)$$

where $I_1 = \frac{V_1}{R_1}$ & $V_1 = I_B^+ R_{comp}$

and

$$V_0 = I_2 R_f - V_1$$

$$= I_2 R_f - I_B^+ R_{comp}$$

$$\therefore V_0 = R_f [I_B^- - I_B^+]$$

$$\boxed{V_0 = R_f I_{os}}$$

The T-feedback network will allow large feedback resistance and keeping R_{comp} low.

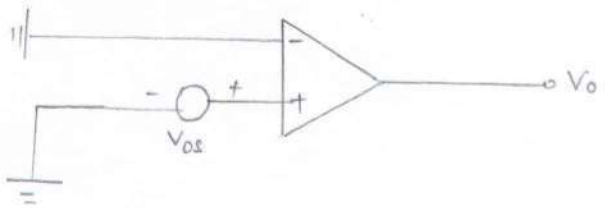
Converting T-network to Π-network,

$$R_f = \frac{R_t^2 + 2R_tR_s}{R_s}$$

To design a T-network,

$$R_t << \frac{R_f}{2} \quad \& \quad R_s = \frac{R_t^2}{R_f - 2R_t}$$

* Input Offset voltage :



The output voltage will not be zero for zero input voltage because of imbalances inside the op-amp. A small voltage is applied at the input to make the output voltage zero. This voltage is called as input offset voltage.

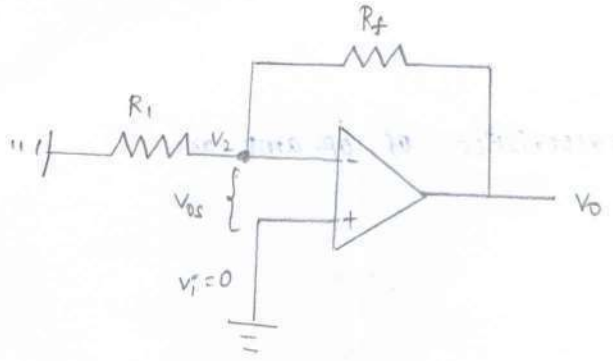
$$V_2 = \left(\frac{R_1}{R_1 + R_f}\right) V_o$$

$$V_o = \left(\frac{R_1 + R_f}{R_1}\right) V_2$$

Since $V_{os} = |V_i - V_2|$ & $V_i = 0$

$$V_{os} = V_2$$

$$\therefore \boxed{V_o = \left(1 + \frac{R_f}{R_1}\right) V_{os}}$$



The total output offset voltage V_{OT} could be either more (or) less than the offset voltage produced at output due to input bias current (or) input offset voltage alone.

$$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_B$$

(or)

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_{os}$$

* Thermal Drift :

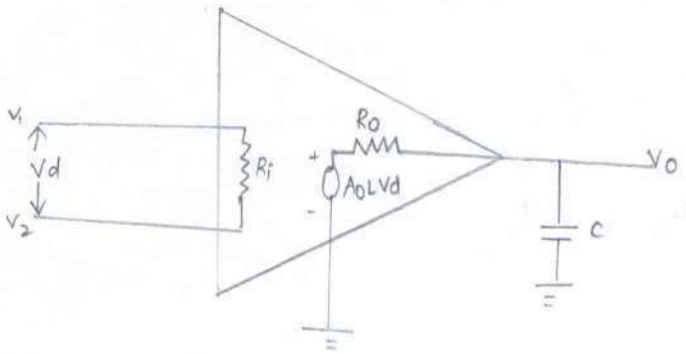
Bias current, offset current and offset voltages changes with temperature. This effect is called as thermal drift. Techniques like forced air cooling and carefully printed circuit boards can be used to minimize thermal drift.

AC Characteristics of OP-Amp :

The various AC characteristics of op-amp are

* Frequency Response
* Frequency compensation
* Stability
* Slew rate.

* Frequency Response :



Consider the high frequency model of op-amp with a capacitor C at output hence capacitive effect. let $-jX_C$ be capacitive reactance due to capacitor. Using voltage divider rule,

$$V_o = -jX_C \left[\frac{A_{OL} V_d}{R_o - jX_C}\right]$$

$$-j = \frac{1}{j} \quad \text{and} \quad X_C = \frac{1}{2\pi fC}$$

$$\boxed{V_o = \frac{A_{OL} V_d}{1 + j2\pi f C R_o}}$$

Hence the open loop voltage gain as a function of frequency is,

$$A_{OL}(f) = \frac{V_o}{V_d}$$

$$A_{OL}(f) = \frac{A_{OL}}{1 + j2\pi f R_o C}$$

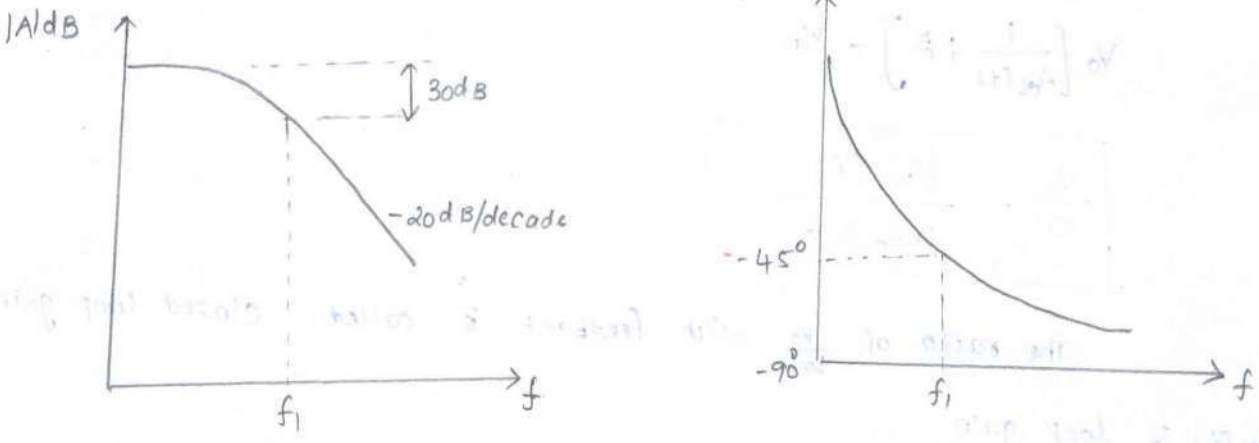
let $f_o = \frac{1}{2\pi R_o C}$

$$\therefore \boxed{A_{OL}(f) = \frac{A_{OL}}{1 + j\left(\frac{f}{f_o}\right)}}$$

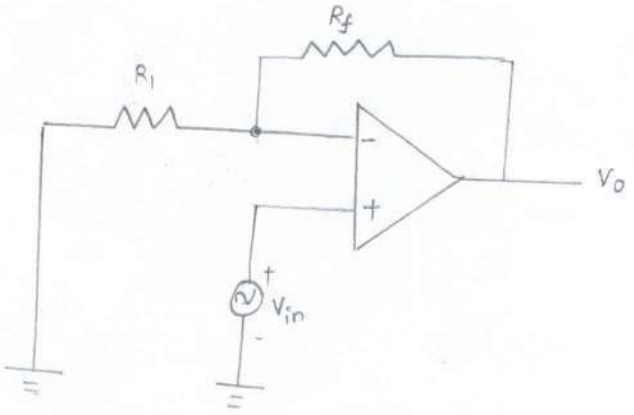
The magnitude and Phase response is given by,

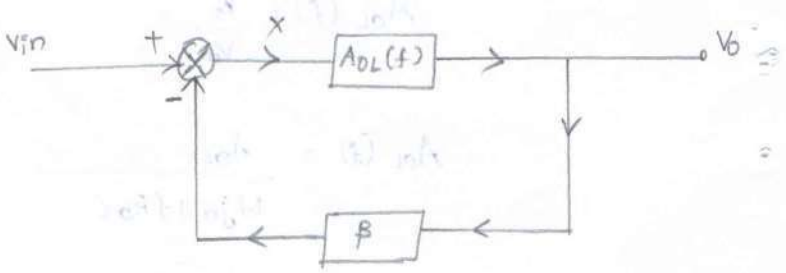
$$|A_{OL}(f)| = \frac{A_{OL}}{\sqrt{1 + \left(\frac{f}{f_o}\right)^2}}$$

$$\angle A_{OL}(f) = \phi(f) = -\tan^{-1}\left(\frac{f}{f_o}\right)$$



* Stability of op-amp :





$$X = V_{in} - \beta V_o \quad \text{—①}$$

$$V_o = X[A_{OL}(f)]$$

$$\therefore \boxed{X = \frac{V_o}{A_{OL}(f)}} \quad \text{—②}$$

Sub ② in ① we get,

$$\frac{V_o}{A_{OL}(f)} = V_{in} - \beta V_o$$

$$\frac{V_o}{A_{OL}(f)} + \beta V_o = V_{in}$$

$$V_o\left[\frac{1}{A_{OL}(f)} + \beta\right] = V_{in}$$

$$\boxed{\frac{V_o}{V_{in}} = \frac{A_{OL}(f)}{1 + A_{OL}(f)\beta}}$$

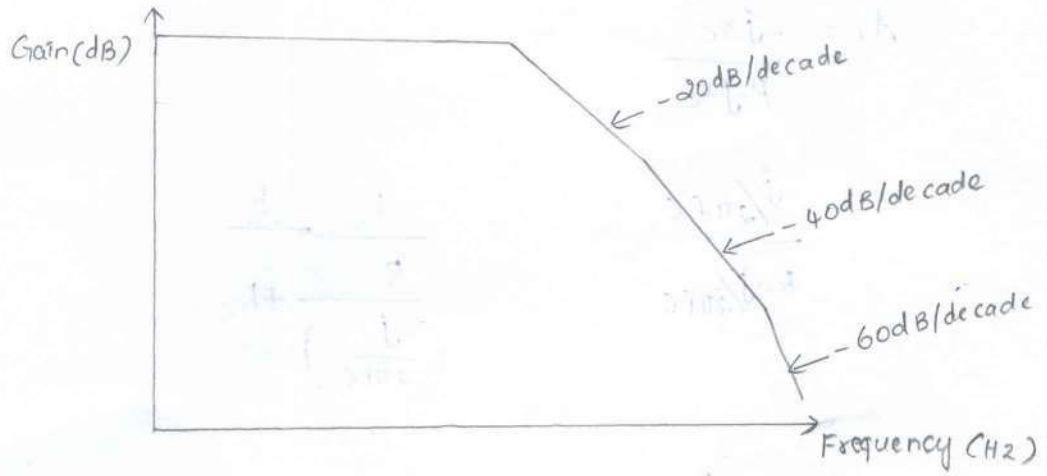
The ratio of $\frac{V_o}{V_{in}}$ with feedback is called closed loop gain.

and $A_{OL}(f)$ is loop gain.

$$\therefore 1 + A_{OL}(f)\beta = 0$$

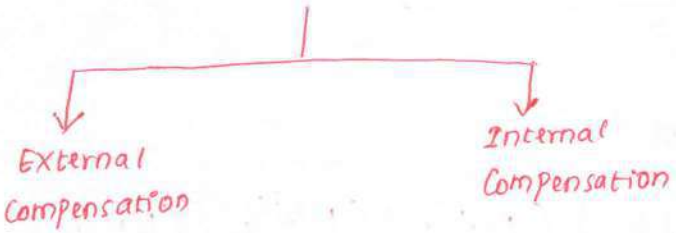
$$\boxed{A_{OL}(f)\beta = -1}$$

$|A_{OL}(f)\beta| = 1$ and $\angle A_{OL}(f)\beta = 0^\circ$ (or) $2n\pi$



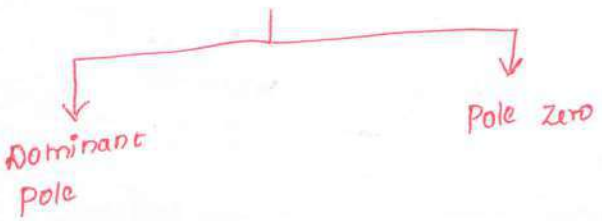
* Frequency Compensation :

The method of modifying loop gain frequency response of OP-amp so that it behaves like single break frequency response which provides sufficient positive phase margin is called as frequency compensation. There are two types of compensation techniques namely

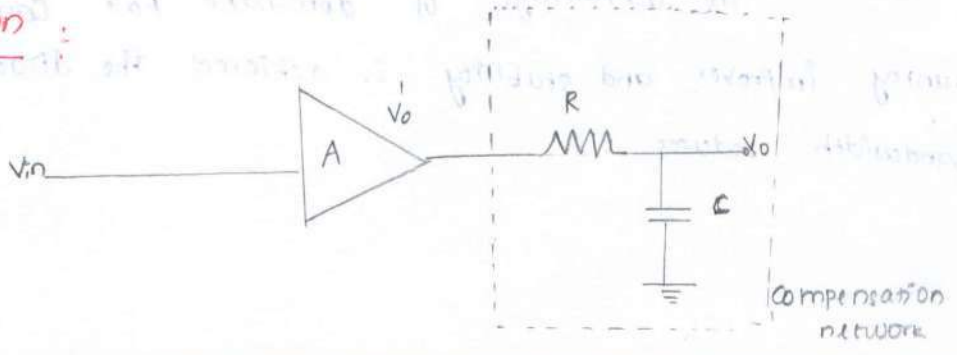


External Compensation Techniques :

There are two types of external compensation namely



Dominant pole compensation :



By voltage divider rule,

$$A_1 = \frac{-jX_C}{R-jX_C}$$

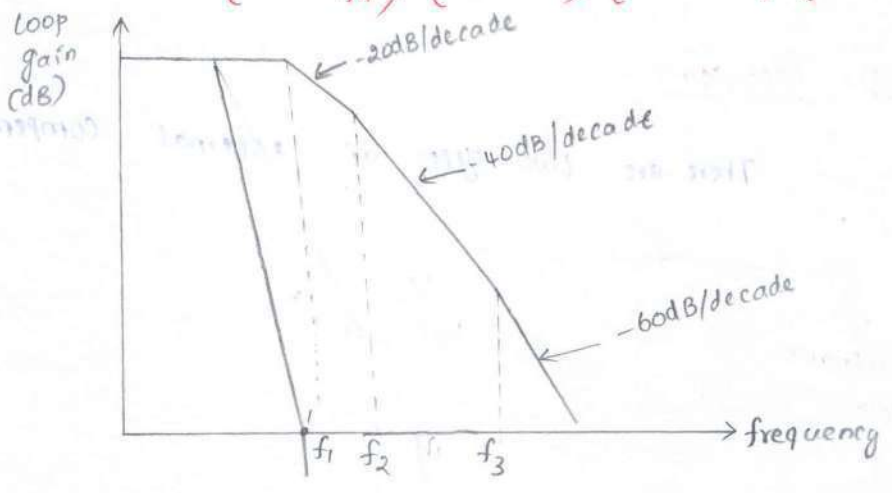
$$= \frac{-j/2\pi fC}{R-j/2\pi fC} = \frac{1}{\frac{R}{\left(\frac{-j}{2\pi fC}\right)}+1}$$

$$\therefore A_1 = \frac{1}{1+j2\pi fRC}$$

$$\text{let } f_d = \frac{1}{2\pi RC}$$

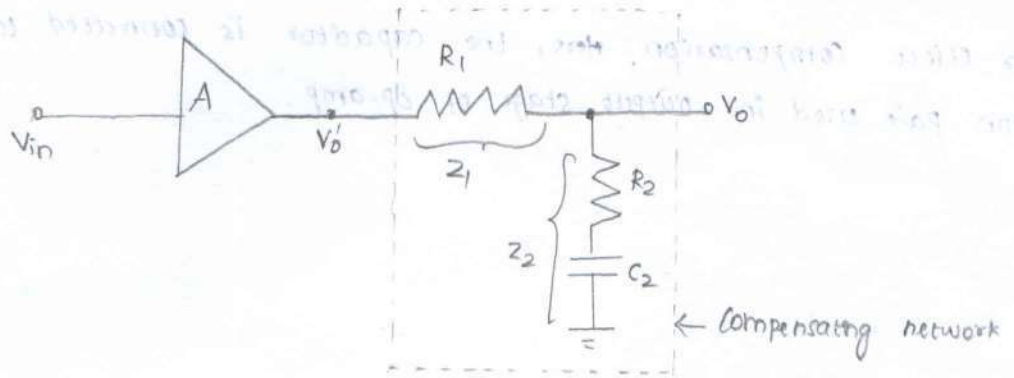
$$\boxed{A_1 = \frac{1}{1+j\left(\frac{f}{f_d}\right)}}$$

$$A' = \frac{A_{OL}}{\left(1+j\frac{f}{f_d}\right)\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_2}\right)}$$



The advantage of dominant pole compensation is the noise immunity improves and stability is achieved. The disadvantage of this method is bandwidth reduces.

Pole - Zero compensation :



The transfer function using voltage divider rule,

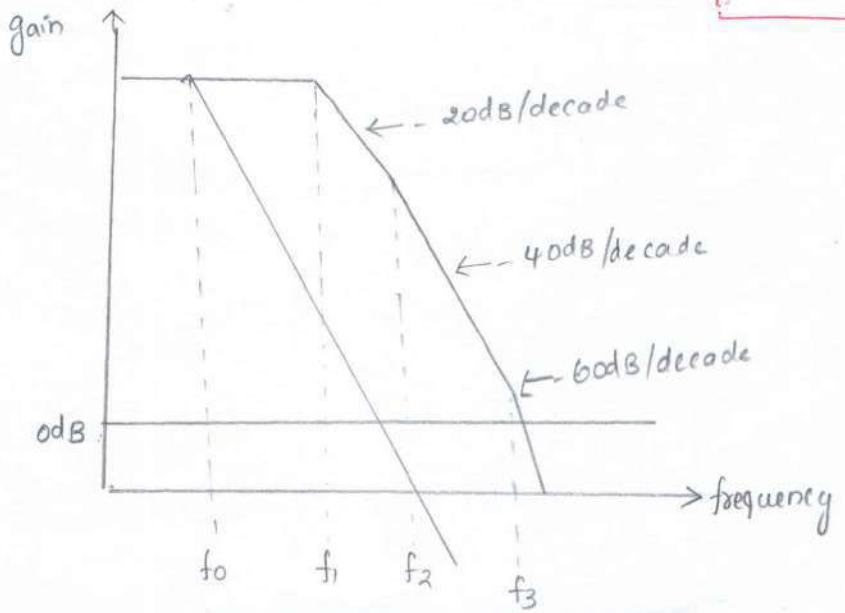
$$Z_1 = R_1$$

$$Z_2 = R_2 - jX_{C2}$$

$$\therefore A_1 = \frac{R_2 - jX_{C2}}{R_1 + R_2 - jX_{C2}} = \frac{R_2 - \frac{j}{2\pi f C_2}}{R_1 + R_2 - \frac{j}{2\pi f C_2}} = \frac{\left[\frac{R_2}{\frac{-j}{2\pi f C_2}}\right] + 1}{\frac{R_1 + R_2}{\left[\frac{-j}{2\pi f C_2}\right]} + 1}$$

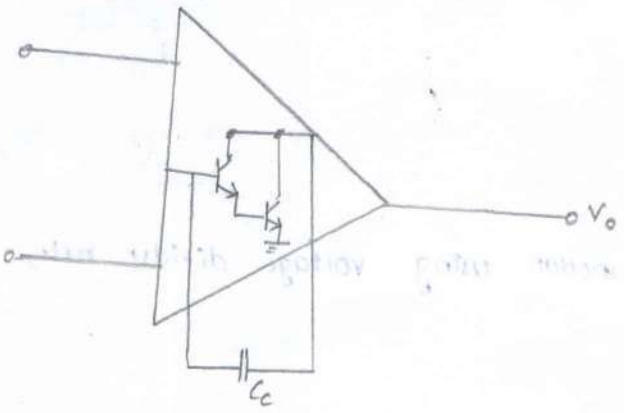
$$\boxed{A_1 = \frac{1 + j2\pi f R_2 C_2}{1 + j2\pi f (R_1 + R_2) C_2}}$$

let $f_1 = \frac{1}{2\pi R_2 C_2}$ and $f_0 = \frac{1}{2\pi (R_1 + R_2) C_2}$, $\boxed{A_1 = \frac{1 + j\left(\frac{f}{f_1}\right)}{1 + j\left(\frac{f}{f_0}\right)}}$



Internal Compensation / Miller Compensation :

The drawbacks of external compensation can be overcome by using miller effect compensation. Here, the capacitor is connected to feedback path of darlington pair used in output stage of op-amp.



The C_c is compensating capacitor, the gain of darlington stage is

$$A_2 = -G_{mc} R_o$$

Using Miller capacitance C_M and results of miller effect,

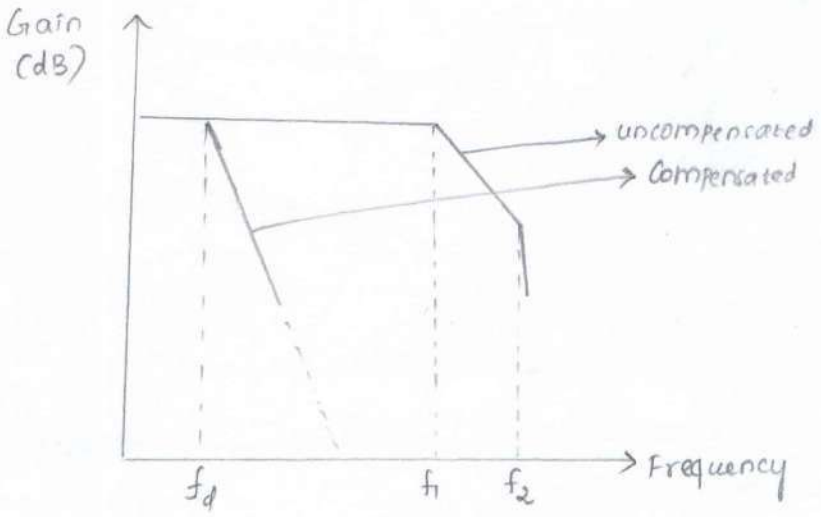
$$Z_{GM} = \frac{Z_c}{1+a_2}$$

where $Z_{GM} = \frac{1}{j\omega C_M}$ & $Z_c = \frac{1}{j\omega C_c}$

$$\boxed{C_M = (1+a_2)\, C_0}$$

The miller effect capacitance C_M forms a low pass RC section with input resistance (R_i) whose corner frequency is given by

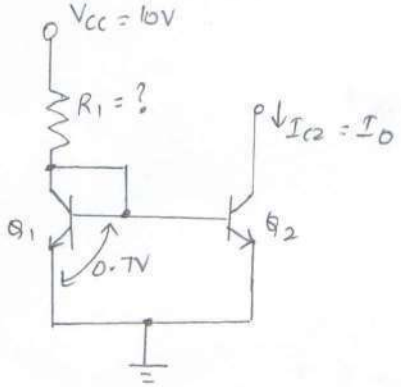
$$\boxed{f_d = \frac{1}{2\pi C_M R_i}}$$



UNIT - 1

PROBLEMS

1) For a simple current mirror as shown below is to provide 1mA current with $V_{CC} = 10V$. Assume $\beta = 125$ and $V_{BE} = 0.7V$. Determine the value of R_1. (May/June - 2012)



Soln :

$$I_{ref} = \left(\frac{V_{CC} - V_{BE}}{R_1}\right)\frac{\beta}{\beta+2}$$

$$\therefore R_1 = \frac{V_{CC} - V_{BE}}{I_{ref}} \Rightarrow \left(\frac{10 - 0.7}{.1\times10^{-3}}\right)\left(\frac{125}{125+2}\right)$$

$$\boxed{R_1 = 9.15\,k\Omega}$$

2) Design a Widlar current source for generating a constant current $I_O = 10\mu A$. Assume $V_{CC} = 10V$, $V_{BE} = 0.7V$, $\beta = 125$ and use $V_T = 25mV$

Soln :

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1}$$

$$R_1 = \frac{V_{CC} - V_{BE}}{I_{ref}} = \frac{10 - 0.7}{1\times10^{-3}} = \frac{9.3}{1\times10^{-3}} \quad [\text{Assume } I_{ref} = 1mA]$$

$$\boxed{R_1 = 9.3\,k\Omega}$$

$$R_E = \frac{V_T}{I_{C2}\left(1 + \frac{1}{\beta}\right)} \ln\left(\frac{I_{C1}}{I_{C2}}\right) = \frac{0.025}{10\times10^{-6}\left(1+\frac{1}{125}\right)} \ln\left(\frac{1\times10^{-3}}{10\times10^{-6}}\right) \Rightarrow$$

$$\boxed{R_E = 11.5\,k\Omega}$$

3) For a dual input, balanced output differential amplifier, $R_C = 2.2k\Omega$ and $R_E = 4.7k\Omega$, $R_{S1} = R_{S2} = 50\Omega$. The supply voltage is $\pm 10V$, $h_{fe} = 50$. Assume silicon transistor with $hie = 1.4k\Omega$. Determine the operating point value, Ad, Ac and CMRR. (May/June - 2013)

Soln

$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$

$$= 10 + 0.7 - 1\times10^{-3} \times 2.2\times10^{-3}$$

$$V_{CEQ} = 8.52\ V$$

$$I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E} = \frac{-0.7}{2\times4.7\times10^{3}}$$

$$A_d = \frac{h_{fe} R_C}{R_S + hie} = \frac{50 \times 22 \times10^{3}}{50 + 1.4\times10^{3}}, \quad A_d = 75.862$$

$$A_C = \frac{h_{fe} R_C}{2R_E (1+h_{fe}) + R_S + hie} = \frac{50\times22\times10^{3}}{2(4.7\times10^{3})(51) + 50 + 1.4\times10^{3}}$$

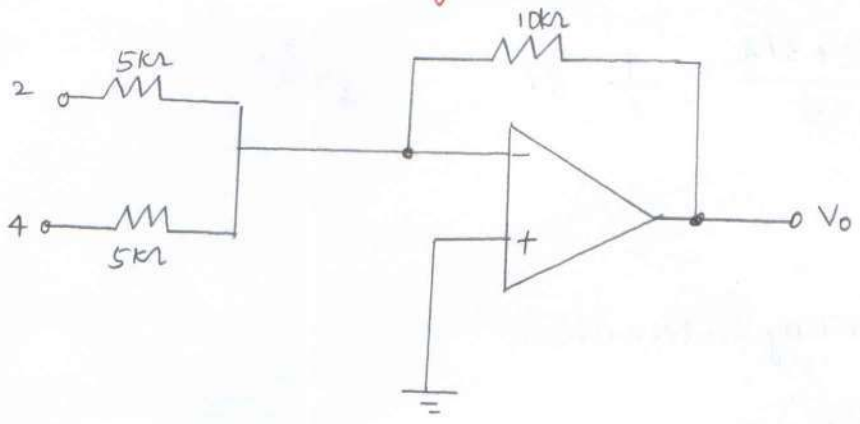
$$A_C = 0.2287$$

$$CMRR = \frac{A_d}{A_C} = \frac{75.862}{0.2287} = 331.62$$

$$= 20\log(331.62)$$

$$CMRR = 50.41\ dB$$

4) Find V_o for the following circuit



Soln

$R_f = 10k\Omega$, $R_1 = 5k\Omega$, $R_2 = 5k\Omega$, $V_1 = 2V$, $V_2 = 4V$.

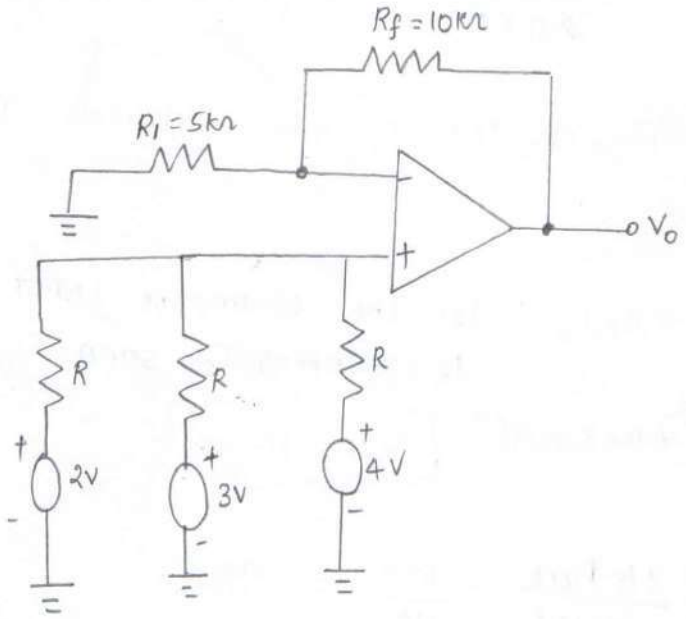
Since the above circuit is inverting amplifier

$$V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2\right]$$

$$= -\left[\frac{10}{5}\times 2 + \frac{10}{5}\times 4\right] = -[4+8]$$

$$V_o = -12V$$

5) For non-inverting OP-amp shown below, find output voltage V_o (April/May 2011)



Soln

$$V_A = \frac{V_1 + V_2 + V_3}{3} = \frac{2+3+4}{3} = \frac{9}{3} = 3V$$

$$\boxed{V_A = 3V}$$

Since it is a non-inverting adder circuit,

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_A$$

$$= \left(1 + \frac{10k}{5k}\right) 3V = 3 \times 3V \quad \therefore \boxed{V_o = 9V}$$

6) Find the maximum frequency for an op-amp with sine wave output voltage of 10V peak and slew rate is 2V/μs.

Soln

$$V_m = 10V$$

$$S = 2V/\mu s = 2 \times 10^6 V/s$$

$$S = 2\pi f_m V_m$$

$$f_m = \frac{S}{2\pi V_m} = \frac{2 \times 10^6}{2\pi \times 10} \Rightarrow \boxed{f_m = 31.83\ kHz}$$

7) For a non-inverting amplifier, $R_1 = 1k\Omega$, $R_f = 10k\Omega$, calculate I_B and maximum output offset voltage, R_{comp}.

Soln

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_B$$

Let the op-amp be LM311 for which $V_{os} = 10mV$, $I_B = 300nA$ & $I_{os} = 50nA$

$$= \left(1 + \frac{10k}{1k}\right) 10 \times 10^{-3} + 10k \times 300 \times 10^{-9}$$

$$\boxed{V_{OT} = 113mV}$$

$$R_{comp} = R_1 \| R_f = \frac{1k \times 10k}{1k + 10k} = \frac{10k}{11k} = 990\Omega$$

7/11/04

UNIT-II

APPLICATIONS OF OP-AMPs

Linear appln
Non-linear appln

Linear ckt:
The o/p varies with i/p in a linear manner

Non-linear ckts:
The o/p varies with i/p in a non-linear manner

Linear Appln

1) Adder
2) Subractor
3) I-V convertor
4) V-I convertor
5) Instrumentation amp^r etc.

Non-linear appln

1) Rectifier
2) Clipper & clamper
3) Multiplier
4) log & antilog amp^r
5) Other non-linear ckts etc

Basic circuits

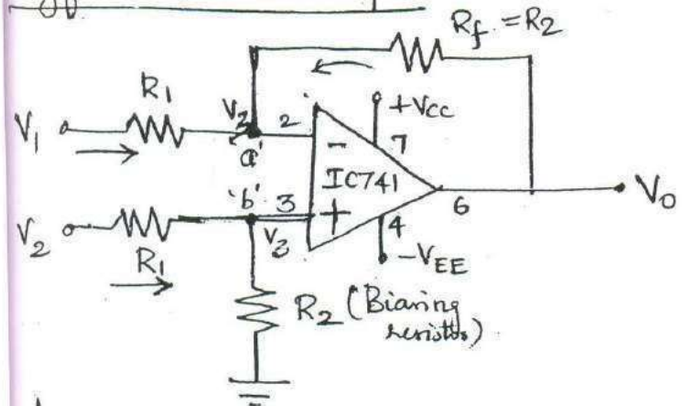
(i) Inverting amp, $V_o = -\frac{R_f}{R_1} \cdot V_i$ & $A_V = -R_f/R_1$

(ii) Non-inverting amp. $V_o = \left(1 + \frac{R_f}{R_1}\right) \cdot V_i$ & $A_V = (1 + R_f/R_1)$

(iii) Voltage follower (or) unity gain amp.

$V_o = V_i \Rightarrow A_V = 1$

Differential amp^r



Analysis:

Using KCL at node 'a', V_3 – ground potential.

$V_2 = V_3$

$$\frac{V_3 - V_1}{R_1} + \frac{V_3 - V_o}{R_2} = 0 \quad \text{—— (1)}.$$

At node 'b'

$$\frac{V_3 - V_2}{R_1} + \frac{V_3}{R_2} = 0 \quad \text{—— (2)}.$$

(2) $\frac{V_2 - V_1}{} - \frac{V_o}{} = 0$

$$\Rightarrow \frac{V_2 - V_1}{R_1} = \frac{V_o}{R_2} \Rightarrow \boxed{V_o = \frac{R_2}{R_1}(V_2 - V_1)}$$

WKT, $V_o = A_d V_d + A_c V_c$

where $V_d = V_2 - V_1$ — (3)

$$V_c = \frac{V_1 + V_2}{2} \Rightarrow 2V_c = V_1 + V_2 \text{ — (4)}$$

(3)+(4), $V_d + 2V_c = 2V_2 \Rightarrow V_2 = \frac{V_d + 2V_c}{2}$

$$\therefore V_1 = V_2 - V_d = \frac{V_d}{2} + V_c - V_d = V_c - \frac{V_d}{2}$$

We have: $V_1 = V_c - \frac{V_d}{2}$ & $V_2 = \frac{V_d}{2} + V_c$ — (A)

Consider, $V_o = A_1 V_1 + A_2 V_2$ — (B)

Sub (A) in (B),

$$V_o = A_1 \cdot \left(V_c - \frac{V_d}{2}\right) + A_2 \left(\frac{V_d}{2} + V_c\right)$$

$$V_o = (A_2 - A_1) \cdot \frac{V_d}{2} + (A_1 + A_2) \cdot V_c$$

$$\boxed{V_o = A_d V_d + A_c V_c}$$

where $A_D = \frac{1}{2}(A_2 - A_1)$

$A_c = A_1 + A_2$;

$$CMRR = \left|\frac{A_d}{A_c}\right| = \infty$$

The main parameter in a diff amp is CMRR

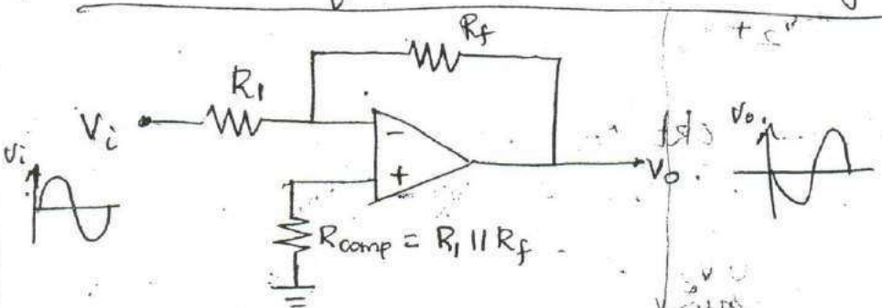
ie., $CMRR = \left|\frac{A_d}{A_c}\right| = \infty$ (Theoretical value)

$= 1000$ or very high (Practical value)

(expressed in dB) — 120 dB

Basic Op amp Applns

* Phase shifter (or) Scale changer



Inverting amp

If $R_f = R_1$ => $A_{CL} = -1$

It is called Inverter

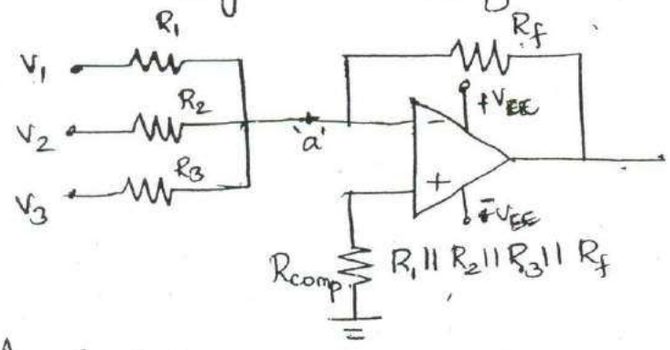
o/p is 180° out of phase with i/p

Analysis: Here $V_o = -\frac{R_f}{R_1} \cdot V_i = -kV_i$

where $k = \frac{R_f}{R_1} = 1$ = Scale changing factor.

* Adder (or) Summing Amp^r

(i) Inverting summing amp^r (with 3 i/ps)



$$V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}.V_2 + \frac{R_f}{R_3}.V_3\right]$$

Analysis:

Node 'a' is at virtual ground.

Apply KCL at 'a',

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_o}{R_f} = 0$$

Rearranging, $\frac{V_o}{R_f} = -\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]$.

$$\Rightarrow V_o = -\left[\frac{R_f}{R_1}.V_1 + \frac{R_f}{R_2}.V_2 + \frac{R_f}{R_3}.V_3\right]$$

Case (i) Let $R_1 = R_2 = R_3 = R_f = R$.

$\therefore V_o = -(V_1 + V_2 + V_3)$

Case (ii) Let $R_1 = R_2 = R_3 = 3R_f = R$

$$V_o = -\left[\frac{V_1 + V_2 + V_3}{3}\right]$$

Case (iii): Let $R_1 = R_2 = R_3 = \frac{R_f}{3} = R$.

$$V_o = -3\left[V_1 + V_2 + V_3\right]$$

1) Design an adder ckt (or) summing amp^r using op-amps to get the o/p equation as

$V_o = -(0.1V_1 + V_2 + 10V_3)$ — ①

Soln: WKT, o/p voltage is inv summer and basic eqn is

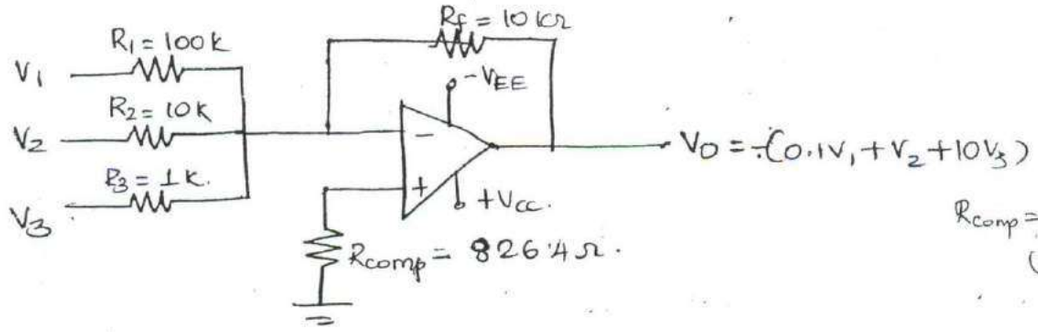
$$V_o = -\left[\frac{R_f}{R_1}.V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}.V_3\right]$$ — ②

Comparing ① & ②,

$\frac{R_f}{R_1} = 0.1$; $\frac{R_f}{R_2} = 1$; $\frac{R_f}{R_3} = 10$

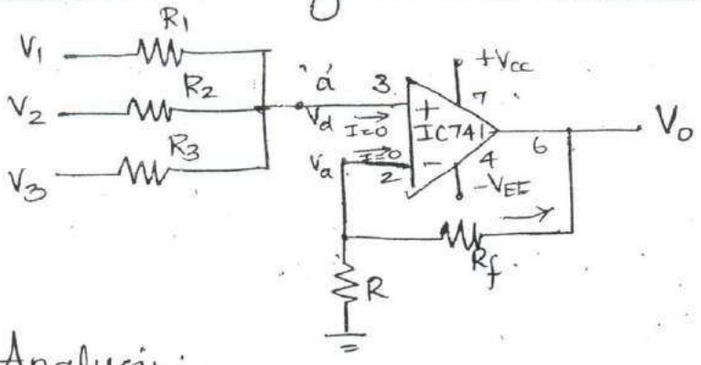
Select $R_f = 10\ k\Omega$

$\Rightarrow R_1 = 100\ k\Omega$, $R_2 = 10\ k\Omega$; $R_3 = 1\ k\Omega$.



$R_{comp} = \frac{R_1 R_2 R_3 R_f}{(R_1 R_2 R_3) + C}$

* Non-inverting Summing amp^r.



Analysis:

At node 'a', applying KCL,

$$\frac{V_a - V_1}{R_1} + \frac{V_a - V_2}{R_2} + \frac{V_a - V_3}{R_3} = 0$$

$$\Rightarrow \frac{V_a}{R_1} + \frac{V_a}{R_2} + \frac{V_a}{R_3} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

$$\Rightarrow V_a = \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)}{\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)} \quad \text{---} \ (1)$$

WKT, as per the non-inv amp^r analysis, $V_o = \left(1 + \frac{R_f}{R_1}\right) V_i$

(where V_i is the i/p signal)

Here $V_i = V_a$ & $R_1 = R$

$\therefore V_o = \left(1 + \frac{R_f}{R_1}\right) \cdot V_a$

Sub V_a in V_o.

$$V_o = \left(1 + \frac{R_f}{R_1}\right) \left\{ \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)}{\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)} \right\}$$

We have, $V_o = \left(1 + \frac{R_f}{R_1}\right)\left[\frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}\right]$

Case (i) : When $R_1 = R_2 = R_3 = \frac{R_f}{2} = R$

$\therefore V_o = (1+2)\left[\frac{\frac{1}{R}(V_1+V_2+V_3)}{\frac{3}{R}}\right]$

$$\boxed{V_o = V_1 + V_2 + V_3}$$

Case (ii) : ~~When~~ To get $V_o = \frac{V_1+V_2+V_3}{3}$

then $R_1 = R_2 = R_3 = R$ & $R_f = 0$

1) Design an adder ckt for the o/p voltage.

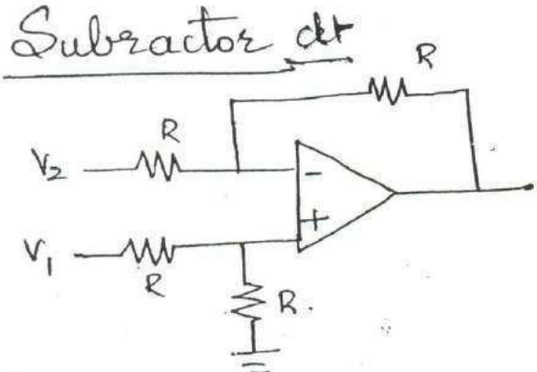
$V_o = \frac{2}{3}(V_1+V_2+V_3)$

Sol^n : Choose $R_1 = R_2 = R_3 = R_f = R = 1\,k\Omega$.

$\therefore V_o = \left(1+\frac{R}{R}\right)\frac{\left[\frac{V_1+V_2+V_3}{R}\right]}{\frac{3}{R}}$

$V_o = \frac{2}{3}[V_1+V_2+V_3]$ (Draw the ckt')

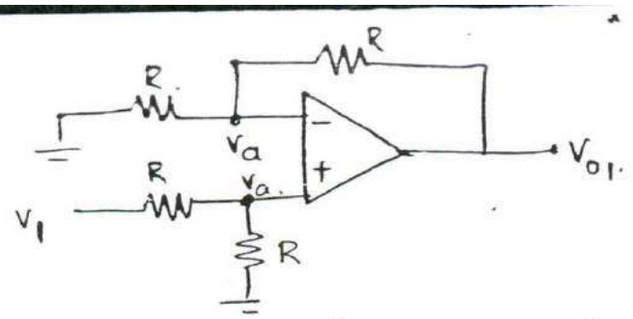
* Subractor ckt



Analysis

When all the resistors have equal value and 2 vge sources are operated then $\therefore$ Superposition theorem is used

Case (i) Consider $V_2 = 0$ and V_1 exist then the ckt is non-inv amp^r.



Here, $V_a = \left(\frac{R}{R+R}\right) \cdot V_1 \Rightarrow V_a = \frac{V_1}{2}$ — (1).

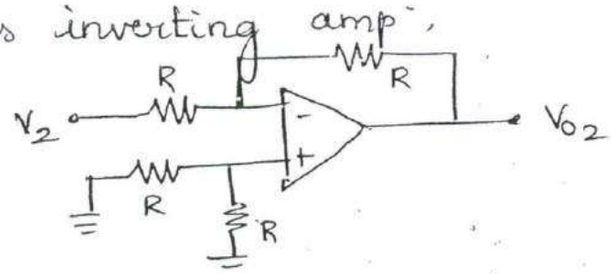
WKT, as per non-inv' analysis,

$V_{01} = \left(1 + \frac{R_f}{R}\right) \cdot V_a$ [Here $V_a = \frac{V_1}{2}$, $R_f = R_1 = R$]

$= \left(1 + \frac{R}{R}\right) \cdot \frac{V_1}{2} = 2 \cdot \frac{V_1}{2}$

$\therefore \boxed{V_{01} = V_1}$ — (A)

Case (ii) When V_2 exist and $V_1 = 0$, then ckt ~~as~~ behaves as inverting amp'.



It is a simple inverting amp',

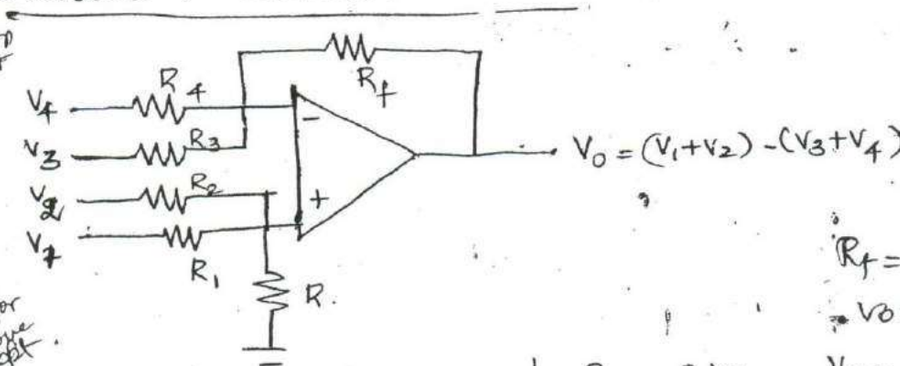
$\therefore V_{02} = \frac{-R}{R} \cdot V_2 \Rightarrow V_{02} = -V_2$ — (2)

$\therefore V_0 = V_{01} + V_{02}$ (By superposition theorem)

$\therefore \boxed{V_0 = V_1 - V_2}$

* Adder - subtractor circuit.

Assign



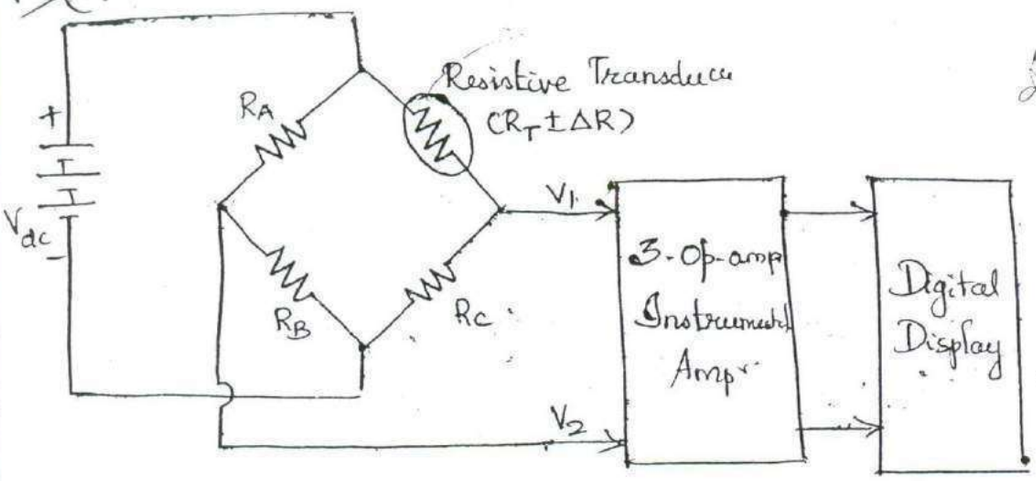
Proof for above ckt.

Anjan: $R_1 = 4k\Omega$, $V_1 = 5V$
$R_2 = 1k\Omega$, $V_2 = 4V$

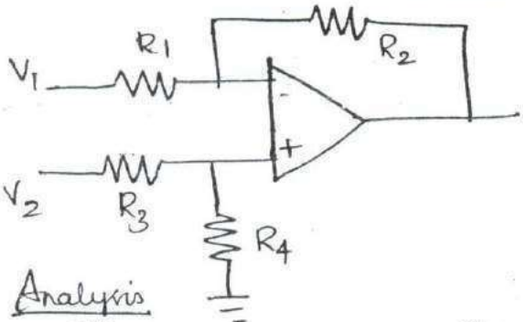
$R_f = 10\ k\Omega$
$V_0 = ?$
$R_3 = 2k\Omega$, $V_3 = 3V$
$R_4 = 8\ k\Omega$, $V_4 = 2V$

28/1/09 Part B (X.)

Instrumentation amplifier



Basic diff^r amp^r



Analysis

$$V_o = -\frac{R_2}{R_1}\cdot V_1 + \left(1+\frac{R_2}{R_1}\right)\cdot V_2\left(\frac{R_4}{R_3+R_4}\right)$$

Analysis

Using superposition principle

$$V_o = -\frac{R_2}{R_1}\cdot V_1 + \left(1+\frac{R_2}{R_1}\right)\cdot V_2\left(\frac{R_4}{R_3+R_4}\right)$$

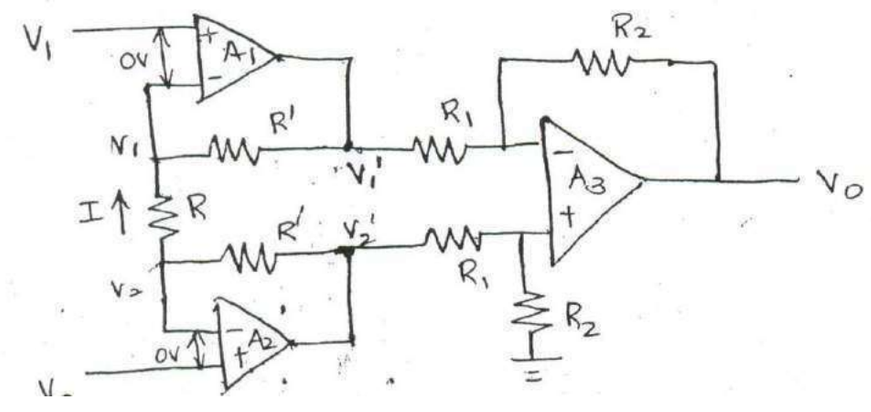
Assume $\frac{R_1}{R_2} = \frac{R_3}{R_4}$

$$\therefore V_o = -\frac{R_2}{R_1}\cdot V_1 + \frac{R_2}{R_1}\left(1+\frac{R_1}{R_2}\right)\cdot V_2\left(\frac{1}{1+R_3/R_4}\right)$$

$$\boxed{V_o = \frac{R_2}{R_1}(V_2 - V_1)}$$

8 mark

Instrumentation Amp (3-opramp IA)



The op-amps A_1 and A_2 working in non-inverting mode and its difference i/p voltage is zero.

The op-amp A_3 works in diffl amp^r mode.

When $V_1 = V_2$ & then resistor $R' = 0$, then A_1 and A_2 act as voltage follower.

If $V_1 \neq V_2$, current flows thro' resistor R & R' then $(V_2' - V_1') > (V_2 - V_1)$. The o/p vge V_o of the op-amp A_3 (considering the +ve i/p terminal) as $V_o = V_2' \left(\frac{R_2}{R_1 + R_2}\right)$

Using superposition theorem

$$V_o = -\frac{R_2}{R_1} \cdot V_1' + \left(1 + \frac{R_2}{R_1}\right) \cdot V_2' \left(\frac{R_2}{R_1 + R_2}\right)$$

$$\boxed{V_o = \frac{R_2}{R_1} (V_2' - V_1')} \quad \text{—(1)}$$

To determine the values of V_1' and V_2' as by the current I, since no current enters op-amp then $I = \frac{V_2 - V_1}{R}$ and also $V_1' = -IR' + V_1$ — (2)

$$V_2' = +IR' + V_2 \quad \text{—(3)}$$

Sub (2) & (3) in (1),

$$V_o = \frac{R_2}{R_1} \left[+IR' + V_2 + IR' - V_1\right]$$

$$= \frac{R_2}{R_1} \left[V_2 - V_1 + 2\left(\frac{V_2 - V_1}{R}\right) \cdot R'\right]$$

$$\boxed{V_o = \frac{R_2}{R_1} (V_2 - V_1) \left[1 + \frac{2R'}{R}\right]}$$

Comparing with the basic diffl amp^r, the term $\left(1 + \frac{2R'}{R}\right)$ is increased as further amplification to tune the digital display.

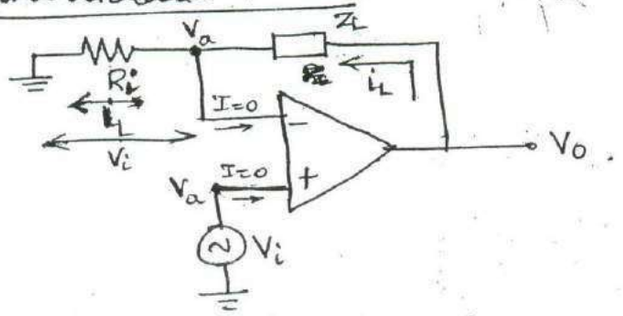
X) List the features of instrumentation amplifier.

29/1/04

* V to I convertor (transconductance amp^r)

This transconductance amp^r having many applications, which converts an i/p v$_{ge}$ signal to a proportional o/p current. There are two types as (i) V to I converter with floating load
(ii) V to I converter with grounded load.

(i) Floating ~~Grounded~~ load



Non-inv amp^r

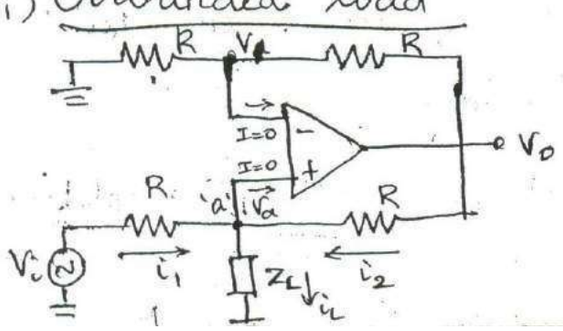
The load Z_L is a floating type which is connected across the i/p and o/p ~~terminals~~ (in the place of feedback element). As we know, no current enters into op-amp then, the i/p voltage V_i flows across R_i to carry out the load current i_L. Thus i/p voltage is converted to o/p current.

Analysis:

As per the non-inv amp^r configuration, the node pt (or) voltage $V_a = V_i$

$\Rightarrow$ Voltage drop across $R_i = V_i$ and from the ckt diagram, $V_i = R_i \cdot i_L \Rightarrow \boxed{i_L = \frac{V_i}{R_i}}$ (V_i and R_i are known)

(ii) Grounded load



$V_1 = V_2 = 0$

$V_o = V_1 + V_2$

Analysis:

Apply KCL at node 'a', $i_1 + i_2 = i_L = 0$

$\Rightarrow \frac{-V_a + V_i}{R} + \frac{V_o - V_a}{R} - i_L = 0$

Here $V_a = V_i$ (~~virtual ground~~)

$\Rightarrow \frac{V_i}{R} + \frac{V_o}{R} - i_L = \frac{2V_i}{R} \Rightarrow V_i + V_o - i_L R = 2V_i$ — (1)

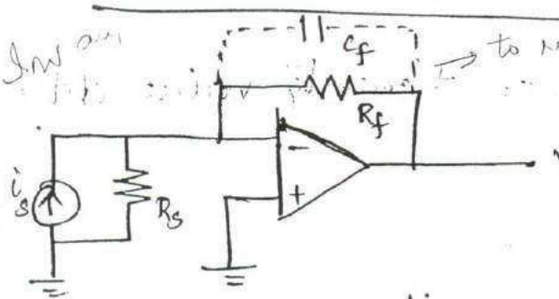
As per the non-inv amp^r, $V_o = \left(1 + \frac{R}{R}\right) V_i$

$V_o = 2V_i$ — (2)

Sub (2) in (1), $2V_i + V_o - i_L R = V_o$

$$\boxed{i_L = \frac{V_i}{R}}$$

* I to V converter (Transresistance amp^r)



To carry out this transresistance amp^r operating in inv configuration then the o/p voltage $V_o = -R_f$ is

The capacitor C_f makes the ckt to withstand the noise interference and R_f and C_f acts as filter ckt then $V_o = -R_f i_s - j\omega R_f C_f$ is

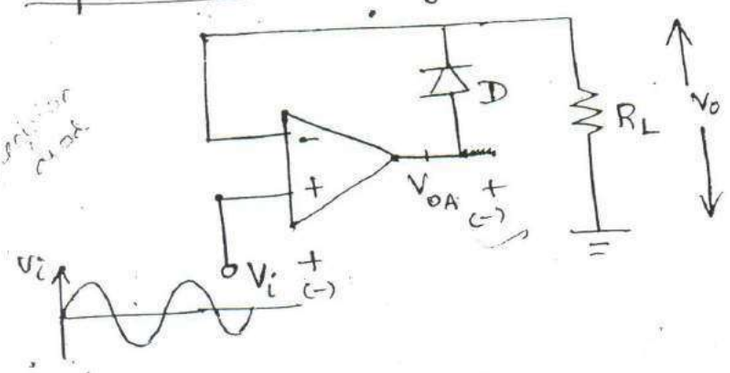
$\therefore |A| = |-j\omega R_f C_f| \cong |\omega R_f C_f|$

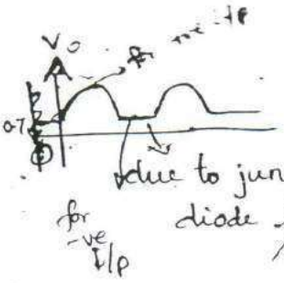
$= |2\pi f R_f C_f|$ $\left(\because f_a = \frac{1}{2\pi R_f C_f}\right)$

$|A| = \left|\frac{f}{f_a}\right|$

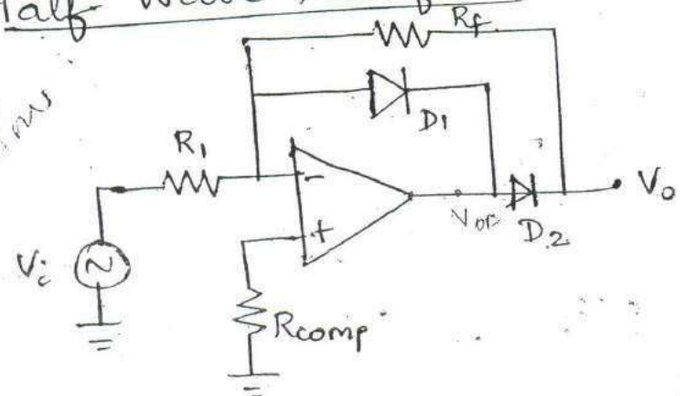
(*). The noise interference or high freq implemental to withstand the ckt, the gain will be decayed with a value f/f_a.

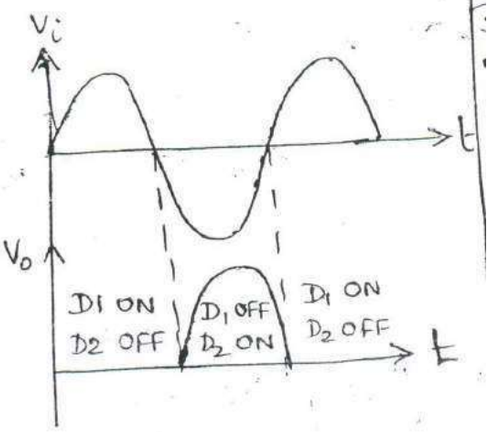
* Op-amps using diodes (Precision diode)



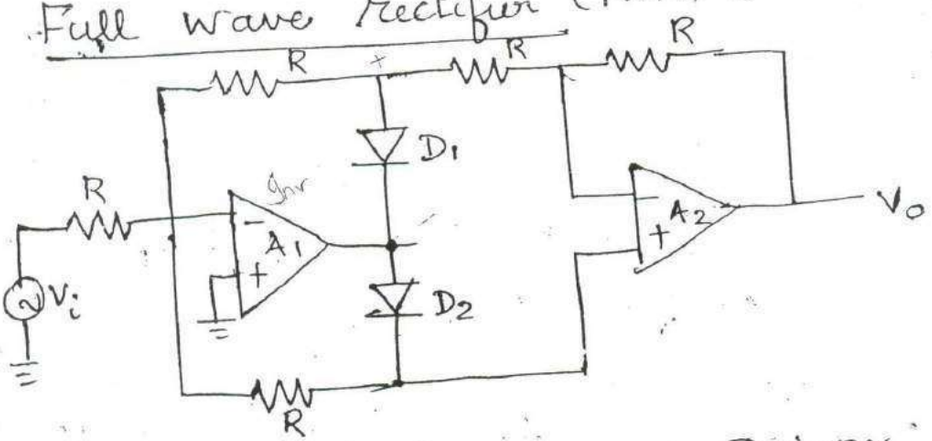


Half wave rectifier

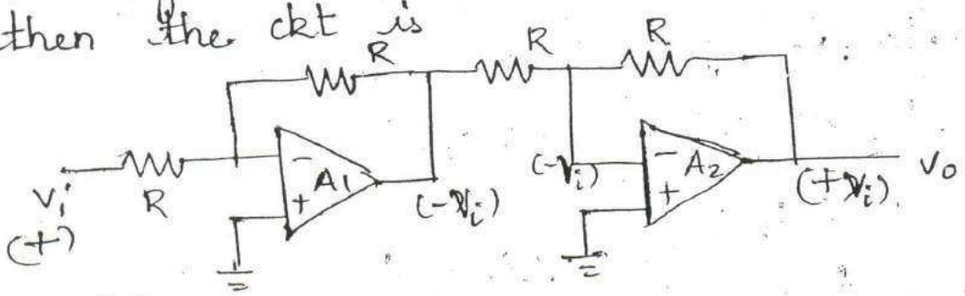


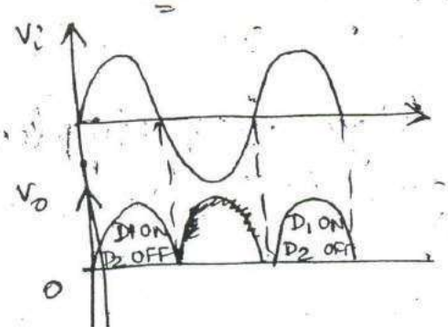


Full wave rectifier (FWR) (or) Absolute value ckt

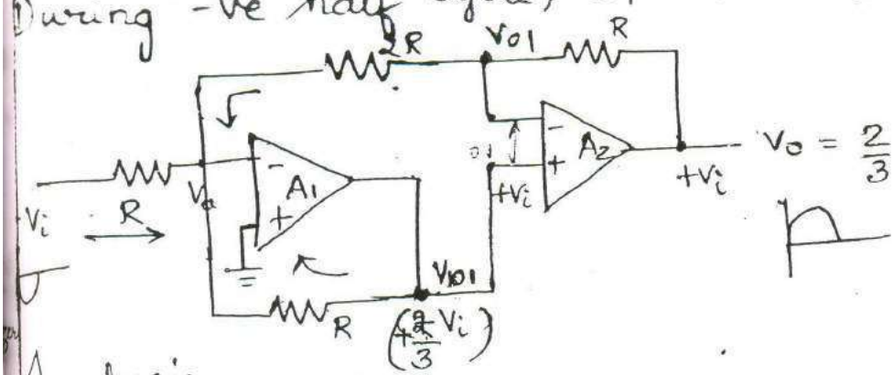


During +ve half cycle, D_1 is ON and D_2 is OFF then the ckt is





During -ve half cycle, D_1 OFF & D_2 ON.



$$V_o = \frac{2}{3} \cdot V_i \left(1 + \frac{R}{2R}\right)$$

Analysis

~~for A~~ Apply KCL, ~~$\frac{-V_i - V_a}{R}$~~

For first op-amp, inv confg.

The resistor in FB part, using KCL

$$\frac{V_i}{R} + \frac{V_{01}}{2R} + \frac{V_{01}}{R} = 0 \Rightarrow \frac{V_i}{R} = -\frac{V_{01}}{R}\left[\frac{1}{2} + 1\right]$$

$$\frac{V_i}{R} = -\frac{3}{2} \cdot \frac{V_{01}}{R}$$

$$\Rightarrow V_{01} = -\frac{2}{3} V_i \quad (\because V_i = -V_i) \hookrightarrow \text{-ve i/p}$$

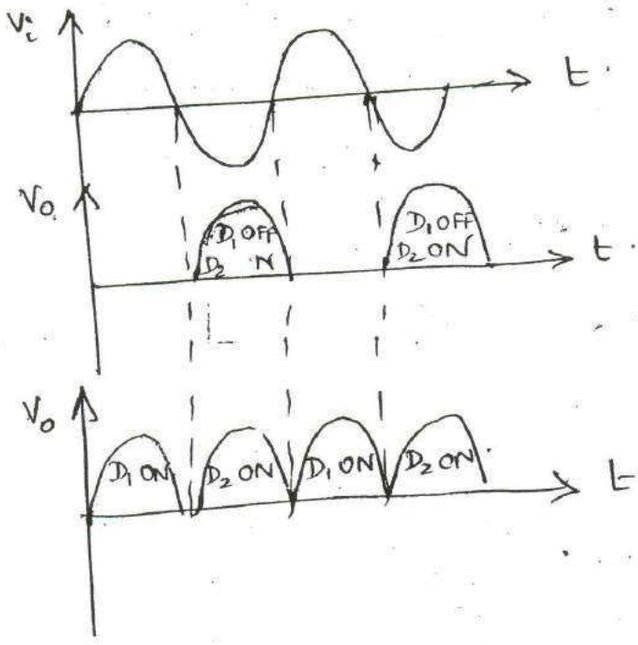
$$\boxed{V_{01} = \frac{2}{3} V_i} \quad \text{---} (1)$$

At second op-amp, non-inv amp confg

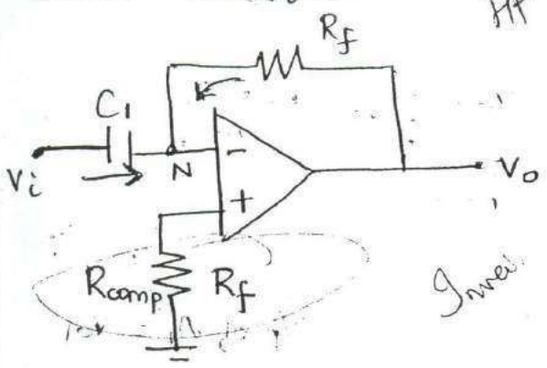
$$V_o = \left(1 + \frac{R}{2R}\right) V_{01}$$

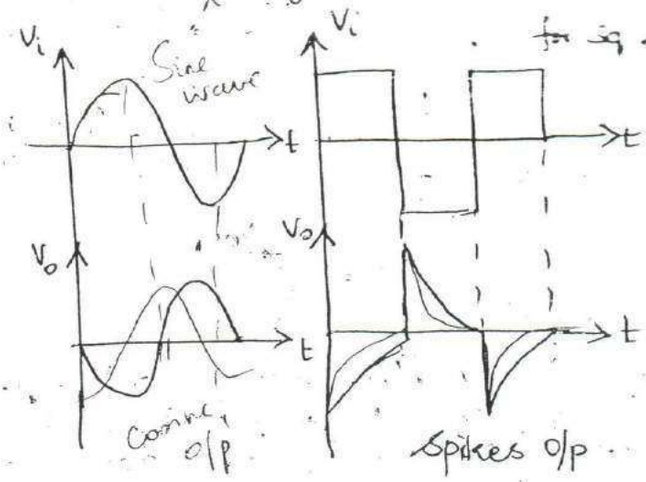
$$= \left(1 + \frac{1}{2}\right) \cdot \frac{2}{3} V_i = \frac{3}{2} \times \frac{2}{3} V_i$$

$$\boxed{V_o = V_i}$$



30.1.04) * Differentiator (I order Active High Pass filter)





Analysis

Apply KCL, ∵ 'N' is virtual ground

$$\therefore C_1 \frac{dV_i}{dt} + \frac{V_o}{R_f} = 0 \quad \Rightarrow \quad \frac{V_o}{R_f} = -C_1 \frac{dV_i}{dt}$$

$$\Rightarrow \boxed{V_o = -R_f C_1 \frac{dV_i}{dt}}$$

(-ve ⇒ 180° phase shift)

Phasor equivalent of above eqn.

Taking L.T, $V_o(s) = -R_f C_1 s V_i(s)$.

$$\left|\frac{V_o(s)}{V_i(s)}\right| = s R_f C_1$$

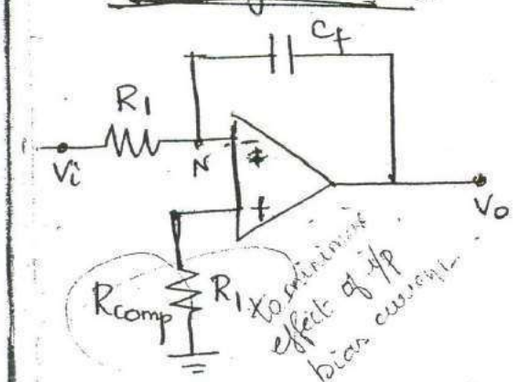
Put $s = j\omega$, $= j\omega R_f C_1$

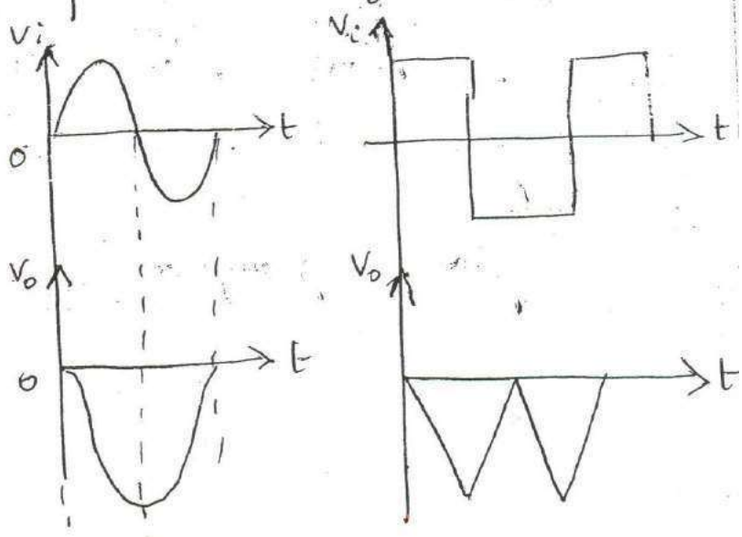
$$\left|\frac{V_o(s)}{V_i(s)}\right| = \left|\frac{\omega}{\omega_a}\right| = \left|\frac{f}{f_a}\right| \quad \left(\because f_a = \frac{1}{2\pi R_f C_1}\right)$$

The transfer fn of this differentiator ckt increases/decayed in the rate +20 dB / decade (since it is I order high pass active filter)

(2)

* Integrator (LP)





(i) Analysis

Apply KCL, Node 'N' is at virtual ground.

$$\frac{V_i}{R_f} + C_f \cdot \frac{dV_o}{dt} = 0 \Rightarrow C_f \frac{dV_o}{dt} = \frac{-V_i}{R_1}$$

$$\Rightarrow \int \frac{dV_o}{dt} = \int \frac{-V_i}{R_f C_f}$$

$$\therefore \text{Satg}, \quad V_o = \frac{-1}{R_f C_f} \int_0^t V_i\, dt + V_i(0)$$

$$\Rightarrow \boxed{V_o = \frac{-1}{R_1 C_f} \int_0^t V_i\, dt}$$

-ve sign ⇒ inverting integrator

In phasor notation.

Taking L.T,

$$V_o(s) = \frac{-1}{R_1 C_f}\left[\frac{V_i(s)}{s} + \frac{V_i(0)}{s}\right]$$

$$\left|\frac{V_o(s)}{V_i(s)}\right| = \frac{1}{sR_1C_f}$$

Put $s = j\omega \Rightarrow \left|\frac{V_o(s)}{V_i(s)}\right| = \left|\frac{1}{j\omega R_1 C_f}\right| = \frac{1}{\omega R_1 C_f}$.

Take $f_b = \frac{1}{2\pi R_1 C_f} \Rightarrow \left|\frac{V_o(s)}{V_i(s)}\right| = \left|\frac{\omega_b}{\omega}\right| = \left|\frac{f_b}{f}\right|$

freq at which gain is 0dB.

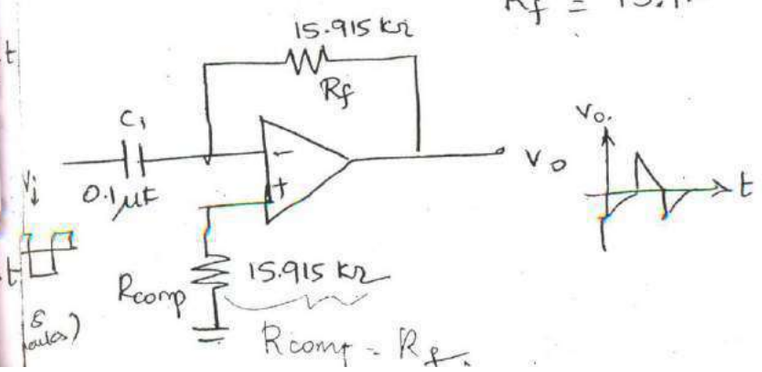
gain decreases at the rate of -20dB/decade

Design an op-amp differentiator at differentiates an i/p signal with the freq $f_{max} = 100$ Hz (consider $C = 0.1\,\mu F$)

∴ Given: $f_a = f_{max} = 100$ Hz & $C = 0.1\,\mu F$

$$\therefore f_a = \frac{1}{2\pi R_f C_1} \Rightarrow R_f = \frac{1}{2\pi(100)\times(0.1\times10^{-6})}$$

$$R_f = 15.915\ K\Omega$$



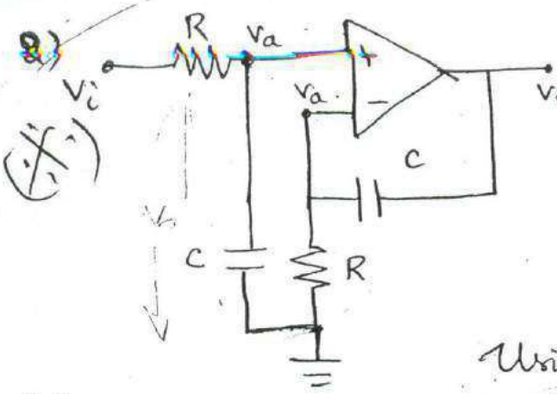
2) 

fig shows a non-inv integrator. S.T $V_o = \frac{1}{RC}\int V_i\,dt$

Sol: Using voltage divider theorem,

$$V_a = \frac{V_i}{R+\frac{1}{sC}} \cdot \frac{1}{sC} = \frac{V_i}{sRC} \quad \text{---(1)}.$$

WKT for the non-inv amp^r confg for the i/p V_a, then $V_o = \left(1+\frac{R_f}{R}\right) \cdot V_a$

$$= \left(1+\frac{1/Cs}{R}\right) \cdot \frac{V_i}{\left(R+\frac{1}{Cs}\right)} \cdot \frac{1}{sC}.$$

$$= \left(\frac{R+1/sC}{R}\right) \cdot \frac{V_i}{(R+1/Cs)} \cdot \frac{1}{sC}.$$

$$V_o(s) = \frac{V_i(s)}{sRC}.$$

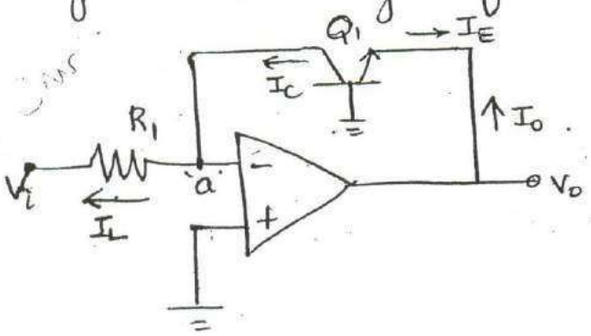
Taking ILT, $V_o(t) = \frac{1}{RC}\int V_i(t)\,dt$.

(Inv)

3|1|

Logarithmic Amplifier

One would like to have a direct decibel display on a multimeter or digital voltmeter or spectrum analyser can perform the log amp^r operation. It also be used to compress the dynamic range of the given signal.



In this ckt, the feedback element as a grounded base transistor along with collector terminal of Q_1 is connected to virtual ground (at node 'a')
∴ Our analysis will be proceeded by considering diode equation.

Analysis:

As per diode eqn (or) current I_E as:

$$I_E = I_S\left(e^{qV_E/KT} - 1\right) \quad \text{— (1)}$$

where I_E – emitter current of grounded base transistor Q_1

q – charge of $e^- = 1.69 \times 10^{-19}$ K – Boltzmann const $= 1.38 \times 10^{-23}$.

I_S – saturation current $\simeq 10^{-13}$ A

T – Temp^r = 0K.

As per the ckt diagram, $I_E = I_C$

∴ (1) $\Rightarrow I_C = I_S\left(e^{qV_E/KT} - 1\right)$

$$\Rightarrow e^{\frac{qV_E}{KT}} = \frac{I_C}{I_S} + 1 \Rightarrow \frac{qV_E}{KT} = \ln\left(\frac{I_C}{I_S} + 1\right)$$

But $\frac{I_C}{I_S} \gg 1$ ($\because I_S = 10^{-13}$ A)

$$\therefore V_E = \frac{KT}{q}\ln\left(\frac{I_C}{I_S}\right) \quad \text{— (2)}$$

At the i/p side, $I_L = \frac{V_i}{R_1} = I_C$.

(2) $\Rightarrow V_E = \frac{KT}{q}\ln\left(\frac{V_i}{R_1 I_S}\right)$

Let $V_{ref} = R_1 I_S$ and $V_E = -V_o$ (inv amp)

$$\therefore V_E = -V_o = \frac{KT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$$

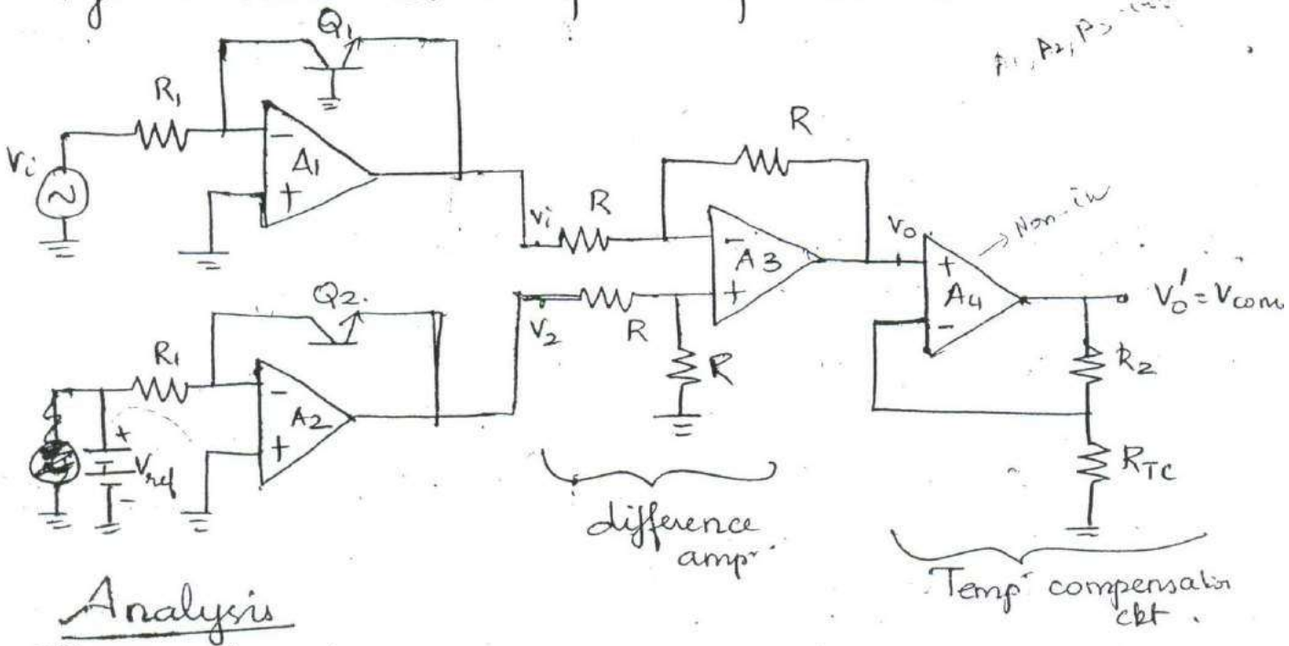
or

$$\boxed{V_o = -\frac{KT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)}$$

The o/p voltage is proportional to logarithm of i/p voltage.

In this log ckt, the main drawback (or) temp^r compensation ckt and proper reference vgs

are not given. Therefore to make proper application oriented ckt using a constant ref vge as well as temp' compensation ckt



Analysis

Basic log ckt, $V_1 = -\frac{KT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right)$

$V_2 = -\frac{KT}{q} \ln\left(\frac{V_{ref}}{R_1 I_S}\right)$

} If Q_1 & Q_2 are identical.

For diff amp',

$$V_2 - V_1 = +\frac{KT}{q} \ln\left[\frac{V_i}{R_1 I_S} \times \frac{R_1 I_S}{V_{ref}}\right]$$

$$V_o = \frac{KT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

$V_o = -\frac{KT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$

$\therefore V_o' = V_{comp} = \left(1 + \frac{R_2}{R_{TC}}\right) V_o$ (Non-inv)

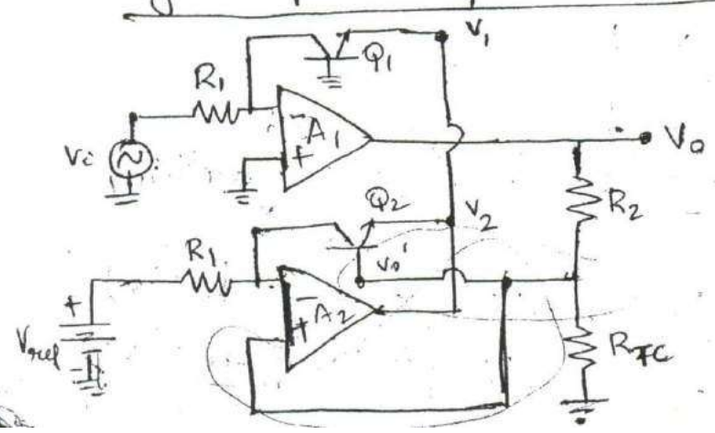
$V_o' = \left(1 + \frac{R_2}{R_{TC}}\right) \frac{KT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$

$$\boxed{V_o' = \left(1 + \frac{R_2}{R_{TC}}\right) \cdot \frac{KT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)}$$ where R_{TC} – sensistor

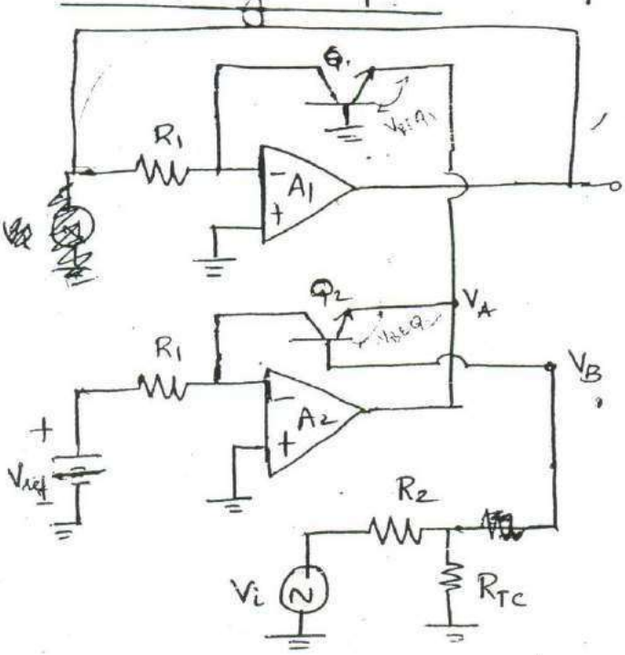
2/2/04

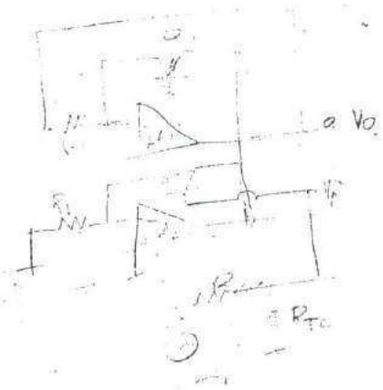
* log-amp' - Compensation ckt (Using 2 op-amps only)

(inv)



* Anti-log amp^r - Compensation ckt





The i/p V_i for the anti-log amp^r is fed into the temp^r compensation ckt via a voltage divider R_2 and R_{TC} and then to the base of Q_2 O/p V_o of antilog amp^r is fed to inv i/p of A'1 thro' a resistor R_1. Therfore, base-emitter vge of transistor Q_1 and Q_2

$$V_{Q_1 BE} = -\frac{KT}{q} \ln\left(\frac{V_o}{R_1 I_S}\right) \quad \text{— (1)}$$

$$V_{Q_2 BE} = -\frac{KT}{q} \ln\left(\frac{V_{ref}}{R_1 I_S}\right) \quad \text{— (2)}$$

from the ckt,

$$V_A = V_{Q_1 BE} = -\frac{KT}{q} \ln\left(\frac{V_o}{I_1 R_1}\right) \quad \text{— (3)}$$

W^{kg}

$$V_A = V_{Q_2 BE} + V_B = V_{Q_2 BE} + \frac{V_i \cdot R_{TC}}{R_2 + R_{TC}} \quad \text{— (4)}$$

$$= -\frac{KT}{q} \ln\left(\frac{V_{ref}}{I_1 R_S}\right) + \frac{V_i R_{TC}}{R_2 + R_{TC}}$$

Equating (3) & (4),

$$-\frac{KT}{q} \ln\left(\frac{V_o}{I_1 R_S}\right) = -\frac{KT}{q} \ln\left(\frac{V_{ref}}{I_1 R_S}\right) + \frac{V_i R_{TC}}{R_2 + R_{TC}}$$

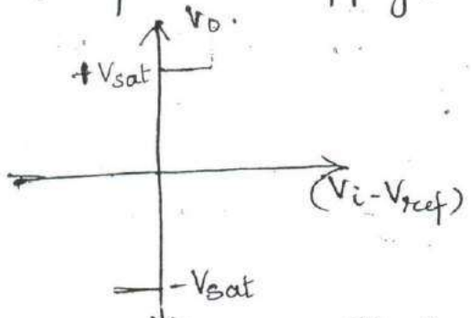
$$-\frac{KT}{q} \ln\left(\frac{V_o}{V_{ref}}\right) = \frac{V_i \cdot R_{TC}}{R_2 + R_{TC}}$$

$$\ln\left(\frac{V_o}{V_{ref}}\right) = -\frac{q V_i}{KT} \cdot \frac{R_{TC}}{R_2 + R_{TC}}$$

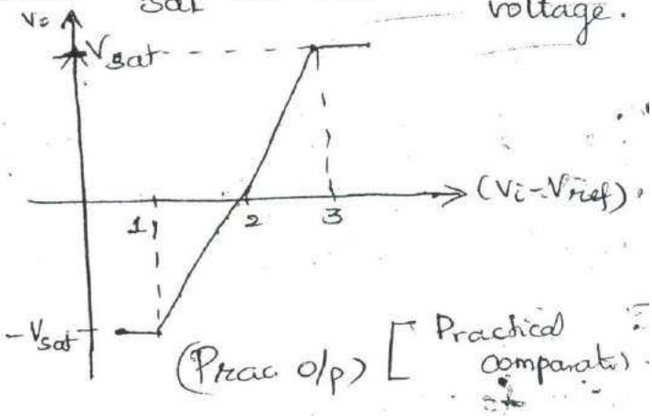
Taking anti-log $\Rightarrow$ $V_o = V_{ref} \cdot 10^{-k' V_i}$

* Comparator

It is a ckt which compares a signal voltage applied at one i/p of an op-amp with the applied dc voltage V_{ref} at the other i/p. It basically works in open-loop config with the o/p levels at $\pm V_{sat}$ (ie $+V_{cc}$ & $-V_{EE}$ applied dc power supply) where V_{sat} is dc saturation voltage.



(Theoretical o/p) [Ideal comparator]

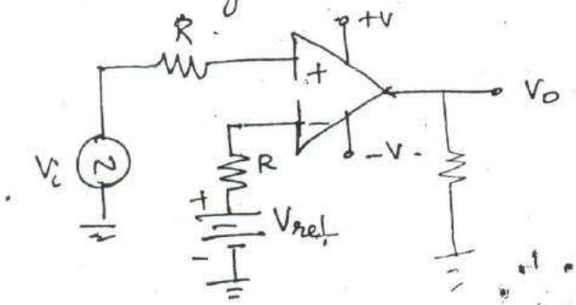


(Prac o/p) [Practical comparator]

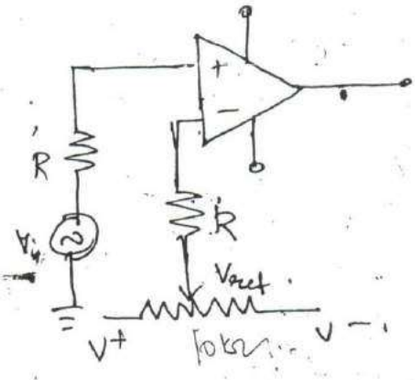
4/2/04

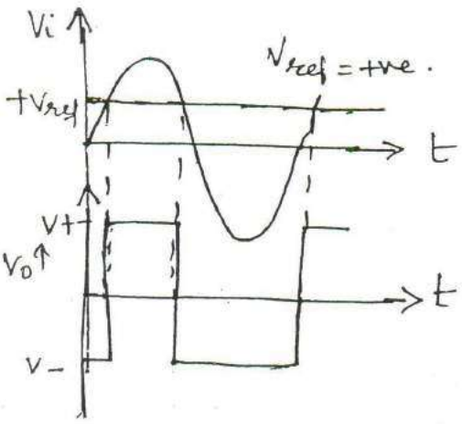
Comparator < Non-inv comp.
Inv. comp.

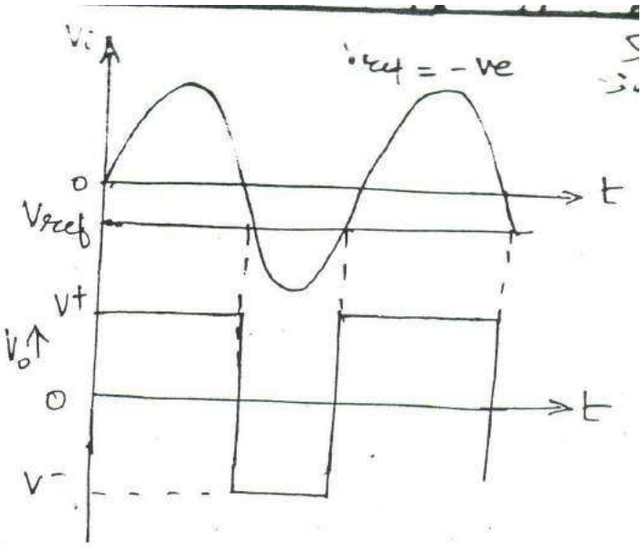
Non-inverting comparator.



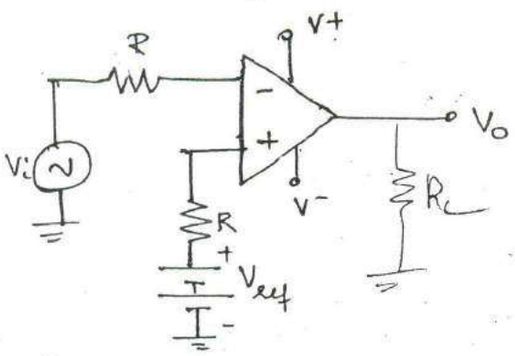
Practical Non-inv co



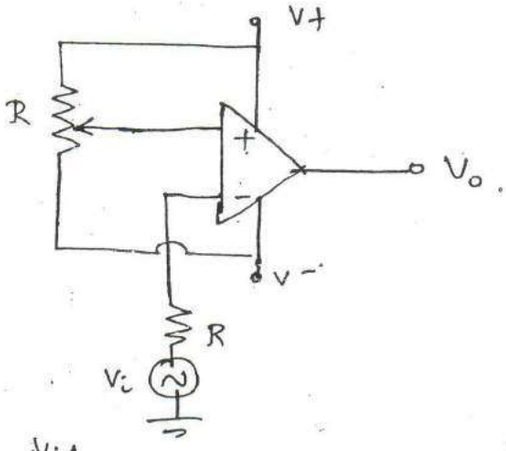


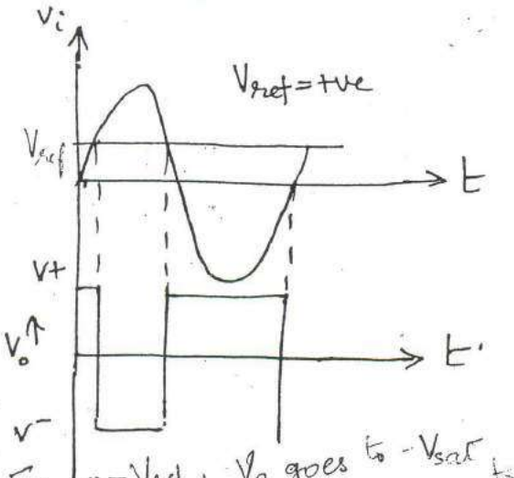


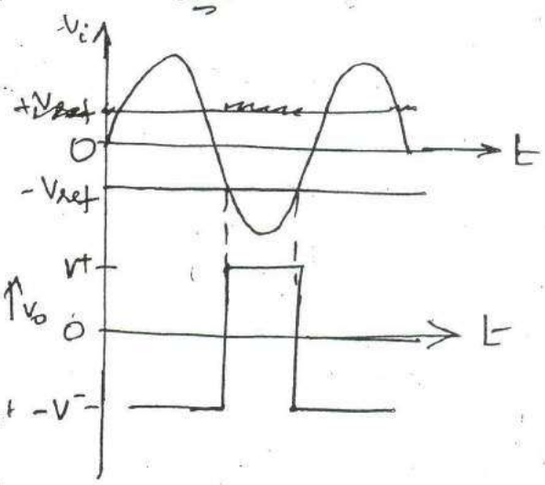
*Inverting comparator



Practical type







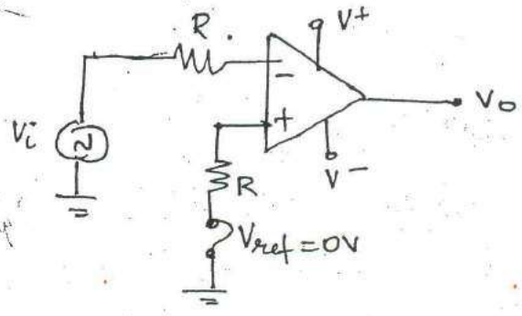
For $V_i > V_{ref}$, V_o goes to $-V_{sat}$
for $V_i < V_{ref}$, V_o goes to $+V_{sat}$

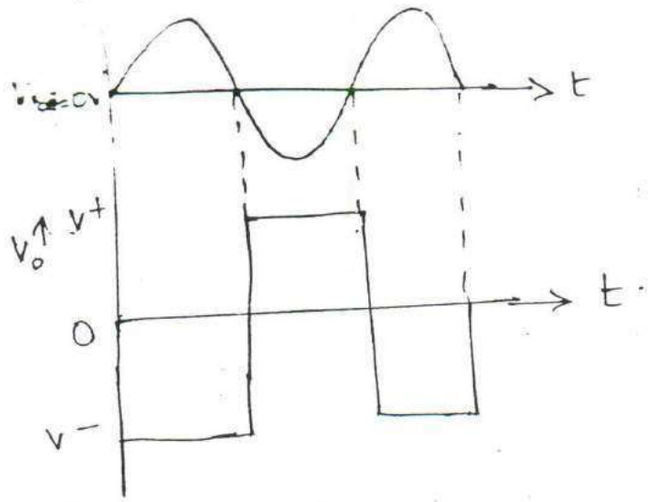
Applications of Comparator:

1). Zero crossing detector
2) Time marker generator
3) Window detector
4) Phase meter

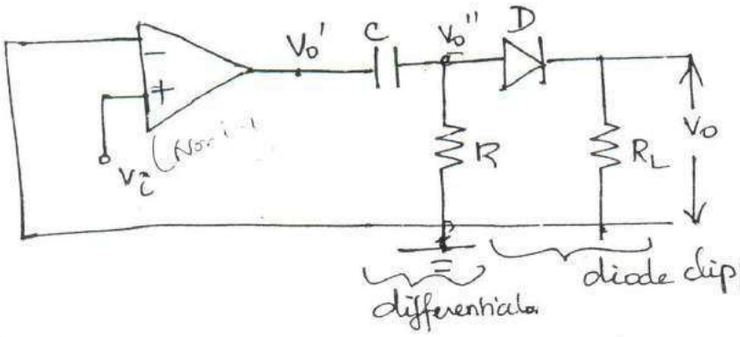
Sine - Square wave generator

Zero crossing detector

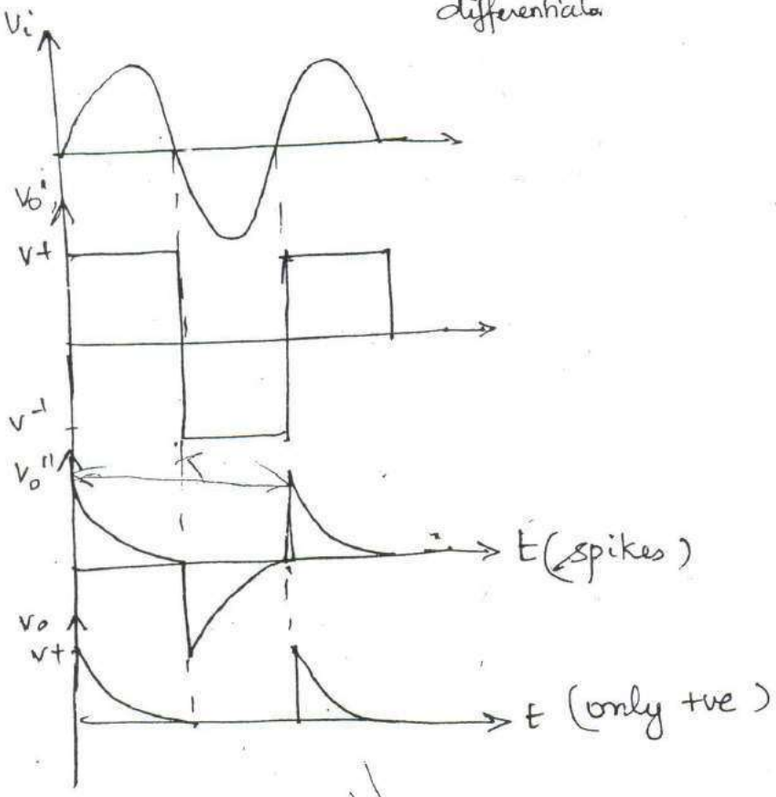




Time Marker generator



Sinusoid → train of +ve pulse of spacing T

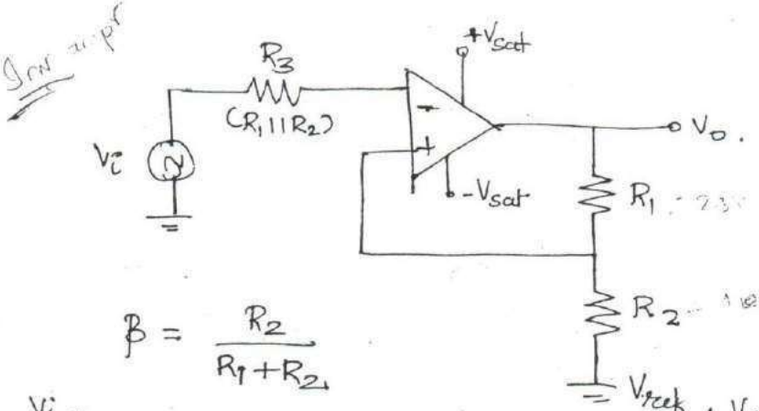


Regenerative Comparator

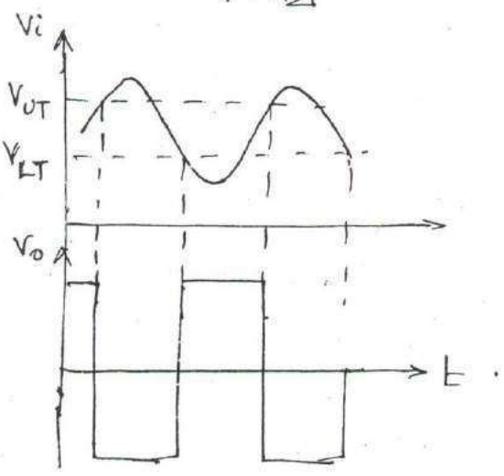
Schmitt Trigger :

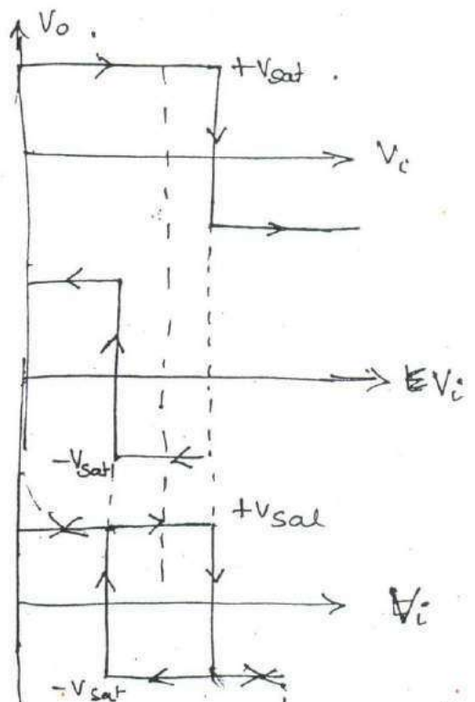
If +ve FB is added to an amp^r ckt, gain can be increased abruptly. Therefore the transfer chara is

now closely to the ideal curve. If the loop gain $A_{OL}\beta$ is unity, then gain with FB A_{VF} becomes infinite. This results in a transition between the extreme values of o/p voltage. However it may not be possible to maintain loop gain exactly unity for a long time because of supply voltage and temp^r variation ie., a value greater than 1 is chosen. This gives an o/p virtually discontinuous. Thus ckt exhibits a phenomenon called Hysteresis phenomenon or backlash. This principle implies in this Schmitt trigger ckt and the comparator action regenerates and also called regenerative comparator.



$$\beta = \frac{R_2}{R_1 + R_2}$$





I/p voltage is applied to the inverting terminal and the FB voltage to the non-inv

The voltage V_i triggers the o/p V_o every time it exceeds certain voltage levels and are called upper threshold point UTP and lower threshold pt LTP. The hysteresis width is the difference between two threshold voltages $V_{UT} - V_{LT}$.

Analysis:

Consider the o/p $V_o = +V_{sat}$ at the +ve I/p terminal (the non-inv terminal)

$$\therefore V_{UT} = V_{ref} + \frac{R_2}{R_1+R_2}(V_{sat} - V_{ref}) \quad \text{---} (1)$$

As long as $V_i < V_{UT}$, o/p V_o remains constant at $+V_{sat}$. When $V_i > V_{UT}$, o/p switches to $-V_{sat}$ and remains as long as $V_i > V_{UT}$

$$V_{LT} = +V_{ref} - \frac{R_2}{R_1+R_2}(V_{sat} + V_{ref}) \quad \text{---} (2)$$

(For $V_o = -V_{sat}$)

I/p $V_i < V_{LT}$, causes V_o to switch from $-V_{sat}$ to $+V_{sat}$. A regenerative transition takes place and the o/p returns from $-V_{sat}$ to $+V_{sat}$ instantaneously

$\therefore$ hysteresis width $V_H = V_{UT} - V_{LT}$

$$= \frac{R_2}{R_1+R_2}[V_{sat} - V_{ref} + V_{sat} + V_{ref}]$$

$$= \frac{2R_2}{R_1+R_2} \cdot V_{sat}.$$

The resistance R_3 is chosen as $R_1 \| R_2$ as a compensating resistor for the i/p bias current.

Applications:

This ckt applies in the electronic devices to convert a very slowly varying i/p voltage into a square wave o/p.

Lab Design ckt

For the practical ckts consider $V_{ref} = 0V$ and $V_{UT} = V_{LT}$ then,

$$V_H = V_{UT} + (-V_{LT}) = \frac{2R_2}{R_1+R_2}(\pm V_{sat})$$

$$= \frac{R_2}{R_1+R_2} V_{sat} - \frac{R_2}{R_1+R_2}(-V_{sat})$$

$$\Rightarrow V_{UT} = V_{LT} = \frac{R_2}{R_1+R_2}(\pm V_{sat})$$

Practical sinusoidal freq $f = \frac{1}{t}$ is calculated from the symmetrical square wave achieved at the o/p. CMOS IC's available as with the inverting Schmitt trigger with its number 74C14 & CD40106

AIM :- Design & construct a Schmitt trigger ckt such that the i/p voltage triggers the o/p voltage levels between the threshold levels ± 0.5 V.

Consider $\pm V_{sat} = \pm 12$ V.

Design:

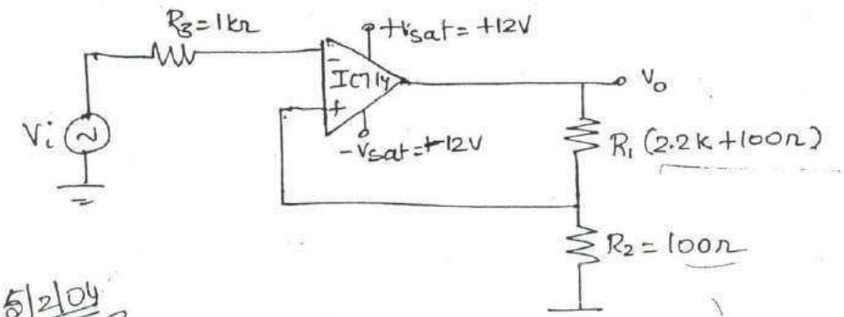
$$V_{UT} = \frac{R_2}{R_1+R_2}(\pm V_{sat})$$

Consider $R_2 = 100\,\Omega$, $V_{UT} = 0.5$V, $\pm V_{sat} = +12$ V.

$$\Rightarrow 0.5 = \frac{100}{R_1+100} \times 12$$

$$\Rightarrow 0.5R_1 + 50 = 1200 \Rightarrow \boxed{R_1 = 2300\,\Omega}$$

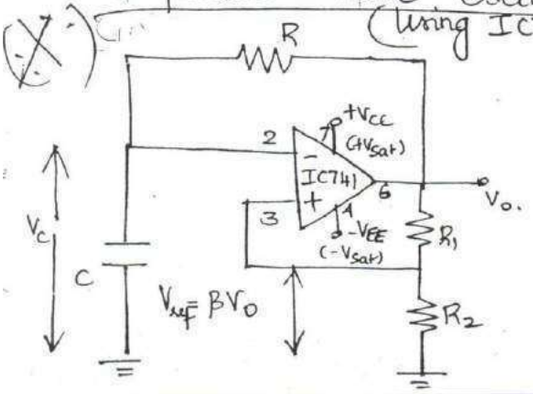
$\therefore R_3 = R_1 \| R_2 \simeq 1$ K.

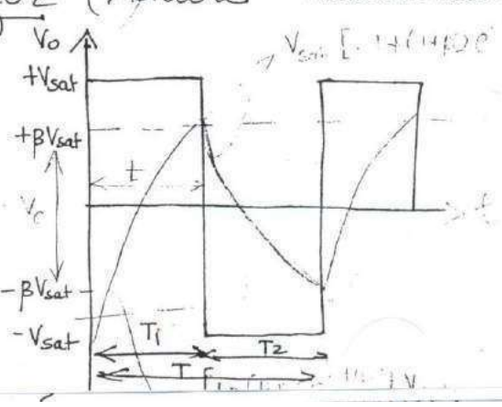


5/2/04

Square Wave Oscillator (Astable Multivibrator)

(using IC741)





UNIT – III

ANALOG MULTIPLIER AND PLL

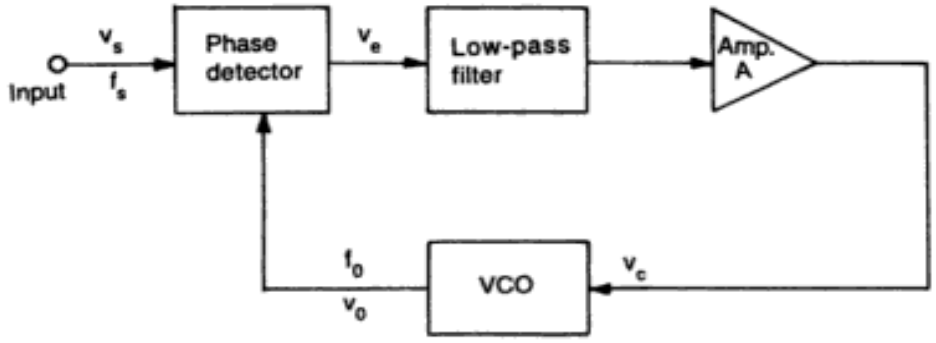
Analog Multiplier using Emitter Coupled Transistor Pair-Gilbert Multiplier cell-Variable transconductance technique- Analog multiplier ICs and their applications-Operation of the basic PLL-Closed loop analysis-Voltage controlled oscillator-Monolithic PLL IC 565, Application of PLL for AM detection,FM detection; FSK modulation and demodulation and Frequency synthesizer.

Operation of the basic Phase Locked Loop (PLL)

- The PLL is a basic building block in all linear system.
  - Electronic PLL came into existence in 1930 when it was used for Radar synchronization and all communication applications.
  - Monolithic IC PLL are used as electronic frequency control in today's satellite communication system, air borne navigational systems, FM communication systems ,computers etc…

Basic Principles of PLL

The basic block diagram of the PLL is



This feedback system consists of

1. Phase comparator circuit/Detector circuit
2. Low Pass Filter
3. Error amplifier
4. Voltage Controlled Oscillator

- The VCO is a free running multivibrator and operates at a set frequency f_o called free running frequency. This frequency is determined by external timing capacitorC_T and an external resistor R_T .It can be shifted to either side by applying a dc control voltage V_C to the terminal of the IC

- The frequency deviation is directly proportional to the dc control voltage V_C and hence it is called VCO.

- If an input signal V_S of the frequency f_s is applied to the phase detector. It compares the phase and frequency of the incoming signal to that of the output V_o of the VCO.

- If the two signals differ in freq and phase an error voltage V_e is generated.

- The phase detector is a multiplier and produces the sum ($f_S + f_o$) and difference ($f_S - f_o$) components at its output.

- The high frequency component is removed by the LPF and the difference frequency component is amplified and then applied as control voltage V_C to VCO.

- The signal V_C shifts the VCO frequency in a direction to reduce the frequency difference between f_S and f_o.During this action the signal is in the capture range.

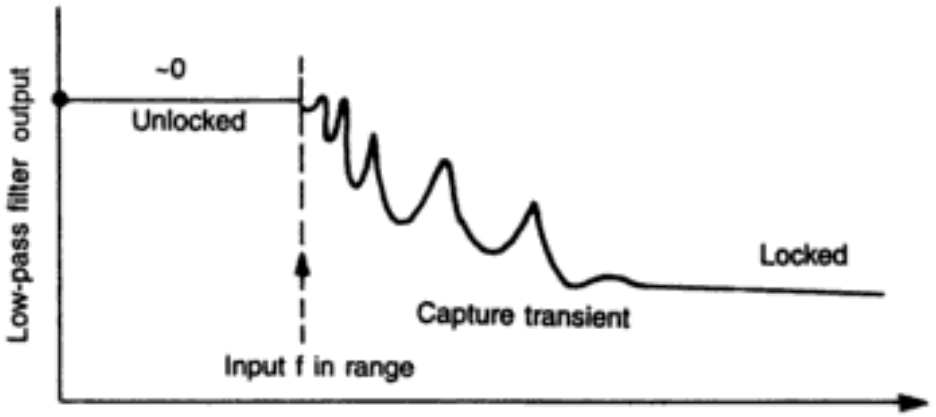
- The VCO continues to change freq till its output freq is exactly the same as the input signal frequency .The circuit is then said to be locked.

- Once locked the output frequency f_o of VCO is identical to f_S except for a finite phase difference φ. This phase difference φ generates a corrective control voltage V_C to shift the VCO frequency from f_o. to f_S and thereby maintain the lock.

- Once locked PLL tracks the freq changes of the input signal.

Three frequencies range of PLL

- Free running frequency (f_o)
- Capture range frequency
- Lock in range/Tracking range frequency



Free running frequency (f_o) (or) VCO frequency.

- In this PLL, VCO circuit is used to generate a square wave form of its own through an external timing resistor (R_T) and capacitor C_T. And this frequency is called as a free running frequency

$$f_o = \frac{0.25}{R_T C_T} = \frac{1}{4R_T C_T}$$

Lock in range/Tracking range frequency

- The PLL circuit is said to be locked ,it can trap frequency changes in the incoming signal. The range of frequency over which the PLL can maintain lock with the incoming signals is called Lock in range/Tracking range frequency

Capture range frequency

- The range of frequency over which the PLL can acquire lock with the input signal called Capture range .This parameter is also expressed as a percentage of f_o

- From the capture transient curve it indicates a sine wave appears due to the difference frequency between VCO and input signal. And also lock in range is always greater than the capture range.

Pull in time

- The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference and loop filter characteristics.

PHASE DETECTOR /COMPARATOR

There are two types of phase detector are available

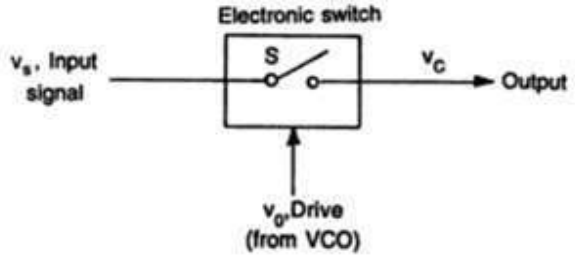
- Analog phase detector
- Digital phase detector

ANALOG PHASE DETECTOR:

- Two types of analog phase detectors are
  - switch type phase detector
  - Balanced modulator type phase detector

SWITCH TYPE PHASE DETECTOR:

- Switch type phase detector consists of electronic switches.



- The switch is opened and closed by signal coming from VCO.[normally Vo is square wave].The switch is closed when VCO output is positive otherwise it is open.

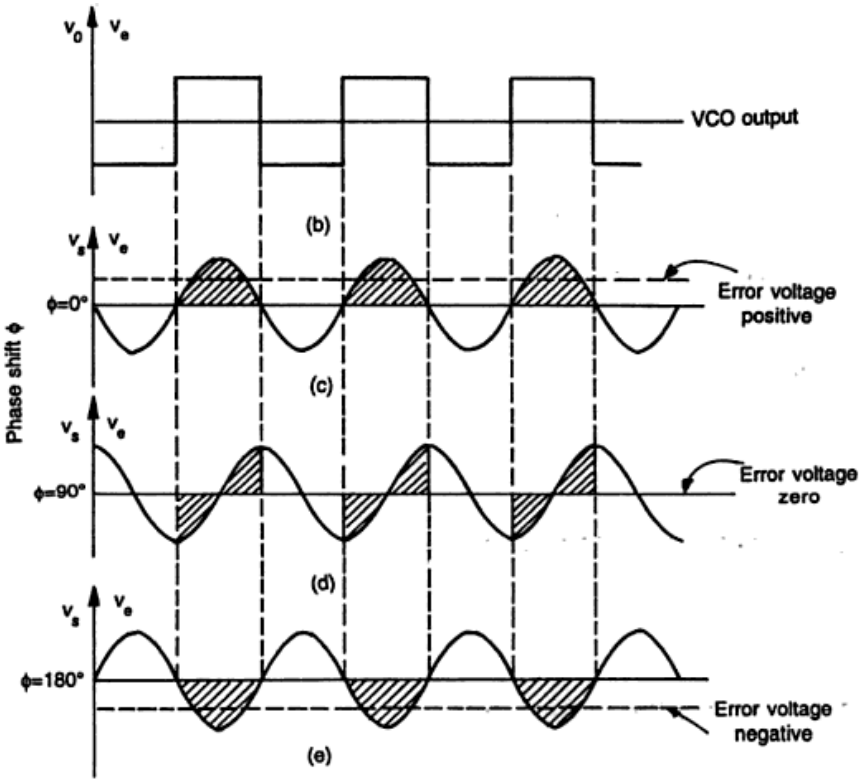
OUTPUTS OF PHASE DETECTOR AT DIFFERENT PHASE ANGLES OF INPUT SIGNALS:

- When φ=0. ie) when the input V_s is in phase with when VCO output phase detector waveform V_e will be half sinusoids.
- When φ=90^o; the output waveform V_e contains half portion of negative cycle and half portion of positive half cycle.
- When φ=180^o; the output waveform V_e contains negative half sinusoidal.

- The error voltage is zero when the phase shift between the two inputs [V_s&V_o] is 90^o .This is a perfect lock condition.

- The switch type phase detector is called a half wave detector. Since the phase information for only one half of input waveform is detected and averaged.

- The output of the phase comparator when filtered through a low pass filter gives an error signal which is the average value of the output waveform.



Phase detector for PLL (a) Basic scheme (b) VCO output waveform.
Input and output waveform (hatched) of phase detector for
(c) $\phi = 0$ (d) $\phi = 90°$ (e) $\phi = 180°$

ANALYSIS:

- A phase comparator is a multiplier which multiplies the input signal $V_s = v_s \sin 2\pi f_s\, t$ by the vco signal signal $V_o = v_o \sin 2\pi f_o\, t + \varphi$

The phase comparator output is $V_e = v_s v_o$

$$V_e = v_s v_o$$

$$V_e = v_s\, v_o \sin 2\pi f_s\, t \sin 2\pi f_o\, t + \varphi$$

$$V_e = \frac{\text{kVsVo}}{2}[\cos(2\pi f_s - 2\pi f_o\, t - \varphi)\ - \cos\,(2\pi f_s + 2\pi f_o\, t + \varphi)]$$

k→ phase comparator gain
φ→ phase shift between input and vco output

When at a lock $f_s = f_0$

$$V_e = \frac{k v_s v_o}{2}[\cos(-\varphi) - \cos(2\pi * 2 f_o t + \varphi)]$$

- The phase comparator output contains a double frequency term and a dc term $\left(\frac{kVoVs}{2}\right)\cos\varphi$ which varies as a function of phase φ ie; cosφ between the two signals.

- The double freq term is eliminated by the LPF and the dc signal is applied to the modulating input terminal of a VCO. For perfect locked state ($f_s = f_0$), the phase shift should be 90^o [cos 90=0] ie; Ve=0.

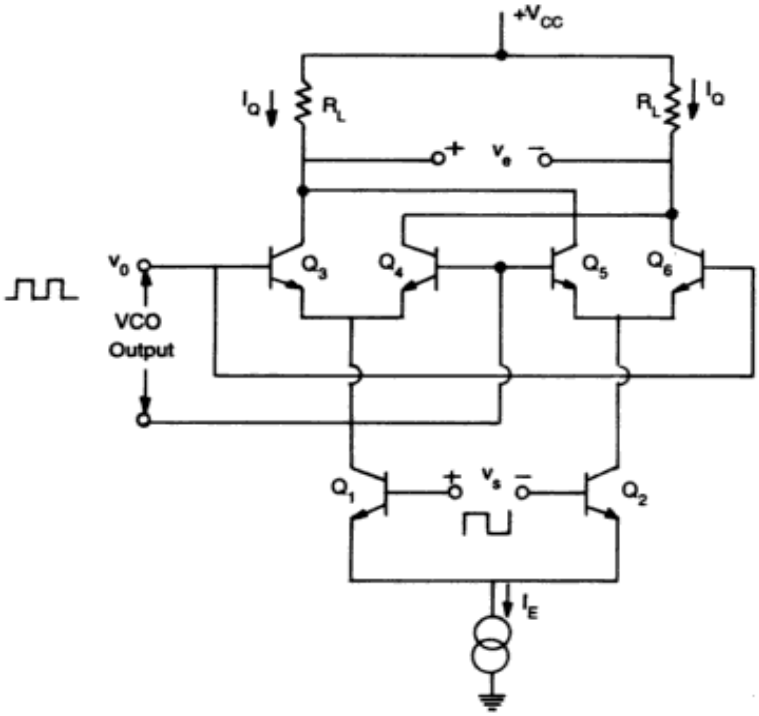
PROBLEMS ASSOCIATED WITH SWITCH TYPE PHASE DETECTOR

- The output voltage Ve is proportional to the input signal amplitude Vs. this is undesirable. Since it makes phase detector gain and the loop gain dependent on the input signal amplitude. The output is proportional to cosφ and not proportional to φ making it non- linear.

- Both these problem can be eliminated by limiting the amplitude of the input signal.ie; converting the input to a constant amplitude square wave.

BALANCED MODULATOR TYPE PHASE DETECTOR:

- This is a balanced modulator used as full-wave switching phase detector.



- Here the input signal is applied to the differential pair Q_1 Q_2.Transistors $Q_3 - Q_4$ and $Q_5 - Q_6$ are two set of SPDT switches activated by the VCO output.

- The input signal Vs and the VCO output Vo are assumed to be high enough to switch the transistors in fully on (or) off

- When Vs and Vo both are high during the time 0 to (π-φ),transistors Q1 and Q3 are driven on and current I_E flows through Q_1 and Q_3

- This gives an output voltage

$$V_e = -I_E R_L$$

- For the period (π-φ)for π , when Vs is high and Vo is low, transistors Q1 and Q4 are driven on resulting in an output voltage

$$V_e = I_E R_L$$

- The average value of the phase detector output Ve can be calculated as

$$(V_e)_{av} = \frac{1}{\pi}[(\boldsymbol{area\ A_1 + area\ A_2})]$$

$$= \frac{\mathbf{1}}{\boldsymbol{\pi}}[(\boldsymbol{I_E R_L \varphi} + (-\boldsymbol{I_E R_L}) * (\boldsymbol{\pi - \varphi})$$

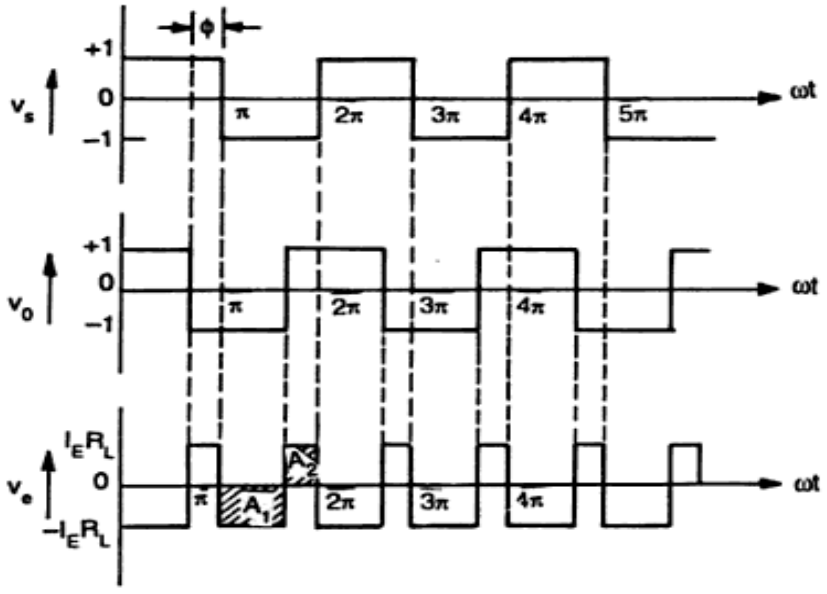
$$= \boldsymbol{I_E R_L}\left[\frac{\mathbf{2\varphi}}{\boldsymbol{\pi}} - \mathbf{1}\right]$$

$$(V_e)_{av} = \mathbf{4}\frac{I_Q R_L}{\pi}\left[\varphi - \frac{\pi}{2}\right] \qquad \boldsymbol{since I_E = 2I_Q}$$

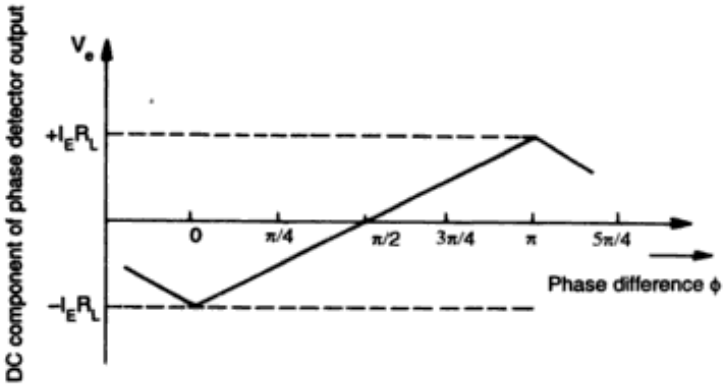
$$(V_e)_{av} = \boldsymbol{K_\varphi}[\boldsymbol{\varphi} - \frac{\boldsymbol{\pi}}{\mathbf{2}}]$$

Kφ->phase angle to voltage transfer coefficient or the conversion ratio of the phase detector.

- The output dc voltage versus input phase difference of balanced modulator full-wave switching phase detector is shown below.



(b) Timing diagram of input and output waveforms for balanced modulator circuit



DIGITAL PHASE DETECTOR

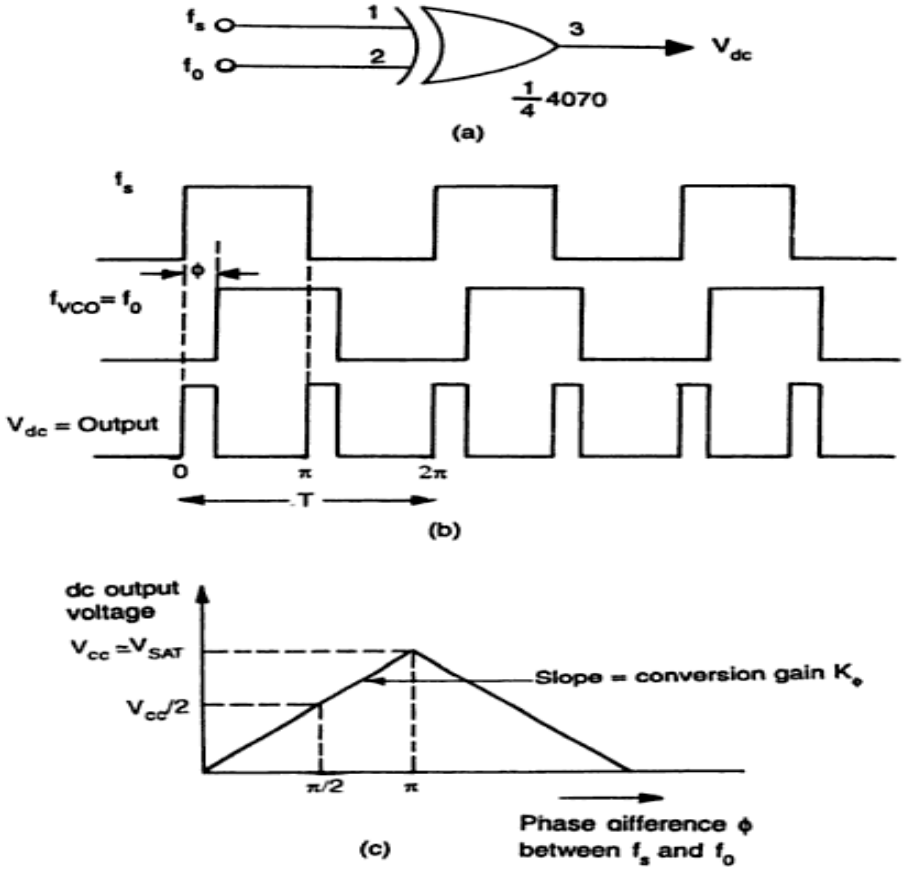
Two types of digital phase detectors are

- Exclusive –OR phase detector
- Edge-triggered phase detector using CD4001.

EXCLUSIVE –OR PHASE DETECTOR

- It uses CMOS type 4070 quad 2-input XOR gate.

- The output of the XOR gate is high when only one of the inputs signal fs or fo high. This type of detector is used when both the input signals are square waves.



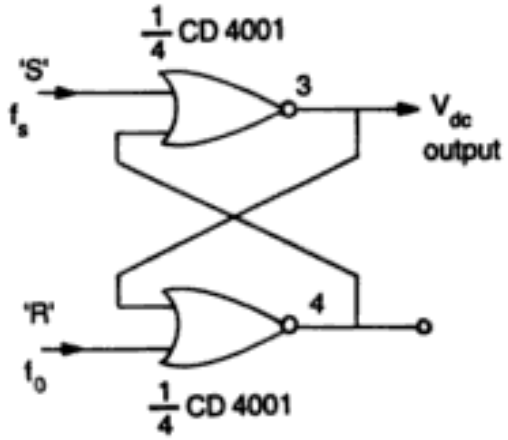
- In this figure fs is leading fo by φ degrees. From the dc output versus phase difference φ curve, the maximum dc output voltage occurs when the phase difference is π because the output of the gate remains high throughout.

- The slope of the curve gives the conversion ratio kφ of the phase detector. So the conversion ratio Kφ for a supply voltage Vcc=5v is

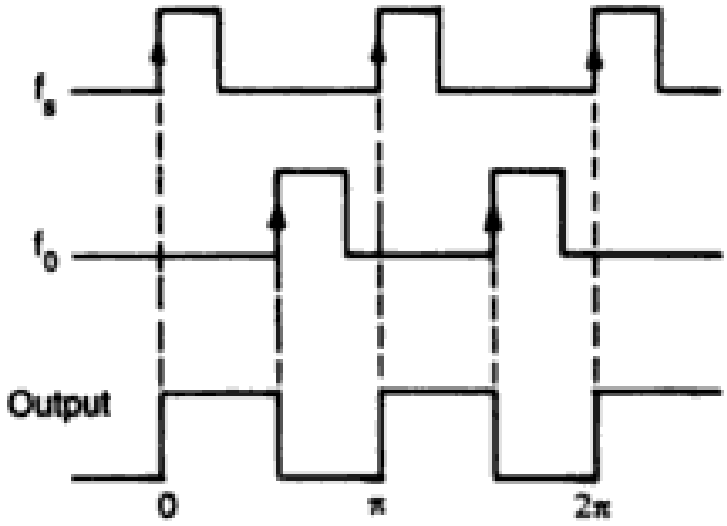
$$K\varphi = \frac{5}{\pi} = 1.59 \text{ v/rad}$$

EDGE –TRIGGERED PHASE DETECTOR

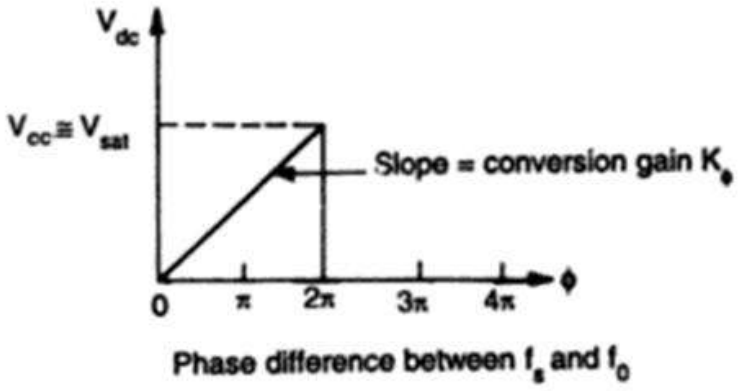
- Edge –triggered phase detector circuit is an R-S flip-flop made by NOR gates such as CD4001.



- This circuit is useful when fs and f0 are both pulse wave-forms with duty cycle less than 50%.The output of the R-S flip-flop changes its state on the leading edge of fs and f0.

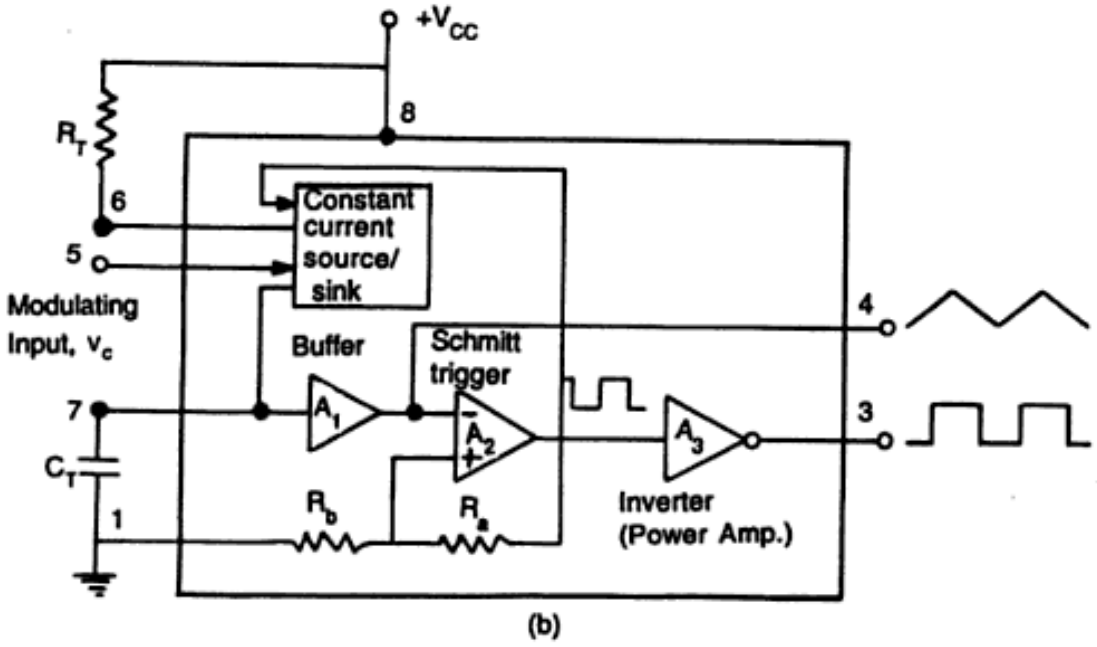


- This type of detector has better capture tracking and locking characteristics as the dc output voltage up to 360˚ compared to 180˚ in the case of exclusive-OR detector.



VOLTAGE CONTROLLED OSCILLATOR (VCO) [566 VCO]

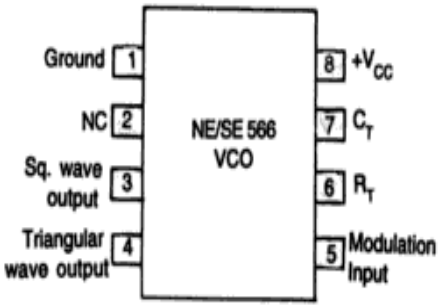
- A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage. Applied voltage is called control voltage.



(b)

- The control of freq with the help of control voltage is called voltage is called voltage to frequency conversion.VCO is called voltage to frequency conversion.

- A timing capacitor C_T is linearly charged or discharged by a constant current source.The amount of current can be controlled by changing the voltage Vc applied at the modulating input, or by changing the timing resistor R_T external to IC chip.



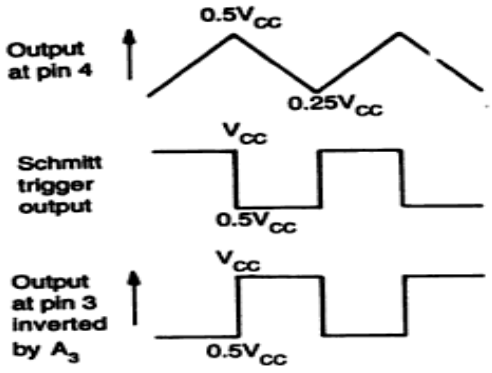
- The voltage at pin.6 is held at the same voltage as pin.5. Thus if the modulating voltage at pin.5 is increased, the voltage at pin.6 also increased ,resulting in less voltage across R_T and thereby decreasing the charging current. The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A2 via buffer amplifier A1.

- The output voltage swing of the Schmitt trigger is designed to Vcc and 0.5Vcc.If Ra=Rb in the positive feedback loop, the voltage at the non-inverting input terminal of A2 swings from 0.5 Vccto 0.25 Vcc.

- From the waveform ,when the voltage on the capacitor CT exceeds 0.5 Vcc during charging the output of the Schmitt trigger goes low(0.5 Vcc).

- The capacitor now discharges and when it is at 0.25 Vcc,the output of Schmitt trigger goes high(Vcc).Since the source and sink currents are equal.Capacitor charges and discharges for the same amount of time .This gives a triangular voltage waveform across CT which is also available at pin.4.

- The square wave output of the Schmitt trigger is inverted A3 and is available at the pin.3.



OUTPUT FREQUENCY OF THE VCO

- The total voltage on the capacitor changes from 0.5 Vcc to 0.5 Vcc.Thus $\Delta v = 0.25vcc$.

- The capacitor charges with a constant current source.

$$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

$$\frac{0.25\ Vcc}{\Delta t} = \frac{i}{C_T}$$

$$\Delta t = \frac{0.25\ Vcc\ C_T}{i}$$

FOR FULL CYCLE

$$2\Delta t = t = \frac{0.5\ Vcc\ C_T}{i}$$

The time period T of the triangular waveform =2Δt.The frequency of oscillator f_o is

$$f_o = \frac{1}{T} = \frac{1}{2\Delta t}$$

$$f_o = \frac{1}{T} = \frac{i}{0.5\ Vcc\ C_T}$$

To eliminate the value of i, from the ckt diagram we have

$$i = \frac{Vcc - Vc}{R_T}$$

$$f_o = \frac{2(Vcc - Vc)}{Vcc\ R_T C_T}$$

The output frequency of the VCO can be changed either by

- R_T
- C_T
- The voltage Vc at the modulating input terminal pin.

The components R_T and C_T are first selected so that VCO output frequency lies in the centre of the operating freq. range. Now the modulating input voltage is usually varied from 0.75 Vcc which can produce a frequency variation of about 10-1.
With no modulating input signal, if the voltage at pin.5 is biased at 7/8 Vcc.

$$\text{VCO freq is} \qquad \Delta f_o = \frac{2[Vcc - Vc + \Delta v_c]}{Vcc\ R_T C_T} = \frac{0.25}{R_T C_T}$$

$$f_o = \frac{0.25}{R_T C_T}$$

APPLICATION:

- It is many used in generation of FM output.
- It is also a basic building block in PLL ckt.

VOLTAGE TO FREQUENCY CONVERSION FACTOR K_V

This factor makes the ratio b/w the change in vcofreq to the change in control voltage Vc ie; modulation input voltage.

$$K_V = \frac{\Delta f_o}{\Delta v_c}$$

Δv_c–modulation voltage required to produce the frequency shift Δf_o for a VCO.

Assume that the original frequency f_o and the new freq is f_1 then,

$$\Delta f_o = f_o - f_1$$

$$\Delta f_o = \frac{2[\mathrm{Vcc} - \mathrm{Vc} + \Delta v_c]}{\mathrm{Vcc}\ \mathrm{R_T C_T}} - \frac{2[\mathrm{Vcc} - \mathrm{Vc}]}{\mathrm{Vcc}\ \mathrm{R_T C_T}}$$

$$\Delta f_o = \frac{2[\Delta v_c]}{\mathrm{Vcc}\ \mathrm{R_T C_T}} \ ; \qquad \mathrm{R_T C_{T_o}} = \frac{0.25}{\mathrm{f_o}}$$

$$\Delta f_o = \frac{8\mathrm{f_o}\Delta v_c}{\mathrm{Vcc}}$$

$$K_v = \frac{\Delta f_o}{\Delta v_c} = \frac{8\mathrm{f_o}}{\mathrm{Vcc}}$$

LOW PASS FILTER:

The filter used in a PLL many be either passive type (or) active type.
The functions of LPF in PLL are

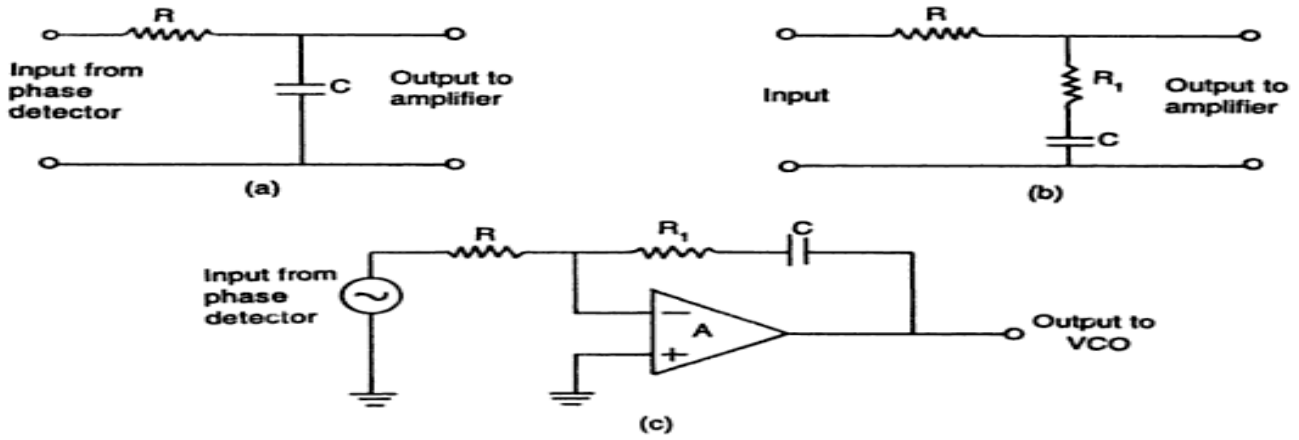
- Removes the high freq components.
- Control the dynamic characteristics of the PLL.
- Change on the capacitor gives a short time to the PLL.

Normally noise freq is considered as a high freq and it is removed by LPF.PLL control the dynamic characteristics, these characteristics include capture and lock range, bandwidth and transient response.

If filter bandwidth is reduced, the response time increases. Reducing the bandwidth of the filter also reduces the capture range of the PLL.

$$\text{Bandwidth} \propto \frac{1}{\text{responce time}} \propto \text{capture range}$$

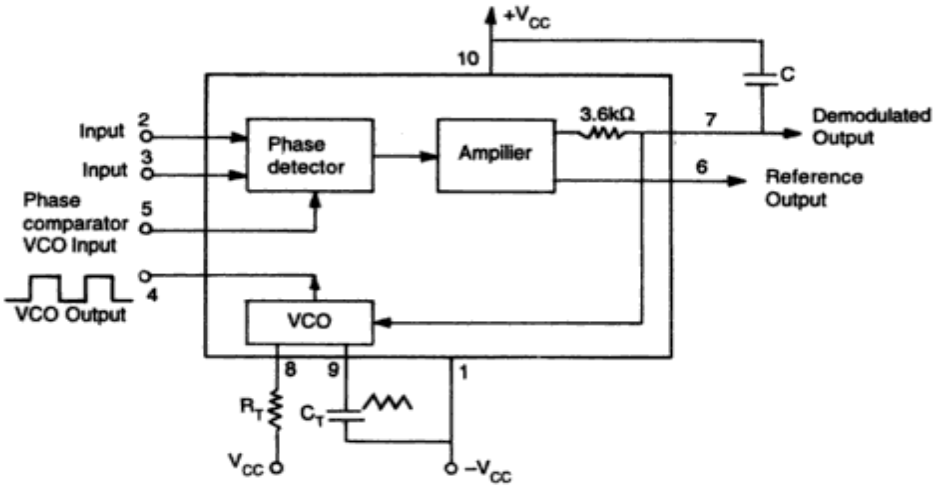
The charge on the filter, capacitor gives a short time memory to the PLL. Thus even if the signal becomes less than the noise for a few cycles , the dc voltage on the capacitor continues to shift the freq of the VCO till it picks up signal again. This produces a high noise immunity and locking stability.



Low pass filter (a, b) Passive filter (c) Active filter

Monolithic PLL IC 565

- Monolithic PLL IC available in 56x series introduced by PLL signetics and national semiconductor, as a 14 pin DIP IC.The most commonly used PLL IC is 565.
- The VCO free running frequency $f_o = \frac{1}{4R_TC_T}$; Where R_T and C_T are the external resistor and capacitor connected to pin 8 and pin 9.
- The conversion ratio of the phase detector of 565 PLL is $K_\varphi = \frac{0.7-(-0.7)}{\pi} = \frac{1.4}{\pi}$
- The value between 2KΩ to 20KΩ is recommended for R_T. The VCO free running frequency is adjusted with R_T and C_T to be at the centre of input frequency range.
- A short circuit between pin 4 and 5 connects the VCO output to phase comparator, so as to compare f_o with input signalf_s.
- A capacitor C is connected between pin 7 and pin 10 to make a LPF with internal resistance of 3.6 KΩ



Derivation of Lock –in Range

If φ radians is the phase difference between the signal and the VCO voltage,then the output voltage of the analog phase detector is given by,

$$V_e = K_\varphi \, (\varphi - \frac{\pi}{2})$$

K_φ =phase angle –to-voltage transfer coefficient of the phase detector.
The control voltage to VCO is

$$V_c = AK_\varphi \, (\varphi - \frac{\pi}{2})$$

A=voltage gain of the amplifier. This V_c shifts VCO frequency from its free running frequency f_o to a frequency f .

$$f = f_o + K_v \, v_c$$

K_v=the voltage to frequency transfer coefficient of the VCO.

When PLL is locked-in to signal frequency f_s ,then

$$f = \ f_s = f_o + K_v \, v_c$$

$$since \ V_c = \frac{f_s - f_o}{K_v} = AK_\varphi \, (\varphi - \frac{\pi}{2})$$

$$\varphi = \frac{\pi}{2} + \ (f_s - f_o)/ \, K_V \, K_\varphi \, \mathrm{A}$$

The maximum output voltage magnitude available from the phase detector occurs for φ=π and 0 radian. And

$$V_e(max) = \pm K_\varphi \pi/2$$

.The corresponding value of the maximum control voltage available to drive the VCO will be

$$V_{cmax} \ = \pm \pi/2K_\varphi A$$

.The maximum VCO frequency swing that can be obtained is given by

$$(f - f_o)_{max} \ = K_V \, v_{cmax} \ = K_V \, K_\varphi A \frac{\pi}{2}$$

Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be

$$f_s = f_o \pm (f - f_o)_{\ max}$$

$$= f_o \pm K_V \, K_\varphi A \frac{\pi}{2} = f_o \pm \Delta f_L$$

Where $2\Delta f_L$ will be the lock in frequency range and is given by'

Lock –in –range = $2\Delta f_L = K_V\, K_\varphi A\pi$

(or) $\Delta f_L = \pm K_V\, K_\varphi A(\frac{\pi}{2})$

The lock in range is symmetrically located with respect to VCO free running frequency f_o

For IC PLL 565

$$K_V = \frac{8f_o}{V}$$

Where V=+V_{cc} –(- V_{cc})

$$K_\varphi = \frac{1.4}{\pi}$$

A=1.4

Hence locked in range becomes $\Delta f_L = \pm 7.8 f_o\, /V$

The maximum output voltage magnitude available from the phase detector occurs for φ= π and 0 radian.

We know average error voltage is $(\boldsymbol{V_e})_{\boldsymbol{av}} = \boldsymbol{K_\varphi}[\boldsymbol{\varphi} - \frac{\boldsymbol{\pi}}{\boldsymbol{2}}]$

So $V_e(max) = \pm K_\varphi \pi/2$

The corresponding value of the maximum control voltage available to drive the VCO will be,

$$V_c(max) = \pm A K_\varphi \pi/2$$

The maximum VCO frequency swing that can obtained is given by

$$(f - f_o)_{max} = K_V\, v_{cmax} = K_V\, K_\varphi A \frac{\pi}{2}$$

Therefore ,the maximum range of signal frequencies over which the PLL can remain locked will be

$$f_s = f_o \pm (f - f_o)_{\,max}$$

$$= f_o \pm K_V\, K_\varphi A \frac{\pi}{2} = f_o \pm \Delta f_L$$

Derivation of capture Range

- When PLL is not initially locked to the signal ,the frequency of the VCO will be free running frequency f_o.The phase angle difference between the signal and the VCO output voltage will be

$$\varphi = (\omega_s t + \theta_s) - (\omega_o t + \theta_o) = (\omega_s - \omega_o)t + \Delta\theta \; --- (1)$$

- The phase angle difference does not remain constant but will change with time at a rate given by

$$\frac{d\varphi}{dt} = \omega_s - \omega_o$$

- The phase detector output voltage not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K_\varphi \frac{\pi}{2}$ and a fundamental frequency $(f_s - f_o) = \Delta_\mathrm{f}$.

- The low pass filter (LPF) is a simple RC network having transfer function

$$T(jf) = \frac{1}{1 + j(f/f_1)} - - - (2)$$

Where $f_1 = 1/2\pi RC$ is the 3-dB point of LPF.In the slpoe portion of LFP Where $(\frac{f}{f_1})^2 \gg 1$ then

$$T(f) = \frac{f_1}{jf} - - - (3)$$

- The fundamental frequency term supplied to the LPF by the phase detector will be the difference frequency $(f_s - f_o) = \Delta\mathrm{f}$.If $\Delta\mathrm{f} > 3f_1$, the LPF transfer function will be approximately,

$$T(\Delta f) \approx \frac{f_1}{\Delta\mathrm{f}} = \frac{f_1}{(f_s - f_o)} - - - (4)$$

- The voltage V_C to drive the VCO is

$$V_C = V_e * T(f) * A \qquad - - - (5)$$

$$(o\,r)\ V_{C(max)} = V_{e(max)} * T(f) * A$$

$$V_{C(max)} = \pm K_\varphi \frac{\pi}{2} A \frac{f_1}{\Delta\mathrm{f}} \qquad - - - (6)$$

- Then the corresponding value of the maximum VCO frequency shift is

$$(f - f_o)_{max} = K_v v_{c(max)} = \pm K_v K_\varphi (\frac{\pi}{2}) A \frac{f_1}{\Delta\mathrm{f}} - - - (7)$$

- For the acquisition of signal freq,we should put $f = f_s$ so that the max signal freq range that can be acquired by PLL is

$$(f_s - f_o)_{max} = \pm K_v K_\varphi \left(\frac{\pi}{2}\right) A \frac{f_1}{\Delta\mathrm{f}} - - - (8)$$

$$Now \quad \Delta f_c = (f_s - f_o)_{max}$$

$$So \quad (\Delta f_c)^2 = K_v K_\varphi \left(\frac{\pi}{2}\right) A f_1$$

$$Since \quad (\Delta f_L) = \pm K_v \, K_\varphi \left(\frac{\pi}{2}\right) A$$

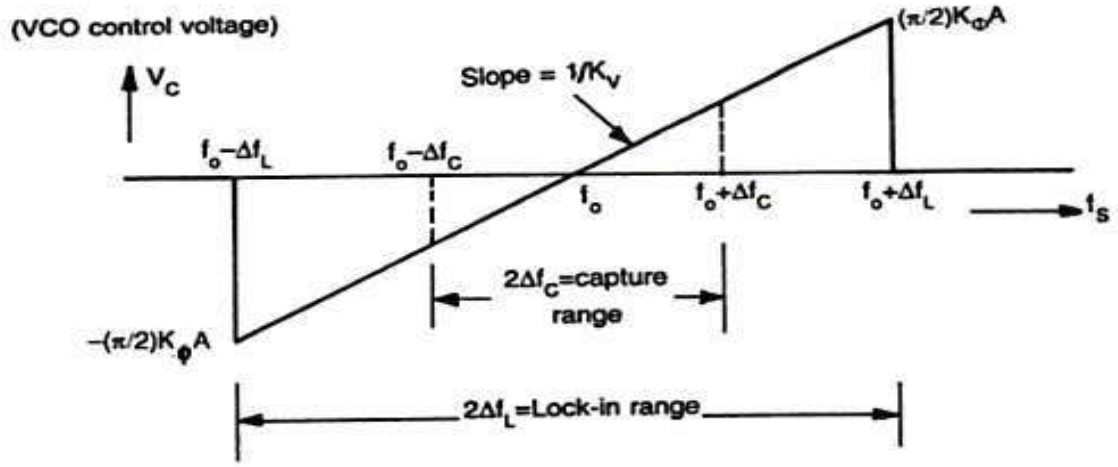
$$We\ get\ (\Delta f_c) \approx \pm\sqrt{f_1 \Delta f_L} \; - - - \; (9)$$

$$Therefore\ the\ total\ capture\ range\ is\ (2\Delta f_c) \approx 2\sqrt{f_1 \Delta f_L} \; - - - \; (10)$$

Where the lock in range = $2\Delta f_L = K_V \, K_\varphi \, A\pi$.In case of IC PLL 565 , R=3.6kΩ ,So the capture range.

$$\pm\left[\frac{\Delta f_L}{2\pi(3.6\times10^3)C}\right]^{\frac{1}{2}}$$

The capture range is symmetrically located with respect to VCO free running frequency f_o .To increase the ability of lock –in –range ,large capture range is required.



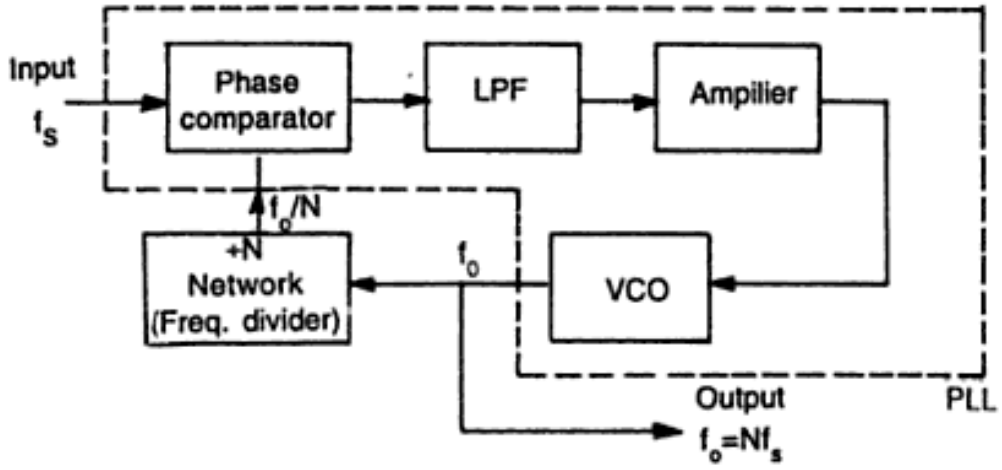
PLL lock-in range and capture range

PLL APPLICATIONS:

PLL can be used in the following applications

- Frequency multiplier/Divider
- Frequency synthesizer
- Frequency translation
- AM detector
- FM demodulator
- FSK demodulator

Frequency multiplier/Divider



Frequency multiplier using IC PLL

- A divider by N Network is inserted between the VCO output and the phase comparator input.In the locked state, the VCO output frequency f_o is N f_s

$$f_o = Nf_s$$

- The multiplication factor can be obtained by selecting a proper scaling factor N of the counter. Frequency multiplication can also be obtained by using PLL in its harmonics locking mode.

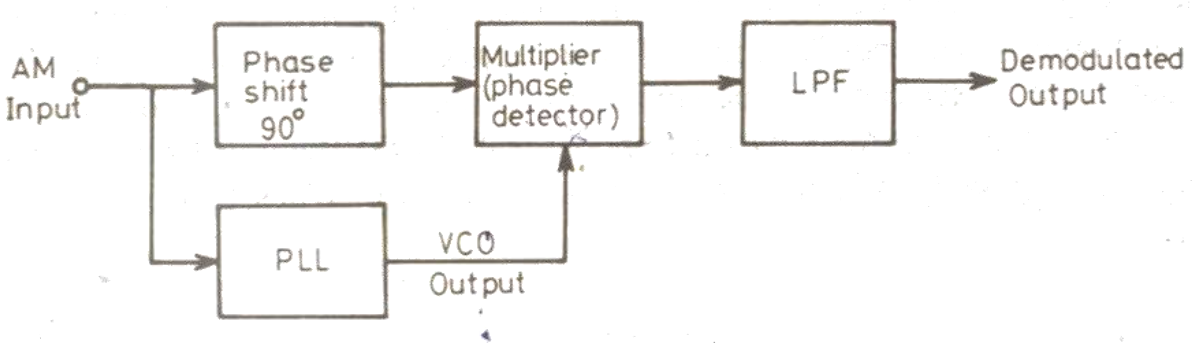
- If the input signal is rich in harmonics eg:: square wave, pulse train etc……..,then VCO can be directly locked to the n^{th} harmonic of the input signal without connecting any frequency divider in between.

- But the amplitude of the higher order harmonics becomes less effective locking may not take place for high values of n. The above circuit can also be used for frequency division

- Since the VCO output is rich in harmonics it is possible to lock the m^{th} harmonics of the VCO output with the input signal fs. The output fo of VCO is

$$f_o = \frac{f_s}{m}$$

AM Detection



- The PLL is locked to the carrier frequency of the incoming AM signal. Once locked the output frequency of VCO is same as the carrier frequency but it is in unmodulated form.

- The modulated signal with 90° phase shift and the unmodulated carrier from output of PLL are fed to the multiplier. Since VCO output is always 90° out of phase with the incoming AM signal under the locked condition, both the signals applied to the multiplier are in same phase.

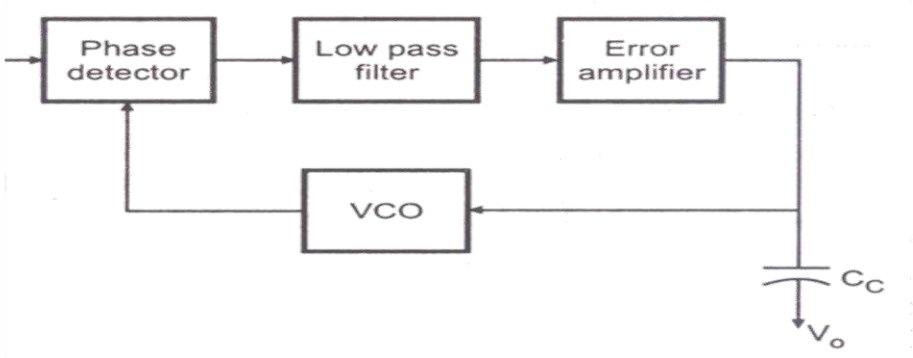
- The output of the multiplier contains both the sum and the difference signal.The low pass filter rejects high frequency components gives demodulated output.As PLL follows the input frequencies with high accuracy.

FM DEMODULATOR

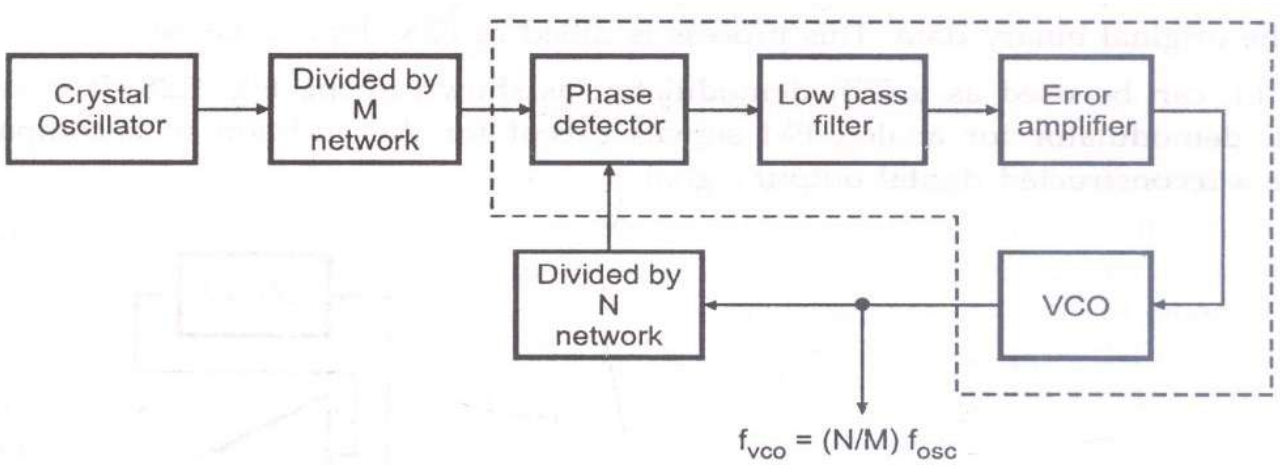
- The PLL can be used as a FM demodulator.

- When the PLL is locked in on the FM signal, the frequency of the VCO follows the instantaneous frequency of the FM signal, and the error voltage or VCO control voltage is proportional to the deviation of the input frequency from the center frequency. Therefore, AC control voltage of VCO will represent as modulating voltage.

- The modulating voltage depends on the linearity between the instantaneous frequency deviation and the control voltage of VCO.



FREQUENCY SYNTHESIZER



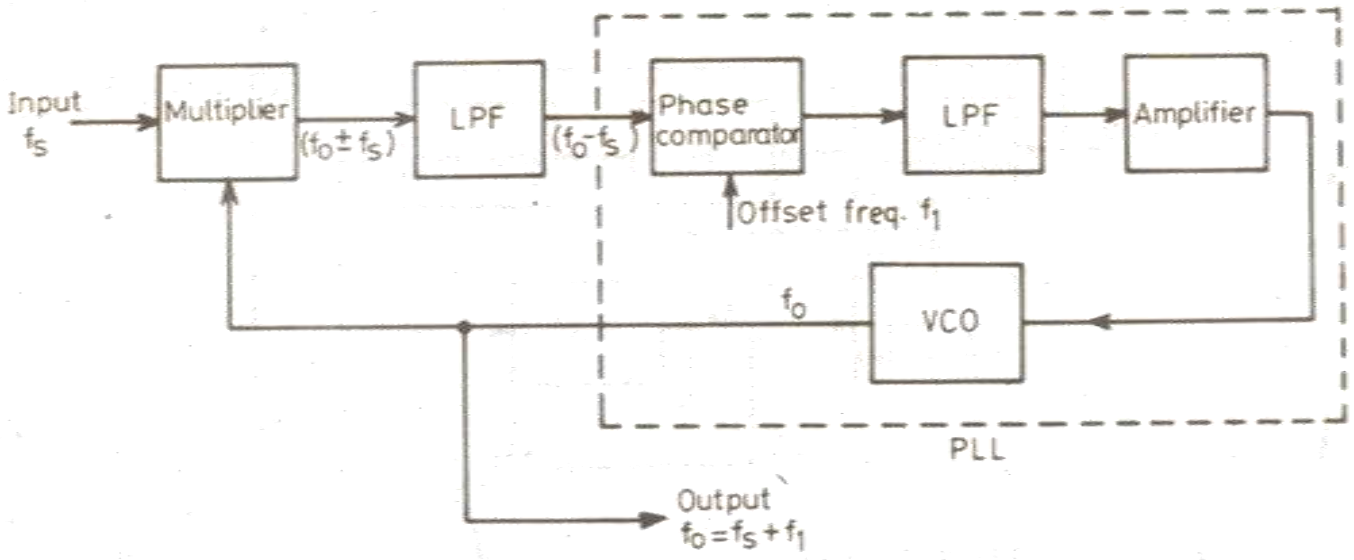
- The PLL can be used as the basis for the frequency synthesizer than can produce the precise series of frequencies that are derived from a stable crystal controlled oscillator

- The frequency of the crystal oscillator is divided by an integer factor M by divider network to produce a frequency fosc/M.

- The VCO frequency f_{VCO} is similarly divided by factor N by divider network to give frequency equal to f_{VCO}/N.

- When the PLL is locked in on the divided low oscillator frequency fosc/M=fVCO/N , so that fVCO= Nfosc/M=(N/M)fosc.By adjusting divider counts to desired values large number of frequencies can be produced.

FREQUENCY TRANSLATION



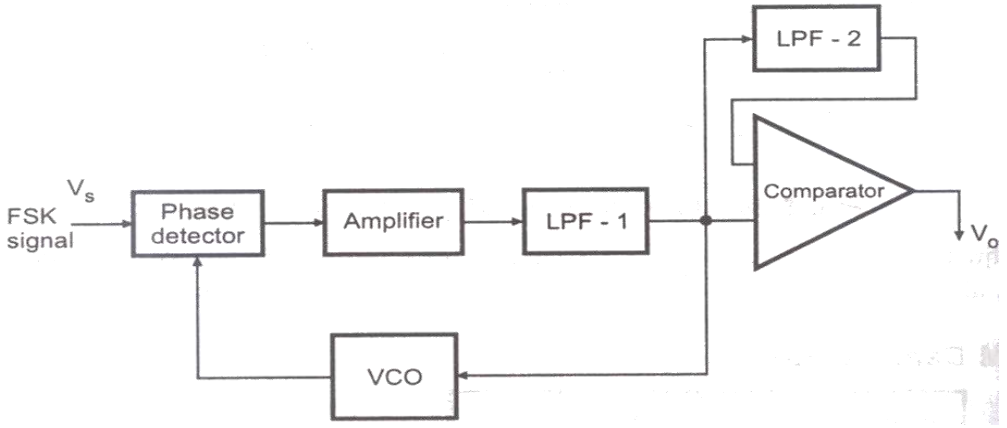
- A multiplier (or) mixer and a LPF are connected externally to the PLL.The signal fs and the output frequency f0 of the VCO applied as inputs to the mixer.The output of the mixer contains the sum and difference of fs and fo.

- The output of the LPF contains only the difference signal (fo-fs).The (fo-f1) signal is applied to the phase detector another input for phase detector is offset frequency f_1.

- In locked mode, the VCO output frequency is adjusted to make low input frequencies of phase detector equal.This gives $f_o - f_s = f_1 \quad ; f_o = f_s + f_1$

- By adjusting offset frequency f1, we can shift the frequency of the oscillator to the desired value.

FSK demodulator



- Binary data is transmitted by means of the carrier frequency. It uses two frequencies for logic 1 and logic 0 states of binary data signal.This type of data transmission is called FSK.

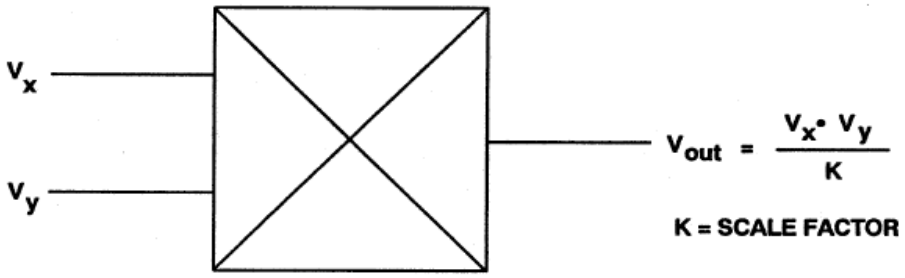
- In this data transmission, on the receiving end to carrier frequency is converted into 1 and 0 to get the original binary data. Hence one comparator is used to demodulate and produce the reconstructed output signal.

- Let us consider two frequencies one frequencyf1 and it is represented as ‘0’ and other frequency f2 is represented as ‘1’.If the PLL remain is locked into the FSK signal at both

ANALOG MULTIPLIER

- There are a number of applications of analog multiplier such as frequency doubling, frequency shifting, phase angle detection, real power computation, multiplying two signals dividing and squaring of signals.
-

Multiplier schematic symbol



- The two input symbols are v_x and v_y , the output is the product of the two inputs divided by a reference voltage v_{ref}.

$$V_0 = \frac{v_x v_y}{v_{ref}.}$$

- Normally v_{ref} is internally set to 10 Volts. So

$$V_0 = \frac{v_x v_y}{10.}$$

- As long as $v_x < v_{ref}$ and $v_y < v_{ref}$ the output of the multiplier will not saturate.If both inputs are positive, the IC is said to be one quadrant multiplier.

- A two quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative. If both inputs may be either positive or negative, the IC is called a four quadrant multiplier

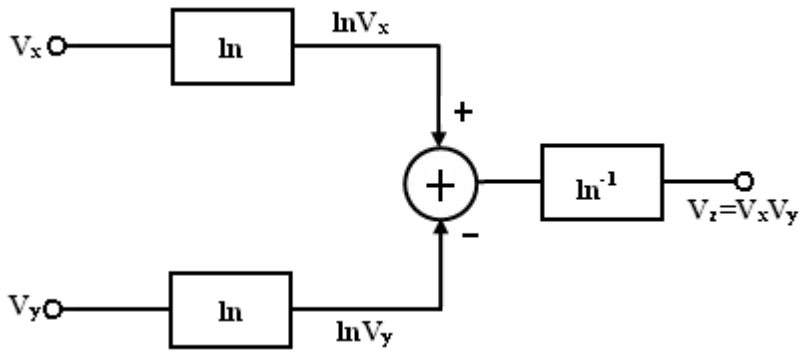
LOG ANTILOG METHOD

- A simple and common method to make a multiplier circuit is log- antilog method.

- The log- antilog method relies on the mathematical relationship that the sum of the logarithm of two numbers equals the logarithm of the product of those numbers.

$$\ln v_x + \ln v_y = \ln v_x v_y$$

Block diagram of log-antilog



- Log –amps require the input and the reference voltages to be of the same polarity.
- A technique that provides four quadrant multiplications is transconductance multiplier.

Type	Vx	Vy	Vout
Single Quadrant	Unipolar	Unipolar	Unipolar
Two Quadrant	Bipolar	Unipolar	Bipolar
Four Quadrant	Bipolar	Bipolar	Bipolar

Analog multiplier applications

Frequency Doubling:

- The multiplication of two sine waves of the same frequency, but of possibly different amplitudes and phase allows to double a frequency and to directly measure real power.
- Let $v_x = v_x \sin \omega t$
  $v_y = v_y \sin(\omega t + \theta)$ Where θ is the phase difference between the two signals.

- Appling these two signals to the inputs of a four quadrant multiplier will give an output as

$$V_0 = \frac{V_X V_Y}{V_{ref}} = \frac{v_x \sin \omega t \; v_y \sin(\omega t + \theta)}{V_{ref}} = \frac{v_x \; v_y}{V_{ref}} (\sin \omega t \sin(\omega t + \theta))$$

$$V_0 = \frac{V_X V_Y}{V_{ref}} \sin \omega t \, (\sin \omega t \cos \theta + \sin \theta \cos \omega t)$$

$$V_0 = \frac{V_X V_Y}{V_{ref}}(\sin^2 \omega t \cos\theta + \sin\theta \sin\omega t \cos\omega t)$$

We know that $\sin^2\theta = 1 - \cos^2\theta : \cos^2\theta = \frac{1+\cos 2\theta}{2}$ $\sin^2\theta = 1 - \frac{1+\cos 2\theta}{2} = \frac{1}{2} - \frac{1}{2}\cos 2\theta$

$$V_0 = \frac{V_X V_Y}{V_{ref}}(\cos\theta\left(\frac{1}{2} - \frac{1}{2}\cos 2\omega t\right) + \sin\theta \sin\omega t \cos\omega t)$$

$$\text{We know that} \quad \sin\theta\cos\theta = \frac{1}{2}\sin 2\theta$$

$$\text{Hence} \quad V_0 = \frac{V_X V_Y}{2V_{ref}}(\cos\theta - \cos\theta\cos 2\omega t + \sin\theta \sin 2\omega t)$$

$$V_0 = \frac{V_X V_Y}{2V_{ref}}\cos\theta + \frac{V_X V_Y}{2V_{ref}}(\sin\theta \sin 2\omega t - \cos\theta \cos 2\omega t)$$

The first term is a DC and is set by the magnitude of the signals and their phase difference. The second term varies with time, but at twice the frequency of the inputs (ωt).Multiplier IC can be used for squaring a signal.

Divider:

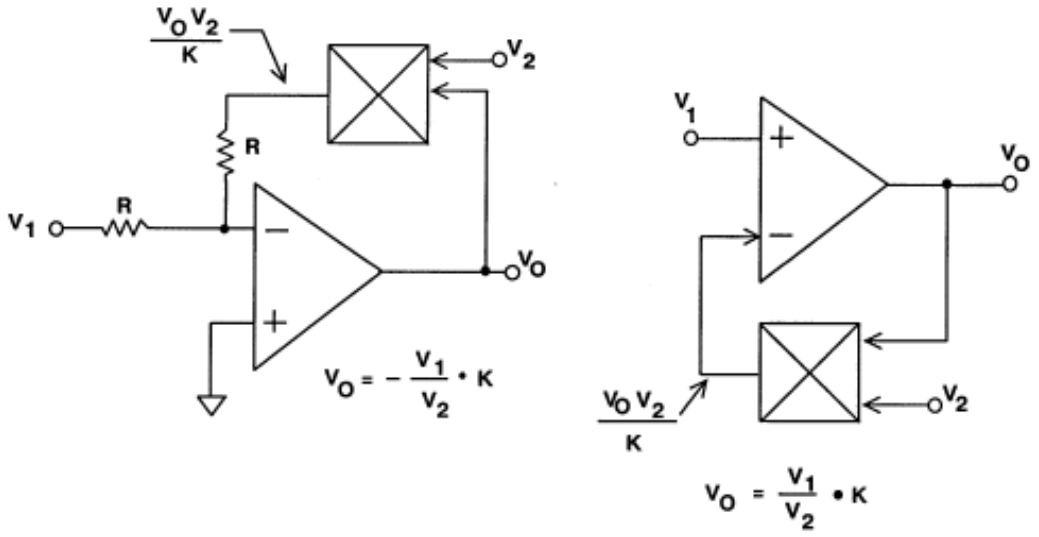
- Division, the complement of multiplication, can be accomplished by placing the multiplier circuit element in the op-amp's feedback loop. The output voltage from the divider with input signals v_z and v_x as dividend and divisor respectively.

$$V_0 = -V_{ref}\frac{V_z}{V_x}$$

- The op-amp's inverting terminal is at virtual ground. so,

$$I_z = I_A$$

$$I_z = \frac{V_z}{R}$$



The output voltage V_A of the multiplier is determined by the multiplication of V_x and V_y

$$V_A = \frac{V_x V_y}{V_{ref}} = \frac{V_x V_o}{V_{ref}}$$

$$\text{Again} \quad V_A = -I_A R$$

$$\text{So} \quad I_A = -\frac{V_A}{R} = -\frac{V_x V_o}{V_{ref}\, R}$$

$$I_Z = -\frac{V_x V_o}{V_{ref}\, R}$$

$$V_z = I_Z R = -\frac{V_x V_o}{V_{ref}}$$

$$V_o = -V_{ref}\, \frac{v_z}{v_x}$$

Division by zero is prohibited. Divider circuit can be used to take the square root of a signal.

Basic one quadrant Variable Transconductance Multiplier (VTM)

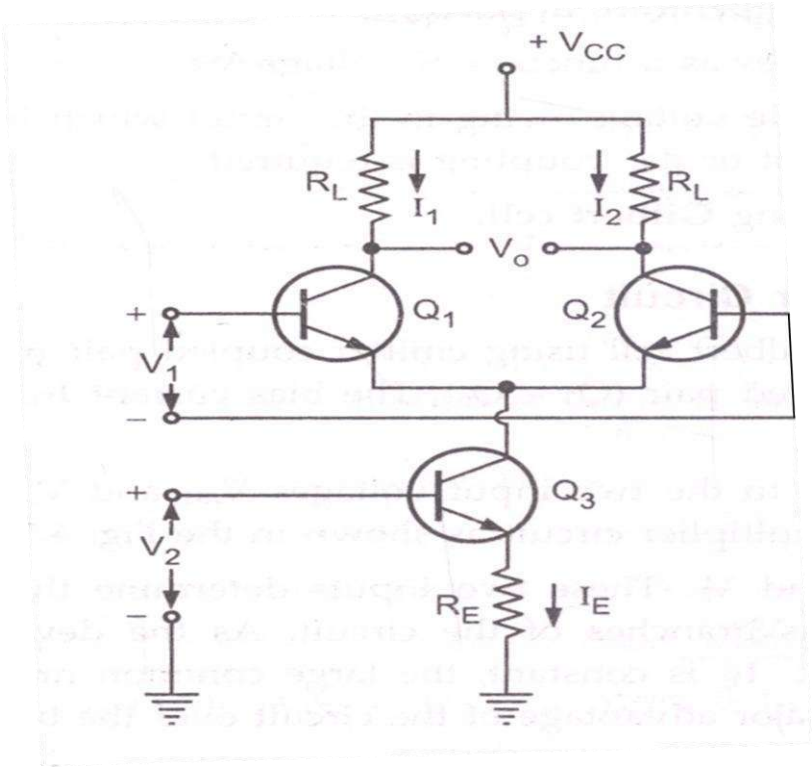
- The symmetrical differential amplifier is the main part of the variable transconductance technique. It uses the principle of the dependence of the transistor transconductance on the emitter current bias.

- Differential amplifier is formed by transistor Q_1 and Q_2 .For very small values of differential input voltage $\boldsymbol{V_1}$,the output voltage V_o is,

$$V_0 = g_m R_L V_1$$

Where $g_m = I_E / V_T$ is the transconductance of the stage.

- The transconductance $\boldsymbol{g_m}$ dependence on emitter current I_E.Which in turn can be controlled by applying second voltage $\boldsymbol{V_2}$ **to the transistor**$\boldsymbol{Q_3}$**.**



Thus, if $R_E I_{EE} >> V_{BE}$, the bias voltage V2 is related to I_{EE} by the relation $V2 = I_E R_E$. Then, the overall voltage transfer expression is given

$$V_o = \frac{I_E}{V_T} R_L V_1 = \frac{V_2}{R_E V_T} R_L V_1$$

$$V_o = (\frac{R_L}{R_E V_T})V_1 V_2$$

$$V_o = KV_1 V_2$$

Thus the output is proportional to the product of the two inputs.

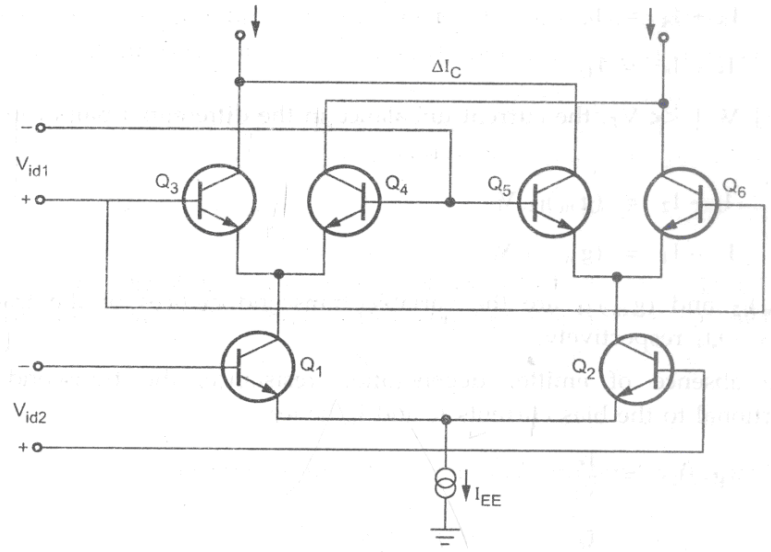
The Limitation of the emitter coupled pair are,

1. The scale factor K is temperature dependent.
2. The total current I_E varies as a function of voltage V_2
3. The large common mode voltage swing in the circuit which is highly objectionable, if a single ended output or d.c coupling is required.

Basic Gilbert Cell

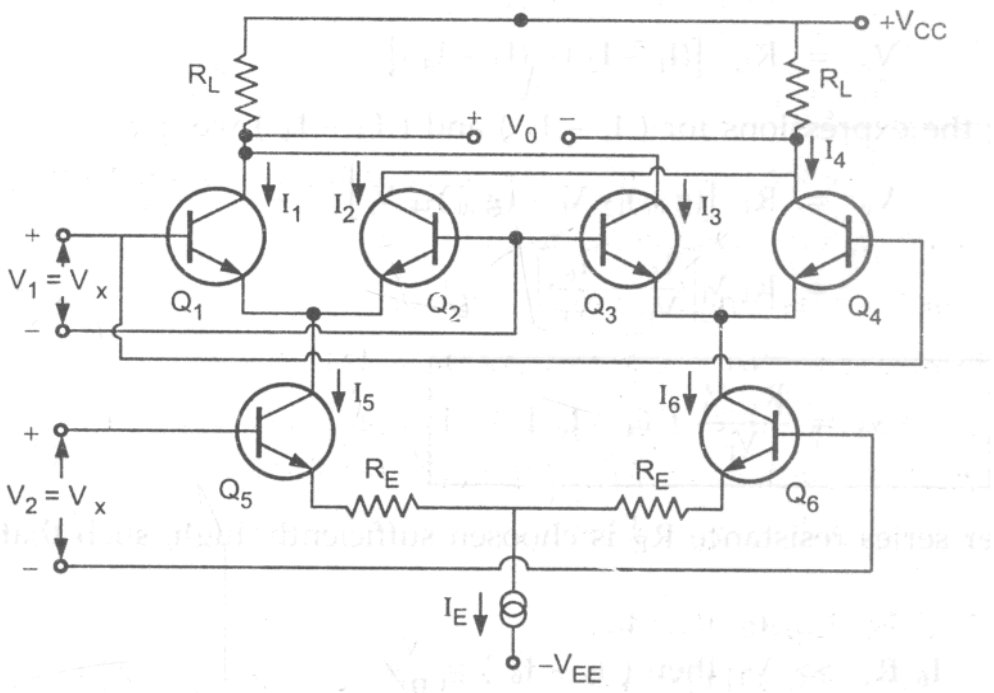
- In Gilbert cell using emitter coupled pair $(Q_1 - Q_2)$ in series with a cross-coupled, emitter coupled pair $(Q_3 - Q_6)$.The bias current I_E is emitter bias current for Q_1 and Q_2.

- The current ΔI_c is related to the input voltages V_{id1} and V_{id2}



- The two inputs are V_1 and V_2.These two inputs determine the division of the total current I_E among the various branches of the circuit.

- As the devices are symmetrically cross –coupled and the current I_E is constant, the large common mode shift at the output gets eliminated. This is the major advantage of the circuit over the basic multiplier circuit.



While analyzing this circuit, assume

i) All the transistors are well matched.

ii) The h_{fe} for the transistors is very high, $h_{fe} \gg 1$

Hence the various current relations is

$$I_1 + I_2 = I_5$$

$$I_3 + I_4 = I_6$$

$$I_5 + I_6 = I_E$$

Assuming $|V_1| \ll V_T$, the current unbalance in the differential pairs can be expressed as,

$$I_1 - I_2 = (g_m)_{12}\, V_1$$

$$I_3 - I_4 = (g_m)_{34}\, V_1$$

Where $(g_m)_{12}$ and $(g_m)_{34}$ are the variable transconductance of the transistor pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ res. Under the absence of emitter degeneration resistance, the transconductance are directly proportional to the bias current $I_5 and\ I_6\ hence$

$$(g_m)_{12} = \frac{I_5}{V_T}$$

$$(g_m)_{34} = \frac{I_6}{V_T}$$

The total differential output voltage V_0 is given by,

$$V_0 = R_L[(I_1 - I_2) - (I_3 - I_4)]$$

Substituting the expressions for$(I_1 - I_2)$ and $(I_3 - I_4)$ we get ,

$$V_0 = R_L[(g_m)_{12} V_1 - (g_m)_{34} V_1]$$

$$V_0 = R_L V_1 \left[\frac{I_5}{V_T} - \frac{I_6}{V_T}\right]$$

$$V_0 = \frac{R_L V_1}{V_T}[I_5 - I_6]$$

If the emitter series resistance R_E is chosen sufficiently high, such that $I_5\ R_E \gg V_T$ and $I_6 R_E \gg V_T$ then $(I_5 - I_6) = \frac{V_2}{R_E}$

$$V_0 = \frac{R_L V_1 V_2}{R_E V_T}$$

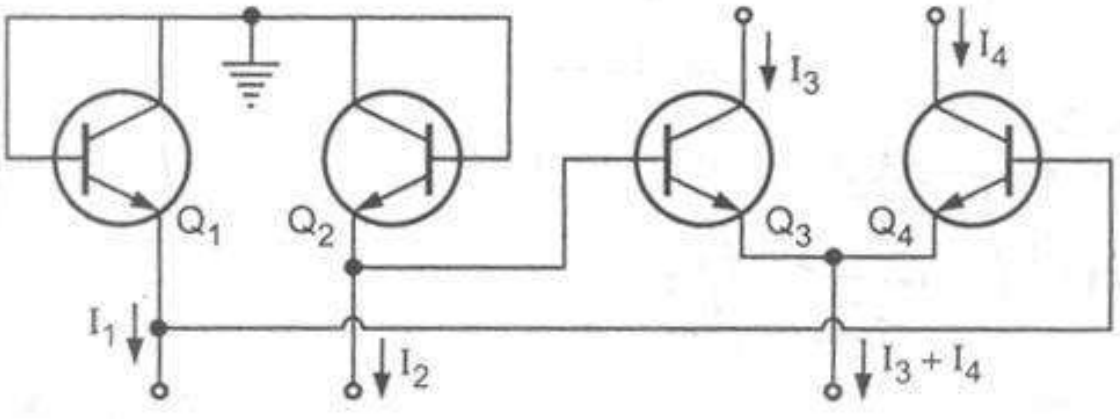
$$V_0 = K V_1 V_2$$

Thus the output is proportional to the product of the input voltages.

Four Quadrant Variable Transconductance Multiplier Circuit:

Linearized Transconductance Multiplier:

This circuit consists of a differential pair of transistors $(Q_3 - Q_4)$ to provide a variable transconductance and the transistors $(Q_1 - Q_2)$ used as diode with base-collector shorted.



Applying KVL to the pair $(Q_1 - Q_2)$ and $(Q_3 - Q_4)$

$$V_{BE_1} + V_{BE_4} = V_{BE_2} + V_{BE_3}$$

$$i.e.\ \ V_{BE_3} - V_{BE_4} = V_{BE_1} - V_{BE_2} - - - (1)$$

For the two matched transistors, the change in V_{BE} is proportional to the log ratio of their currents.
Hence, $\Delta\, V_{BE} \propto \ln\left(\frac{I_1}{I_2}\right)\ for\ matched\ (Q_1 - Q_2)$.

Applying to equation (1),

$$\ln\left(\frac{I_3}{I_4}\right) = \ln\left(\frac{I_1}{I_2}\right)$$

$$So\ \ \left(\frac{I_3}{I_4}\right) = \left(\frac{I_1}{I_2}\right)$$

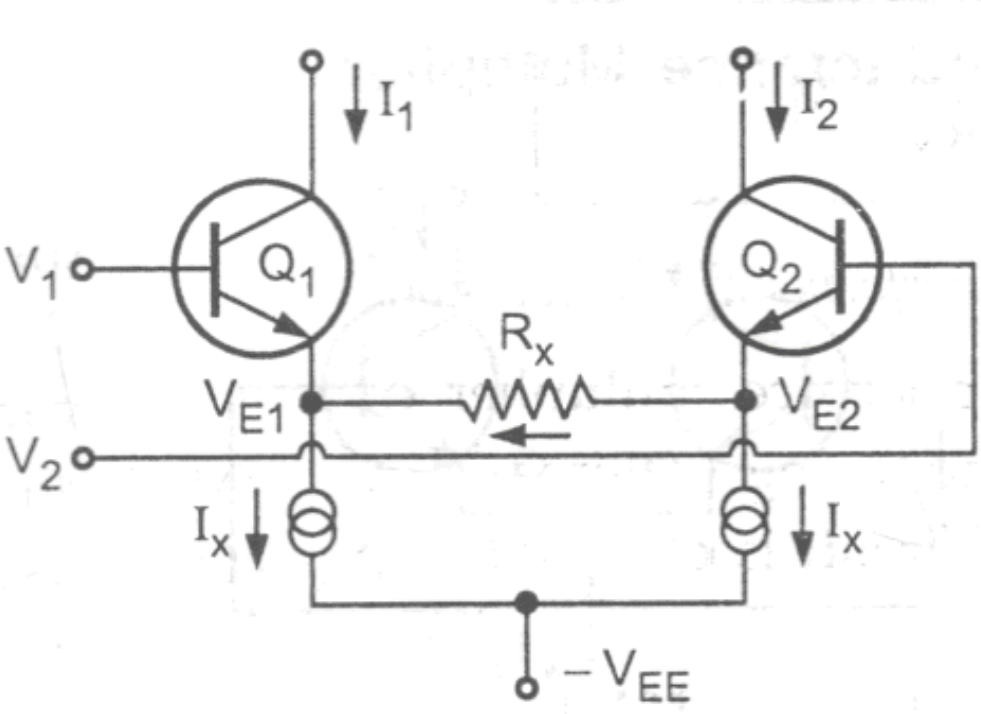
Mathematically it can be written as,

$$\frac{I_3 - I_4}{I_3 + I_4} = \frac{I_1 - I_2}{I_1 + I_2}$$

Thus current multiplies the differential current $(I_1 - I_2)$ by total emitter current $(I_3 + I_4)$.

Differential V – I Converter

To convert input voltages to get differential current V – I Converter circuit is used. Ignoring the two base currents and applying KCL we get,



$$I_1 = I_x + I_{RX} - - - (1)$$

$$I_2 = I_x - I_{RX} - - - (2)$$

$$I_1 - I_2 = 2I_{RX} - - - (3)$$

Let V_{E1} and V_{E2} be the emitter voltages of the transistors Q_1 and Q_2.

$$I_{RX} = \frac{V_{E1} - V_{E2}}{R_x} - - - (4)$$

Substituting (4) in (3)

$$I_1 - I_2 = \frac{2(V_{E1} - V_{E2})}{R_x}$$

By applying KVL we can write

$$V_{E1} = V_1 - V_{BE1}$$

$$V_{E2} = V_2 - V_{BE2}$$

$$V_{E1} - V_{E2} = (V_1 - V_2) - (V_{BE1} - V_{BE2})$$

Substituting in the equation

$$I_1 - I_2 = \frac{2(V_{E1} - V_{E2})}{R_x}$$

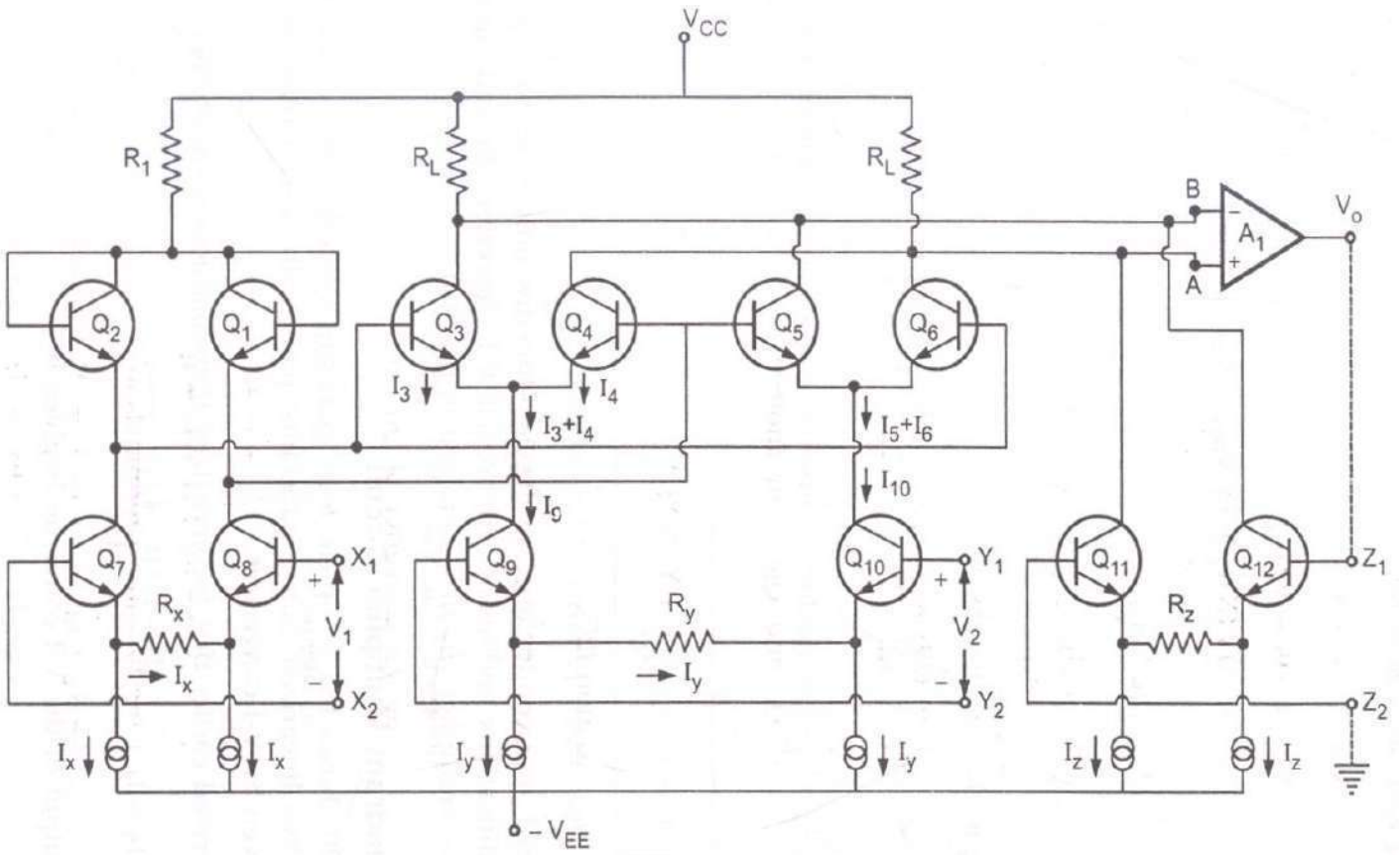
$$I_1 - I_2 = \frac{2}{R_x}(V_1 - V_2) - \frac{2V_T}{R_x} \ln\left(\frac{I_1}{I_2}\right)$$

The term $\frac{2V_T}{R_x} \ln\left(\frac{I_1}{I_2}\right)$ is negligibly small in well designed multiplier and can be neglected.

$$I_1 - I_2 = \frac{2}{R_x}(V_1 - V_2)$$

Thus circuit performs V-I conversion.

Circuit Diagram



The four quadrant multiplier uses two linearized transconductance pairs with bases driven in antiphase.The emitters are driven by V-I converters

$$I_3 - I_4 = \frac{I_1 - I_2}{I_1 + I_2}\,(I_3 + I_4) - - - (1)$$

$$I_1 - I_2 = 2(\frac{X_1 - X_{\mathrm{E}}}{\mathrm{R_x}}) - - - (2)$$

Sub(2) in (1)

$$I_3 - I_4 = \frac{X_1 - X_2}{\mathrm{R_x}(I_1 + I_{2)}}\,(I_3 + I_4) - - - (3)$$

WKT

$I_1+I_2=2I_x$

From fig $I_3+I_4=I_9$

Substituting above equation in (3)

$$I_3 - I_4 = I_9 \frac{X_1 - X_2}{I_X \mathrm{R_x}} \quad ---(4)$$

Similarly

$$I_6 - I_5 = I_{10} \frac{X_1 - X_2}{I_X \mathrm{R_x}} \quad ---(5)$$

Subtracting (4) from (5)

$$(I_4 + I_6) - (I_3 + I_5) = \frac{X_1 - X_2}{I_X \mathrm{R_x}} (I_{10} - I_9) \quad ---(6)$$

From (2)

$$I_{10} - I_9 = 2(\frac{Y_1 - Y_2}{\mathrm{R_Y}})$$

Substituting this in (6)

$$(I_4 + I_6) - (I_3 + I_5) = 2\frac{(X_1 - X_2)(Y_1 - Y_2)}{I_X \mathrm{R_x} \mathrm{R_Y}} \quad ---(6)$$

Also

$$I_{12} - I_{11} = 2\left(\frac{Z_1 - Z_2}{\mathrm{R_Z}}\right) \quad -----(7)$$

$$2\left(\frac{Z_1 - Z_2}{\mathrm{R_Z}}\right) = 2\frac{(X_1 - X_2)(Y_1 - Y_2)}{I_X \mathrm{R_x} \mathrm{R_Y}}$$

$$Z_1\text{-}Z_2 = K(X_1\text{-}X_2)(Y_1\text{-}Y_2)$$

Where $K=R_z/I_xR_xR_y$

Generally K is selected as 1/10

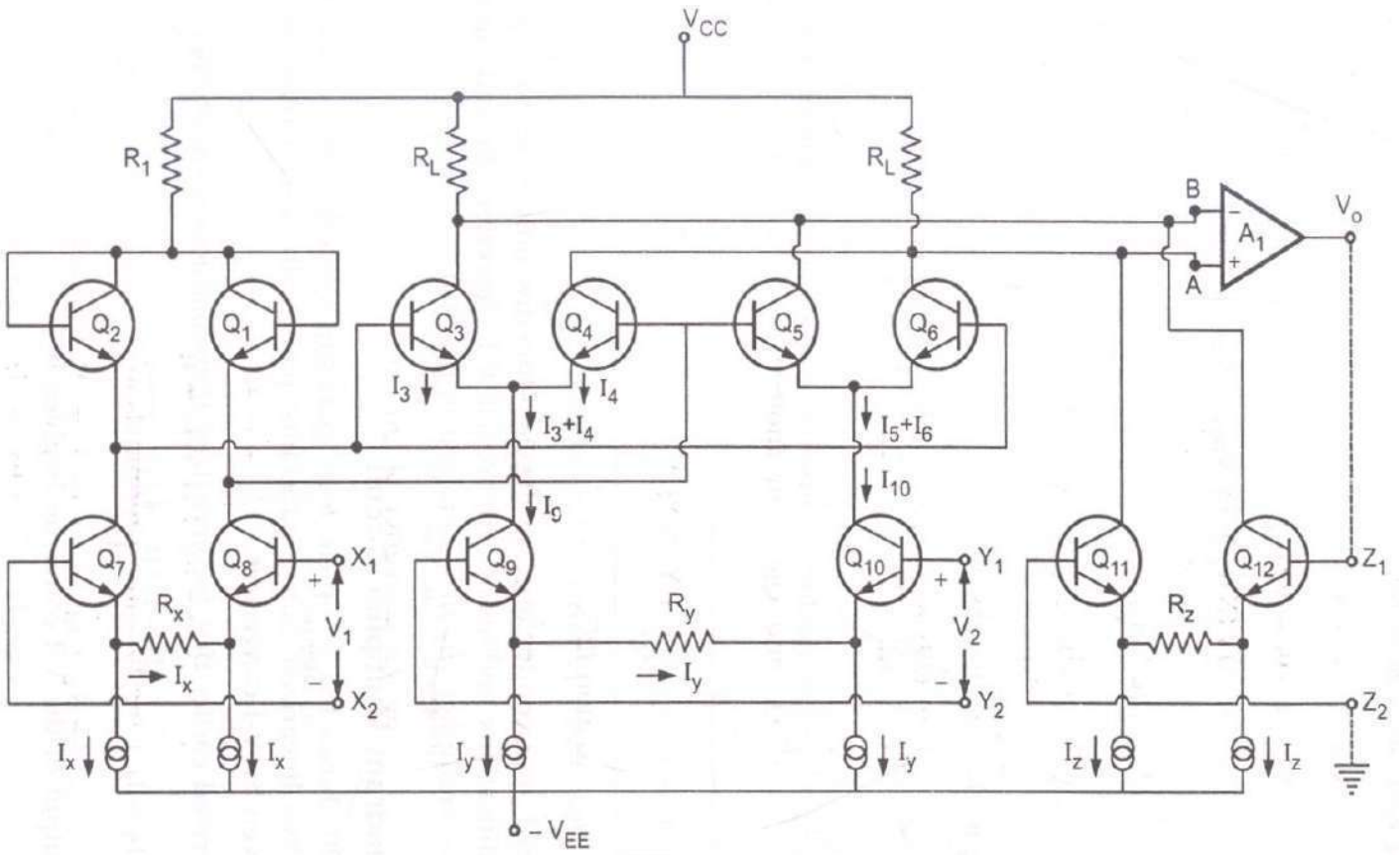
Let $V_1=X_1\text{-}X_2$

$V_2=Y_1\text{-}Y_2$

$V_0=Z_1\text{-}Z_2$

Therefore $V_0=KV_1V_2$

Circuit Diagram



The four quadrant multiplier uses two linearized transconductance pairs with bases driven in antiphase.The emitters are driven by V-I converters

$$I_3 - I_4 = \frac{I_1 - I_2}{I_1 + I_2}\,(I_3 + I_4) - - - (1)$$

$$I_1 - I_2 = 2(\frac{X_1 - X_{\mathrm{E}}}{\mathrm{R_x}}) - - - (2)$$

Sub(2) in (1)

$$I_3 - I_4 = \frac{X_1 - X_2}{\mathrm{R_x}(I_1 + I_{2)}}\,(I_3 + I_4) - - - (3)$$

WKT

$I_1+I_2=2I_x$

From fig $I_3+I_4=I_9$

Substituting above equation in (3)

UNIT - IV

ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS

Analog and Digital Data Conversions, D/A converter – specifications - weighted resistor type, R-2R Ladder type, Voltage Mode and Current-Mode $R-2R$ Ladder types - switches for D/A converters, high speed sample-and-hold circuits, A/D Converters – specifications - Flash type - Successive Approximation type - Single Slope type - Dual Slope type - A/D Converter using Voltage-to-Time Conversion - Over-sampling A/D Converters

INTRODUCTION

- Most of the information carrying signals such as voltage, current, temperature, pressure and time are available in the analog form. For processing, transmission and storage purposes it is often convenient to express these variable in digital form. Digital form data provides better accuracy and reduces noise.

- The circuit that performs the analog to digital conversion is called as analog to digital converter.

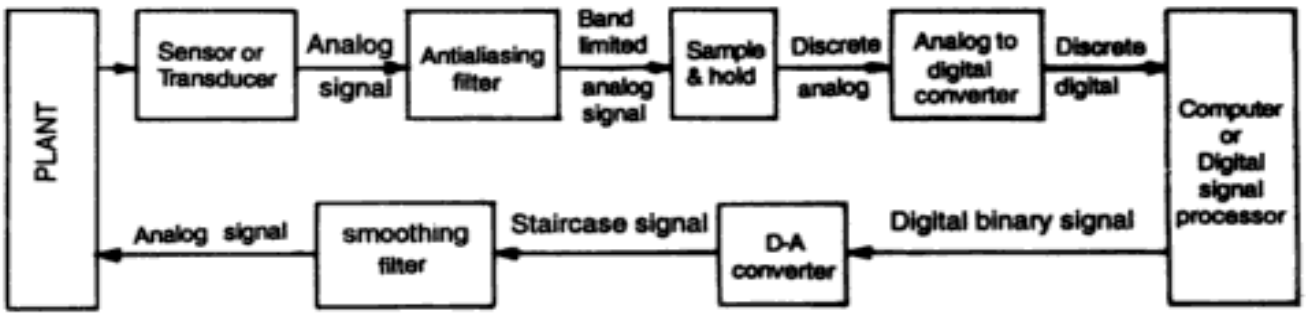
- A digital to analog converter is used when a binary output from a digital system to be converted to some equivalent analog voltage and current. The operation of any digital communication system is based upon analog to digital and digital to analog conversion.

- The analog signal obtained from the transducer is band limited by antialising filter.

- The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal. The sampled signal is held constant while conversion is taking place in A/D converter. The ADC output is a sequence in binary digits.

- The micro computer or digital signal processor performs the numerical calculations of the desired control algorithm. The D/A converter is used to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The DAC is usually operated at the same frequency as the ADC.

- The discrete signal is passed through a smoothing filter to reduce the effect of quantization noise. Both ADC and DAC are also known as data converters and are available in IC form.



DAC SPECIFICATION

The various important specifications of DAC are

- Resolution
- Accuracy
- Monotonicity
- Conversion time
- Setting time
- Stability

Resolution

It is the smallest change that can be detected in the analog output by a single bit change in the digital input.

For example;

An 8-bit D/A converter has 2^8-1=255 equal intervals, hence the smallest change in output voltage is (1/255) of the full scale output range.

$$\text{Resolution} = \frac{V_{fs}}{2^n - 1} = 1\text{LSB increment}$$

$$V_{fs} = \text{full scale voltage}$$

Accuracy

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative accuracy is the maximum deviation after gain and offset errors have been removed. It is expressed in percentage.

The accuracy of DAC should be ½ of its LSB.

$$\text{Accuracy} = \frac{V_{fs}}{(2^n - 1)^2}$$

Monotonicity

A monotonic DAC is the one whose analog output increases for an increase in digital input.

A converter is said to have good monotonicity if it does not miss any step backward when stepped through its entire range by a counter.

If a DAC has to be monotonic, the error should be less than $\pm$ (1/2) LSB at each output level.

Settling Time

Settling time is the time taken for the output to settle within a specified band $\pm$ (1/2) LSB of its final value following a code change at the input. It depends upon the switching time of the logic circuitry due to internal parasitic capacitance and inductances.

Settling time ranges from 100ns to 10μs depending on word length and type of circuit used.

Conversion time:

It is defined as the total time required to convert an analog signal in to its digital output .It depends on the conversion technique used and the propagation delay of the circuit component.

Stability

The performance of converter changes with temperature, age and power supply variations so all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

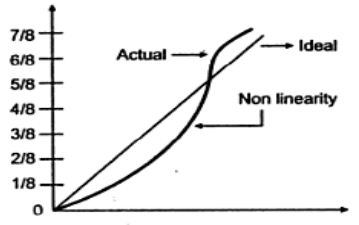
SOURCES OF ERRORS IN DAC

There are mainly three errors in DAC

Linearity
Offset
Gain error

Linearity Error:

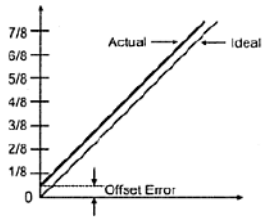
The error is defined as the amount by which the actual output differs from the ideal straight line output. Linearity error is mainly due to the errors in the current source resistor values.



Linearity error in transfer characteristics of DAC

Offset Error:

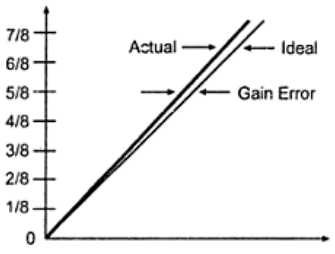
The offset error is defined as the non-zero level of the output voltage when all inputs are zero. It is due to the presence of offset voltage in op-amp and leakage currents in the current switches.



Offset error in transfer characteristics of DAC

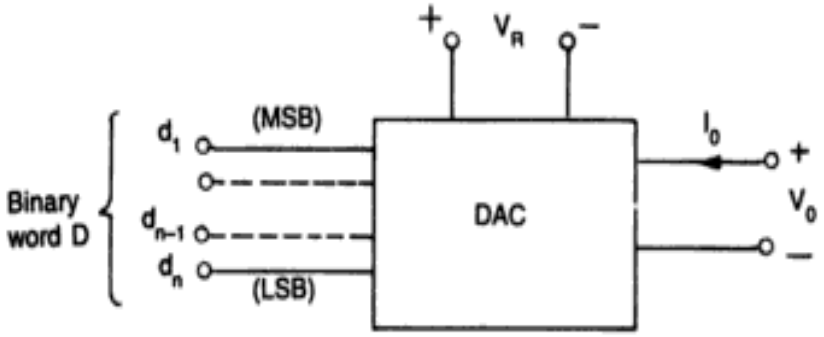
Gain Error:

The gain error is defined as the difference b/w the calculated gain of the current to voltage converter and the actual gain achieved. It is due to the errors in the feedback resistor on the current to voltage converted op-amp.



Gain error in transfer characteristics of DAC

BASIC DAC TECHNIQUES



- The input is an n-bit binary word 'D' and is combined with a reference voltage V_R to give an analog output signal. The output of a DAC can be either a voltage or current.

- For voltage output DAC,the D/A converter is mathematically described as

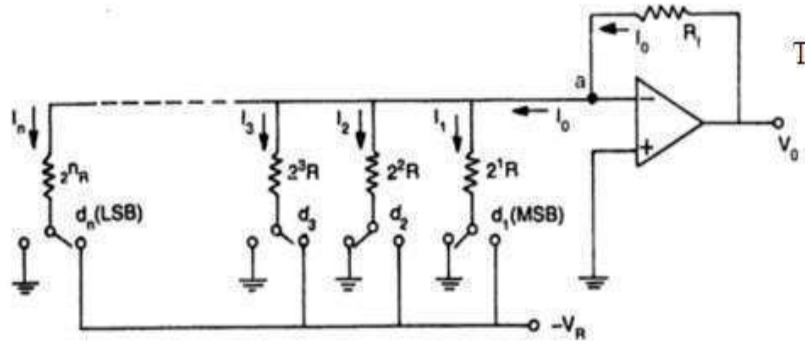
$$V_o = KV_{FS}[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} \dots\dots + d_n 2^{-n}] - - - -(1)$$

V_o = output voltage
V_{FS} = full scale output voltage
K= scaling factor [adjusted to unity]
$d_1, d_2, d_3, \dots\dots d_n$ = n-bit binary fractional word with the decimal point located at the left.
d_1 = MSB with a weight of $V_{FS}/2$
d_2 = LSB with a weight of $V_{FS}/2^n$

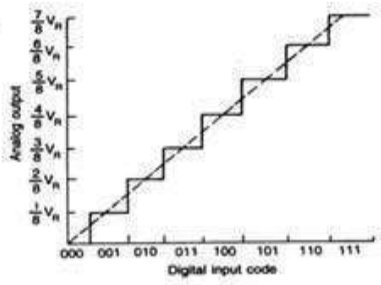
DIGITAL TO ANALOG CONVERTER TYPES

- Weighted resistor
- R-2R ladder
- Inverter R-2R ladder

WEIGHTED RESISTOR DAC



Transfer Characteristics of a 3-bit DAC



Weighted DAC consist of

- ❖ Summing amplifier
- ❖ Binary weighted resistor
- ❖ n-electronic switches

- ➢ The n-electronic switches $d_1, d_2, d_3, \ldots \ldots d_n$ controlled by binary input word. These switches are single pole double through switch.

- ➢ If the binary input to a particular switch is 1, it connects the resistor to the reference voltage ($-V_R$).

- ➢ If the input bit is 0, the switch connects the resistor to the ground. The output current I_o for an ideal op-amp is given by

$$I_o = I_1 + I_2 + I_3 \ldots . I_n$$

$$\frac{V_o}{R_f} = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \frac{V_R}{2^3 R} d_3 + \cdots \frac{V_R}{2^n R} d_n$$

$$\frac{V_o}{R_f} = \frac{V_R}{R} [2^{-1} d_1 + 2^{-2} d_2 + \cdots 2^{-n} d_n]$$

$$V_o = V_R \frac{R_f}{R} [2^{-1} d_1 + 2^{-2} d_2 + \cdots 2^{-n} d_n] - - - -(2)$$

Comparing (1) and (2)

$$V_{FS} = V_R$$

$$K = \frac{R_f}{R} \quad If\ R_f = R; K = 1$$

The reference voltage is negative, so analog output voltage is positive.

MERITS:

1. For weighted resistor DAC, the op-amp is connected in inverting mode, it can be connected in non-inverting mode.
2. The op-amp is simply working as a current to voltage converter.
3. The polarity of the ref voltage is chosen in accordance with the type of the switch used.

The accuracy &stability of a DAC depends upon the accuracy of the resistor& the tracking of each other with temperature.

DEMERITS:

Wide range of resistor values are required for 8-bit DAC ,the resistors required are $2R, 2^2R..2^8R$ Therefore ,the largest resistor is 128 times the smallest one.

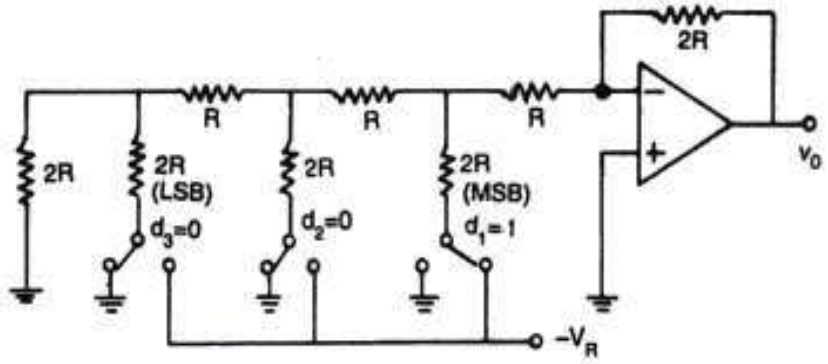
For better resolution, the input binary word length has to be increased. Thus as the number of bit increases, the range of resistance value increases.

- The fabrication of large resistance in IC is not practical.
- The voltage drops across a large resistor due to the bias current affect the accuracy.
- For smaller value of resistor loading effect may occur.

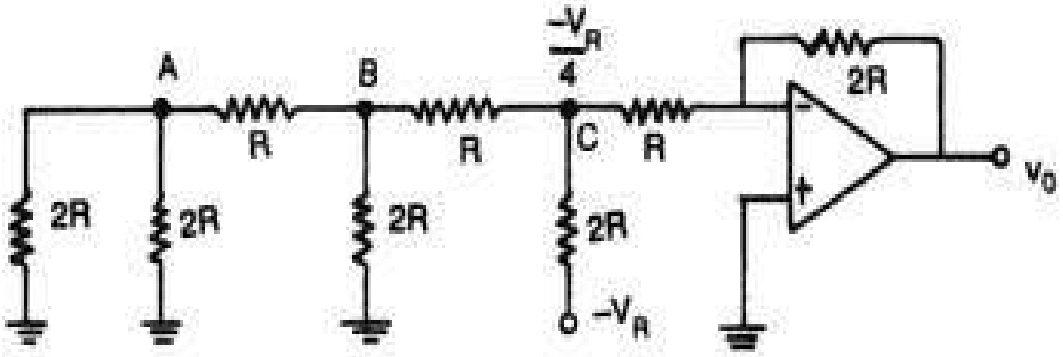
R-2R LADDER TYPE
(Or)
VOLTAGE MODE R-2R LADDER D/A CONVERTER

- Wide range of resistor are required is binary weighted resistor type DAC.This can be avoided by using R-2R ladder type DAC where only two values of resistors are required.
- The value of ranges from 2.5kΩ to 10kΩ.

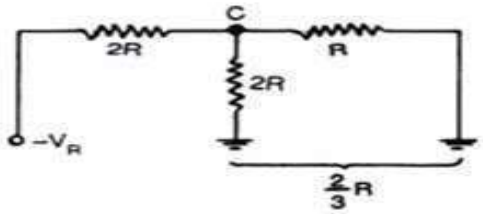
Consider a 3-bit DAC with the switch position d_1, d_2, d_3 corresponds to the binary word 100.



Equivalent circuit of R-2R ladder is,



At node C



$$V_c = \frac{\frac{2}{3}R}{\frac{2}{3}R + 2R} * -V_R$$

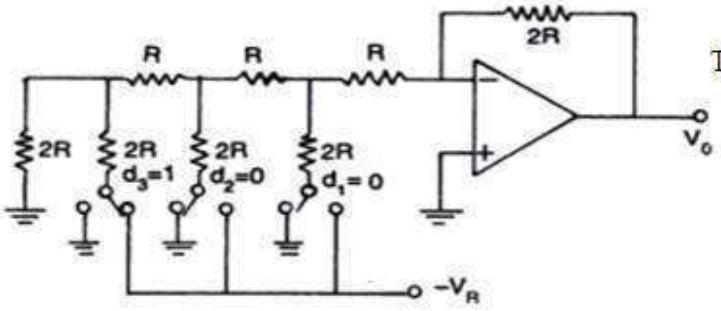
$$V_c = -\frac{V_R}{4}$$

$$By\ inverting\ mode \quad V_o = -\frac{R_f}{R_i} V_i$$

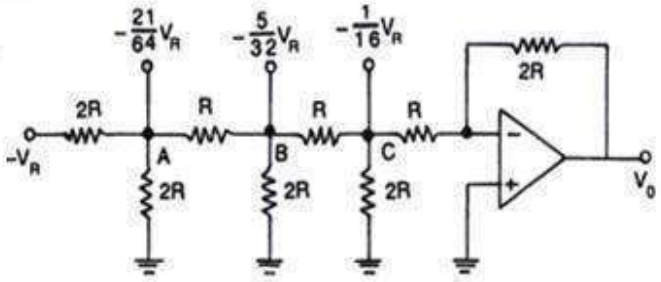
$$V_o = -\frac{2R}{R} * -\frac{V_R}{4}$$

$$V_o = \frac{V_R}{2}$$

The switch position corresponding to the binary word 001in 3-bit DAC is shown below.

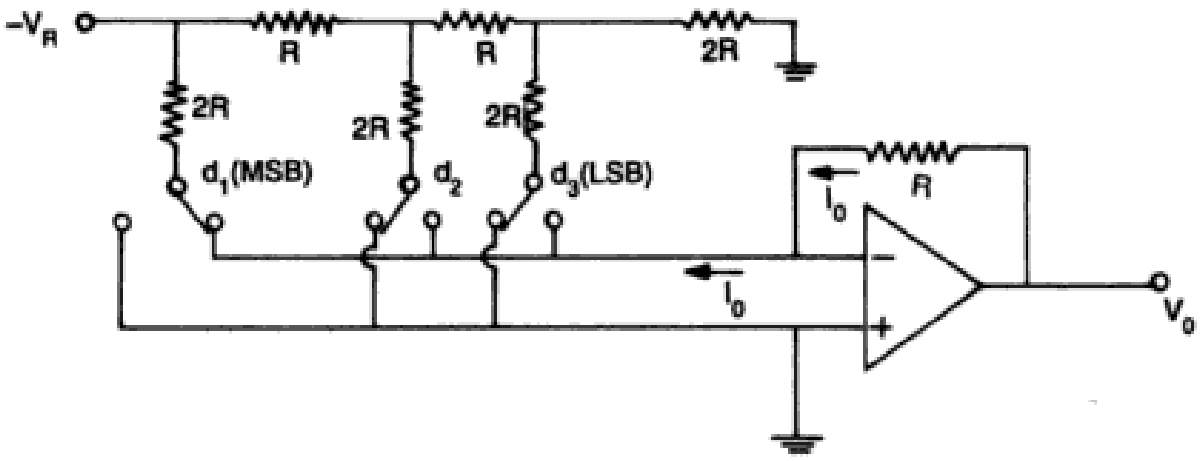


The circuit can be simplified to the equivalent form as.

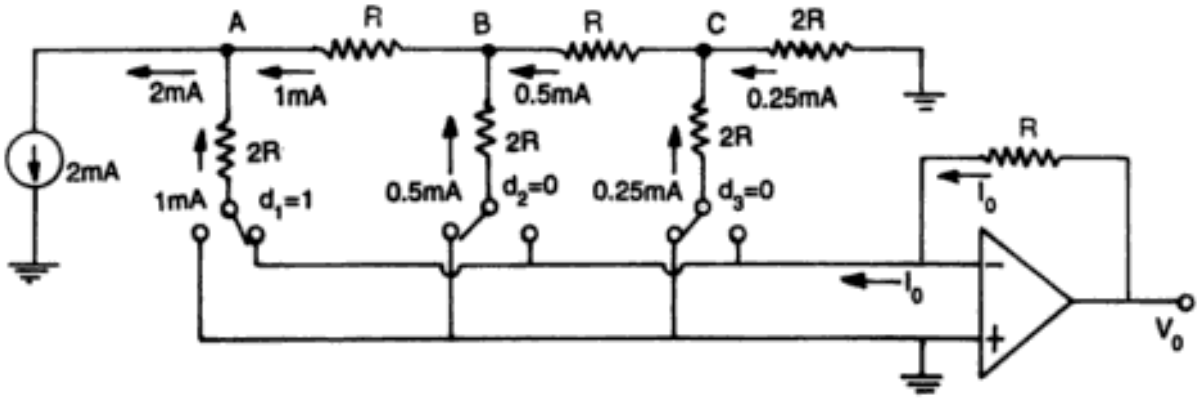


INVERTED R-2R LADDER
(Or)
CURRENT MODE R-2R LADDER D/A CONVERTER.

- In weighted resistor type DAC and R-2R ladder type DAC, current flowing on the resistors changes as the input data changes.More power dissipation causes heating, creates non linearly in DAC.



- In 3-bit inverted R-2R ladder type DAC the position of MSB and LSB is interchanged.Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground.



- Since both the terminals of switches are at ground potential, current flowing in the resistance is constant and independent of switch position ie; independent of input binary word.
  - When switch d_i is at logical '0' the current through 2R resistor flows to the ground.
  - When switch d_i is at logical '1' the current through 2R sinks to the virtual ground.

- The circuit has the important property that the current divides equally at each of the nodes. This is because the equivalent resistant to the right or the left of any node is exactly 2R.

ADVANTAGES:

1. Easier to build accurately as only two precision metal filling resistors are required.
2. We can add more sections of same R-2R values.
3. Ladder node voltages remains constant, the stray capacitance are not able to produce slowly down effects on the performance of circuit.
4. The circuit works on the principle of summing currents and also said to operate in current mode.

SAMPLE AND HOLD CIRCUITS

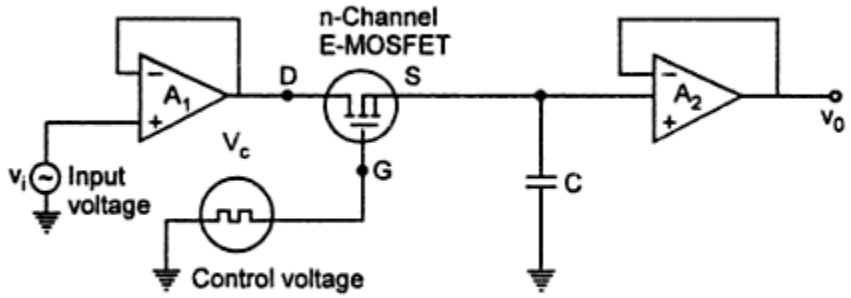
- A sample and hold circuit samples an input signals and holds ON to its last sampled value until the input is sampled again. This type of circuit is very useful in digital interfacing and analog to digital and pulse code modulation systems.

- In the sample and hold circuit, the n-channel E-MOSFET works as a switch and is controlled by the control voltage V_c and the capacitor C stores the charge.

- The analog signal V_i to be sampled is applied to the drain of E-MOSFET and V_c to its gate terminal.

- When V_c is positive, the E-MOSFET turns ON and the capacitor C charges to the instantaneous value of input V_i with a time constant $[R_o + r_{DS(ON)}]$ C.
  R_o =output resistance of the voltage follower A1.
  $r_{DS(ON)}$= resistance of the MOSFET when ON.

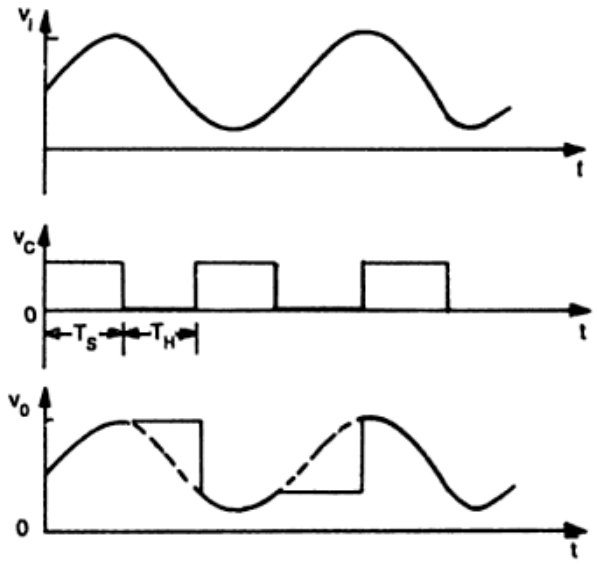
- Thus the input voltage V_i appears across the capacitor C and then at the output through the voltage follower A_2. When V_c is zero, the E-MOSFET is off. The capacitor c is now facing the high input impedance of the voltage follower A_2. and hence cannot discharge.



(a) Sample and hold circuit

- The capacitor holds voltage across it. The time period T_s, the time during which voltage across the capacitor is equal to input voltage is called sampling period.

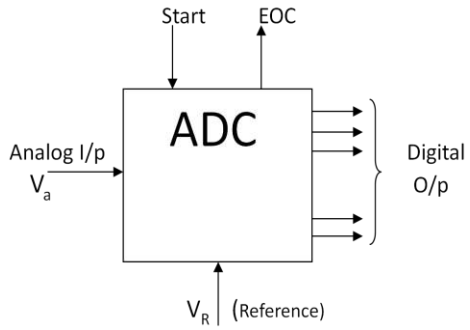
- The time period T_H of V_c during which voltage across the capacitor is held constant is called hold period. The frequency of the control voltage should be kept higher than input and also a low leakage capacitance.



Input and output waveforms

A-D CONVERTERS

- The schematic of Analog to Digital Converter is shown below



- Analog to digital converters accepts an analog input voltage V_a and produces an output binary word $d_1, d_2, d_3, \ldots \ldots d_n$ of functional value D.

$$D = 2^{-1}d_1 + 2^{-2}d_2 + \cdots 2^{-n}d_n - - - - - (1)$$

$d_1 = Most\ significant\ bit$
$d_n = Least\ \ significant\ bit$

- An ADC has two additional control lines
  - START
  - EOC

- The start input to tell the ADC when to start the conversion. The EOC (End of Conversion) output to announce when the conversion is complete.

TYPES OF ADC

- ADC'S are classified broadly into two groups
  - Direct type ADC
  - Integrating type ADC

DIRECT TYPE ADC:

Direct types ADCs compare a given analog signal with the internally generated equivalent signal. This group includes

- Flash type converter
- Counter type converter
- Tracking (or) servo comparator
- Successive approximation type converter

INTEGRATING TYPE ADC

Integrating type ADC'S perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. This groups includes

- Charge balancing ADC
- Dual slope ADC

ADC SPECIFICATIONS

RESOLUTION:

It is defined as the ratio of a change in the value of input voltage V_i needed to change the digital output by one LSB. If full scale input (V_{iFS}) required to cause a digital output of all 1's in (V_{iFS}) then resolution is

$$\frac{V_{iFS}}{(2^n - 1)}$$

QUANTISATION ERROR (QE):

- There is an unavoidable uncertainty about the exact value of V_i. The magnitude of the quantization error at the sampling instant is between zero and half of one LSB.
- In order to make the quantizing error independent of the input signal, noise with amplitude of 1 quantization step is added to the signal. This slightly reduces signal to noise ratio, but completely eliminates the distortion. It is known as dither.
- It is represented as

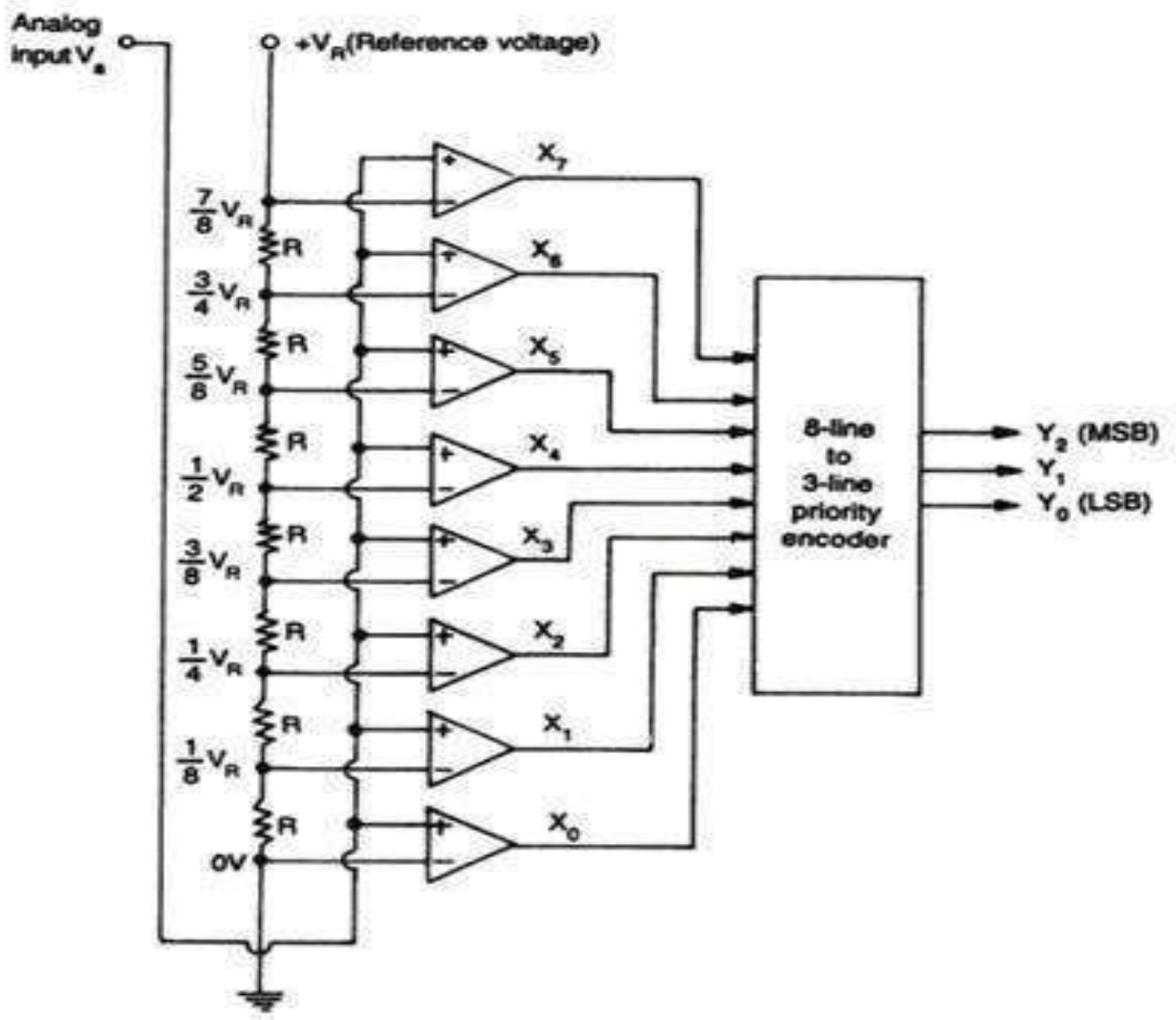
$$Q_E = \frac{V_{iFS}}{(2^n - 1)^2}$$

CONVERSION TIME:

It is defined as the total time required to convert an analog signal into its digital output. It depends on the conversion technique used and the propagation delay of the circuit components.

Parallel Comparator (Flash) type ADC

This is the simplest possible Analog to Digital Converter. It is the fastest and most expensive technique. The 3-bit Analog to Digital Converter is shown below.



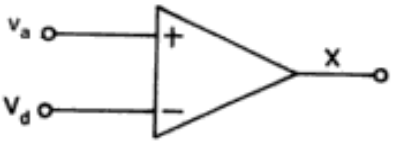
- The circuit consists of
  - Resistive divider network
  - 8 op-amp comparator.
  - A 8-line to 3-line encoder.

- At each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R and the ground.

- The purpose of the circuit is to compare the analog input voltage V_a with each of the node voltages.

- The Comparator and its truth table is shown below.

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value



- A small amount of hysteresis is built in to the comparator to resolve any problem that might occur if both inputs were of equal voltage.

- The Truth table for a flash type ADC is shown below

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Merits

- High speed as the conversion takes place simultaneously rather than sequentially. Conversion time is limited by the speed of the comparator and of the priority encoder.

Demerits

- The number of comparators required almost doubles for each added bit. The number of comparators required are $2^n - 1$ where n is the desired number of bits.

- Priority encoder is more complex for the larger value of n.

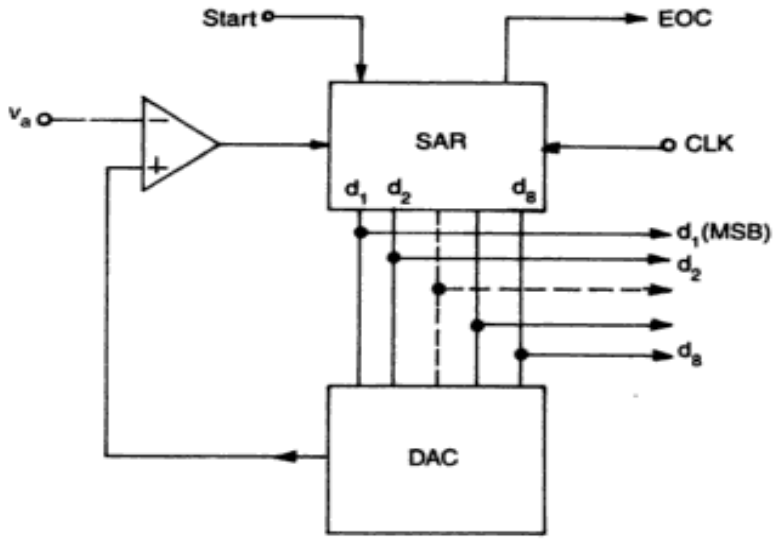
Successive Approximation type ADC:

- Successive-approximation ADC is a conversion technique based on a successive-approximation register (SAR). This is also called bit-weighing conversion that employs a comparator to weigh the applied input voltage against the output of an N-bit digital-to-analog converter (DAC).

- The Successive-approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n-clock periods.

- An 8- bit counter required eight pulses to obtain a digital output.

- An 8-bit Analog to Digital Converter is shown below.

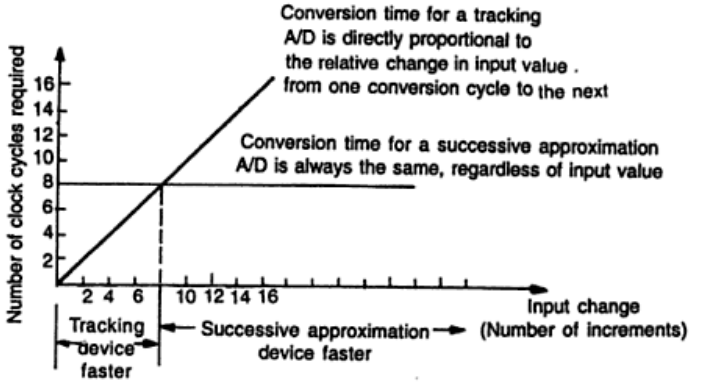


- The circuit uses successive-approximation register (SAR) to find the required value of each bit by trial and error. With the arrival of the START command, the SAR sets the MSB $d_1 = 1$ with all other bits to zero so that the trail code is 10000000.

- The output V_d of the DAC is now compared with analog input V_a.
  - If V_a is greater than the DAC output V_d then 10000000 is less than the correct digital representation. The MSB is left at 'I' and the next lower significant bit is made 'I' and further tested.

  - If V_a is less than the DAC output V_d then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go to the next lower significant bit.

- This procedure is repeated for all subsequent bits , one at a time, until all bit positions have been tested.
- Whenever the DAC output crosses V_a the comparator changes state and this can be taken as the EOC command.



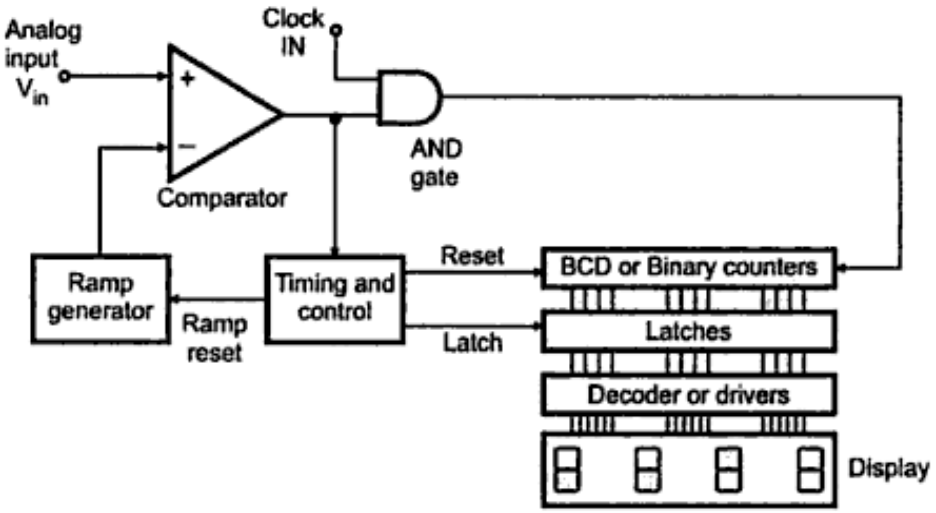
Comparison of conversion times for tracking and successive approximation A/D devices

INTEGRATING TYPE ADC

- The integrating types of ADC do not require a S/H circuit at the input .If the input changes during conversion, the ADC output code will be proportional to the value of the input averaged over the integration period.

SINGLE SLOPE ADC:

- It consists of a ramp generator and BCD or binary counters.



- At the start, the reset signal is provided to the ramp generator and the counters .Thus counters are resetted to '0'.

- The analog input V_{in} is applied to the positive terminal of the comparator .As this is more positive than the negative input, the comparator output goes high.
- The output of the ramp generator is applied to the negative terminal of the comparator .The high output of the comparator enables the AND gate which allows clock to reach the counters and also this high output starts the ramp.

- The ramp voltage goes positive until it exceeds the input voltage. When it exceeds V_{in} comparator output goes low.This Disable AND gate which inturn stops the clock of the counter.

Dual –slope ADC

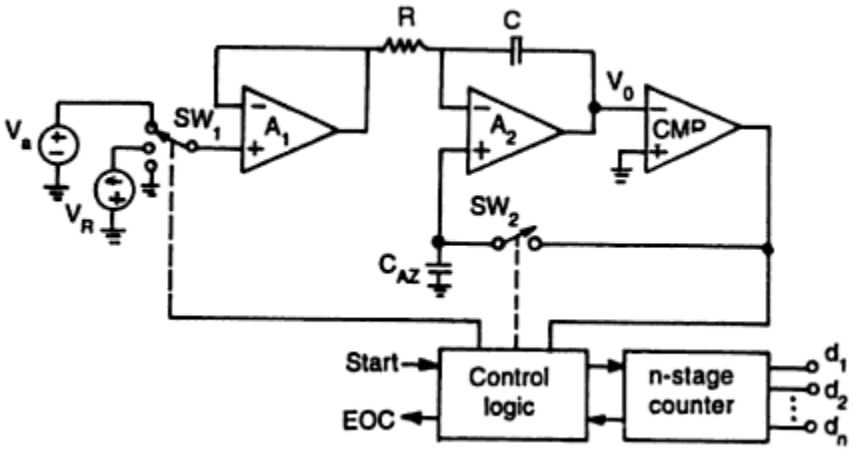
- The analog parts of the circuit consist of a high input impedance buffer A_1, precision integrator A_2 and a voltage comparator.

- The convertor first integrates the analog input signal V_a for a fixed duration of 2^n clock periods. Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero.

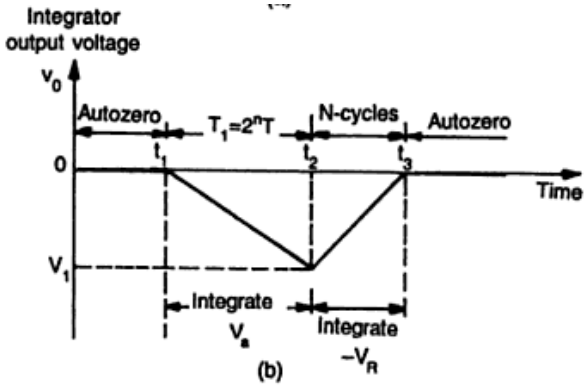
- The number N of clock cycles required to return the integrator to zero is proportional to the value of V_a averaged over the integration period. Hence N represents the desired output code.

- Before the START command arrives, the switch SW_1 is connected to ground and SW_2 is closed. Any offset voltage present in the A_1, A_2, comparator loop after integration ,appears across the capacitor C_{AZ} till the threshold of the comparator is achieved. The capacitor C_{AZ} thus provides automatic compensation for the input-offset voltages of all the three amplifiers.

- Later, when SW_2 opens, C_{AZ} acts as a memory to hold the voltage required to keep the offset nulled.At the arrival of the START command $t = t_1$,the control logic opens SW_2 and connects SW_1 to V_a and enables the counter starting from zero.



- The circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting 2^n pulses. The analog voltage V_a is integrated for a fixed number 2^n counts of clock pulses after which the counter resets to zero.If the clock period is T, the integration takes place for a time $T_1 = 2^n * T$ and the output is a ramp going downwards.



(a) Functional diagram of the dual slope ADC (b) Integrated output waveform for the dual slop ADC

- The counter resets itself to zero at the end of the interval T_1 and the switch SW_1 is connected to the reference voltage $(-V_R)$.The output voltage V_o will now have a positive slope.As long as V_o is negative ,the output of the comparator is positive and the control logic allows the clock pulse to be counted.

- When V_o becomes just zero at time $t = t_3$, the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter.

- The reading of the counter at t_3 is proportional to the analog input voltage V_a .

From the functional diagram

$$T_1 = t_2 - t_1 = \frac{2^n counts}{clock\ rate}$$

And

$$t_3 - t_2 = \frac{digital\ counts\ N}{clock\ rate}$$

$$\text{For the integrator, } \Delta V_o = \left(-\frac{1}{RC}\right) V(\Delta t)$$

The voltage V_o will be equal to V_1 at the instant t_2 and it is

$$V_1 = \left(-\frac{1}{RC}\right) V_a (t_2 - t_1)$$

The voltage V_1 is also given by

$$V_1 = \left(-\frac{1}{RC}\right)(-V_R)(t_2 - t_3)$$

So

$$V_a (t_2 - t_1) = (V_R)(t_3 - t_2)$$

Putting the value s of $(t_2 - t_1) = 2^n \ \ and \ \ (t_3 - t_2) = N \ \ we\ get$

$$V_a 2^n = V_R N$$

$$V_a = V_R (N/2^n)$$

Dual slope converters are suitable for accurate measurement of slowly varying signals, such as thermo couples and weighing scales.

The important observation of Dual slope can be made:

- Since V_R and n are constants, the analog voltage V_a is proportional to the count reading N and is independent of R, C and T.
- The dual slope ADC integrates the input signal for a fixed time, hence it provides excellent noise rejection of ac signals whose periods are integral multiples of the integration time T_1.Thus ac noise superimposed on the input signal such as 50 Hz power , line pickup will be averaged during the input integration time.So choose clock period T, so that $2^n T$ is an exact multiple integral of the line period (1/50)sec=20ms
- The main disadvantages of the dual slope ADC is the long conversion time .For instant if $2^n - T = 1/50$ issued to reject line pick-up, the conversion time will be 20ms.

Comparison of ADC

Parameters	**Flash type**	**SA type**	**Dual Slope**
Speed	Fastest	Fast	Slow
Accuracy	Less	Medium	More
Resolution	Upto 2^8	Upto 2^{16}	2^{16} (or) more
I/p hold time	Very less	Depends on No. of bits	Max.
Cost	Very Costly	Medium	Less
Application	High speed Fibre optic communication DSO, Imaging devices	Data Acquisition Systems	Not repeatedly used

Charge Balancing VFCs

- In charge balancing technique, a capacitor is supplied with a continuous charge at a rate linearly proportional to the input signal.
- Then capacitor is discharged and simultaneously discrete charge pulse is generated with the help of one shot .Therefore, for each charge -discharge cycle one pulse is generated.
- The repetition rate of these train pulses is directly proportional to the input signal since charge rate is linearly proportional to the input signal.

A/D Converter using Voltage-to-Time Conversion

- The voltage to time conversion can be easily obtained by using voltage to frequency converter. As the time is reciprocal of the frequency , the frequency output of voltage to frequency output of voltage to frequency converter can be easily converted to time using a counter , monostable multivibrator and a latch.

- A negative going pulse is used to trigger the monostable multivibrator .The same pulse is used to reset the counter .The input voltage is applied to the voltage to frequency converter. It produces the output pulses whose frequency is linearly proportional to the input.

- When the trigger is applied to the monostable multivibrator its output goes high for the particular time period At the same time the counter starts counting the pulses.

- After the time period of monostable multivibrator ,its output goes low .This output is applied to the latch which is negative edge triggered. Hence the counter output gets latched.
- The number of pulses which occurs during the specific time period is counted and the latched output is then displayed by the decade counting assemblies .Such a digital count when calibrated gives equivalent value corresponds to analog input and be used as A/D counter.

Over-sampling A/D Converters

- In conventional A/D converters the input signal is sampled ar a rate that is only twice that of the band of the input signal itself .The digital output , generated at the same rate , following to the sampling theorem, retains all the informative contents of the input signal which represents it.

- To avoid aliasing , the input signal must be band-limited by an anti-aliasing filter before sampling. Such analog filters suffer from limitations such as noise, distortion , group delay , and passband ripple ; unless great care is taken, it is difficult for downstream A/D converters to achieve resolution beyond 18 bits.

- In many applications, brick-wall analog anti-aliasing filters and SAR A/D converters have been replaced by oversampling A/D converters with digital filters.

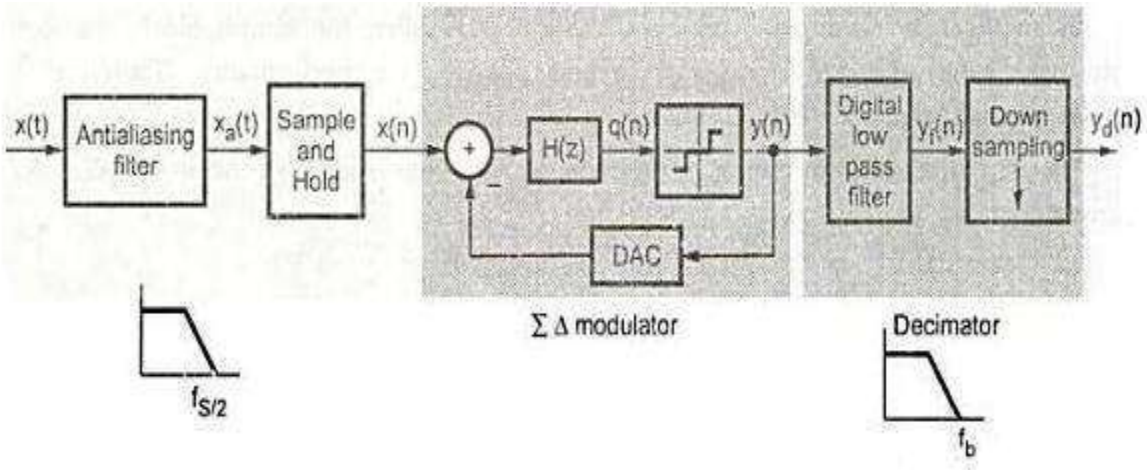
- A/D converter wher the input signal is sampled much faster than the Nyquist rate , is called an over sampling A/D converter.

- The signal bandwidth of the input signal is denoted by f_b and the Nyquist rate , which is the minimum sampling frequency required to avoid aliasing equals

$$f_N = 2f_b$$

- The over sampling ratio is defined as the ratio between the sampling frequency and the Nyquist rate .In other words , it indicates how much faster the input signal is sampled than minimally required by the Nyquist theorem.

$$OSR = \frac{f_s}{f_N} = \frac{f_s}{2f_b}$$



Antialiasing filter (AAF):

- It eliminates spectral components above half the sampling frequency from the input signal so that the modulator input signal is band-limited and the subsequent sampling operation does not alise input signals from higher frequencies into the band of interest.

∑Δ Modulator:

- It performs the actual A/D conversion by means of sampling and quantizing the band-limited input signal as well as by filtering the quantization error from the internal quantizer out of the in-band .

- The internal feedback DAC is commonly implemented with the same low resolution as the internal quantizer and thus does not introduce an additional quantization error.

Decimation filter:

- After quantization , a digital low pass filter uses decimation both to reduce the sampling frequency to a nominal rate and prevent aliasing at the new, lower sampling frequency .

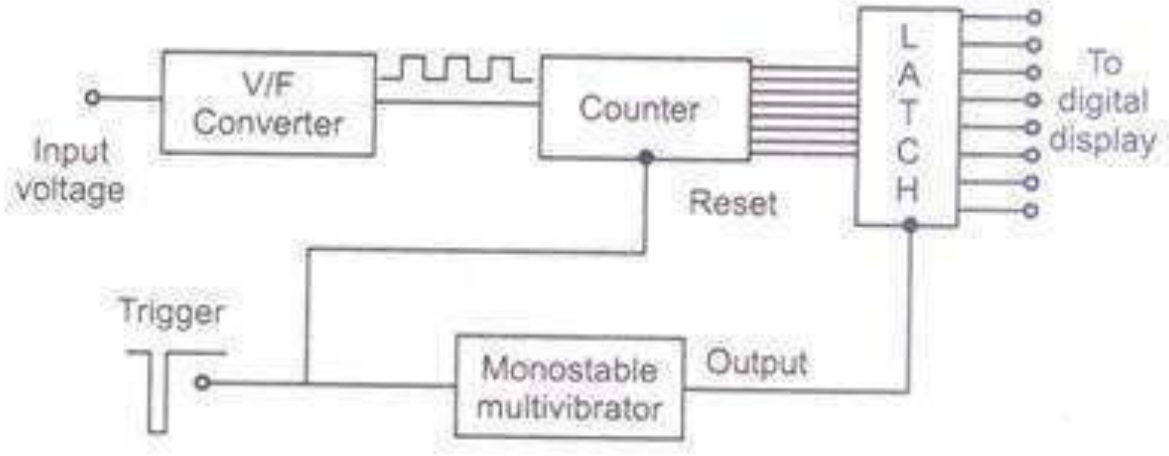
- The decimation low pass filter removes frequency components beyond the Nyquist frequency of the output sampling frequency to prevent aliasing when the output of the digital filterv is resampled (Under - sampled) at the system's sampling frequency.

- The decimator typically consists of two different blocks. First, a digital low pass filter is used to remove all the frequency components above $\frac{f_N}{2}$ to avoid signal degradation due to aliasing in the downsampling block that follows the digital filter .This digital filter also removes all the quantization noise which does not fall inside the signal band. The digital filter operates in the digital domain and its output contains N-bit words.

- The next block in the decimation filter down-samples the output of the digital filter .Down- sampling by a ratio of OSR-1 samples. Since the sampling rate of signal is changed , aliasing can occur.

- The decimation process does not result in loss of information since the digital filter removes all the components that could alias in the signal band.

A/D Converter using Voltage-to-Time Converter (VTC)



- The voltage to time conversion can be easily obtained by using voltage to frequency converter. As the time is reciprocal of the frequency , the frequency output of voltage to frequency output of voltage to frequency converter can be easily converted to time using a counter , monostable multivibrator and a latch.

- A negative going pulse is used to trigger the monostable multivibrator .The same pulse is used to reset the counter .The input voltage is applied to the voltage to frequency converter. It produces the output pulses whose frequency is linearly proportional to the input.

- When the trigger is applied to the monostable multivibrator its output goes high for the particular time period At the same time the counter starts counting the pulses.

- After the time period of monostable multivibrator ,its output goes low .This output is applied to the latch which is negative edge triggered. Hence the counter output gets latched.

- The number of pulses which occurs during the specific time period is counted and the latched output is then displayed by the decade counting assemblies .Such a digital count when calibrated gives equivalent value corresponds to analog input and be used as A/D counter.

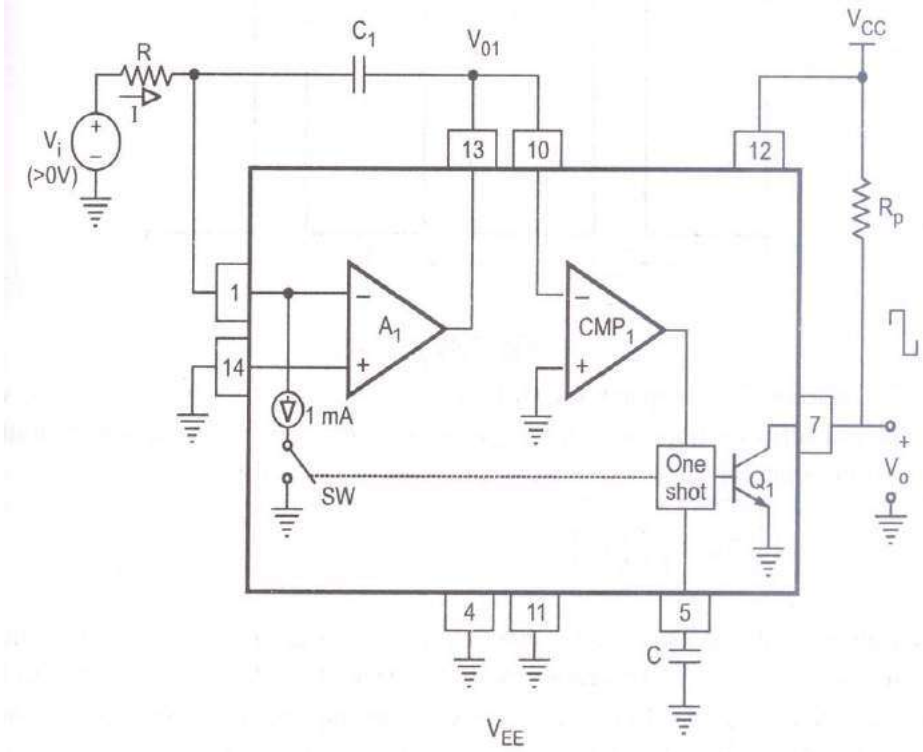
A/D Converter using Voltage-to-Frequency Converter (VFC)

Charge Balancing VFCs

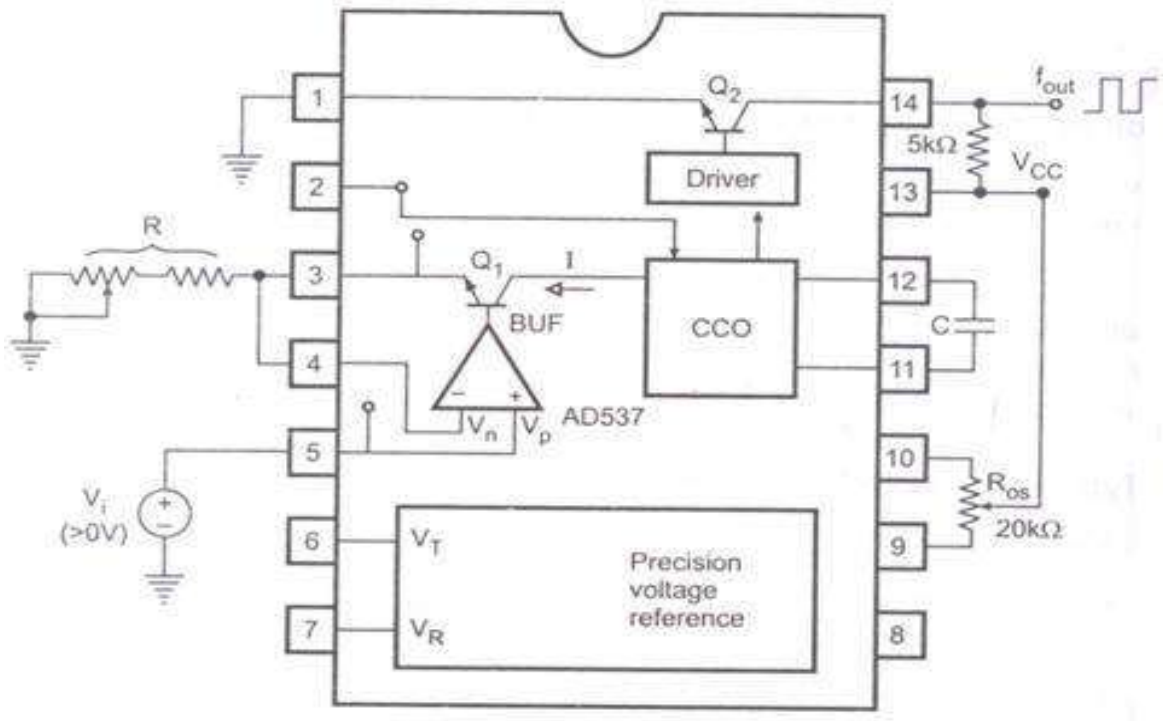
- In charge balancing technique, a capacitor is supplied with a continuous charge at a rate linearly proportional to the input signal.

- Then capacitor is discharged and simultaneously discrete charge pulse is generated with the help of one shot .Therefore, for each charge -discharge cycle one pulse is generated.

- The repetition rate of these train pulses is directly proportional to the input signal since charge rate is linearly proportional to the input signal.



Wide sweep multi vibrator VFC



UNIT V – WAVEFORM GENERATOR & SPECIAL FUNCTION IC

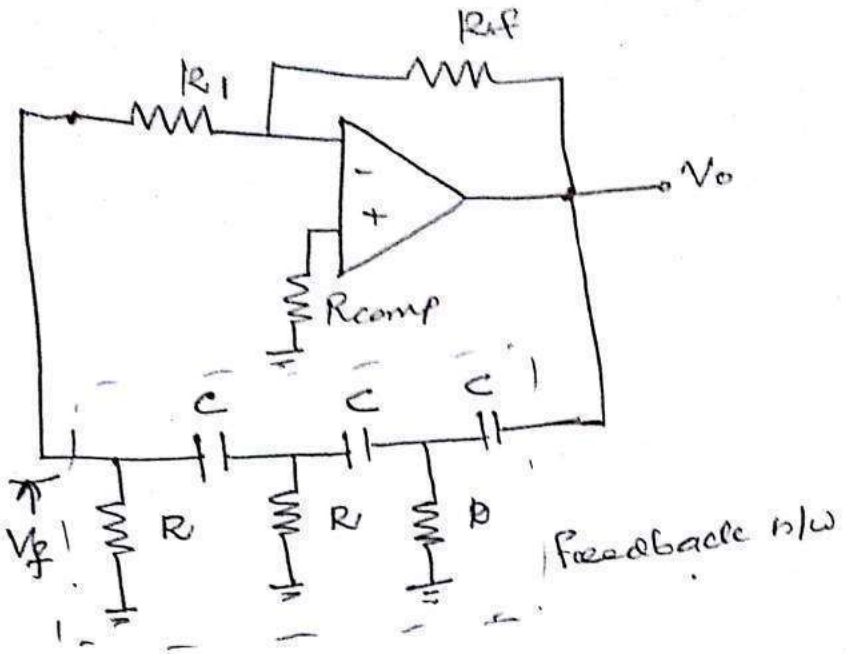
WAVEFORM GENERATORS:

- SINE WAE GENERATORS
  - Phase shift Oscillators
  - Wein-Bridge Oscillators
- SQUARE WAVE GENERATOR
- RECTANGULAR WAVE GEN.,
- TRIANGULAR WAVE GEN.,
- SAW TOOTH GENERATOR
- FUNCTION GENERATOR - IC 8038

SPECIAL FUNCTION IC's:

- TIMER – Astable Multivibrator
  - Monostable Multivibrator
- VOLTAGE REGULATOR
  - Three terminal regualtor
  - Linear regulator
  - Switching regulator
- SWITCHED CAPACITOR FILTER
- AUDIO AMPLIFIER
- POWER & TUNED AMPLIFIER
- VIDEO AMPLIFIER
- ISOLATION AMPLIFIER
- FIBRE OPTIC IC
- OPTO COUPLER

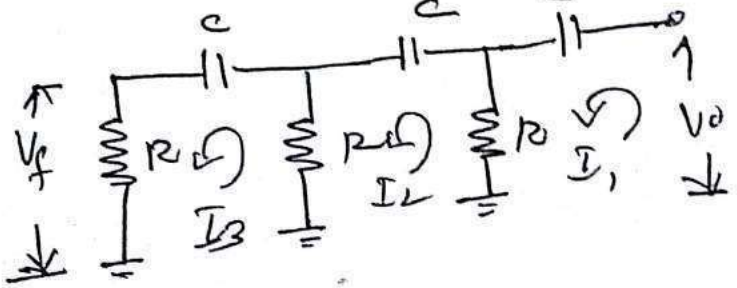
RC phase shift oscillator



The op-amp is used in inverting mode and therefore it provides 180° phase shift. The additional phase of 180° is provided by RC n/w to obtain a total phase shift of 360°.

The feedback n/w consists of three identical RC stages. Each of the RC stages provides a 60° phase shift so that phase shift due to feedback n/w is 180°.

To find feedback factor β.



$$\begin{vmatrix} R+\frac{1}{sc} & -R & 0 \\ -R & 2R+\frac{1}{sc} & -R \\ 0 & -R & 2R+\frac{1}{sc} \end{vmatrix} \begin{vmatrix} I_1 \\ I_2 \\ I_3 \end{vmatrix} = \begin{vmatrix} V_0 \\ 0 \\ 0 \end{vmatrix}$$

$$\Delta = \left[R+\frac{1}{sc}\right]\left[\left(2R+\frac{1}{sc}\right)^2 - R^2\right] + R\left[-R\left[2R+\frac{1}{sc}\right]\right]$$

$$= \left(R+\frac{1}{sc}\right)\left[4R^2 + \frac{1}{s^2c^2} + \frac{4R}{sc} - R^2\right] - 2R^3 - \frac{R^2}{sc}$$

$$= 4R^3 + \frac{R}{s^2c^2} + \frac{4R^2}{sc} - R^3 + \frac{4R^2}{sc} + \frac{1}{s^3c^3} + \frac{4R}{s^2c^2} - \frac{R^2}{sc}$$

$$- 2R^3 - \frac{R^2}{sc}$$

$$= R^3 + \frac{5R}{s^2c^2} + \frac{6R^2}{sc} + \frac{1}{s^3c^3}$$

$$= \frac{R^3s^3c^3 + 5Rsc + 6R^2s^2c^2 + 1}{s^3c^3}$$

$$\Delta_3 = \begin{vmatrix} R+\frac{1}{sc} & -R & V_0 \\ -R & 2R+\frac{1}{sc} & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$= \left(R+\frac{1}{sc}\right)\left[2 \quad V_0 R^2\right]$$

$$I_3 = \frac{\Delta_3}{\Delta} = \frac{V_0 R^2 s^3 c^3}{1 + 5SRC + 6s^2c^2R^2 + s^3c^3R^3}$$

$$V_f = I_3 R = \frac{V_o R^3 s^3 c^3}{1 + 5sRC + 6s^2c^2R^2 + s^3c^3R^3}$$

$$\frac{V_f}{V_o} = \frac{1}{1 + \frac{6}{sRC} + \frac{5}{s^2c^2R^2} + \frac{1}{s^3c^3R^3}}$$

Put $s = j\omega$, $s^2 = -\omega^2$, $s^3 = -j\omega^3$

$$\beta = \frac{1}{1 + \frac{6}{j\omega RC} - \frac{5}{\omega^2c^2R^2} - \frac{1}{j\omega^3R^3c^3}}$$

$$= \frac{1}{\left(1 - \frac{5}{\omega^2c^2R^2}\right) + \frac{j}{\omega RC}\left[\frac{1}{\omega R^2c^2} - \frac{6}{}\right]}$$

$$= \frac{1}{[1 - 5\alpha^2] + j\alpha[\alpha^2 - 6]} \quad \text{where } \alpha = \frac{1}{\omega RC}.$$

for $A\beta = 1$, β should be real ie imaginary term should be zero

$\therefore \alpha(\alpha^2 - 6) = 0$

$\alpha^2 = 6$, $\alpha = \sqrt{6}$

ie $\frac{1}{\omega RC} = \sqrt{6}$

the frequency of oscillation

$\therefore f_o = \frac{1}{2\pi RC\sqrt{6}}$.

putting $\alpha^2 = 6$

$$\beta = -\frac{1}{29}$$

$$|\beta| = \frac{1}{29}$$

$$|A\beta| \geq 1$$

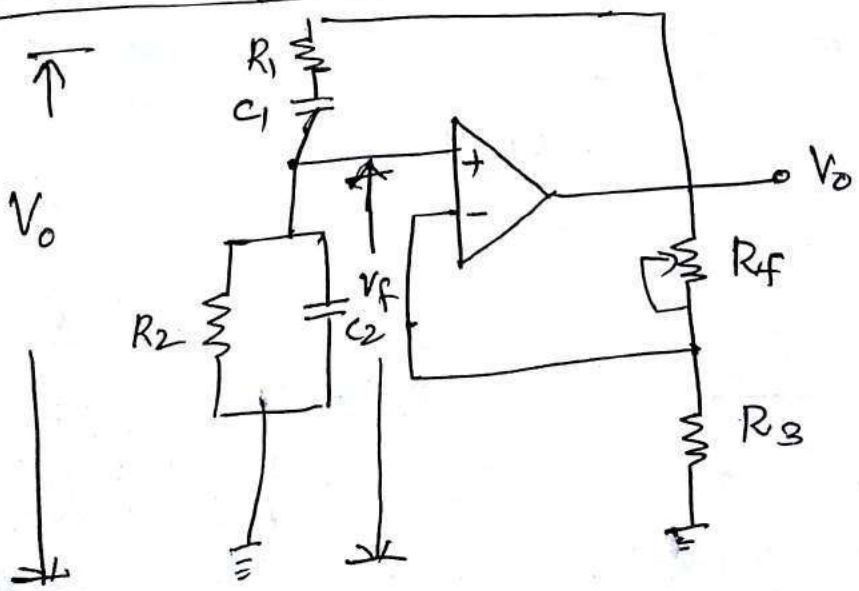
$$\therefore |A\beta| \geq 29$$

$$\left|\frac{R_f}{R_1}\right| \geq 29$$

$$\boxed{R_f \geq 29 R_1}$$

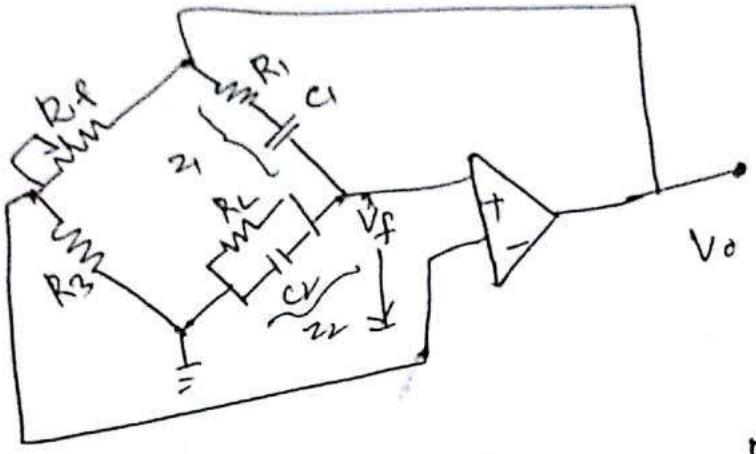
Design a phase shift osullator to osullate at 100 Hz.

Wien Bridge osullator



The feed back signal is connected to non inverting input terminal so that op-amp is working as non inverting amplifier. Therefore feedback n/w need not provide any phase shift.

The ckt can also be redrawn as.



The gain of op-amp = $A = 1 + \frac{R_F}{R_3}$.

feedback factor β.

$$\beta = \frac{V_f}{V_o} = \frac{Z_2}{Z_1 + Z_2}$$

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{sR_1C_1 + 1}{sC_1}$$

$$Z_2 = \frac{R_2 \cdot \frac{1}{sC_2}}{R_2 + \frac{1}{sC_2}} = \frac{R_2}{1 + sR_2C_2}$$

$$\beta = \frac{R_2 / (1 + sR_2C_2)}{\left(\frac{1 + sR_1C_1}{sC_1}\right) + \frac{R_2}{(1 + sR_2C_2)}}$$

$$= \frac{\frac{R_2}{1+sR_2C_2}}{\frac{(1+sR_1C_1)C_1+sR_2C_2)+sR_2C_1}{(sC_1)(1+sR_2C_2)}}$$

$$= \frac{sR_2C_1}{1+sR_2C_2+sR_1C_1+s^2R_1C_1R_2C_2+sR_2C_1}$$

$$= \frac{sR_2C_1}{1+s[R_1C_1+R_2C_2+R_2C_1]+s^2R_1R_2C_1C_2}$$

put $s = j\omega$

$$\beta = \frac{j\omega R_2C_1}{1+j\omega C R_1C_1+R_2C_2+R_2C_1) - \omega^2 R_1R_2C_1C_2}$$

In order β to be real quantity

$$1-\omega^2 R_1R_2C_1C_2 = 0$$

$$\omega^2 R_1R_2C_1C_2 = 1$$

$$f_0 = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

and $$\beta = \frac{R_2C_1}{R_1C_1+R_2C_2+R_2C_1}$$

for $R_1 = R_2 = R$ and $C_1 = C_2 = C$

$$f_0 = \frac{1}{2\pi RC}, \quad \beta = \frac{1}{3}$$

$|A\beta| \geq 1$ for sustained oscillation

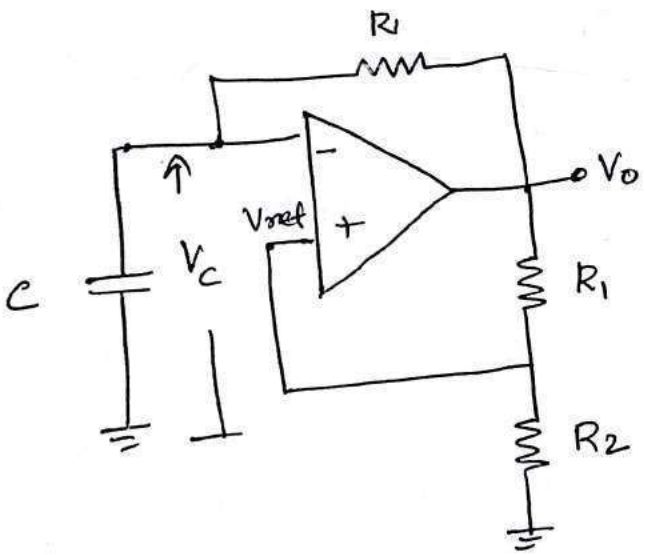
$|A| \geq 3$

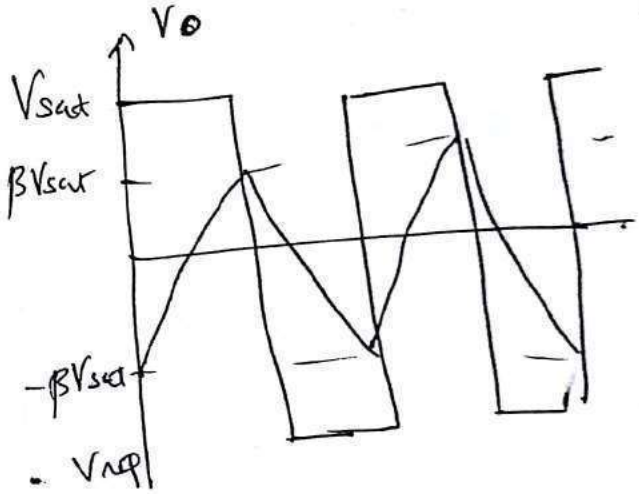
$1 + \frac{R_f}{R_3} \geq 3$

$\frac{R_f}{R_3} \geq 2$

$\boxed{R_f \geq 2R_3}$

Square wave generator: [Astable multivibrator]





Also called a free running oscillator. The principle of generation of square wave output is to force an op-amp to operate in the saturation region.

A fraction $\beta = \frac{R_2}{R_1 + R_2}$ of the output is fed back to the + input terminal.

Thus the reference voltage $V_{ref} = \beta V_o$ and take values $\pm \beta V_{sat}$. The output is also fed back to the − input after integrating by means of a low pass RC combination. whenever the input at − input terminal just exceeds V_{ref} switching takes place resulting in a square wave output. Both the states are quasi stable.

Consider an instant when output is at $+V_{sat}$, the capacitor starts charging towards $+V_{sat}$ through R. the voltage at the + input terminal is held at $+\beta V_{sat}$ by R_1 and R_2. This conditions continues as the charge on C rises until it just exceeded βV_{sat}. the reference voltage. When the voltage at the − input terminal becomes just greater than this ref voltage, the output is driven to $-V_{sat}$. At this instant the voltage on the capacitor is $+\beta V_{sat}$. It begins to discharge through R ie charge towards $-V_{sat}$. When the output switches to $-V_{sat}$, the capacitor charges more negatively until it just exceeds $-\beta V_{sat}$. The o/p switches back to $+V_{sat}$. The cycle repeats itself.

Frequency of osullatn, is determined by the time taken by it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$. and vice versa.

The voltage across the capacitor as a function of time is given by.

$$V_c(t) = V_f + (V_i - V_f)\, e^{-t/RC}$$

final value $V_f = V_{sat}$

inital value $V_i = -\beta V_{sat}$.

$$\therefore V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

$$= V_{sat} - V_{sat}(1+\beta)\, e^{-t/RC}.$$

at $t = T_1$, voltage across the capacitor reaches βV_{sat} and switching takes place

$$\therefore V_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}(1+\beta)\, e^{-T_1/RC}$$

$$\therefore T_1 = RC \ln \frac{1+\beta}{1-\beta}$$

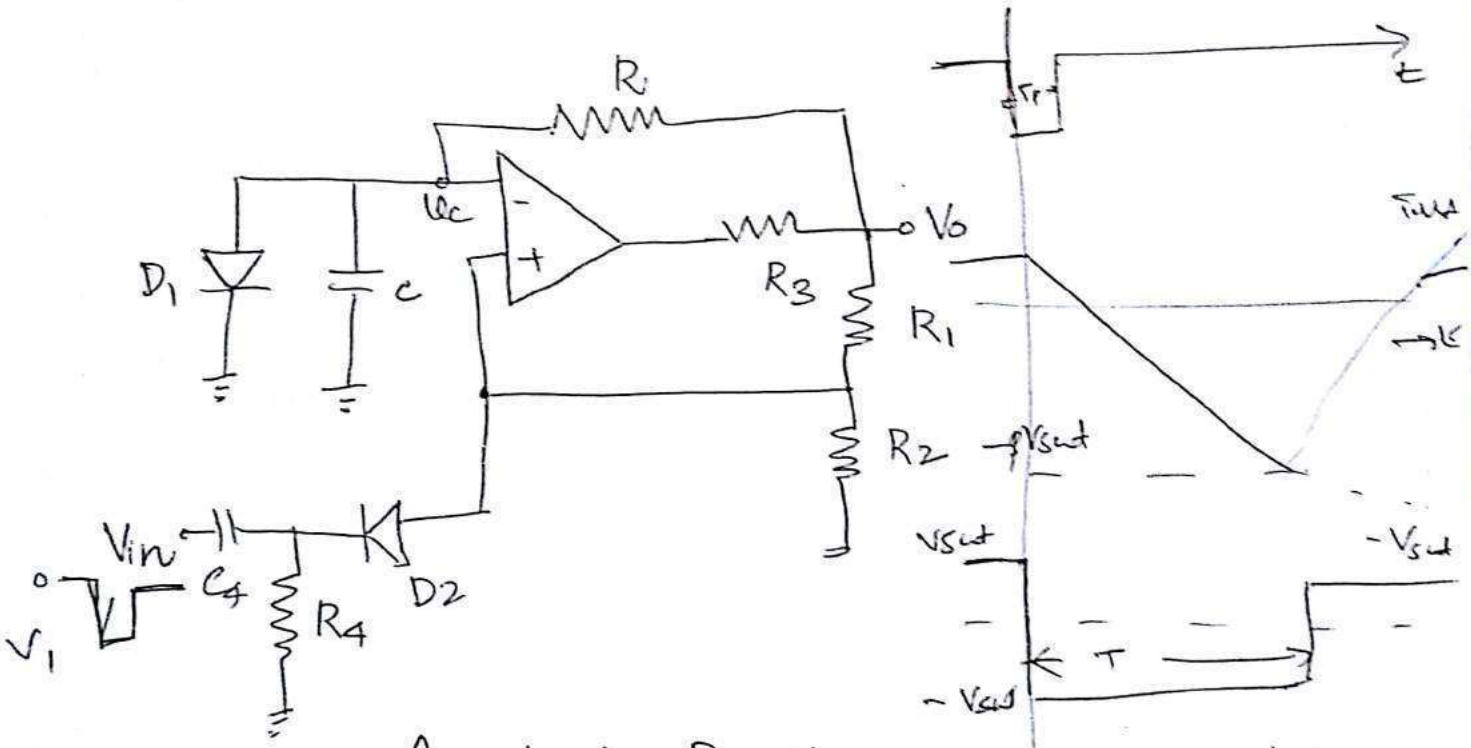
$\therefore$ Total time period,

$$T = 2T_1 = 2RC \ln \left[\frac{1+\beta}{1-\beta}\right]$$

the o/p wave form is symmetrical, if $R_1 = R_2$, then $\beta = 0.5$, $T = 2RC \ln 3$ and for $R_1 = 1.16 R_2$ it can seen that $T = 2RC$, $f_0 = \frac{1}{2RC}$.

Monostable Multivibrator

Monostable multivibrator has one stable state and the other is quasi stable state. The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal. The width of the pulse depends only on external components connected.



A diode D_1 clamps the capacitor voltage to 0.7 V when the o/p is at $+V_{sat}$. A negative going pulse signal of magnitude V_1 passing through the differentiator R_4C_4 and diode D_2 produces a negative going triggering impulse and is applied to the +ve input terminal.

In the stable state the output V_o is at $+V_{sat}$. The diode D_1 conducts and V_c the voltage across

the capacitor is clamped to +0.7V. The voltage at +ve input terminal through $R_1 R_2$ is βV_{sat}.

Now if a negative trigger of magnitude V_1 is applied to +V input terminal so that the effective signal at this terminal is less than 0.7 V i.e $\beta V_{sat} + (-V_1) < 0.7V$, the output of the op-amp will switches from $+V_{sat}$ to $-V_{sat}$. The diode now get reverse biased and capacitor charging exponentially to $-V_{sat}$. through R. The voltage at +ve input terminal is now $-\beta V_{sat}$. When the capacitor voltage v_c becomes slightly more negative than $-\beta V_{sat}$, the o/p of the op-amp switches back to $+V_{sat}$. The capacitor now starts charging to $+V_{sat}$ through R until v_c is 0.7V as capacitor gets clamped to the voltage.

Calculation of pulse width T:

The general soln for a single time constant low pass RC circuit with v_i and V_f as initial and final value is

$$v_c = V_f + (V_i - V_f) e^{-t/RC}$$

here $V_f = -V_{sat}$, $V_i = V_D$

$$\therefore v_c = -V_{sat} + (V_D + V_{sat}) e^{-t/RC}$$

at $t = T$, $v_c = -\beta V_{sat}$

$$-\beta V_{sat} = -V_{sat} + (V_D + V_{sat})\, e^{-T/RC}$$

$$V_{sat}(1-\beta) = (V_D + V_{sat})\, e^{-T/RC}$$

$$\frac{V_{sat}(1-\beta)}{V_{sat}\left(1 + \frac{V_D}{V_{sat}}\right)} = e^{-T/RC}$$

$$\frac{T}{RC} = \ln \frac{1 + V_D/V_{sat}}{1-\beta}$$

$$T = RC \ln\left\{\frac{1 + V_D/V_{sat}}{1-\beta}\right\}$$

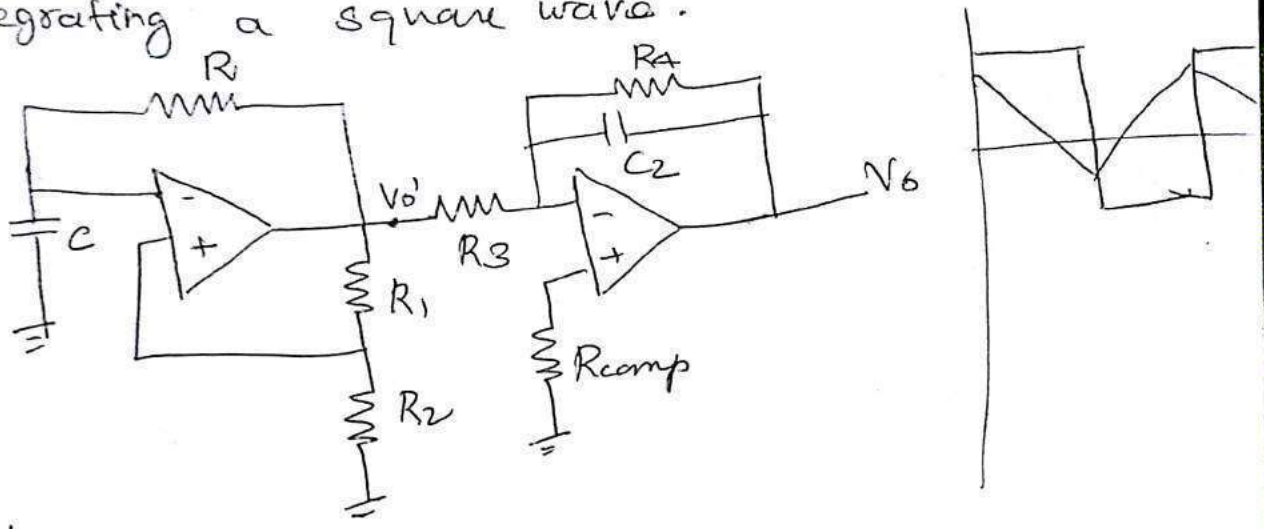
where $\beta = \frac{R_2}{R_1 + R_2}$

If $V_{sat} >> V_D$, and $R_1 = R_2$ so that $\beta = 0$.

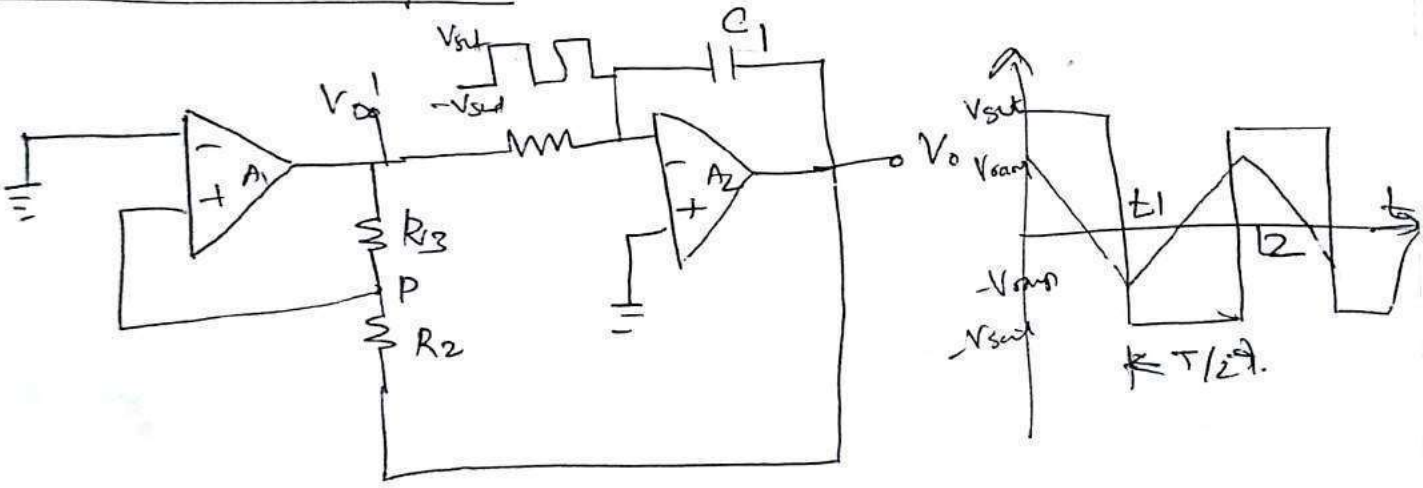
then $\boxed{T = 0.69\ RC}$

Triangular waveform generator

A triangular wave can be obtained by integrating a square wave.



With lesser components:



The effective voltage at point P during the time when o/p of A_1 is at $+V_{sat}$ is given by

$$-V_{ramp} + \frac{R_2}{R_2+R_3}\left[V_{sat} - (-V_{ramp})\right]$$

at $t = t_1$ the voltage at point P becomes equal to zero

$$\therefore \quad -V_{ramp} = -\frac{R_2}{R_3}\left(+V_{sat}\right]$$

at $t = t_2$ the o/p of A_1 switches from $-V_{sat}$ to V_{sat}

$$V_{ramp} = -\frac{R_2}{R_3}(-V_{sat}) = \frac{R_2}{R_3} V_{sat}$$

∴ Peak to peak amp of triangular wave is

$$V_{opp} = +V_{ramp} - (-V_{ramp}) = 2\frac{R_2}{R_3} \cdot V_{sat}$$

The op switches from $-V_{ramp}$ to $+V_{ramp}$ in half the time period $T/2$.

$$\therefore V_o = -\frac{1}{RC}\int V_i \, dt$$

$$V_{o(pp)} = -\frac{1}{R_1 C_1}\int_0^{T/2} -V_{sat}\, dt$$

$$= -\frac{V_{sat}}{R_1 C_1} \cdot T/2$$

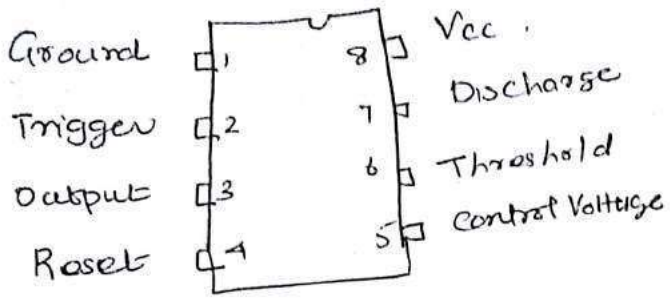
$$T = 2R_1C_1 \cdot \frac{V_{o(pp)}}{V_{sat}}$$

$$T = 2R_1C_1 \cdot \frac{2 \cdot R_2}{R_3} \cdot \frac{V_{sat}}{V_{sat}}$$

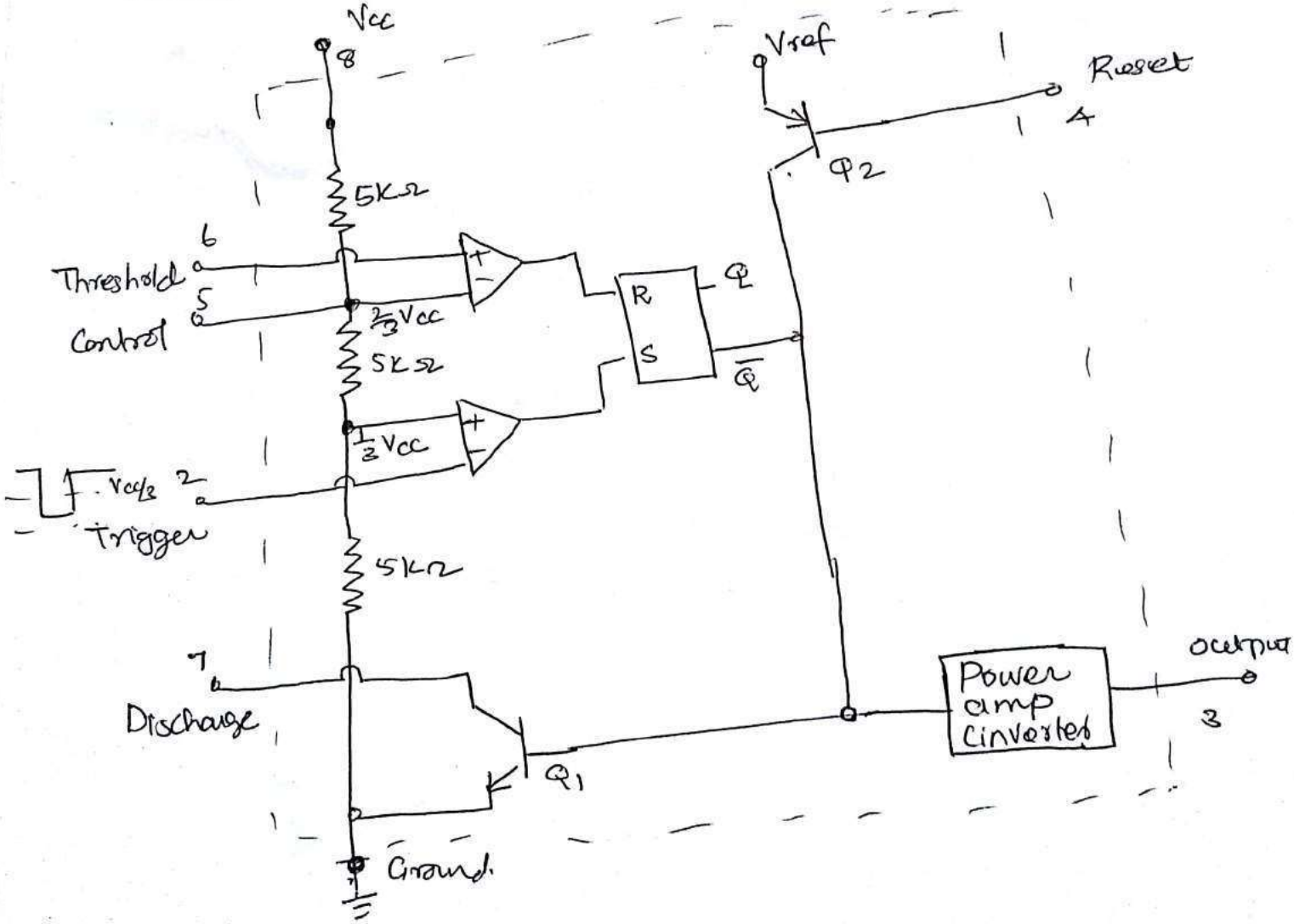
$$T = \frac{4R_1C_1R_2}{R_3}$$

$$f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2}$$

555 Timer



Functional Diagram:

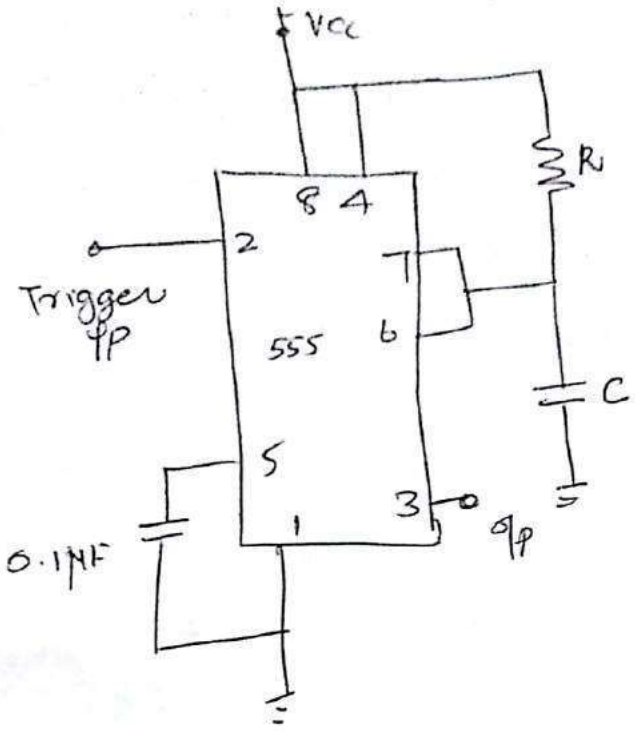


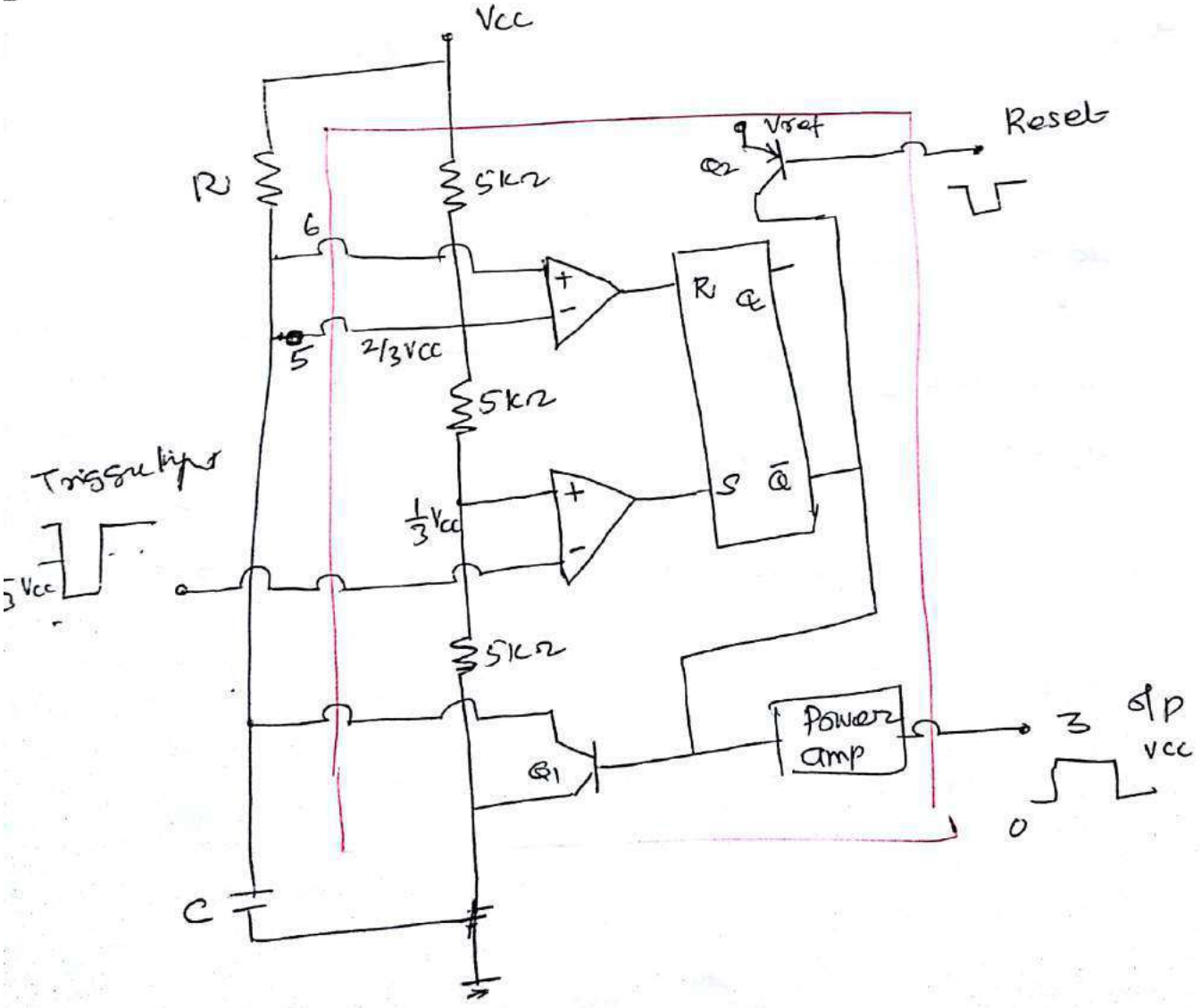
$[-V_{ramp}] = 2\frac{R_2}{R_3} \cdot V_{sat}$

three 5 kΩ resistors acts as voltage divider providing bias voltage of $\frac{2}{3}V_{cc}$ to upper comparator (UC) and $\frac{1}{3}V_{cc}$ to the lower comparator LC. Since these two voltages fix the necessary comparator threshold voltage they also aid in determining the timing interval. It is possible to vary time by applying a modulating voltage to the control voltage input.

In standby (stable) state, the output $\overline{Q}$ of the control FF is high. This makes the o/p low. A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of LC ($\frac{V_{cc}}{3}$). At the negative going edge of the trigger, as the trigger passes through ($\frac{V_{cc}}{3}$) the o/p of LC goes HIGH and sets the FF ($Q=1$, $\overline{Q}=0$). During positive excursion, when the threshold voltage at pin 6 passes through $\frac{2}{3}V_{cc}$ the o/p of UC goes HIGH and resets the FF ($Q=0$, $\overline{Q}=1$)

Monostable Operation:

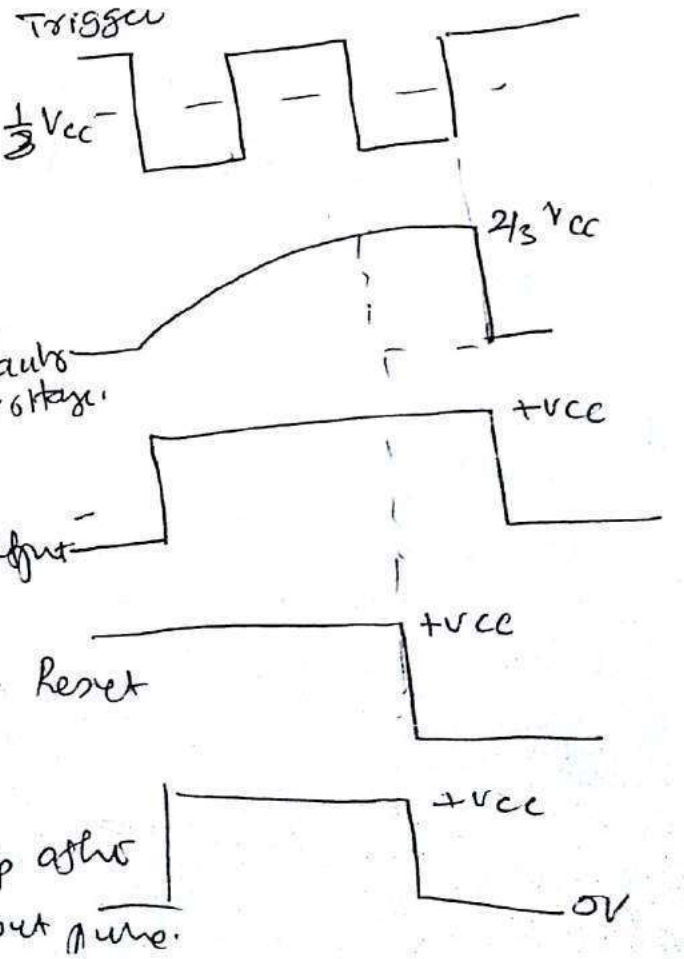




In standby mode FF holds transistor Q1 on. Thus clamping the external timing capacitor to ground. The o/p remains at ground potential. i.e Low

As the trigger pulse pass through $\frac{V_{cc}}{3}$ the FF is set i.e $\bar{Q} = 0$. This makes the transistor Q1 off and the short ckt across the timing capacitor C is released. As $\bar{Q}$ is low, o/p goes high. Now the voltage across the capacitor rises exponentially through R towards Vcc with timing constant RC.

After a time period T, the capacitor voltage is just greater than $\frac{2}{3}V_{cc}$ the UC resets the FF i.e $R=1$, $S=0$ makes $\bar{Q}=1$, transistor Q1 goes on thereby discharging the capacitor C rapidly to ground potential.



The voltage across the capacitor

$$U_c = V_{cc}\left[1 - e^{-t/RC}\right]$$

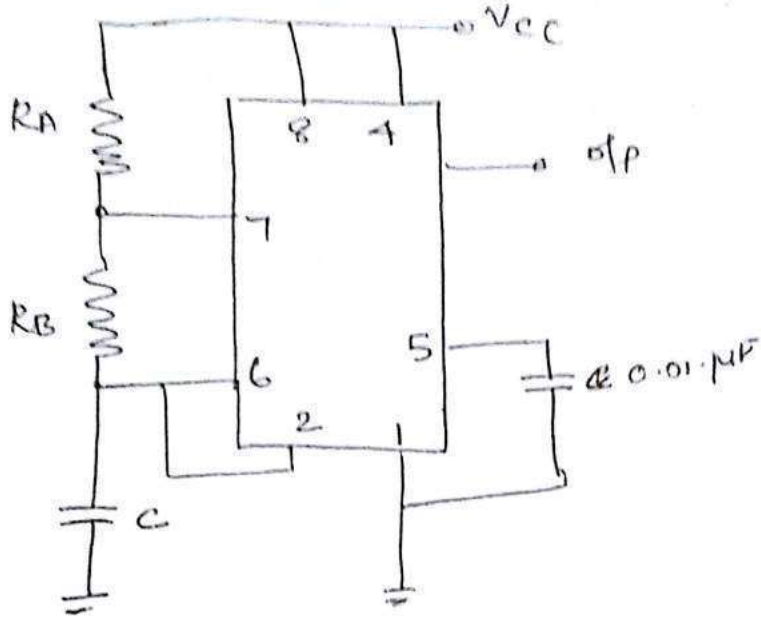
at $t = T$, $V_c = 2/3\ V_{cc}$

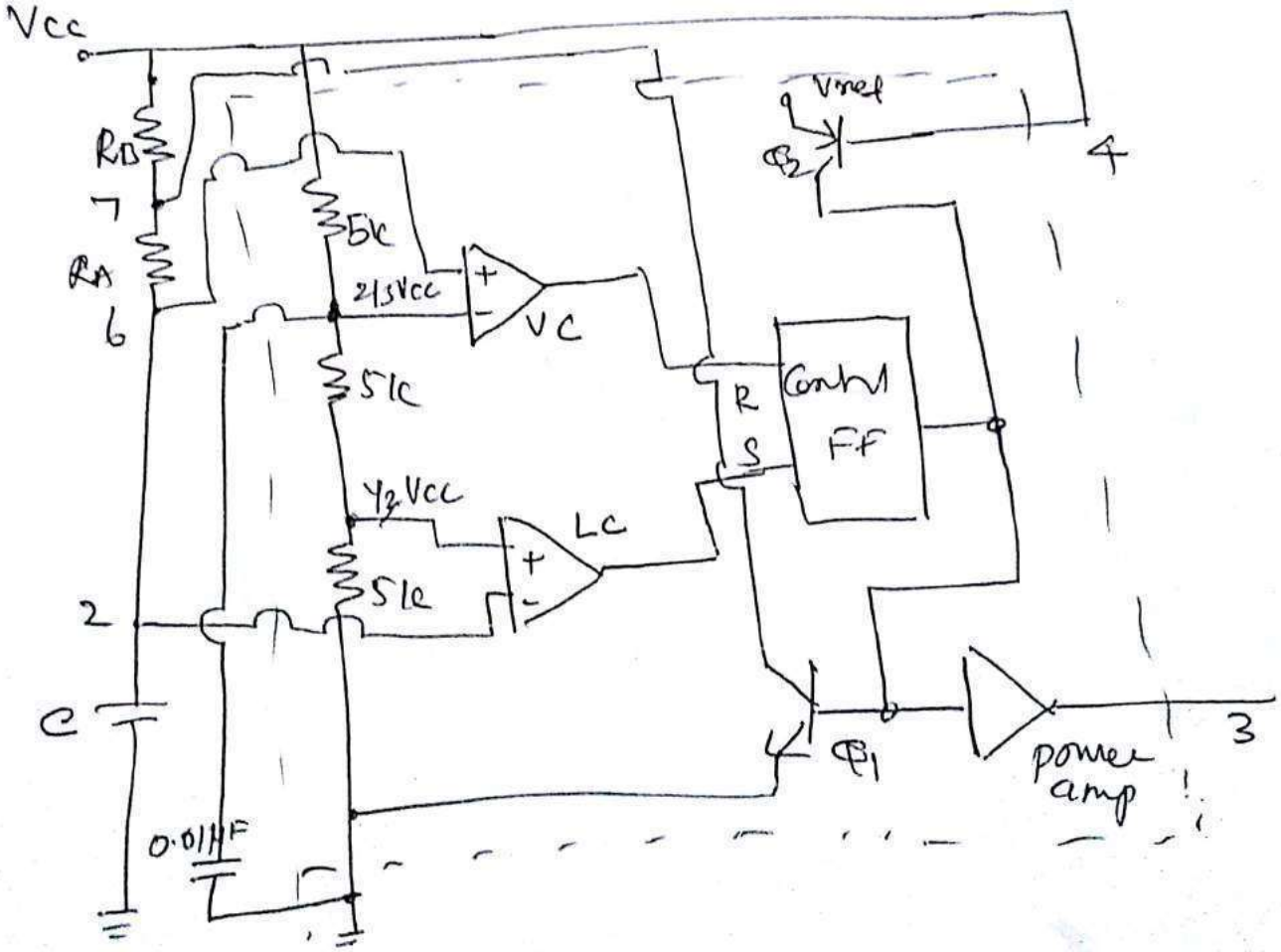
$$2/3\ V_{cc} = V_{cc}\left[1 - e^{-T/RC}\right]$$

$$T = RC \ln\left[1/3\right]$$

$$\boxed{T = 1.1\ RC}$$

Astable operation:

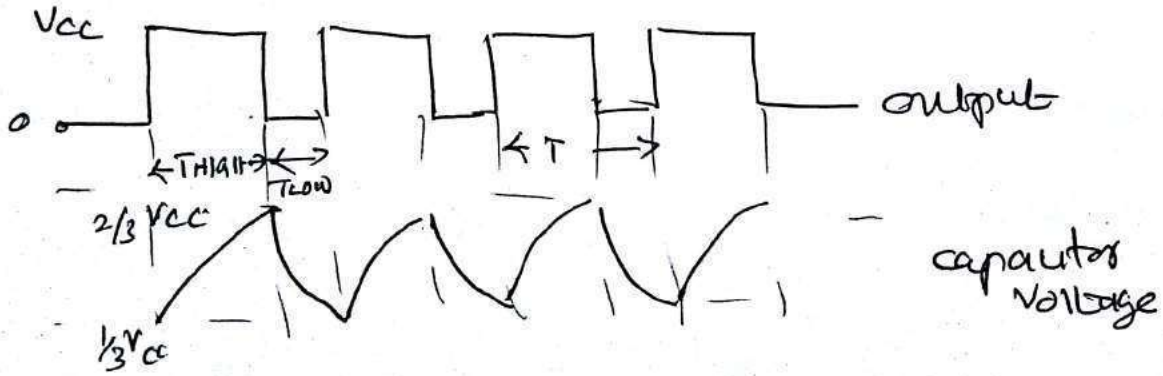




Comparing to monostable operation, the timing resister is split into two sections R_A and R_B. Pin 7 of discharging transistor Q_1 is connected to the junction of R_A and R_B. When the power supply Vcc is connected, the external timing capacitor C charges towards Vcc with a time constant $(R_A + R_B)C$. During this time o/p is high as $R=0$, $S=1$.

When the capacitor voltage equals $2/3\,V_{cc}$ the UC triggers the flipflop so that $\bar{Q}=1$ this makes the transistor Q_1 on and the capacitor C starts discharging towards ground through R_B and Q_1. with a time constant R_BC.

During the Discharge of the timing capacitor C as it reaches $\frac{1}{3}V_{cc}$ the UC is triggered and it sets the FF ie $S=1, R=0$ which turns $\bar{Q}=0$ and output Low. Thus the capacitor C periodically charged and discharged b/w $2/3\,V_{cc}$ and $\frac{1}{3}V_{cc}$.



The capacitor voltage for a Low pass RC circuit subjected to a step input Vcc volts is

$$V_c = V_{cc}\left[1 - e^{-t/RC}\right]$$

The time t_1 taken by the capacitor to charge from 0 to $\frac{2}{3}V_{cc}$ is

$$\frac{2}{3}V_{cc} = V_{cc}\left[1 - e^{-t_1/RC}\right]$$

$$t_1 = 1.09\,RC$$

$e^{-t_1/RC} = 1 - \frac{2}{3}$

$\frac{t_1}{RC} = \ln\left[\frac{1}{3}\right]$

$t_1 = RC \ln 3$

$t_1 = 1.09\,RC$

The time t_2 to charge from 0 to $\frac{1}{3}V_{cc}$ is

$$\frac{1}{3}V_{cc} = V_{cc}\left[1 - e^{-t_2/RC}\right]$$

$$t_2 = 0.405\,RC$$

$e^{-t_2/RC} = 1 - \frac{1}{3}$

$t_2 = RC \ln\left[\frac{3}{2}\right]$

Now $t_{HIGH} = t_1 - t_2$

$= 1.09RC - 0.405RC$

$= 0.69RC$

for the given ckt $\boxed{t_{HIGH} = 0.69\,(R_A + R_B)C}$

The time taken by the capacitor to discharge from $\frac{2}{3}V_{cc}$ to $\frac{1}{3}V_{cc}$ is known calculate as, the voltage across the capacitor

$$\frac{1}{3}V_{cc} = \frac{2}{3}V_{cc}\,e^{-t/RC}$$

$$t = 0.69\,RC$$

$\therefore t_{LOW} = 0.69\,R_B C.$

$T = t_{HIGH} + t_{LOW} = 0.69(R_A + R_B)C + 0.69R_BC$

$T = 0.69\,(R_A + 2R_B)C$

$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$

Duty cycle

$$D = \frac{t_{LOW}}{T} \times 100$$

$$D = \frac{R_B}{R_A + 2R_B} \times 100$$

Duty cycle is defined as the ratio of ON time to the total time period

Design and construct RC phase shift oscillator for f_o = 500 Hz.

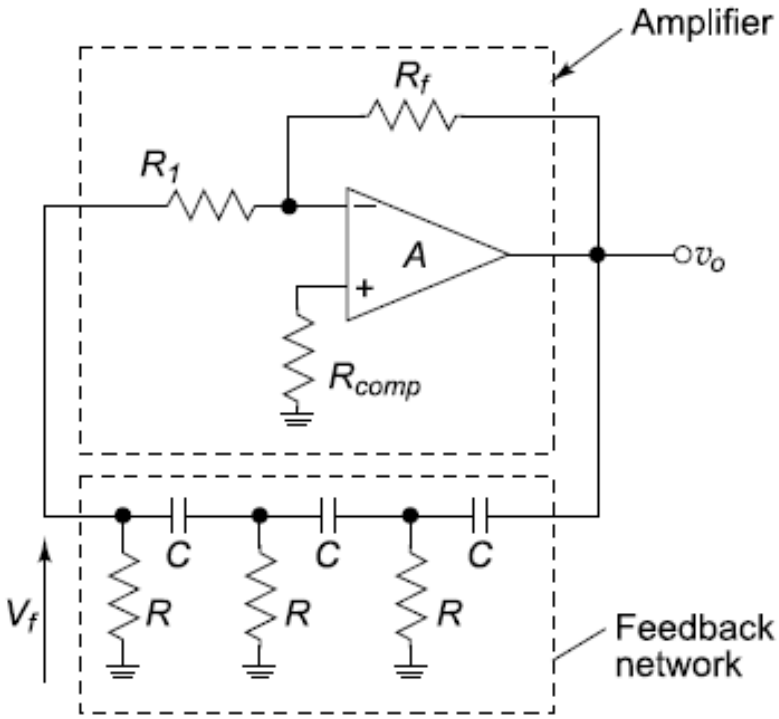
(a) Phase shift oscillator:
In Fig. 5.15,

$$f_o = \frac{1}{2\pi\sqrt{6}\,RC} \text{ and } R_f \geq 29\,R_1$$

Choose $C = 0.1\ \mu F$,

Then $$R = \frac{1}{2\pi(500)(\sqrt{6})(10^{-7})} = 1.3\ k\Omega \text{ (use } 1.5\ k\Omega)$$

To prevent loading, $R_1 \geq 10\,R$
Therefore, take $R_1 = 10\,R = 15\ k\Omega$
$R_f = 29\ R_1 = 29 \times 15\ k\Omega$
$= 435\ k\Omega$
(Use $R_f = 500\ k\Omega$ potentiometer)



Design and construct Wein Bridge oscillator for f_o = 1 KHz.

(b) Wien bridge oscillator:
In Fig. 5.16(a),

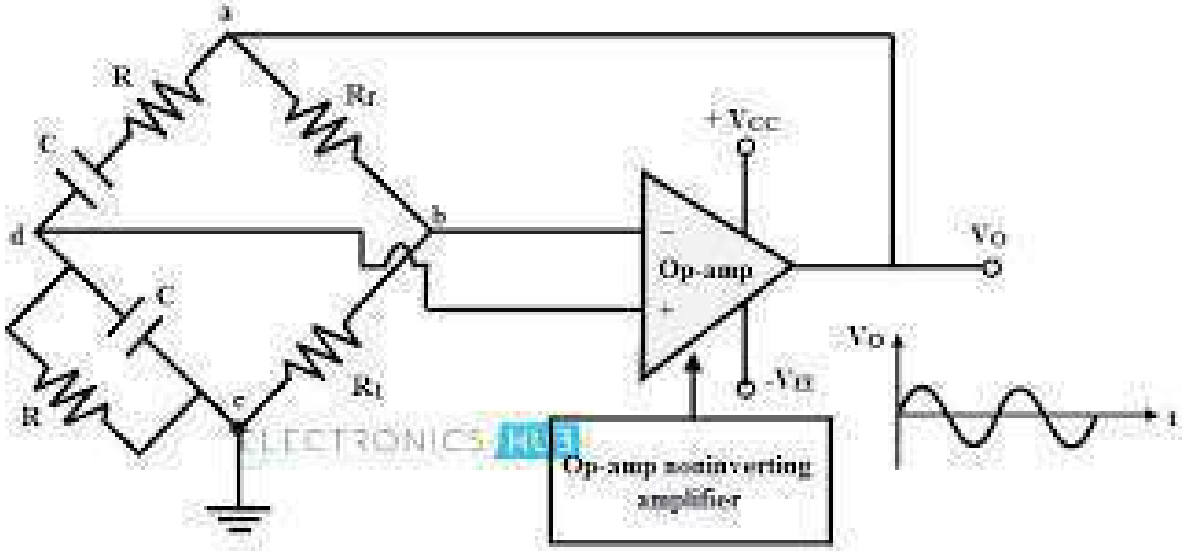
$$f_o = \frac{1}{2\pi RC} \quad \text{and} \quad R_f = 2R_1$$

Choose $C = 0.05$ mF

So, $$R = \frac{1}{2\pi (1000)(0.05 \times 10^{-6})} = 3.1\ \text{k}\Omega$$

Take $R_1 = 10R = 30\ \text{k}\Omega$

and $R_f = 2R_1 = 60\ \text{k}\Omega$ (Use 100 kΩ pot)



Design a square wave oscillator for f_o = 1 kHz using 741 op-amp and DC supply voltage of ±12 V.

Solution

Given frequency of oscillation $f_o = 1$ kHz

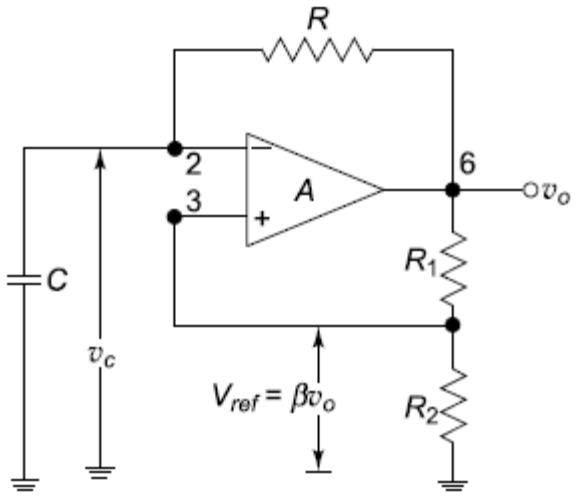
For designing a square wave oscillator, the op-amp based astable multivibrator, shown in Fig. 7.9(a) may be used with the assumption of $R_1 = R_2 = 10$ kΩ. Referring to Eq. (7.22), we have

Considering $R_1 = R_2$, we have $\beta = \dfrac{R}{2R} = 0.5$, $T = 2RC \ln 3$ and

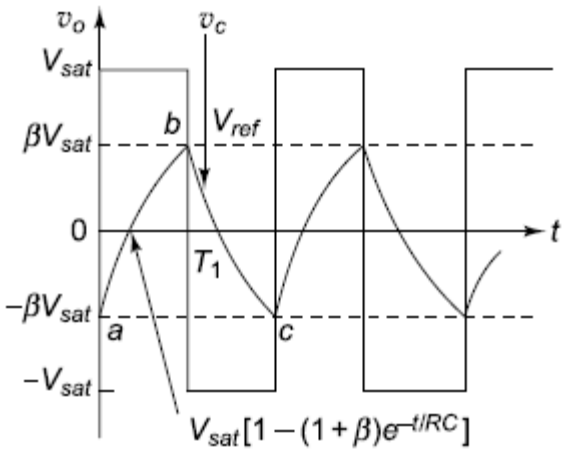
$$f_o = \frac{1}{2RC \ln 3} = \frac{1}{2.2RC} \tag{7.22}$$

$$f_o = \frac{1}{2.2\,RC}$$

Assuming $C = 0.1\mu F$, we get $R = \dfrac{1}{2.2\,Cf_o} = \dfrac{1}{2.2 \times 0.1 \times 10^{-6} \times 1 \times 10^{3}} = 4.545$ kΩ



(a) Circuit diagram



(b) Waveforms at output and capacitor terminal

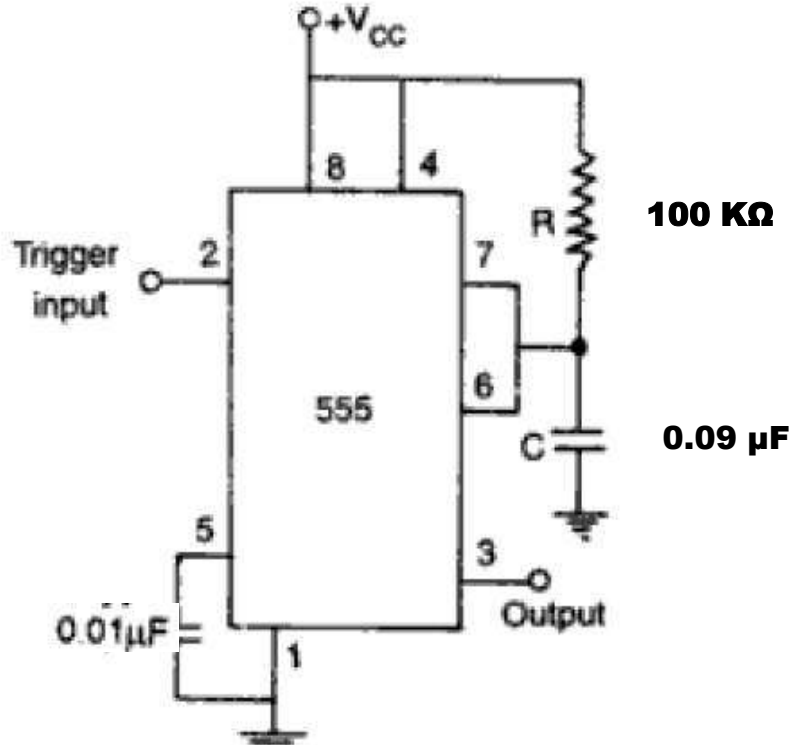
In the monostable multivibrator of Fig. 8.3, $R = 100\ k\Omega$ and the time delay $T = 100$ mS. Calculate the value of C. Verify the value of C obtained from the graphs of Fig. 8.6.

Solution

From Eq. (8.2)., we get $T = 1.1\ RC$ (seconds)

$$C = T/1.1\ R = 100 \times 10^{-3}/1.1 \times 100 \times 10^{3} = 0.9\ \mu F$$

From the graph of Fig. 8.6, the value of C is found to be 0.9 μF also.



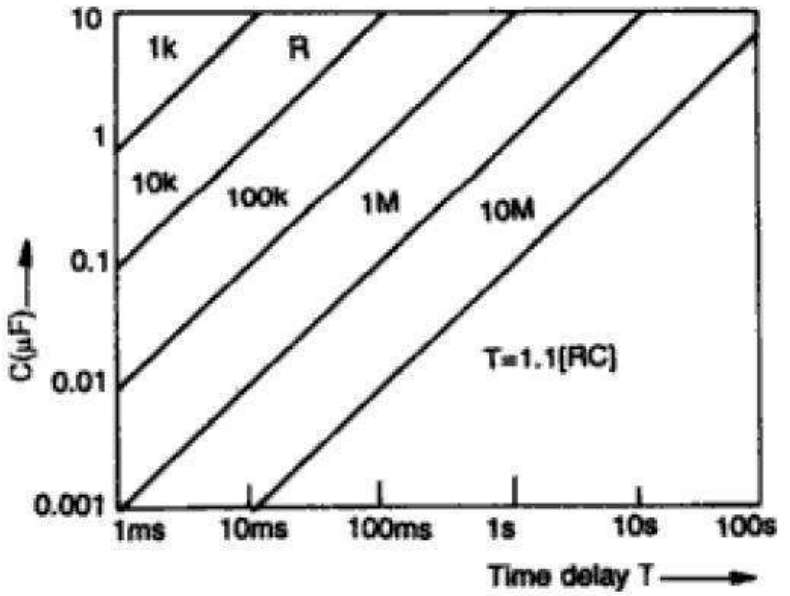
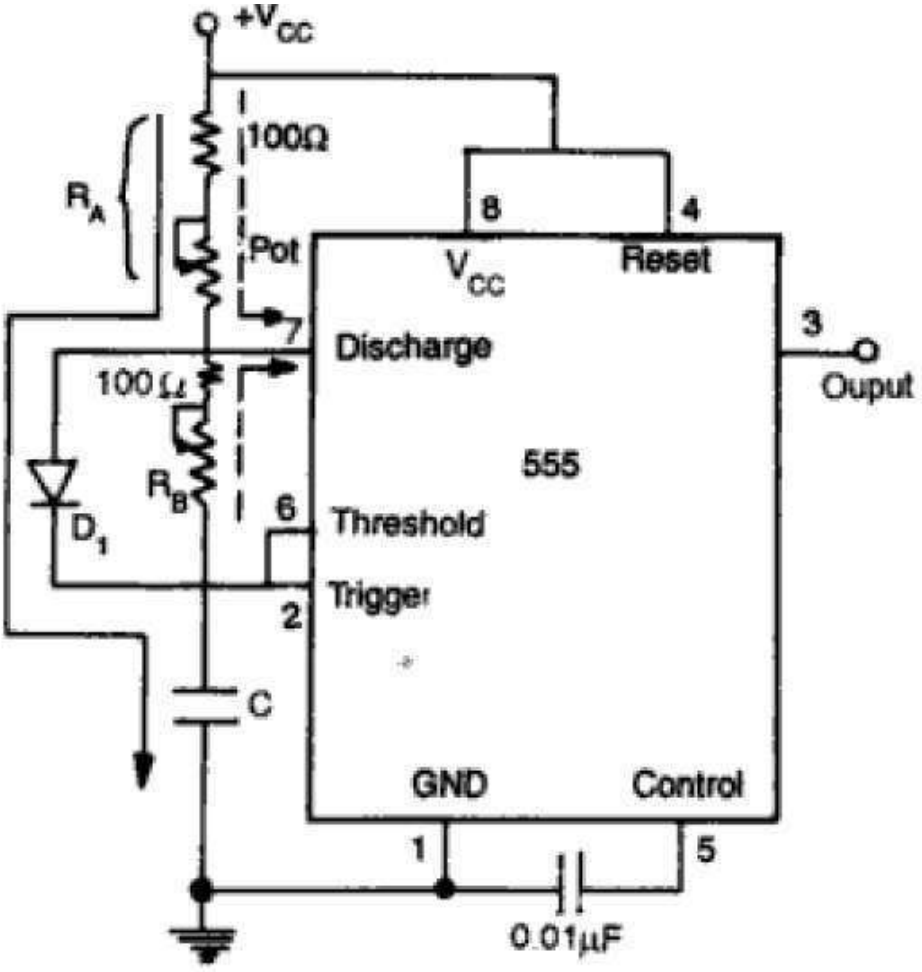


Fig. 8.6 Graph of *RC* combinations for different time delays

An alternative circuit which will allow duty cycle to be set at practically any level is shown in Fig. 8.19. During the charging portion of the cycle, diode D_1 is forward biased effectively short circuiting R_B so that

$$t_{HIGH} = 0.69\ R_A C$$



However, during the discharging portion of the cycle, transistor Q_1 becomes ON, thereby grounding pin 7 and hence the diode D_1 is reverse biased.

So
$$t_{LOW} = 0.69\ R_B\, C \tag{8.15}$$

$$T = t_{HIGH} + t_{LOW} = 0.69\,(R_A + R_B)\,C \tag{8.16}$$

or,
$$f = \frac{1.45}{(R_A + R_B)C} \tag{8.17}$$

and duty cycle
$$D = \frac{R_B}{R_A + R_B}$$

Refer Fig. 8.15. For $R_A = 6.8\ k\Omega$, $R_B = 3.3\ k\Omega$ and $C = 0.1\ \mu F$, calculate (a) t_{HIGH} (b) t_{LOW} (c) free running frequency (d) duty cycle, D.

Solution

(a) By Eq. (8.11)

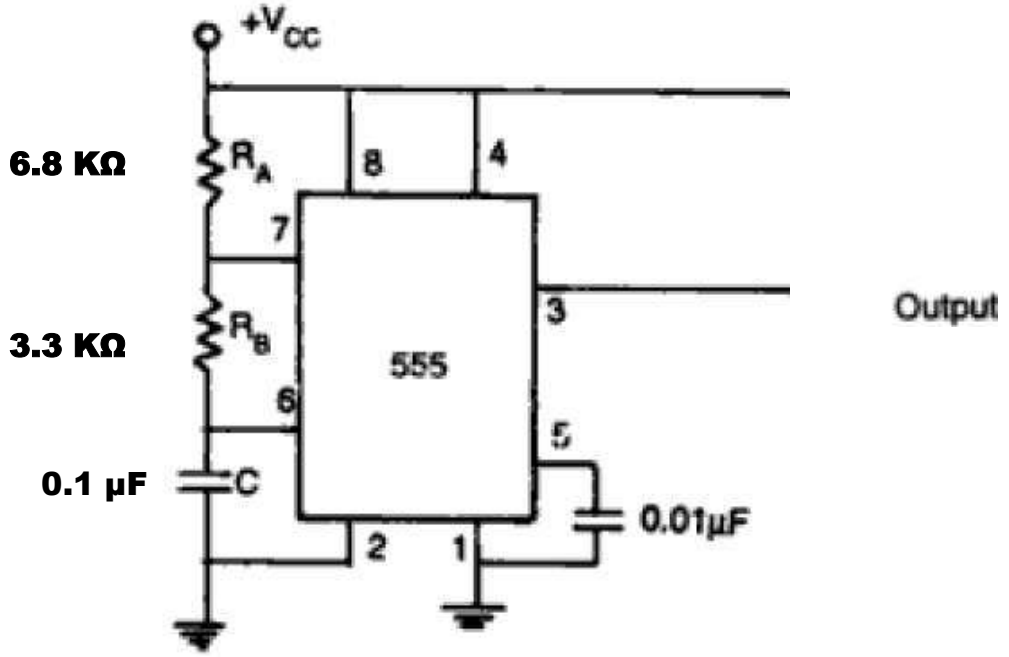
$$t_{HIGH} = 0.69\,(6.8\ k\Omega + 3.3\ k\Omega)\,(0.1\ \mu F) = 0.7\ ms$$

(b) By Eq. (8.12)

$$t_{LOW} = 0.69\,(3.3\ k\Omega)\,(0.1\ \mu F) = 0.23\ ms$$

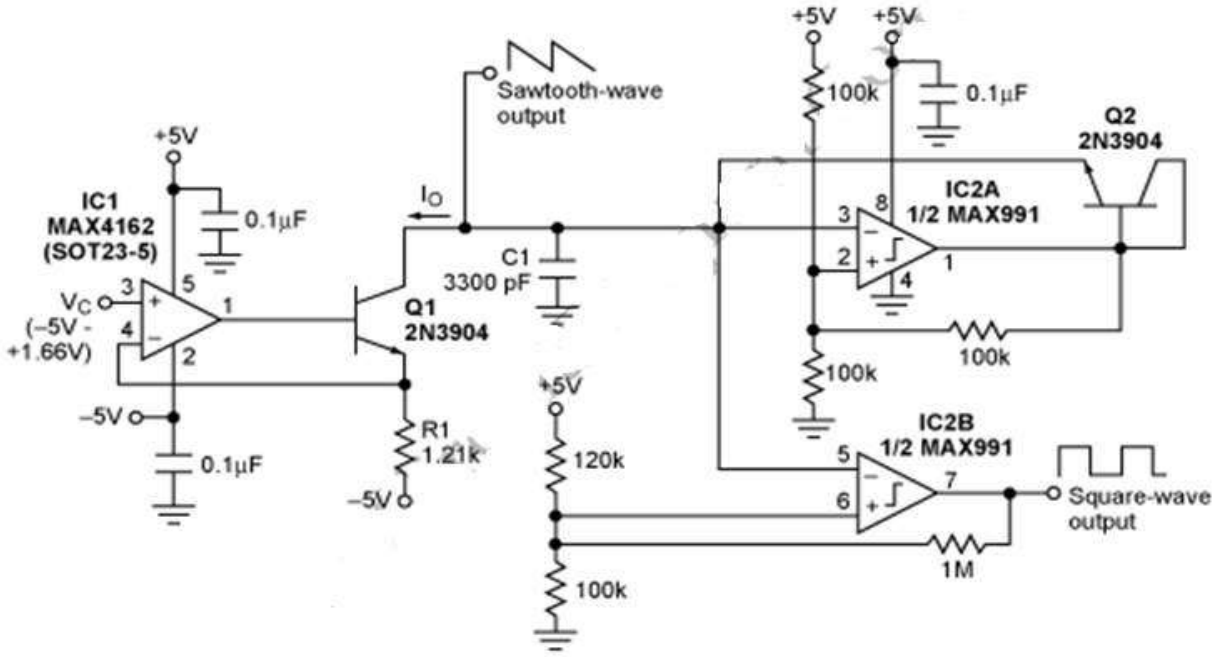
(c) $$f = \frac{1.45}{[(6.8\ k\Omega) + (2)(3.3\ k\Omega)](0.1\ \mu F)} = 1.07\ kHz$$

(d) $$D = \frac{t_{LOW}}{T} = \frac{R_B}{R_A + 2R_B} = \frac{3.3\ k\Omega}{6.8\ k\Omega + 2(3.3\ k\Omega)} = 0.25 \text{ or, } 25\%$$



To construct and observe the waveforms of a 1 kHz square waveform generator using 555 timer for duty cycle, (a) $D = 0.25$; (b) $D = 0.50$.

SAW TOOTH GENERATOR:



This is a simple saw tooth generator circuit. A voltage-controlled current source is formed by IC1 with R1 and Q1. The C1 is discharged by current Io until it's voltage is less than 1.66V. It will swing its output to 5V and trips the IC2A comparator. The C1 is charged by current through the diode-connected transistor (Q2) until its voltage reaches 3.33V, so the IC2A output to swing back to ground. The advantages of this circuit are low cost and produce an auxiliary square wave at the same frequency. This circuit can be used to sweep the frequency of another generator.

The output frequency is determined by : $f_{OUT} = (3(5V + V_C)5V)\left(\frac{1}{R_1 C_1}\right)$

We can set the f_{OUT} as high as desired by adjusting the values of C_1 and R_1, subject to the limitations of comparator IC2A's slew settling and rate time. The frequency range over which it can operate determined by generator's linearity.

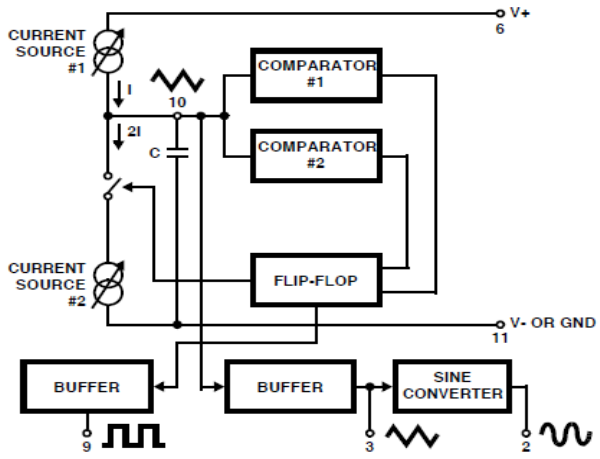
FUNCTION GENERATOR – IC 8038

Function generators are designed to provide the basic waveforms such as square wave, triangular wave and sine wave. The monolithic function generator provides these basic waveforms with a maximum number of external components reducing complexity, but increasing the reliability of the circuit. They find application in communication, telemetry, electronic, music and testing and calibration in labs. In function generators, VCO generates the triangular and square waves. The triangular wave is passed through the on chip wave shaper to generate a sine wave. The sawtooth and pulse waveforms are generated to configure the oscillator for a high asymmetric duty cycle.

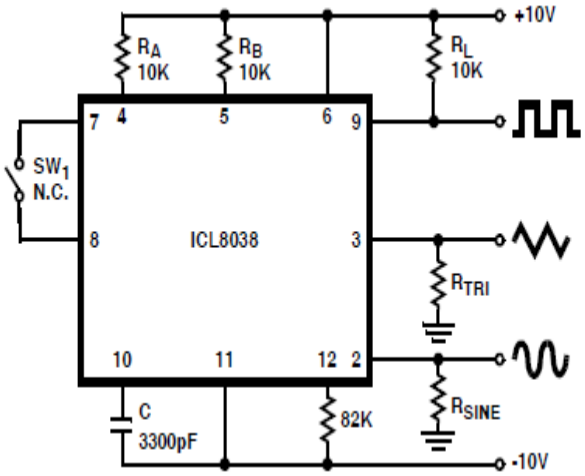
The ICL8038 waveform generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency can be selected externally from 0.001Hz to more than 300kHz using either resistors or capacitors. The ICL8038 is fabricated with advanced monolithic technology and thin film resistors, the output is stable over a wide range of temperature and supply

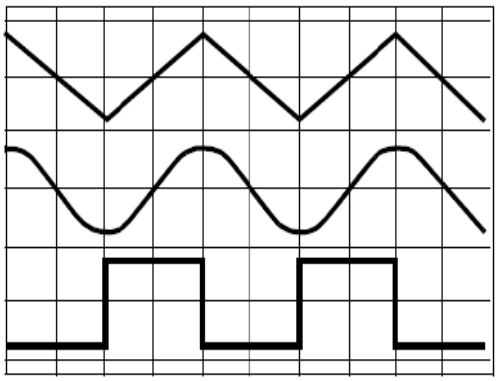
variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 250 ppm/^{o}C.

BLOCK DIAGRAM:

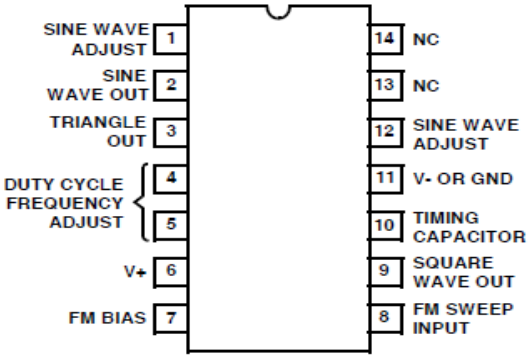


CIRCUIT DIAGRAM:





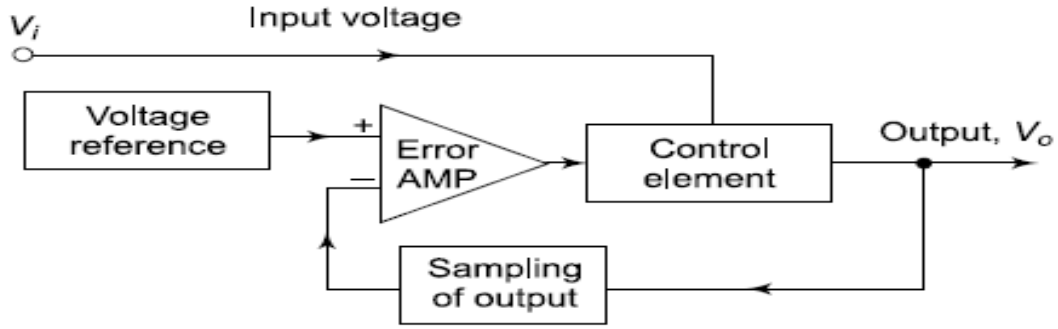
OUTPUT WAVEFORMS



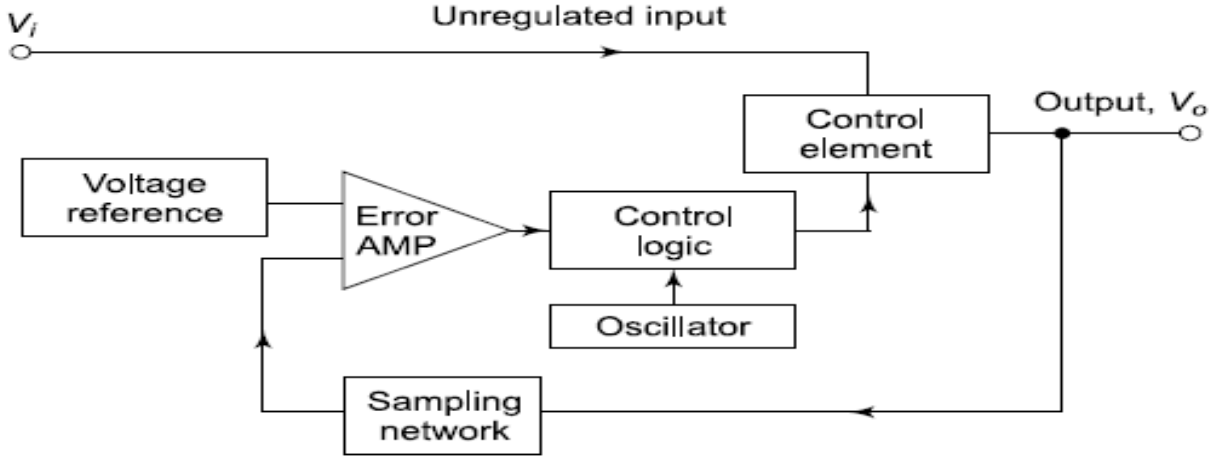
PIN DIAGRAM: IC 8038

Voltage Regulators

The commonly used voltage regulators can be classified into (i) Linear voltage regulators and (ii) Switching regulators. The main difference between these two regulators is seen from the block diagrams g



(a)



(b)

The linear regulators are classified into two types, namely, (i) Series regulator and (ii) Shunt regulator. Their respective block diagrams are shown in Figs. 8.2(a) and (b). The control element connected in *series* or in *shunt* with the load identifies the circuit as a *series* or a *shunt* voltage regulator. The linear regulators are available for fixed positive or negative output voltages and variable positive or negative output voltages. The schematic, important characteristics, specifications, short-circuit protection, current foldback and current boosting techniques for linear voltage regulators such as 78XX, 79XX, LM317/337 and IC 723 types of linear regulators are discussed in this chapter.

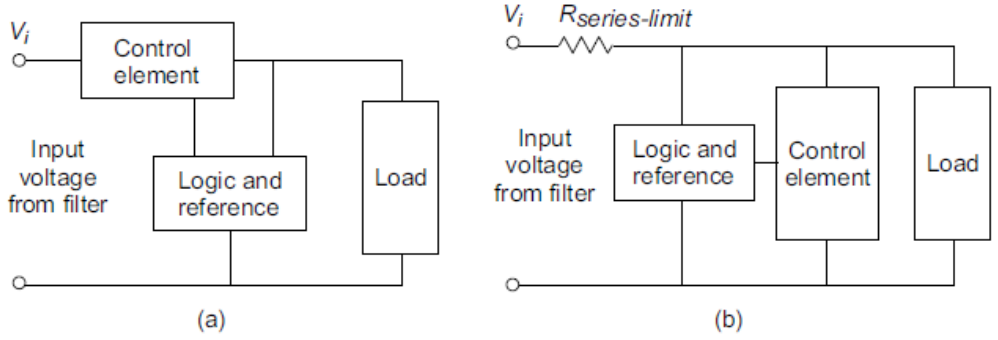


Fig. 8.2 *(a) Block diagram of a series voltage regulator*
(b) Block diagram of a shunt voltage regulator

The switching regulators make use of a power transistor, which acts as a high frequency switch. Therefore, the transistor does not pass current continuously and it results in improved efficiency in regulation. The switching regulators can generate output voltage of opposite polarity, multiple output voltages, or isolated outputs. They can be made to operate directly from the ac power line unlike the linear regulators. The limitations of these regulators are that they need coils, capacitors and complex control circuitry and the operation is noisy. The principle of switching power supply, step-down and step-up switching modes of operation, and switching regulator IC 7840 are also discussed in this chapter.

8.2 BASICS OF VOLTAGE REGULATOR

8.2.1 Linear Mode Power Supply

The basic building blocks of a linear power supply are shown in Fig. 8.3. A transformer supplies ac voltage at the required level. This bidirectional ac voltage is converted into a unidirectional and pulsating dc using a rectifier. The unwanted ripple contents of this pulsating dc are removed by a filter to get a pure dc voltage. The output of the filter is fed to a voltage regulator which gives a steady dc output, independent of load variations and input supply fluctuations.

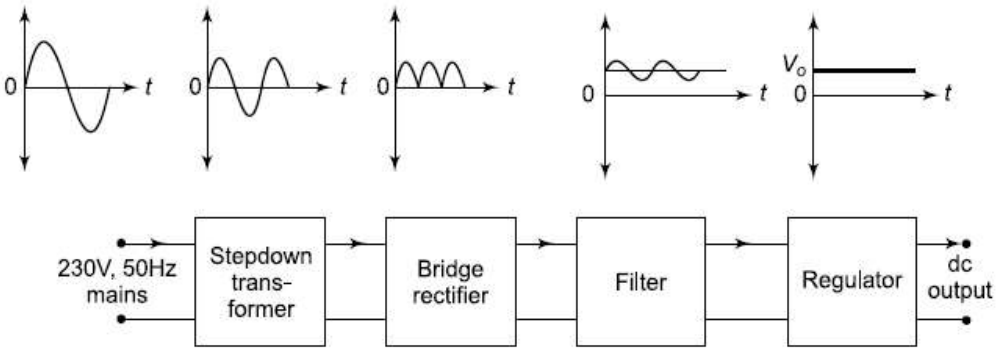


Fig. 8.3 *Basic building blocks of linear mode power supply*

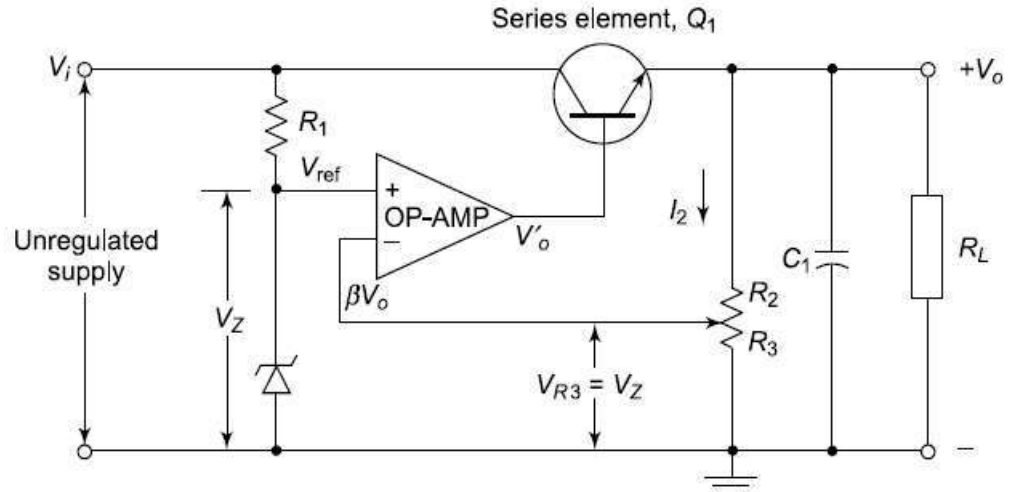
The performance of a voltage regulator is usually defined in terms of the line regulation, load regulation and ripple rejection.

8.3 LINEAR VOLTAGE REGULATORS USING OP-AMPS

If the control element of a voltage regulator operates in its linear region, then the regulator is called a linear voltage regulator. Linear voltage regulators are generally of series mode type. The voltage regulator circuit using Zener diode is vulnerable to the variations in supply voltage since the current through the Zener diode also changes correspondingly. Hence the linear voltage regulator uses an op-amp as an error amplifier, and a pass transistor as a control element. The error output from the op-amp drives the control element, which allows current to the load accordingly and keeps the output voltage constant.

8.3.1 Single Polarity Linear Voltage Regulator using Op-amp

The basic circuit of a linear voltage regulator is shown in Fig. 8.5. The regulating circuit consists of a voltage reference V_{ref}, a differential amplifier called *error amplifier* using op-amp and a series regulating element Q_1 connected as an emitter follower. The output voltage is sampled and fed back to the inverting input of the error amplifier through the potential divider $R_2 - R_3$. The error amplifier produces an output voltage that is proportional to the difference between the reference voltage and the sampled output voltage and it may be written as $V_o' = A\left[V_{ref} - \beta V_o\right]$, where A is the gain of the amplifier and β is the feedback factor which is equal to $R_3/(R_2 + R_3)$. Since the drop across the base-emitter junction of transistor Q_1 is small, the output V_o can be approximated to V_o'.



8.4 IC VOLTAGE REGULATORS

Although voltage regulators can be designed using op-amps, it is quicker and easier to use IC voltage regulators. The IC voltage regulators are versatile, relatively inexpensive and are available with features such as programmable output, current/voltage boosting and floating operation for high voltage application. Some important types of linear IC voltage regulators are:

(i) Fixed positive/negative output voltage regulators

(ii) Adjustable output voltage regulators

Fixed voltage regulators 78XX series are three terminal positive fixed voltage regulators. There are seven voltage regulators with output voltages of 5V, 6V, 8V, 12V, 25V, 18V and 24V. The two digits XX of 78XX are used to identify the fixed output voltage of the regulator.

79XX series are negative fixed voltage regulators which are complements to the 78XX series devices. There are two additional voltage options of –2V and –5.2V available in 79XX series.

The standard circuit connection of the 78XX monolithic voltage regulator is shown in Fig. 8.8. The input capacitor C_i is used to cancel the inductive effects due to long distribution leads and the output capacitor C_o improves the transient response and acts as a ripple filter also.

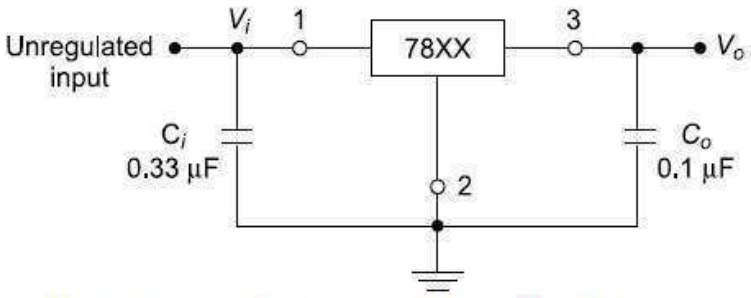


Fig. 8.8 *IC 78XX monolithic voltage regulator*

8.4.2 Dual Voltage Regulator

Figure 8.9 shows a dual voltage regulator. The circuit uses fixed positive (IC 7815) and fixed negative (IC 7915) voltage regulators to provide equal +15 V and −15 V respectively. The dual regulated voltage supplies as required for op-amps can be obtained from this circuit.

The advantage of this method is that it can supply a wide range of voltages at much higher currents with the use of heat sinks and external Metal Can package pass transistor.

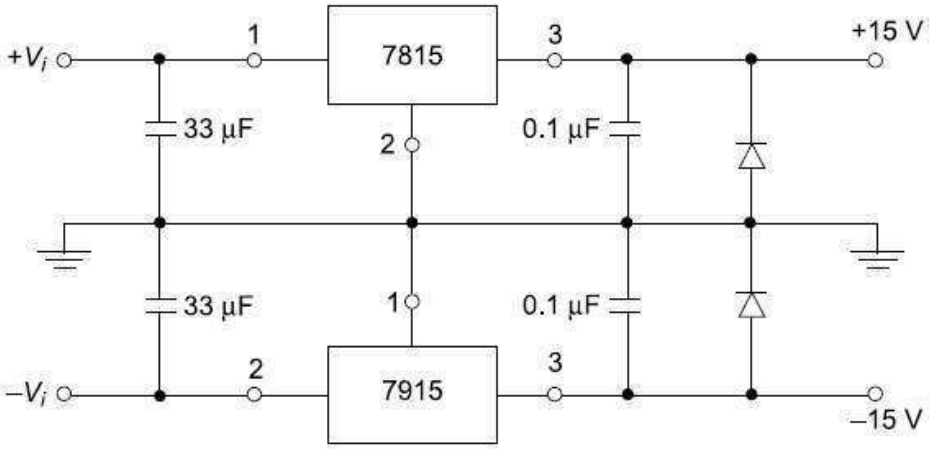


Fig. 8.9 *Dual voltage regulator*

8.4.3 Current Source using 7805 Regulation

The three terminal voltage regulator 7805 can be employed as a current source. This is achieved by connecting a current setting resistor R between the GND and OUT terminals of the regulator IC as shown in Fig. 8.10. Since the voltage at OUT terminal is always constant at 5V, the current through R is also maintained constant. Thus, by the use of KCL,

$$I_L = I_R + I_Q = \frac{5}{R} + I_Q$$

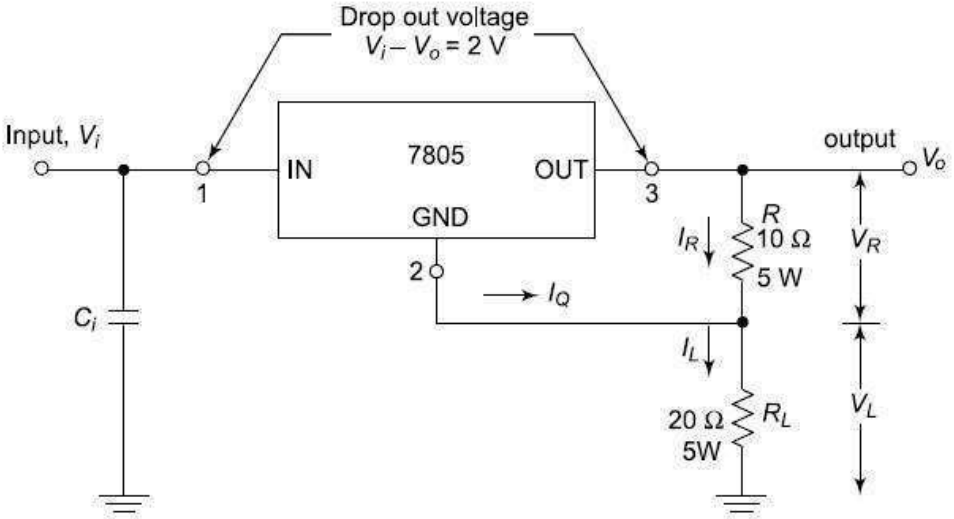


Fig. 8.10 *IC 7805 used as a current source*

8.5.1 LM117/LM317 Adjustable Positive Voltage Regulators

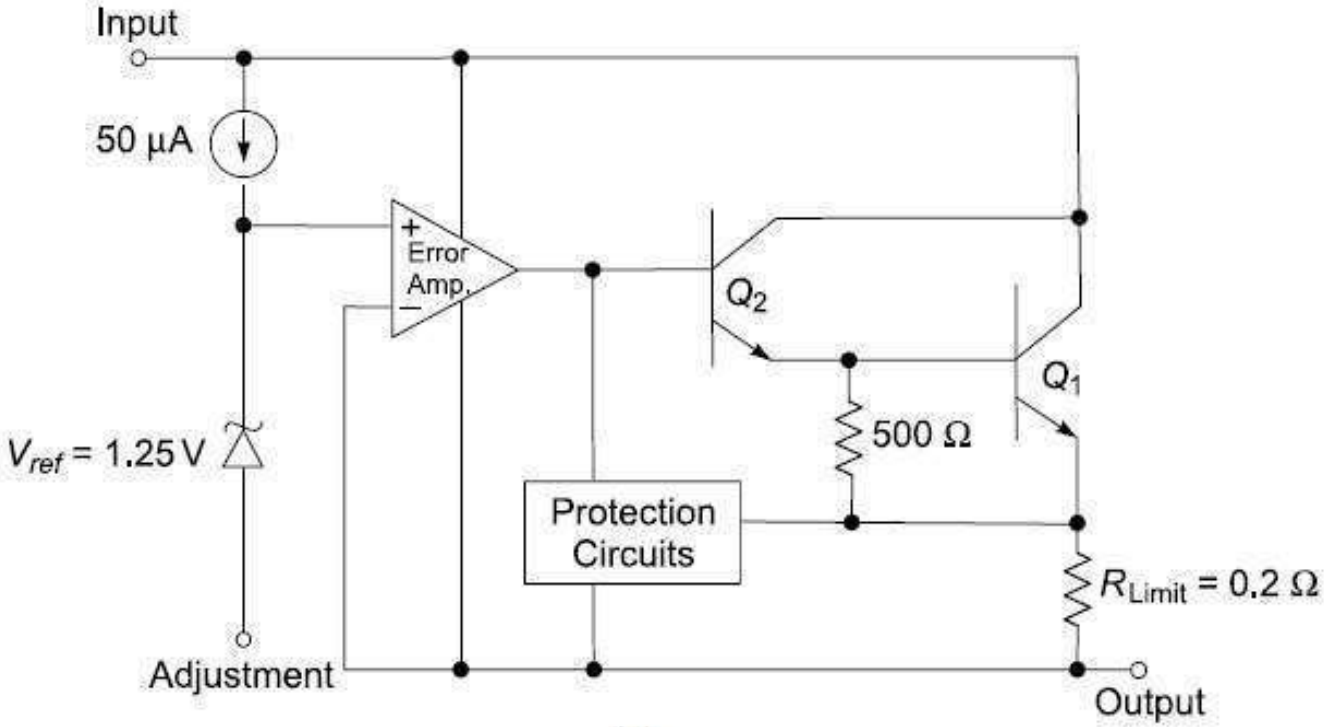
The LM117/LM317 series regulators are adjustable three terminal positive voltage regulators and they are capable of supplying output current of 0.1 A to 1.5A, over a range of 1.2 V to 37 V output voltage range. These regulators are available in standard transistor packages as shown in Table 8.1.

Table 8.1 *Different grades of LM117/ LM317 regulators*

Device	*Available V_o (V)*	*Output Current (A)*	*V_i Max (V)*	*Ripple Rejection (dB)*	*Package Type*
LM317	1.2 to 37	1.5	40	80	TO-39
LM317H	1.2 to 37	0.5	40	80	TO-39
LM317HV	1.2 to 37	1.5	60	80	TO-3
LM317HVH	1.2 to 37	0.50	40	80	TO-39
LM317L	1.2 to 37	0.10	40	65	TO-92
LM317M	1.2 to 37	0.50	40	80	TO-202

The important specifications of LM117/LM337 are given below:

Power dissipation (based on the package)	-	0.6W to 20W
Adjustable output voltage	-	1.2V to 37V
Line regulation	-	0.01% / V (Typ.)
Load regulation	-	0.1% (Typ.)
Standard 3-lead Transistor packages	-	TO-3, TO-39, TO-200, TO-202 and TO-92
Ripple rejection	-	80dB



(a)

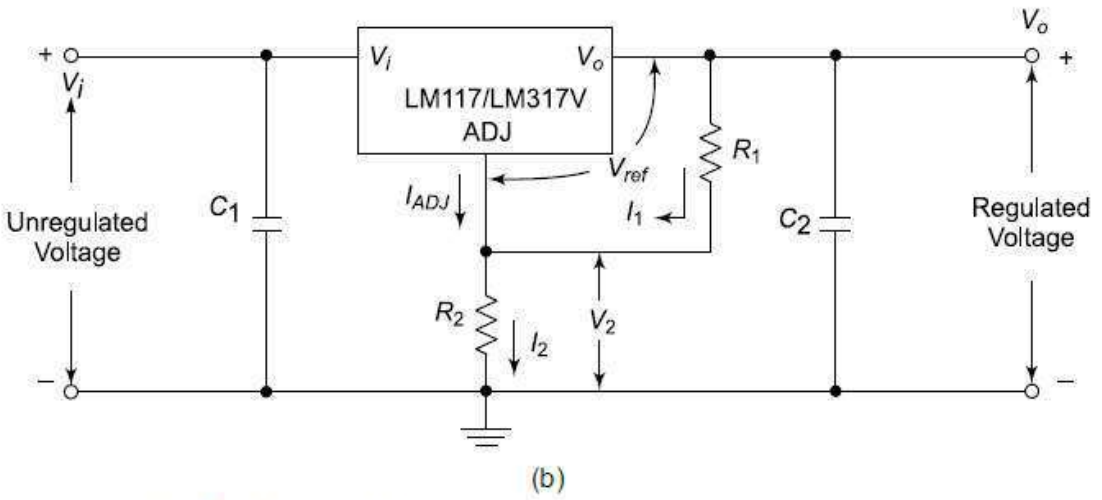


Fig. 8.12 *(a) LM317 voltage regulator functional diagram*
(b) Circuit connection for LM317 regulator

This current also flows through R_2 and an additional current of I_{ADJ} flows out of the adjustment terminal of the regulator through R_2. Thus the net current through R_2 is $I_2 = I_1 + I_{ADJ}$.

The voltage across R_2 is $V_2 = I_2 R_2 = (I_1 + I_{ADJ}) R_2$.

The net output voltage V_o is then given by

$$V_o = V_{ref} + V_2 = V_{ref} + R_2 (I_1 + I_{ADJ}) \tag{8.6}$$

Substituting $I_1 = \dfrac{V_{ref}}{R_1}$ in the above equation,

$$V_o = V_{ref} \left(1 + \frac{R_2}{R_1}\right) + I_{ADJ} R_2 \tag{8.7}$$

The last term $I_{ADJ} R_2$ indicates an error term of a typical value of 50 μA, and when R_2 is low, this term can be neglected.

Then,

$$V_o = 1.25 \left(1 + \frac{R_2}{R_1}\right) \tag{8.8}$$

Hence, the output voltage V_o is a function of R_2 for a specific value of R_1, which is normally 240 Ω. The resistor R_1 is to be connected directly to the regulator output.

Protection diodes can be connected to the regulator circuit as shown in Fig. 8.13, when output capacitors of value greater than 25 μF are used. The diode D_1 prevents the capacitors from discharging into the regulator.

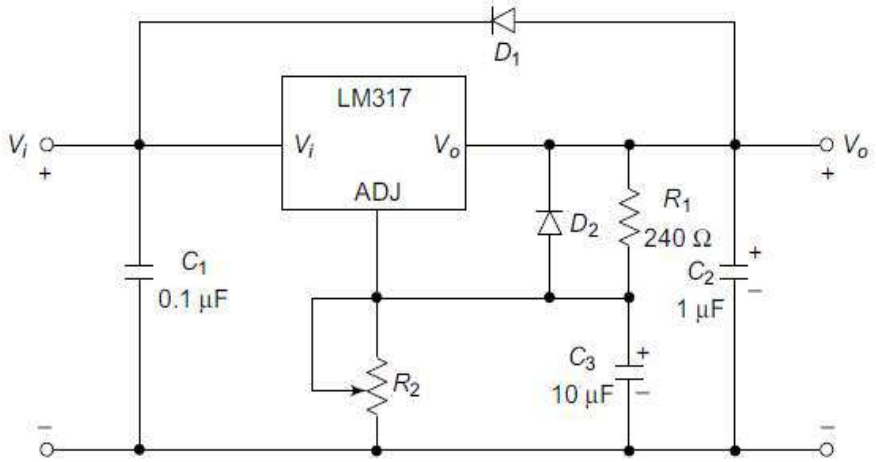


Figure 8.14 shows the circuit arrangement of an adjustable positive voltage regulator using LM317. The operation of the circuit is explained in Example 8.5.

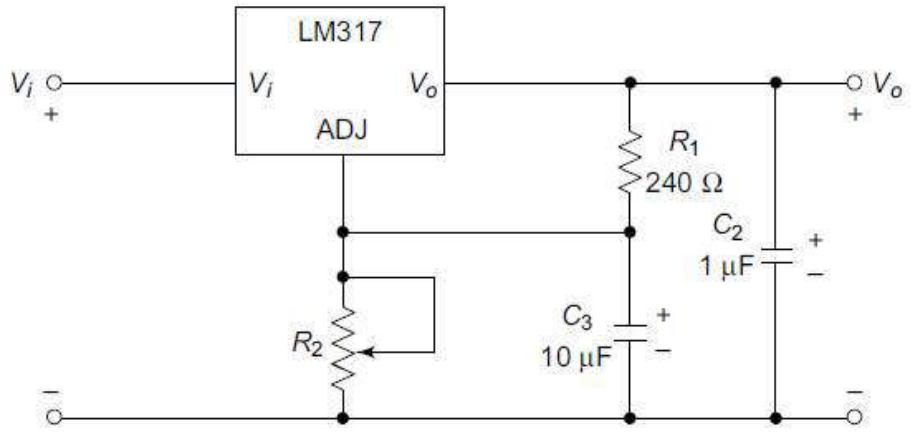


Fig 8.14 *LM317 adjustable positive voltage regulator*

Example 8.4

An LM317 regulator shown in Fig. 8.14 has $R_1 = 240\ \Omega$ and $R_2 = 2k\ \Omega$. If $I_{ADJ} = 50\ \mu A$ and $V_{ref} = 1.25\,V$, find the value of V_o.

Solution

$$V_o = V_{ref}\left(1+\frac{R_2}{R_1}\right) + I_{ADJ}\,R_2$$

$$= 1.25\left(1+\frac{2000}{240}\right) + 50\times10^{-6}\times2\times10^{3} = 11.77\ \text{V}$$

Example 8.5

Referring to Fig. 8.14, design an adjustable positive voltage regulator using LM317 for an output voltage V_o varying from 4 to 12 V and an output current I_o of 1A.

Solution

Maximum I_{ADJ} for LM317 = 100 μA

Assume a typical value of $R_1 = 240\ \Omega$. Here, $V_{ref} = 1.25$ V

We know that $V_o = V_{ref}\left(1+\frac{R_2}{R_1}\right) + I_{ADJ}R_2$

For the output voltage $V_o = 4$ V,

$$4 = 1.25\left(1+\frac{R_2}{240}\right) + 100\times10^{-6}\times R_2$$

$$R_2 = 0.52\ \text{k}\Omega$$

Similarly, for $V_o = 12$ V,

$$12 = 1.25\left(1+\frac{R_2}{240}\right) + 100\times10^{-6}\times R_2$$

$$R_2 = \frac{10.75}{5.3\times10^{-3}} = 2.01\ \text{k}\Omega$$

8.5.2 LM137/LM337 Adjustable Negative Voltage Regulators

The LM137/LM337 series of adjustable three terminal negative voltage regulators are available for the corresponding types of LM117/LM317 positive voltage regulators. The circuit arrangement of LM337 connected for negative variable voltage regulation is shown in Fig. 8.16. Note that R_1 is of value 120 Ω and maximum input voltage which can be fed to V_i terminal is 50 V as against 60 V for LM317. The output voltage V_o is given by

$$V_o = 1.2\left(1 + \frac{R_2}{R_1}\right) = 1.2\left(1 + \frac{R_2}{120}\right)$$

$$V_o = 1.2\ \text{V} + 10\,\text{mA} \times R_2$$

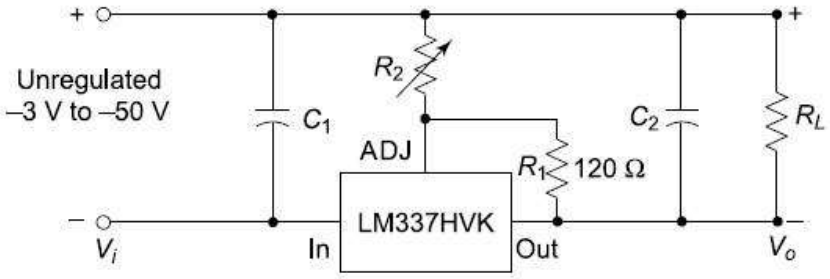


Fig. 8.16 *LM337 adjustable negative voltage regulator*

Table 8.2 shows the package types and grades of LM337 regulators. Figure 8.17 shows the schematic symbols and package types of the negative voltage regulators. The three terminals are input terminal V_i, output terminal V_o and adjustment terminal (ADJ).

8.6 IC 723 GENERAL PURPOSE REGULATOR

The three-terminal regulators such as 7805, 7815, 7905, 7915, etc. are capable of producing only fixed positive, or negative output voltages. Moreover, such regulators do not have short circuit protection. Therefore, these three terminal regulators evolved into dual polarity variable voltage regulators. They have provision for regulating positive and negative voltage inputs. The evolution further led to the monolithic linear voltage regulators and monolithic switching regulators. The monolithic linear voltage regulator type IC 723 is discussed in this section.

The IC 723 general purpose regulator overcomes the limitations of three terminal fixed voltage regulators. The IC 723 is a low current device, and can be employed for providing a load current up to 10 A or more by the addition of external transistors.

The functional block diagram of IC 723 is shown in Fig. 8.21 (a). Figures 8.21 (b) and (c) show the pin diagrams for a 14-pin DIP and 10-pin Metal Can packages for the device. The Zener diode, the constant current source and reference amplifier form one section of the IC. The constant current source helps in maintaining a fixed output voltage from Zener diode D_2. The error amplifier, series pass element Q_1 and current limit transistor Q_2 form the second section. The error amplifier compares the input voltages applied at non-inverting (NI) and inverting (INV) input terminals. The error signal obtainable at the output of error amplifier drives the series pass element Q_1.

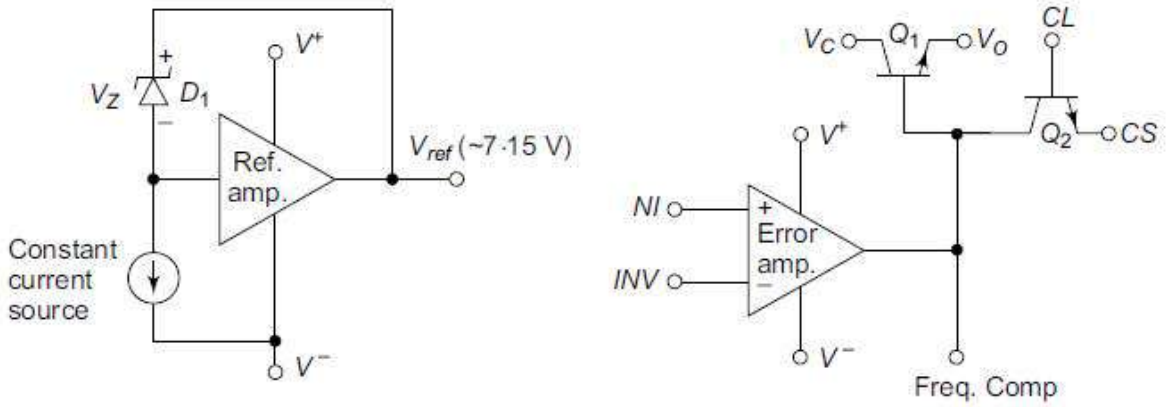
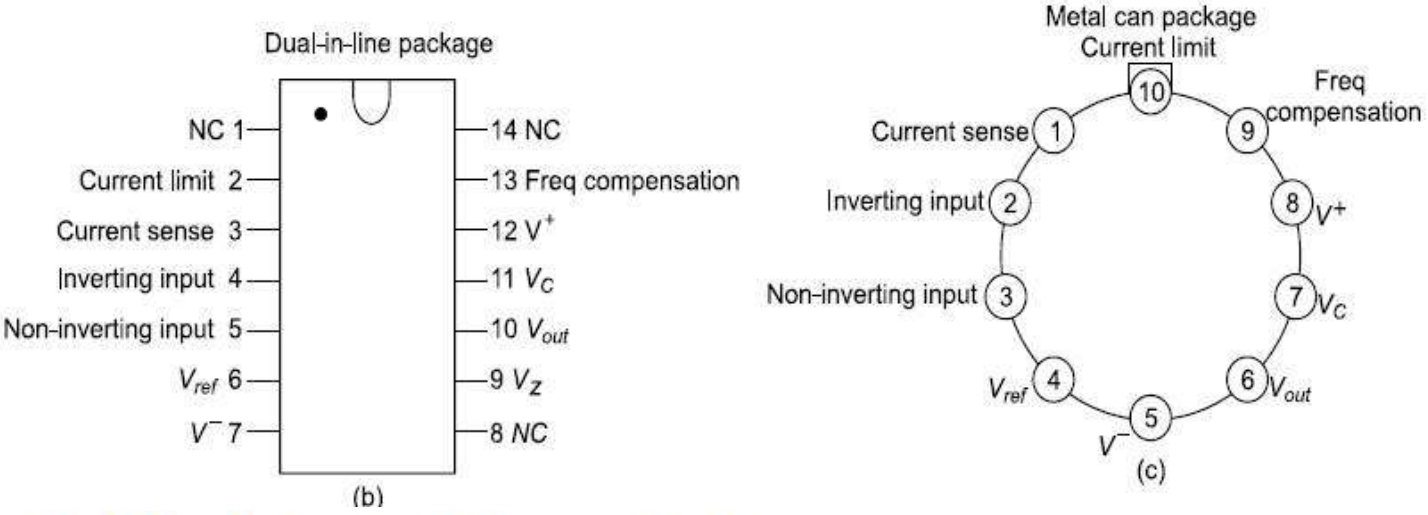


Fig. 8.21 *(a) Functional block diagram of IC 723*



8.6.1 Low Voltage Regulator using IC 723

Figure 8.22 shows the functional block diagram for a low voltage regulator using IC 723. This circuit arrangement is used for regulating voltages ranging from 2V to 7V, and hence it is called a low voltage regulator. The output voltage is directly fed back to the INV input terminal. The non-inverting input (NI) is obtained across the potential divider formed by resistor R_1 and R_2. Hence, voltage at NI terminal is given by

$$V_{NI} = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

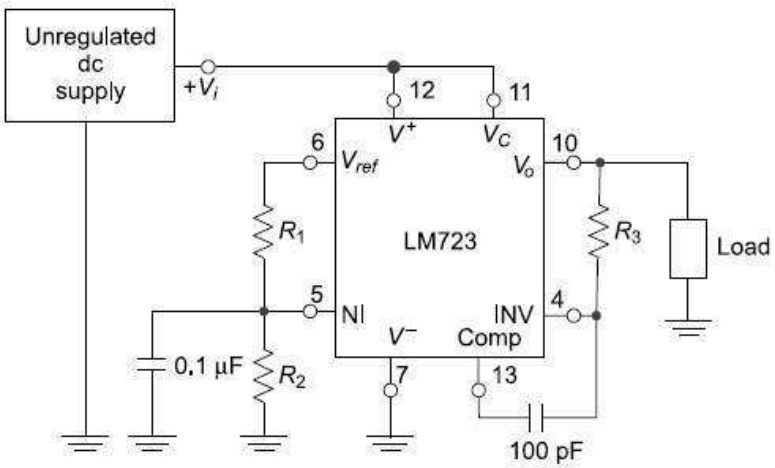


Fig. 8.22 *Functional block diagram of a low voltage regulator using IC 723*

The error amplifier amplifies the difference and it drives the pass transistor Q_1. Depending on the error signal, the pass transistor Q_1, acting as control element, minimises the difference between the NI and INV inputs of error amplifier. Therefore, the output voltage V_o is given by

$$V_o = V_{ref} \times \frac{R_2}{R_1 + R_2} = 7.15 \times \frac{R_2}{R_1 + R_2}.$$

8.6.2 High Voltage Regulator Circuit using IC 723

The IC 723 can be used for designing a high voltage regulator for output voltages ranging from 7V to 37V. The circuit connection diagram is shown in Fig. 8.23. The non-inverting input (NI) terminal is directly connected to V_{ref} through R_3. The inverting input (INV) terminal is connected to the junction of resistors R_1 and R_2 connected with the output V_o. The resistor R_3 is selected to be equal to $R_1 \parallel R_2$. Then the error amplifier acts as a noninverting amplifier with a voltage gain of $A_V = 1 + \dfrac{R_1}{R_2}$.

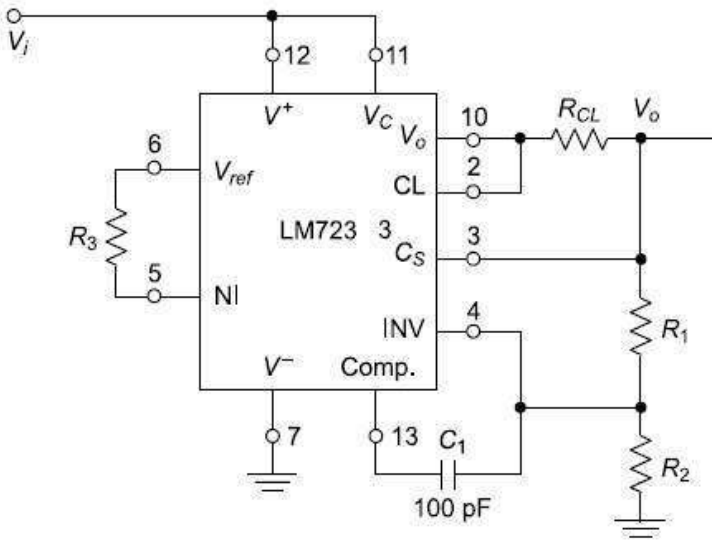


Fig. 8.23 *Functional block diagram of a high voltage regulator using IC 723*

Therefore, the output voltage for the circuit is

$$V_o = V_{ref}\left(1 + \frac{R_1}{R_2}\right) = 7.15\left(1 + \frac{R_1}{R_2}\right)$$

8.6.3 Current Limit Protection

The limitation of the regulator IC 723 is that it has no built-in thermal protection and short circuit protection. Therefore, the current limit protection in regulator ICs is necessary for providing protection against short circuit condition across the load. The low-pass and high-pass regulator circuits discussed in the previous sections have no in-built current limit protection circuit.

An active current limiting circuit for IC 723 is shown in Fig. 8.24(a). This circuit prevents the load current from increasing beyond a safe value. The operation of the circuit can be explained as follows. The series pass element Q_1, which is part of the regulator circuit, is shown connected in series with a current limiting resistor R_{CL}. The voltage drop across the resistance R_{CL} can bias the transistor Q_2 and turn it ON. Assume that the circuit can supply a maximum current of $I_{L(max)}$. The output voltage remains constant for any value of I_{CL} up to the maximum current $I_{CL(\max)}$. In such normal load conditions, the voltage V_{CL} across the resistor R_{CL} (i.e., $V_{CL} = I_{CL} \times R_{CL}$) is insufficient to turn transistor Q_2 ON. Therefore, Q_1 supplies the current demanded by the load conditions at the fixed output voltage V_L. Now, consider that the load current I_L increases. This leads to more current through R_{CL}, and the voltage drop V_{CL} increases too. This turns the transistor Q_2 ON. Hence, any current, which is in excess of $I_{L(max)}$ is diverted away from the base of Q_1. This effectively reduces the emitter current of Q_1, and thus the load current reduces. Similarly, when the load current reduces, the drop across R_{CL} drops, turning Q_2 OFF and allowing Q_1 to pass I_L.

The curve shown in Fig. 8.24(b) shows the output characteristics of series-pass voltage regulator using such a simple current limiting method. The transistor Q_2 supplies an additional small amount of current to the load when the current limiting takes place.

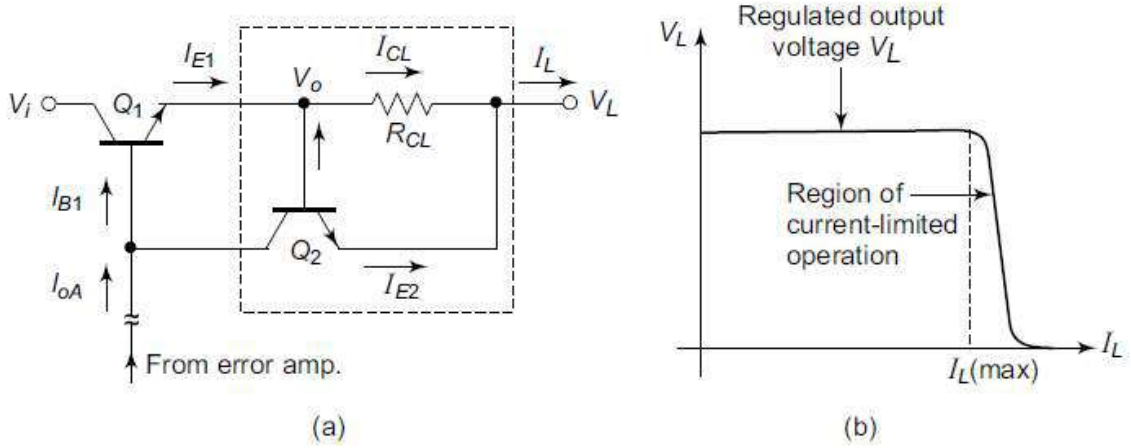
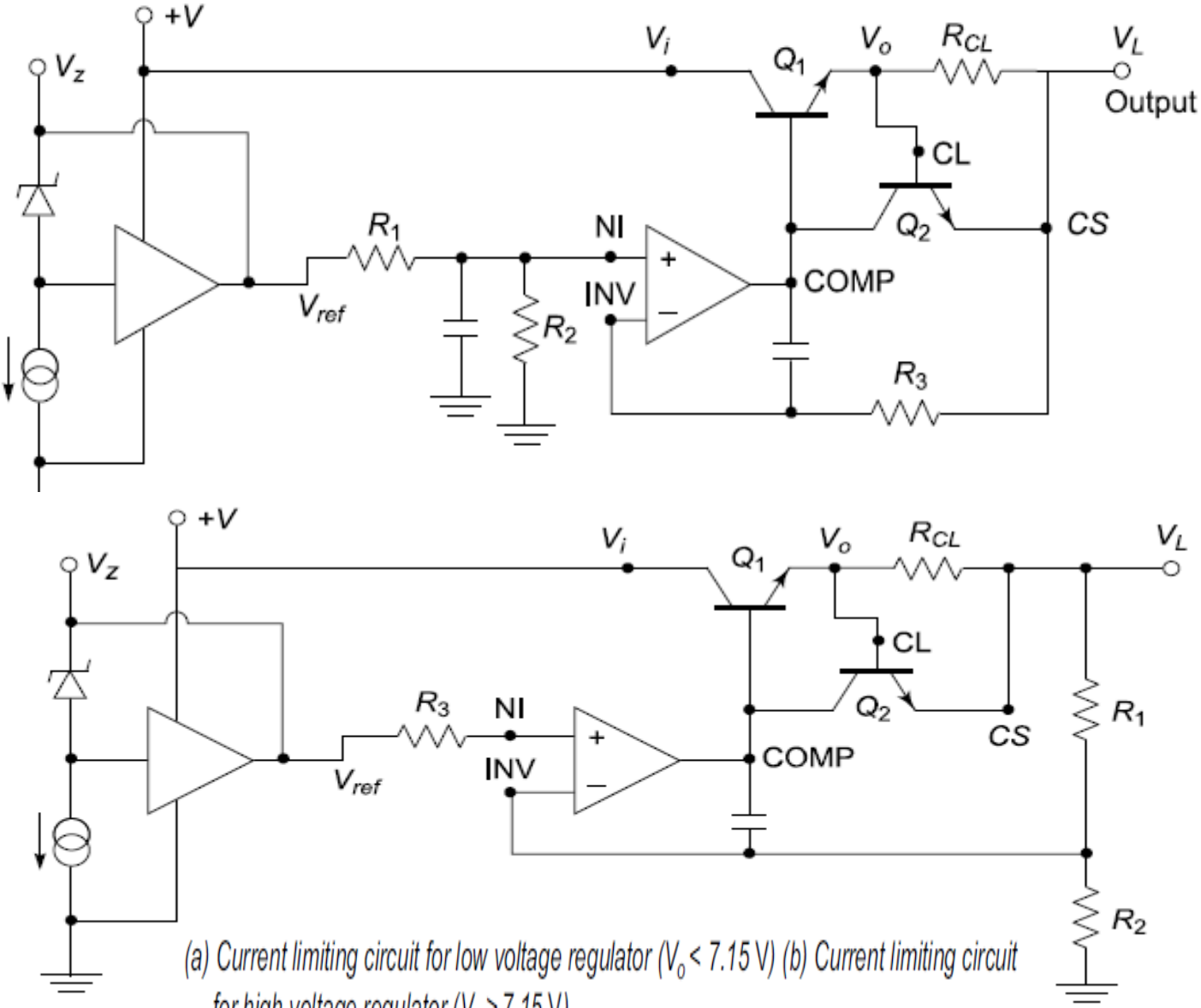


Fig. 8.24 *(a) Current limiting circuit (b) Its output characteristics*

Figures 8.25 (a) and (b) show the two basic configurations of IC 723 for low voltage and high voltage regulations with current limiting capability. The power dissipation P_D in the regulator IC mainly occurs in the transistor Q_2 and thus,



(a) Current limiting circuit for low voltage regulator (V_o < 7.15 V) (b) Current limiting circuit for high voltage regulator (V_o > 7.15 V)

8.6.4 Foldback Current Limiting

In the simple current limiting circuit discussed earlier, the maximum current limit was preset such that the power P_D will never be more than the value set by $P_D = V_L I_{L(max)}$ and the resistance R_{CL} was accordingly chosen. The net effect is that the regulator is under-utilised. In such conditions, the current foldback method provides full protection to the device, in addition to allowing higher currents to the load.

Figure 8.26(a) shows the foldback current limiting characteristics in comparison with the linear foldback method of Fig 8.24(b). The foldback current limiting method reduces both the output current and voltage when $I_{L(max)}$ is reached.

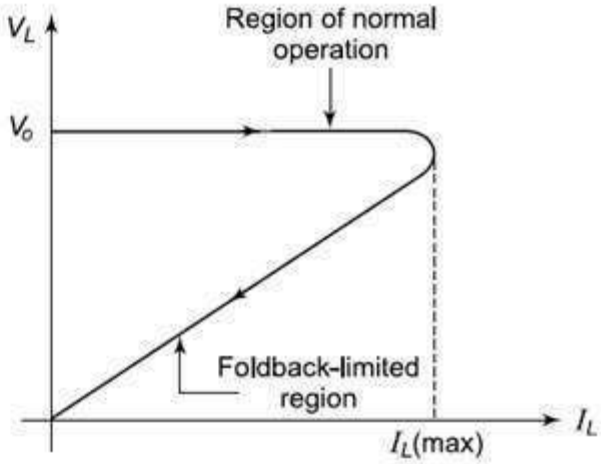


Fig. 8.26 *(a) Foldback current limit characteristics*

The foldback current limiting circuit is shown in Fig. 8.26(b). This method of over-current protection is employed to reduce both the output load current and voltage, when the load resistance becomes smaller than what would draw a specified maximum current of $I_{L(max)}$. In the current limit protected regulator, as $I_{L(max)}$ is exceeded, the output voltage of the regulator decreases. On the other hand, in foldback current limiting, as load resistance decreases beyond a certain minimum value, both load voltage and load current decrease, and when the load becomes a short circuit, they approach zero.

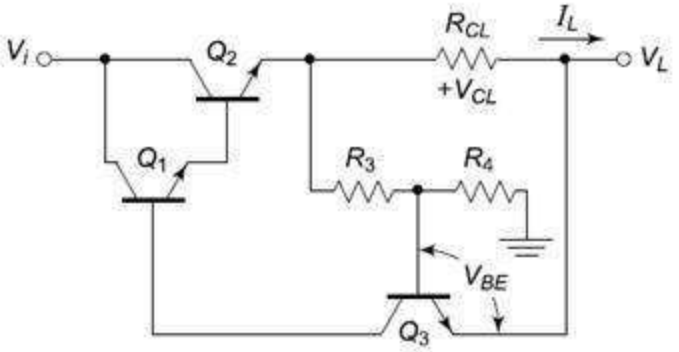


Fig. 8.26 *(b) Foldback current limiting circuit*

The important advantages of foldback method of current limiting are (a) protecting the load from the over-current operation and (b) protecting the regulator itself. The base of Q_3 is connected to the voltage divider formed by R_3 and R_4. Applying Kirchhoff's voltage law around the loop, we get

$$V_{BE} = V_{CL} - V_{R3}$$

The current limit transistor Q_3 starts conducting only when its base to emitter voltage V_{BE} is approximately 0.7 V, that is, V_{CL} must become sufficiently large to exceed the drop across R_3 by a minimum of 0.7 V.

That is,

$$0.7 = V_{BE} = V_{CL} - V_{R3}$$

At this point, current limit starts occurring. As the load resistance decreases, the load voltage drops, and V_{R3} also reduces. As a consequence, a smaller value of V_{CL} is then required to maintain V_{BE} of Q_3 at 0.7 V. Then, as transistor Q_3 starts conducting, transistor Q_1 starts to turn OFF, and the load current decreases. The drop across R_3 further reduces, increasing the conduction of Q_3 and reducing the conduction of Q_1. The load current I_L further reduces. This process continues until V_o becomes 0 V and load current becomes a minimum. If the load resistance is brought to its nominal operating value, the circuit resumes its normal regulation action.

8.6.5 High Current Low Voltage Regulator

The maximum current obtainable from IC 723 is 140 mA. For applications requiring higher current values, boost pass transistor Q_1 can be added to the regulator as shown in Fig. 8.27. The collector of Q_1 is connected to unregulated dc supply. The output terminal V_o of regulator drives the base of Q_1. Therefore, $I_o = \beta_{\text{Boost transistor}} \times I_{o(723)}$. A Darlington connected transistor pair can also be used in place of Q_1 as the pass transistor for obtaining much higher values of load currents.

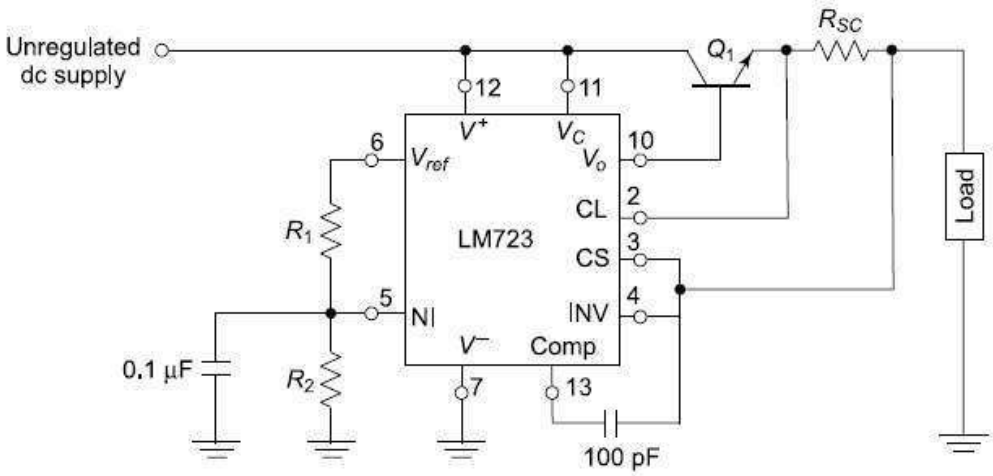


Fig. 8.27 *Low voltage regulator circuit with current boosting*

Design a continuously adjustable power supply for the range of 2 V to 5 V with a current limit of 1A using IC LM723.

Solution The adjustable voltage regulator for high current is shown in Fig. 8.25. The output voltage is given by

In order to produce a 1A load current, an external pass transistor Q_1 is employed. To obtain the desired voltage adjustment, resistor R_1 is replaced with a series potentiometer/resistor combination (R_{1a}, R_{1b}) as shown in Fig. 8.28. Here, the minimum and the maximum values of R_1 will be R_{1b} and $(R_{1a} + R_{1b})$ respectively. Then the three resistors are in series and act as a potential divider. Therefore,

$$\frac{R_1 + R_2}{R_2} = \frac{V_{ref}}{V_o}$$

For the maximum voltage of 5V, we have

$$\frac{R_{1b} + R_2}{R_2} = \frac{V_{ref}}{V_o} = \frac{7.15}{5} = 1.43$$

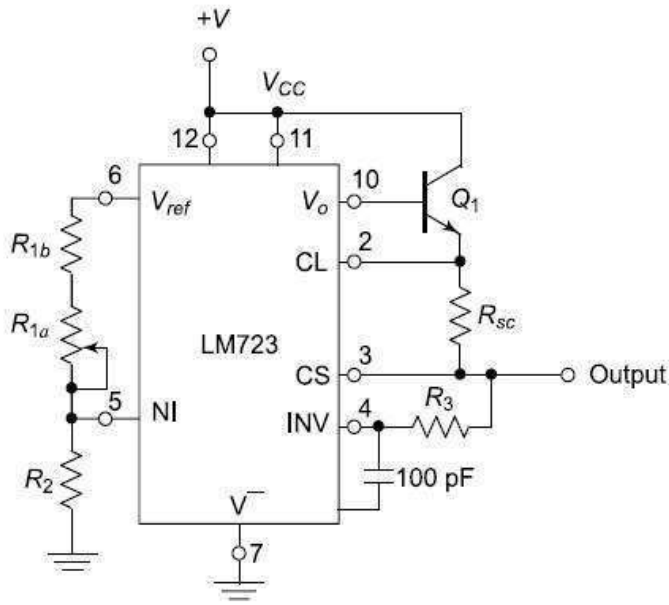


Fig. 8.28 *Adjustable voltage regulator using LM723*

Therefore, $R_{1b} = 0.43\,R_2$

For the minimum voltage of 2V, we have

$$= \frac{R_{1a} + R_{1b} + R_2}{R_2} = \frac{V_{ref}}{V_o} = \frac{7.15}{2} = 3.575$$

Substituting $R_{1b} = 0.43\,R_2$ in the above equation, we get

$$R_{1a} = 2.145\,R_2$$

Choosing a standard value of 10 kΩ for R_{1a},

$$R_2 = \frac{R_{1a}}{2.145} = \frac{10 \times 10^3}{2.145} = 4.66\,\text{k}\Omega$$

Similarly, $R_{1b} = 0.43\,R_2 = 0.43 \times 4.66 \times 10^3 = 2\,\text{k}\Omega$

For choosing a suitable current sense resistor R_{sc},

$$I_{limit} = \frac{V_{sense}}{R_{sc}}$$

$$R_{sc} = \frac{V_{sense}}{I_{limit}} = 0.65\Omega$$

For minimum temperature drift, R_3 is included as given by

$$R_3 = R_1 \,||\, R_2 = 6\,\text{k}\Omega \,||\, 4.66\,\text{k}\Omega = 2.62\,\text{k}\Omega$$

8.7 SWITCHED MODE POWER SUPPLIES (SMPS)

The linear voltage regulators have the following limitations:

(i) The step-down transformer used in the power supply circuit is bulky and it is the most expensive component of the circuit.
(ii) Large values of filter capacitors are required to eliminate ripples, due to the low line frequency (50 Hz) of operation.
(iii) The efficiency of series regulator is normally less than 50%.
(iv) The input voltage must be always more than the required output regulated voltage.
(v) The difference between the input and output voltage drops across the linear pass transistor and dissipates power.

The switched mode regulators overcome these limitations. They operate on the principle of chopping the unregulated dc supply voltage by the use of a transistor switch and filtering the high frequency components using a high frequency filter. Thus, the output voltage is regulated by varying the duty cycle or the switching period of the transistor.

Figure 8.1(b) of Section 8.1 depicted the operating principle of a practical switching regulator in its simplest form. The elements added in addition to the components of an unregulated power supply circuit are the control logic and the oscillator circuits. The oscillator allows the control element to be switched ON and OFF. The control element usually consists of a transistor switch, an inductor and a diode as shown in Fig. 8.29. For each switching ON at the base of the transistor, energy is pumped into the magnetic field associated with the inductor which is a transformer winding in practice. This energy is then released to the load at the desired voltage level. By varying the duty cycle or frequency of switching, one can vary the stored energy in each cycle and thus control the output voltage. As a switch can only be ON or OFF, it either allows energy to *pass* or *stop*, but does not itself dissipate energy. Since only the energy required to maintain the output voltage at a particular load current is drawn, there is no dissipation and hence, a higher efficiency is obtained. Energy is pumped in discrete lumps, but the output voltage is kept constant by capacitor storage.

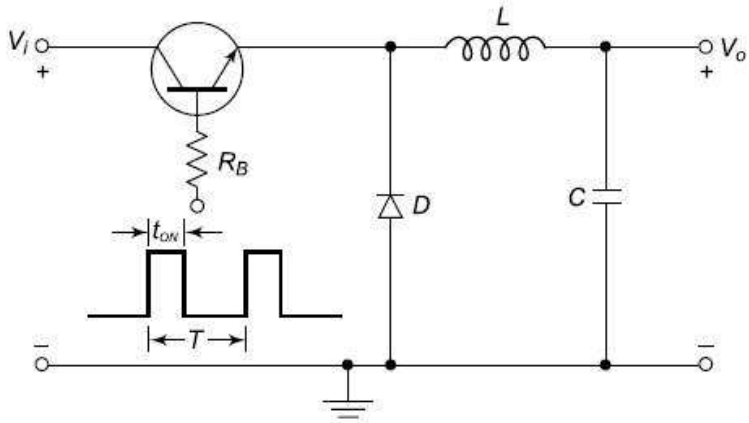


Fig. 8.29 *Principle of a switching regulator*

The major feature of SMPS is the elimination of physically massive power transformers and other power line magnetics. The net result is a smaller, lighter package and reduced manufacturing cost, resulting primarily from the elimination of the 50 Hz line frequency components.

However, the switching regulators suffer from the disadvantages as given below:

(i) In a switching regulator, noise is high on both ac input and output lines due to switching at high frequencies. As a result, heavy filtering is required.
(ii) Since the transient response is limited, switching regulator is normally slower than linear voltage regulator.
(iii) Switching regulator is more complex compared to a linear regulator.

Due to these limitations, the switching regulators are used for high power levels of around 100 W.

8.7.1 Transformer based Switching Regulator

The block diagram of transformer based switching regulator is shown in Fig. 8.30(a). Here, the primary power received from the ac main is rectified and filtered as high voltage dc. It is then switched at a high speed of approximately 15 kHz to 50 kHz and fed to the primary side of a step-down transformer. The step-down transformer is only a fraction of the size of a comparable 50 Hz unit thus relieving the size and weight problems. The output from the secondary side of the transformer is rectified and filtered. Then, it is sent as the output of the power supply. A sample of this output is sent back to the switch to control the output voltage.

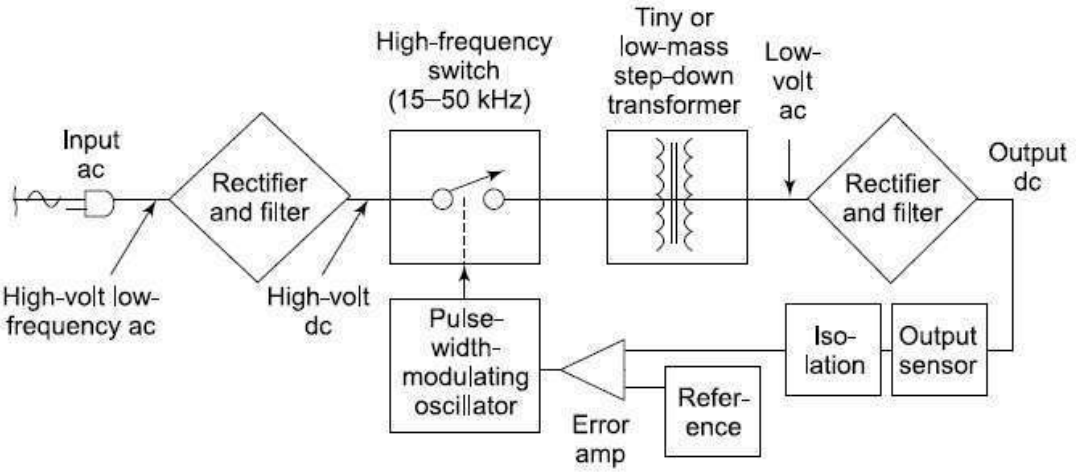
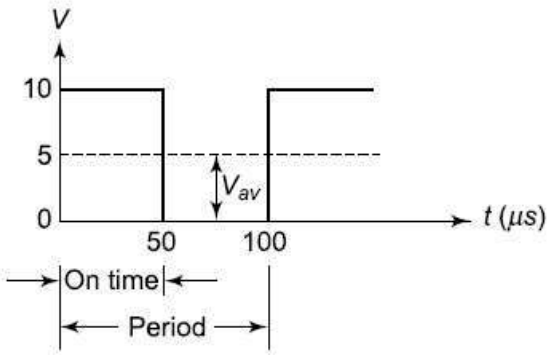


Fig. 8.30 *(a) Block diagram of switching power supply*

SMPS rely on PWM to control the average value of the output voltage. The average value of the respective pulse waveform depends on the area under the waveform. If the duty cycle is varied as illustrated in Fig. 8.30(b), then the average value of the voltage changes proportionally.

As the load increases, the output voltage tends to fall. Most switching power supplies regulate their output using a method called *pulse-width modulation* (PWM). The power switch which feeds the primary side of the step-down transformer is driven by a pulse-width modulated oscillator. When the duty cycle is 50%, the maximum amount of energy will be passed through the step-down transformer. As the duty cycle is decreased, less energy will be passed through the transformer.



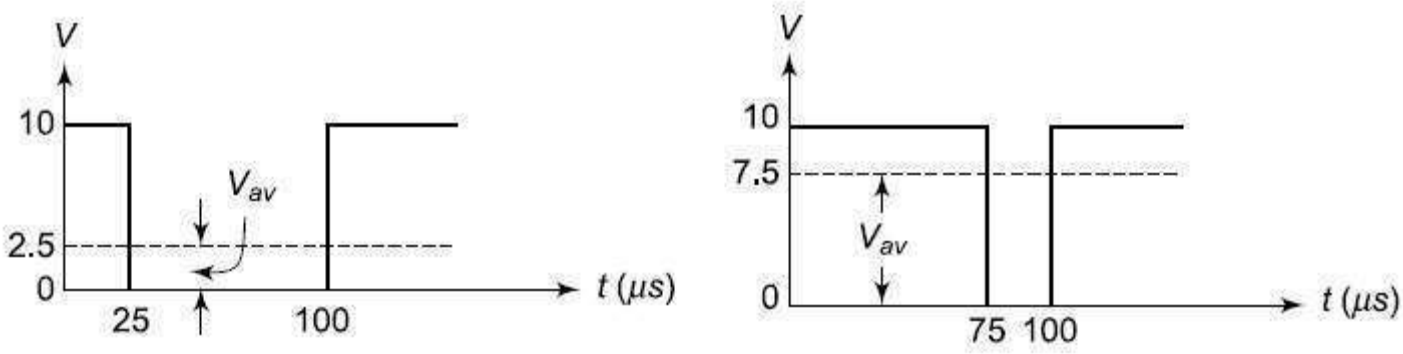


Fig. 8.30 *(b) Pulse width modulation and average value*

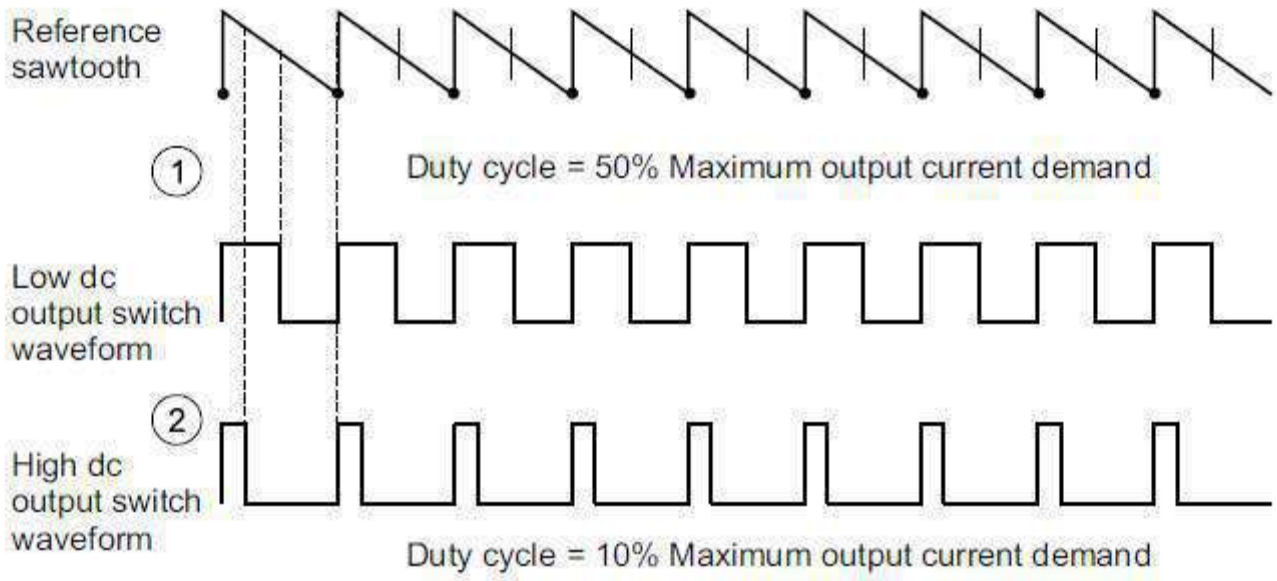
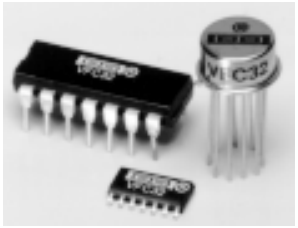


Fig. 8.30 *(c) Switching power supply waveforms*

The width or ON time of the oscillator is controlled by the voltage fed back from the secondary rectifier output forming a closed loop regulator. As shown in Fig. 8.30(c), the pulse width applied to the power switch is inversely proportional to the output voltage. When the output voltage drops, the switch is ON for a longer time, resulting in more energy delivered to the transformer and a higher output voltage. As the output voltage increases, the ON time becomes shorter until the loop stabilises.

BURR - BROWN®



VFC32

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- OPERATION UP TO 500kHz
- EXCELLENT LINEARITY
  ±0.01% max at 10kHz FS
  ±0.05% max at 100kHz FS
- V/F OR F/V CONVERSION
- MONOTONIC
- VOLTAGE OR CURRENT INPUT

APPLICATIONS

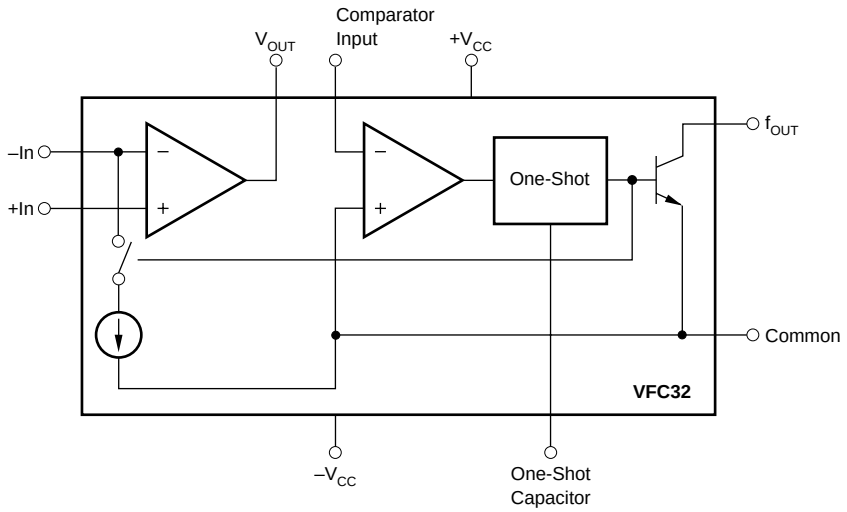
- INTEGRATING A/D CONVERTER
- SERIAL FREQUENCY OUTPUT
- ISOLATED DATA TRANSMISSION
- FM ANALOG SIGNAL MOD/DEMOD
- MOTOR SPEED CONTROL
- TACHOMETER

DESCRIPTION

The VFC32 voltage-to-frequency converter provides an output frequency accurately proportional to its input voltage. The digital open-collector frequency output is compatible with all common logic families. Its integrating input characteristics give the VFC32 excellent noise immunity and low nonlinearity.

Full-scale output frequency is determined by an external capacitor and resistor and can be scaled over a wide range. The VFC32 can also be configured as a frequency-to-voltage converter.

The VFC32 is available in 14-pin plastic DIP, SO-14 surface-mount, and metal TO-100 packages. Commercial, industrial, and military temperature range models are available.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-372G
Printed in U.S.A. October, 1998
SBVS015

SPECIFICATIONS

At T_A = +25°C and V_{CC} = ±15V, unless otherwise noted.

PARAMETER	CONDITIONS	VFC32KP, KU MIN	VFC32KP, KU TYP	VFC32KP, KU MAX	VFC32BM MIN	VFC32BM TYP	VFC32BM MAX	VFC32SM MIN	VFC32SM TYP	VFC32SM MAX	UNITS
INPUT (V/F CONVERTER) $F_{OUT} = V_{IN}/7.5\ R_1\ C_1$											
Voltage Range[1]											
Positive Input		>0		+0.25mA x R_1	✻		✻	✻		✻	V
Negative Input		>0		–10	✻		✻	✻		✻	V
Current Range[1]		>0		+0.25	✻		✻	✻		✻	mA
Bias Current											
Inverting Input			20	100		✻	✻		✻	✻	nA
Noninverting Input			100	250		✻	✻		✻	✻	nA
Offset Voltage[2]			1	4		✻	✻		✻	✻	mV
Differential Impedance		300 || 10	650 || 10		✻	✻		✻	✻		kΩ || pF
Common-mode Impedance		300 || 3	500 || 3		✻	✻		✻	✻		MΩ || pF
INPUT (F/V CONVERTER) $V_{OUT} = 7.5\ R_1\ C_1\ F_{IN}$											
Impedance		50 || 10	150 || 10		✻	✻		✻	✻		kΩ || pF
Logic “1”			+1.0		✻		✻	✻		✻	V
Logic “0”			–0.05		✻		✻	✻		✻	V
Pulse-width Range		0.1		150k/F_{MAX}	✻		✻	✻		✻	µs
ACCURACY											
Linearity Error[3]	0.01Hz ≤ Oper Freq ≤ 10kHz		±0.005	±0.010[4]		✻	✻		✻	✻	% of FSR[5]
	0.1Hz ≤ Oper Freq ≤ 100kHz		±0.025	±0.05		✻	✻		✻	✻	% of FSR
	0.5Hz ≤ Oper Freq ≤ 500kHz		±0.05			✻			✻		% of FSR
Offset Error Input											
Offset Votlage[2]			1	4		✻	✻		✻	✻	mV
Offset Drift[6]			±3			✻			✻		ppm of FSR/°C
Gain Error[2]			5			✻			✻		% of FSR
Gain Drift[6]	f = 10kHz		±75			±50	±100		±70	±150	ppm/°C
Full Scale Drift (offset drift and gain drift)[6, 7]	f = 10kHz		±75			±50	±100		±70	±150	ppm of FSR/°C
Power Supply Sensitivity	f = DC, ±V_{CC} = 12VDC to 18VDC			±0.015			✻			✻	% of FSR/%
OUTPUT (V/F CONVERTER) (open collector output)											
Voltage, Logic “0”	I_{SINK} = 8mA	0	0.2	0.4	✻	✻	✻	✻	✻	✻	V
Leakage Current, Logic “1”	V_O = 15V		0.01	1.0		✻	✻		✻	✻	µA
Voltage, Logic “1”	External Pull-up Resistor Required (see Figure 4)			V_{PU}			✻			✻	V
Pulse Width	For Best Linearity		0.25/F_{MAX}			✻			✻		s
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF			400			✻			✻	ns
OUTPUT (F/V CONVERTER) V_{OUT}											
Voltage	I_O ≤ 7mA	0 to +10			✻			✻			V
Current	V_O ≤ 7VDC	+10			✻			✻			mA
Impedance	Closed Loop			1			✻			✻	Ω
Capacitive Load	Without Oscillation			100			✻			✻	pF
DYNAMIC RESPONSE											
Full Scale Frequency				500[8]	✻			✻			kHz
Dynamic Range		6			✻			✻			decades
Settling Time	(V/F) to Specified Linearity for a Full Scale Input Step		[9]			✻			✻		
Overload Recovery	< 50% Overload		[9]			✻			✻		
POWER SUPPLY											
Rated Voltage			±15								V
Voltage Range		±11		±20					✻		V
Quiescent Current			±5.5	±6.0		✻	✻		✻		mA
TEMPERATURE RANGE											
Specification		0		+70	–25		+85	–55		+125	°C
Operating		–25		+85	–55		+125	–55		+125	°C
Storage		–25		+85	–65		+150	–65		+150	°C

✻ Specification the same as VFC32KP.

NOTES: (1) A 25% duty cycle (0.25mA input current) is recommended for best linearity. (2) Adjustable to zero. See Offset and Gain Adjustment section. (3) Linearity error is specified at any operating frequency from the straight line intersecting 90% of full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. Above 200kHz, it is recommended all grades be operated below +85°C. (4) ±0.015% of FSR for negative inputs shown in Figure 5. Positive inputs are shown in Figure 1. (5) FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage). (6) Exclusive of external components' drift. (7) Positive drift is defined to be increasing frequency with increasing temperature. (8) For operations above 200kHz up to 500kHz, see Discussion of Specifications and Installation and Operation sections. (9) One pulse of new frequency plus 1µs.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Output Sink Current (F_{OUT})	50mA
Output Current (V_{OUT})	+20mA
Input Voltage, –Input	±Supply
Input Voltage, +Input	±Supply
Comparator Input	±Supply
Storage Temperature Range:	
VFC32BM, SM	–65°C to +150°C
VFC32KP, KU	–25°C to +85°C

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
VFC32KP	14-Pin Plastic DIP	010	0°C to 70°C
VFC32BM	TO-100 Metal	007	–25°C to +85°C
VFC32SM	TO-100 Metal	007	–55°C to +125°C
VFC32KU	SO-14 SOIC	235	0°C to +70°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

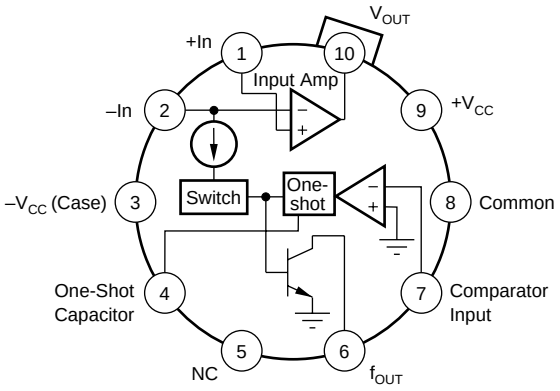
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATIONS

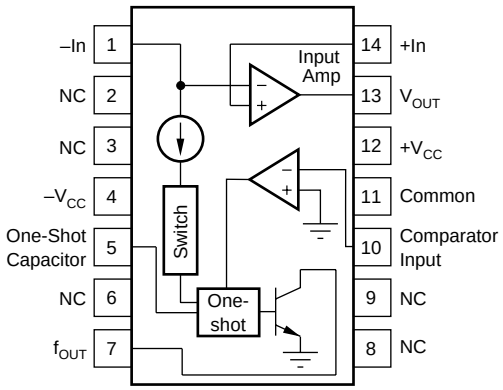
Top View

M Package
(TO-100)



NC = no internal connection
External connection permitted.

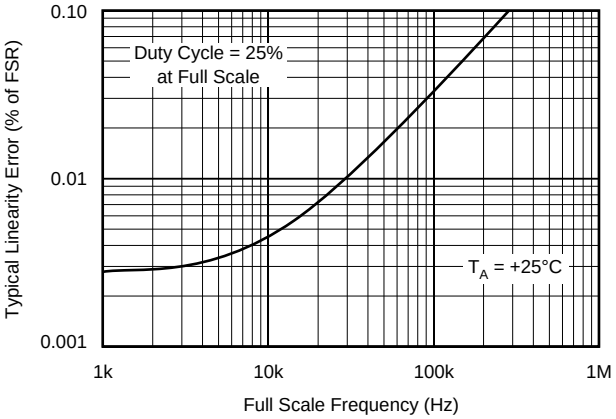
P Package
U Package
(Epoxy Dual-in-line)



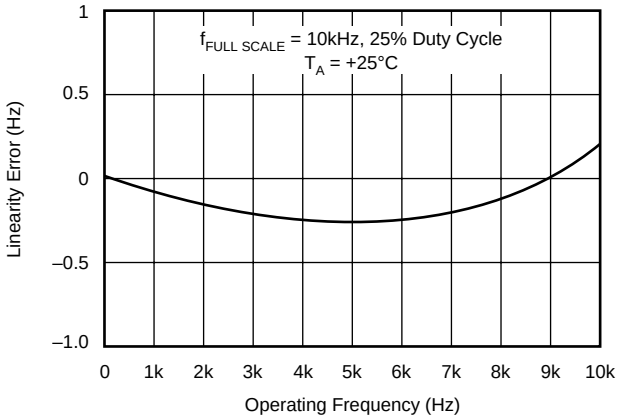
TYPICAL PERFORMANCE CURVES

At T_A = +25°C and V_{CC} = ±15V, unless otherwise noted.

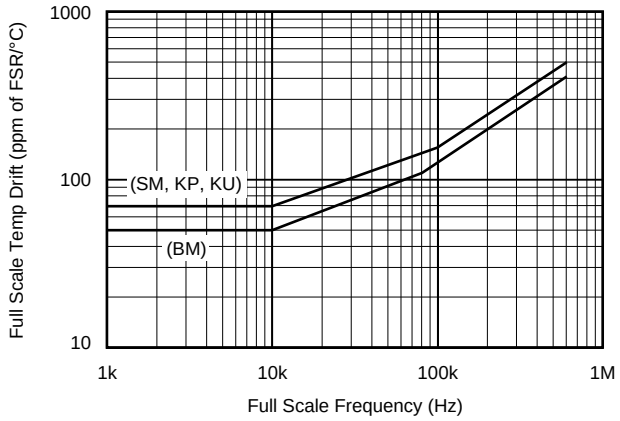
LINEARITY ERROR vs FULL SCALE FREQUENCY



LINEARITY ERROR vs OPERATING FREQUENCY



FULL SCALE DRIFT vs FULL SCALE FREQUENCY



APPLICATION INFORMATION

Figure 1 shows the basic connection diagram for frequency-to-voltage conversion. R_1 sets the input voltage range. For a 10V full-scale input, a 40kΩ input resistor is recommended. Other input voltage ranges can be achieved by changing the value of R_1.

$$R_1 = \frac{V_{FS}}{0.25mA} \quad (1)$$

R_1 should be a metal film type for good stability. Manufacturing tolerances can produce approximately ±10% variation in output frequency. Full-scale output frequency can be trimmed by adjusting the value of R_1—see Figure 3.

The full-scale output frequency is determined by C_1. Values shown in Figure 1 are for a full-scale output frequency of 10kHz. Values for other full-scale frequencies can be read from Figure 2. Any variation in C_1—tolerance, temperature drift, aging—directly affect the output frequency. Ceramic NPO or silver-mica types are a good choice.

For full-scale frequencies above 200kHz, use larger capacitor values as indicated in Figure 2, with R_1 = 20kΩ.

The value of the integrating capacitor, C_2, does not directly influence the output frequency, but its value must be chosen within certain bounds. Values chosen from Figure 2 produce approximately 2.5Vp-p integrator voltage waveform. If C_2's value is made too low, the integrator output voltage can exceed its linear output swing, resulting in a nonlinear response. Using C_2 values larger than shown in Figure 2 is acceptable.

Accuracy or temperature stability of C_2 is not critical because its value does not directly affect the output frequency. For best linearity, however, C_2 should have low leakage and low dielectric absorption. Polycarbonate and other film capacitors are generally excellent. Many ceramic types are adequate, but some low-voltage ceramic capacitor types may degrade nonlinearity. Electrolytic types are not recommended.

FREQUENCY OUTPUT PIN

The frequency output terminal is an open-collector logic output. A pull-up resistor is usually connected to a 5V logic supply to create standard logic-level pulses. It can, however, be connected to any power supply up to $+V_{CC}$. Output pulses have a constant duration and positive-going during the one-shot period. Current flowing in the open-collector output transistor returns through the Common terminal. This terminal should be connected to logic ground.

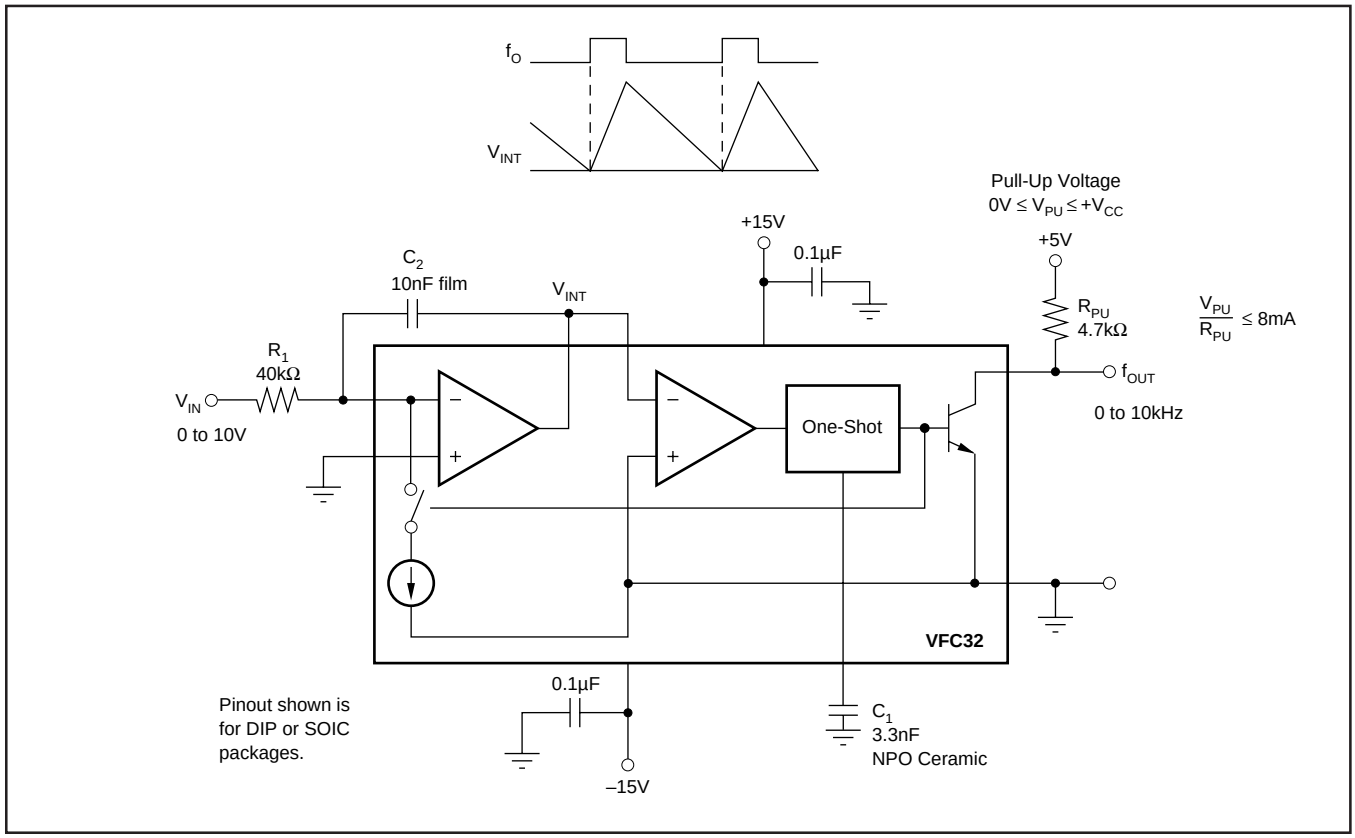


FIGURE 1. Voltage-to-Frequency Converter Circuit.

FREQUENCY-TO-VOLTAGE CONVERSION

Figure 4 shows the VFC32 connected as a frequency-to-voltage converter. The capacitive-coupled input network C_3, R_6 and R_7 allow standard 5V logic levels to trigger the comparator input. The comparator triggers the one-shot on the falling edge of the frequency input pulses. Threshold voltage of the comparator is approximately –0.7V. For frequency input waveforms less than 5V logic levels, the R_6/R_7 voltage divider can be adjusted to a lower voltage to assure that the comparator is triggered.

The value of C_1 is chosen from Figure 2 according to the full-scale input frequency. C_2 smooths the output voltage waveform. Larger values of C_2 reduce the ripple in the output voltage. Smaller values of C_2 allow the output voltage to settle faster in response to a change in input frequency. Resistor R_1 can be trimmed to achieve the desired output voltage at the full-scale input frequency.

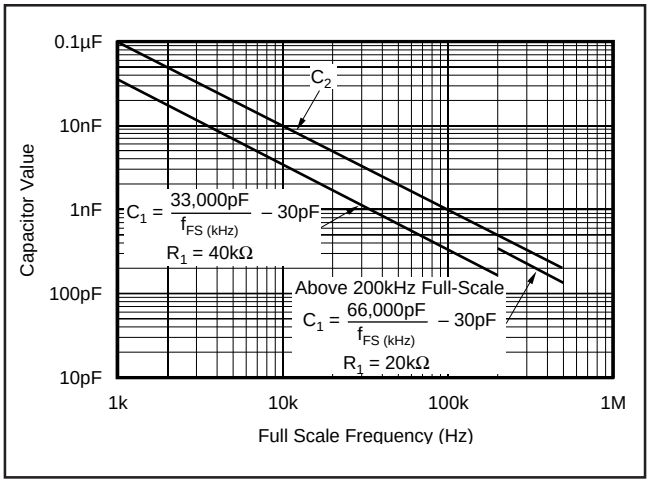


FIGURE 2. Capacitor Value Selection.

PRINCIPLES OF OPERATION

The VFC32 operates on a principle of charge balance. The signal input current is equal to V_{IN}/R_1. This current is integrated by input op amp and C_2, producing a downward ramping integrator output voltage. When the integrator output ramps to the threshold of the comparator, the one-shot is triggered. The 1mA reference current is switched to the integrator input during the one-shot period, causing the integrator output ramp upward. After the one-shot period, the integrator again ramps downward.

The oscillation process forces a long-term balance of charge (or average current) between the input signal current and the reference current. The equation for charge balance is:

$$I_{IN} = I_{R(AVERAGE)} \quad (2)$$

$$\frac{V_{IN}}{R_1} = f_O t_{OS}(1mA) \quad (3)$$

Where:

f_O is the output frequency

t_{OS} is the one-shot period, equal to

$t_{OS} = 7500\ C_1\ (\text{Farads})$ (4)

The values suggested for R_1 and C_1 are chosen to produce a 25% duty cycle at full-scale frequency output. For full-scale frequencies above 200kHz, the recommended values produce a 50% duty cycle.

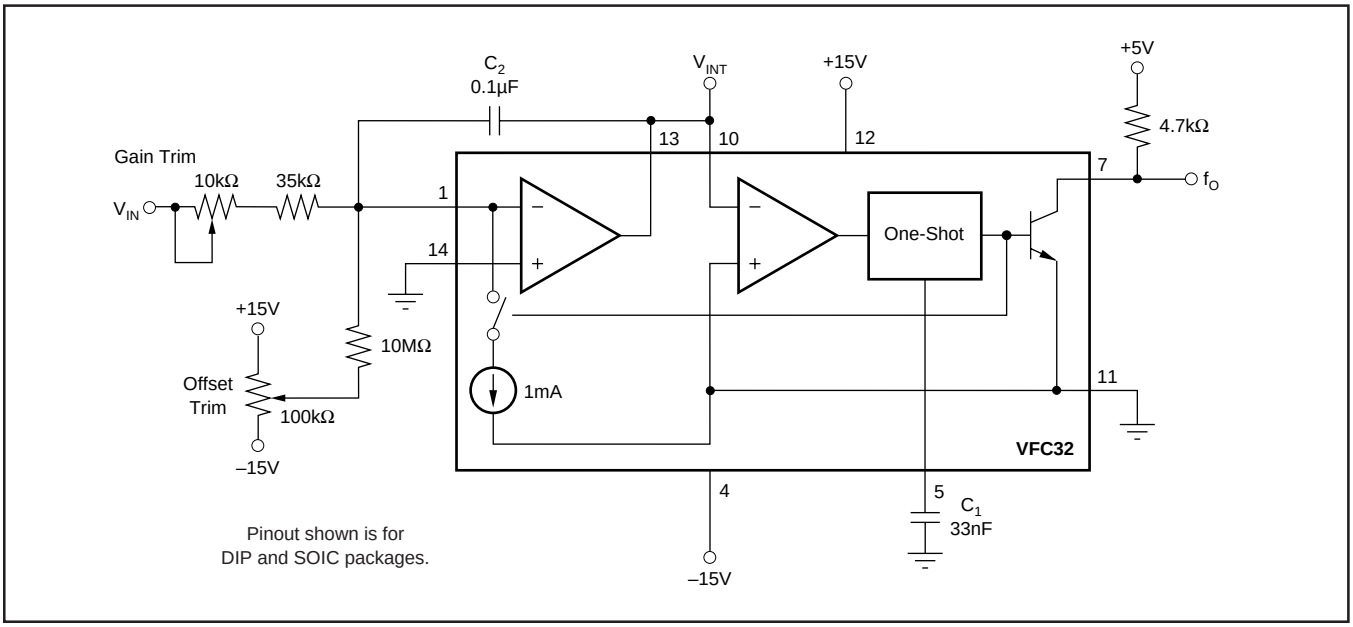


FIGURE 3. Gain and Offset Voltage Trim Circuit.

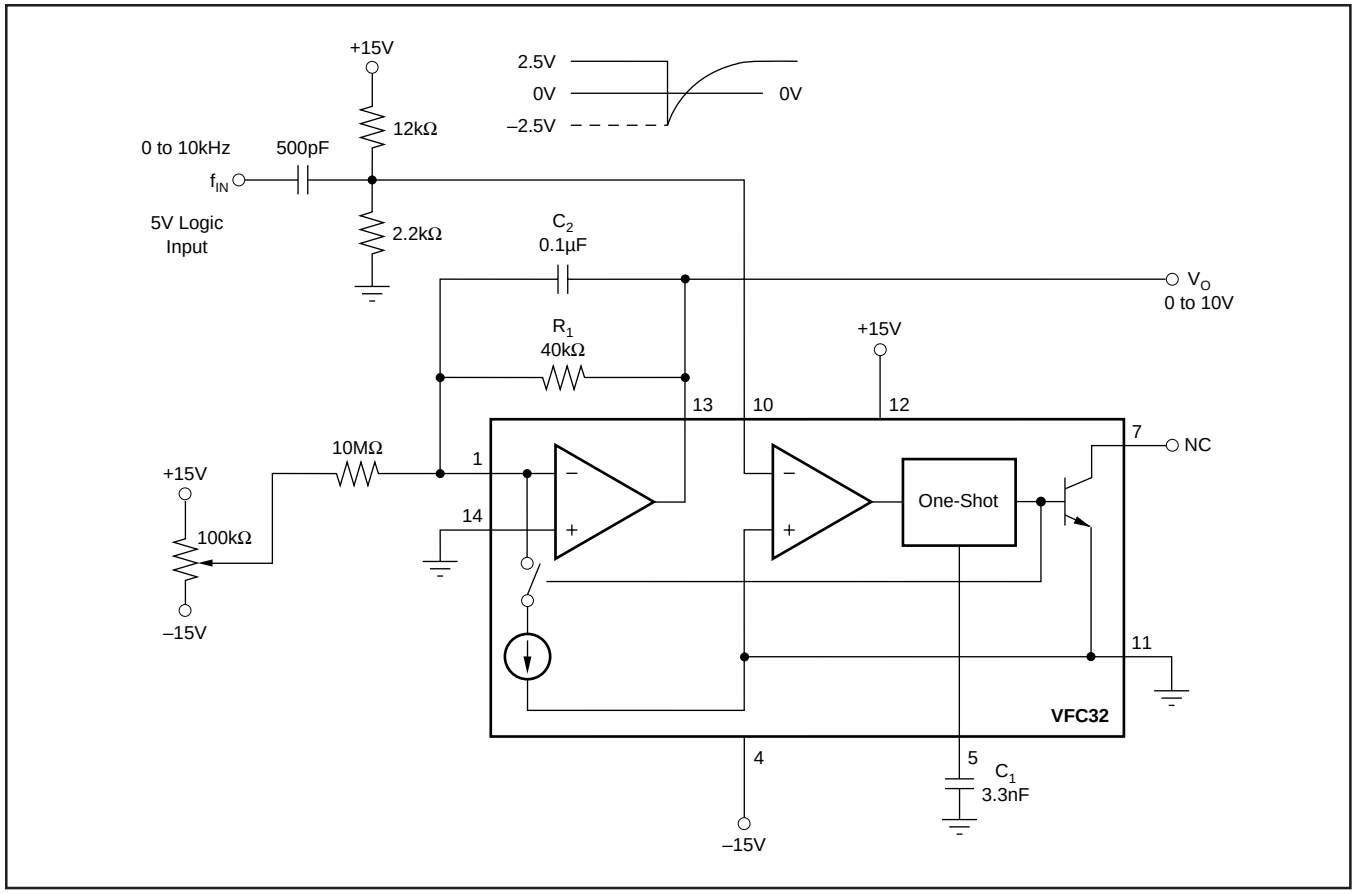


FIGURE 4. Frequency-to-Voltage Converter Circuit.

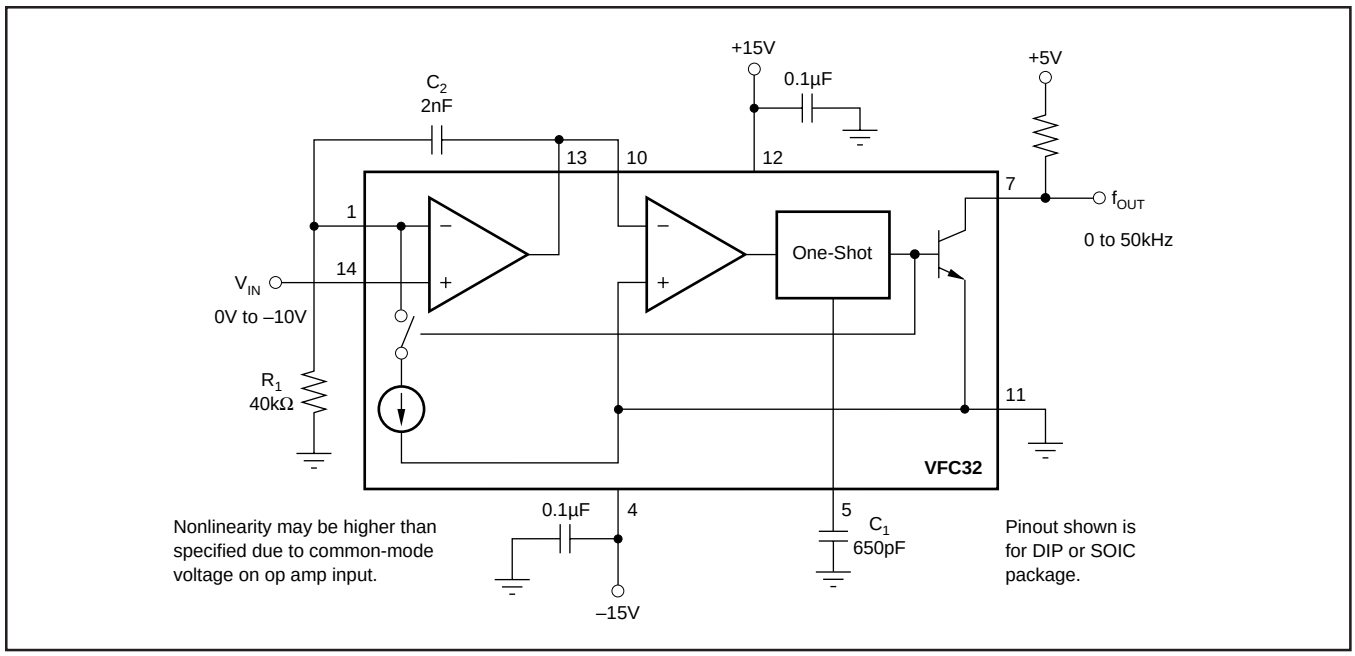


FIGURE 5. V/F Converter—Negative Input Voltage.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VFC32BM	OBSOLETE	TO-100	LME	10		TBD	Call TI	Call TI	-25 to 85		
VFC32KP	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	VFC32KP	Samples
VFC32KPG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	VFC32KP	Samples
VFC32KU	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	VFC32KU	Samples
VFC32KU/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	VFC32KU	Samples
VFC32KUE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	VFC32KU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

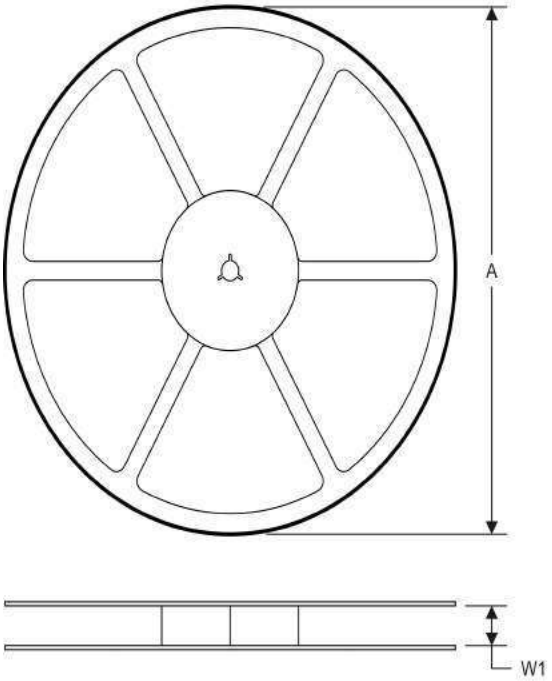
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

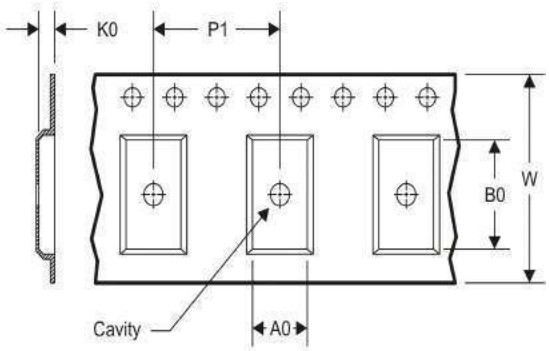
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



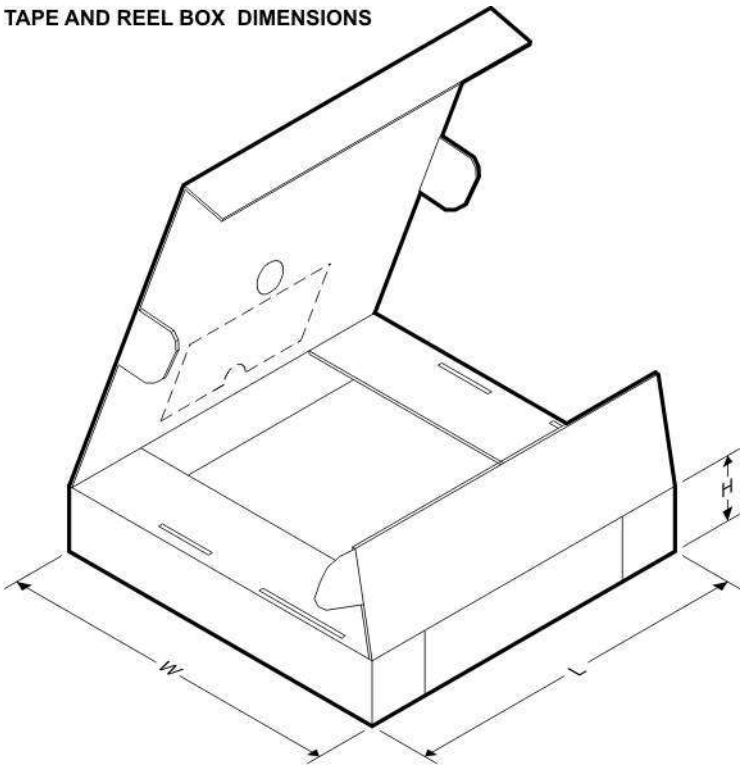
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VFC32KU/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VFC32KU/2K5	SOIC	D	14	2500	367.0	367.0	38.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

MADHA
Expertise | Empathy | Excellence
ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

EC3353 ELECTRONIC DEVICES AND CIRCUITS

Semester - 03

Question Bank

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Vision

To excel in providing value based education in the field of Electronics and Communication Engineering, keeping in pace with the latest technical developments through commendable research, to raise the intellectual competence to match global standards and to make significant contributions to the society upholding the ethical standards.

Mission

- ✓ To deliver Quality Technical Education, with an equal emphasis on theoretical and practical aspects.
- ✓ To provide state of the art infrastructure for the students and faculty to upgrade their skills and knowledge.
- ✓ To create an open and conducive environment for faculty and students to carry out research and excel in their field of specialization.
- ✓ To focus especially on innovation and development of technologies that is sustainable and inclusive, and thus benefits all sections of the society.
- ✓ To establish a strong Industry Academic Collaboration for teaching and research, that could foster entrepreneurship and innovation in knowledge exchange.
- ✓ To produce quality Engineers who uphold and advance the integrity, honour and dignity of the engineering.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

1. To provide the students with a strong foundation in the required sciences in order to pursue studies in Electronics and Communication Engineering.
2. To gain adequate knowledge to become good professional in electronic and communication engineering associated industries, higher education and research.
3. To develop attitude in lifelong learning, applying and adapting new ideas and technologies as their field evolves.
4. To prepare students to critically analyze existing literature in an area of specialization and ethically develop innovative and research oriented methodologies to solve the problems identified.
5. To inculcate in the students a professional and ethical attitude and an ability to visualize the engineering issues in a broader social context.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Design, develop and analyze electronic systems through application of relevant electronics, mathematics and engineering principles.

PSO2: Design, develop and analyze communication systems through application of fundamentals from communication principles, signal processing, and RF System Design & Electromagnetics.

PSO3: Adapt to emerging electronics and communication technologies and develop innovative solutions for existing and newer problems.

EC3353 ELECTRONIC DEVICES AND CIRCUITS

Syllabus

UNIT I SEMICONDUCTOR DEVICES 9

PN junction diode, Zener diode, BJT, MOSFET, UJT –structure, operation and V-I characteristics, diffusion and transition capacitance - Rectifiers – Half Wave and Full Wave Rectifier, Zener as regulator

UNIT II AMPLIFIERS 9

Load line, operating point, biasing methods for BJT and MOSFET**,** BJT small signal model – Analysis of CE, CB, CC amplifiers- Gain and frequency response –MOSFET small signal model– Analysis of CS, CG and Source follower – Gain and frequency response- High frequency analysis.

UNIT III MULTISTAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIER 9

Cascode amplifier, Differential amplifier – Common mode and Difference mode analysis – MOSFET input stages – tuned amplifiers – Gain and frequency response – Neutralization methods.

UNIT IV FEEDBACK AMPLIFIERS AND OSCILLATORS 9

Advantages of negative feedback – Voltage / Current, Series , Shunt feedback Amplifiers – positive feedback–Condition for oscillations, phase shift – Wien bridge, Hartley, Colpitts and Crystal oscillators.

UNIT V POWER AMPLIFIERS AND DC/DC CONVERTERS 9

Power amplifiers- class A-Class B-Class AB-Class C-Power MOSFET-Temperature Effect- Class AB Power amplifier using MOSFET –DC/DC convertors – Buck, Boost, Buck-Boost analysis and design.

Total: 45 Periods

UNIT-I SEMICONDUCTOR DEVICES
PART-A

1. What is a PN Junction? How is it formed?

In a piece of semiconductor material if one half is doped by P-type impurity and other half is doped by N-type impurity, a PN Junction diode is formed. The plane dividing the two halves (or) zones is called PN Junction.

2. What is meant by diffusion capacitance (CD)?

The capacitance that exists in a forward bias junction is called a diffusion (or) storage capacitance (Cp) whose value is usually much larger than Cr, which exists in reverse based junction. This also defined as the rate of change of injected charge with applied voltage

$$Cp = (dQ/dv),$$

3. What is Zener diode?

Zener diode is a specially designed PN junction diode. A reverse biased heavily doped PN junction diode. A reverse biased heavily doped PN junction diode which is operated in the breakdown region is known as Zener diode. It is also called as voltage regulator diode or breakdown diode.

4. Define transition capacitance of P-N diode.

When a diode is reverse biased, the holes in the p- side and the electrons in the n-side drift away from the junction, thereby uncovering more immobile charges. As a result the thickness of depletion increases. This leads to capacitance effect across the region called transition capacitance.

6. Distinguish between shunt and series voltage regulator.

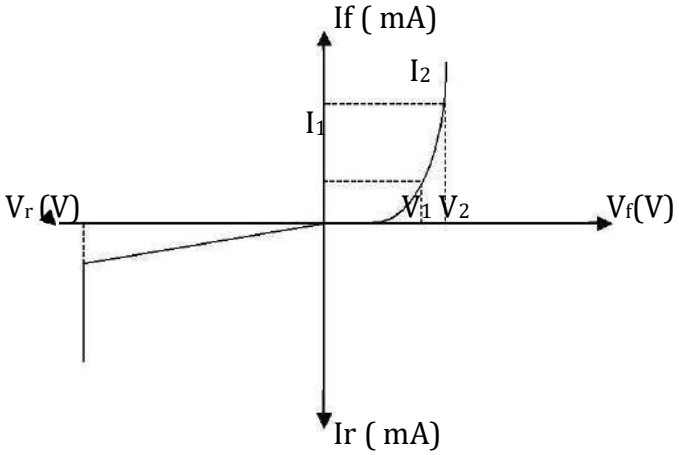
- **Series regulator**

  In a series regulator the regulating element is in series with the load and the regulation is done by varying the voltage across the series element.

- **Shunt regulator**

  In a shunt regulator the regulating element is in shunt with the load and the regulation is done by varying the current across the shunt element.

7. Draw the VI Characteristics of Zener diode.



8. Derive the ripple factor rectifier.

The ripple factor is a measure of how successfully a rectifier converts ac to dc. That is it is the ratio of rms value of ac component to the dc value.

Ripple factor= $V_{(rms)}/V_{dc}$

9. Define peak inverse voltage in a diode.

Peak inverse voltage is the maximum negative voltage which appears across a non conducting reverse biased voltage.

10. What is Drift Current?

Under the influence of the externally applied electric field, the electrons are accelerated in one particular direction. They travel at a speed equal to drift speed. This movement of electrons will give rise to a current which is defined as the drift current.

11. What is barrier potential at the junction?

Due to the presence of immobile positive and negative ions on opposite sides of the junction an electric field is created across the junction. The electric field is known as the barrier potential.

12. What is a Rectifier?

A rectifier is a device which converts a.c. voltage to pulsating d.c. voltage, using one or more PN junction diodes. Its types

i)half wave rectifier
ii)full wave rectifier

13. Define static and dynamic resistance of a PN diode.

The forward resistance of p-n junction diode when p-n junction is used in d.c Circuit and the applied forward voltage is d.c. is called static resistance

The resistance offered by the p-n junction diode under a.c. conditions is called dynamic Resistance of diode.

14. What is break down? What are its types?

When the reverse voltage across the pn junction is increased rapidly at a voltage the junction breaks down leading to a current flow across the device. This phenomenon is called as break down and the voltage is break down voltage. The types of break down are

i) zener break down
ii) ii)Avalanche breakdown

15. What is zener breakdown?

Consequently the depletion layer is thin and consequently the depletion layer is tin. When a small value of reverse bias voltage is applied, a very strong electric field is set up across the thin depletion layer. This electric field is enough to break the covalent bonds. Now extremely large number of free charge carriers are produced which constitute the zener current. This process is known as zener break down.

16. What is avalanche break down?

When bias is applied, thermally generated carriers which are already present in the diode acquire` sufficient energy from the applied potential to produce new carriers by removing valence electron from their bonds. These newly generated additional carriers acquire more energy from the potential and they strike the lattice and create more number of free electrons and holes. This process goes on as long as bias is increased and the number of free carriers get multiplied. This process is termed as avalanche multiplication. Thus the break down which occur in the junction resulting in heavy flow of current is termed as avalanche break down.

17. In a BJT,the emitter current is 12 mA and the emitter current is 1.02 times the collector current. Find the base current.

$I_E = I_C + I_B = 1.02\ I_C$ (Given)
$I_B = 0.02\ I_C$
But $I_C = I_E / 1.02$
$= 12/1.02$
$= 11.76$ mA
$I_B = 0.02 * 11.76 * 10^{-3}$
$= 235.2\ \mu A.$

18. Differentiate FET and BJT.

FET	BJT
Unipolar device (that is current conduction by only one type of either electron or hole).	Bipolar device (current conduction by both electron and hole).
High input impedance due to reverse bias.	Low input impedance due to forward bias.
Gain is characterized by trans Conductance	Gain is characterized by voltage gain
Low noise level	High noise level

19. Define pinch off voltage in FET.

The pinch off voltage V_P is defined as the value of V_{DS} beyond which the drain current becomes constant.

20. What are the special features of FET

- It is a voltage controlled device.
- It is equivalent to a controlled current source.
- The gate source junction is always reverse biased.
- Very small gate current.
- High input resistance and input capacitance.
- Can be used as a switch or as an amplifier.
- It can be used as voltage variable resistance VVR.

21. Why FET is called unipolar device?

FET is a unipolar device that means the current flowing through it is only due to one type of charge particles, holes or electrons. Transistor on the other hand is a bipolar device as holes and electrons both contribute to the flow of current.

22. Define the different operating regions of transistor.

The different operating regions of transistor are

Active Region: It is defined in which transistor function is biased in reverse direction and emitter function in forward direction.

Cutoff Region: The region in which the collector and emitter functions are both reverse biased.

Saturation Region: The region in which both the collector and emitter functions are forward biased.

23. Explain npn and pnp transistor.

npn Transistor: In npn transistor, P-type semiconductor is sandwiched between two

n-type semiconductors. The emitter region is made up of n-type semiconductor base region is made of p-type semiconductor, collector region is made of n-type semiconductor.

pnp Transistor: In pnp transistor, n-type semiconductor is sandwiched between two P-type semiconductor. Emitter region is made of P-type, collector region is made of P-type and the base region is made of n-type, semiconductor.

24. Define Transistor current.

The emitter current (1E) is the sum of the collector current (Ic) and the base current (IB), is called transistor current'. IE = Ic + IB. IB is very small compared to IE or Ic.

25. What is early effect or base and the modulation?

As the collector by voltage Vcc is made to increase the reverse bias, the space charge width between collector and base tends to increase with the result that the effective width of the base decreases. This dependency of base width on collector to emitter -voltage is known as early effect.

26. What is inter base resistance of UJT?

The resistance between the two bases (B1and B2) of UJT is called as inter base resistance. Inter base resistance η= RB1 + RB2

RB1- resistance of silicon bar between B1 and emitter junction.
RB2 - resistance of silicon bar between B2 and emitter junction

27. What is meant by negative resistance region of UJT?

In a UJT when the emitter voltage reaches the peak point voltage, emitter current starts flowing. After the peak point any effort to increase in emitter voltage further leads to sudden increase in the emitter current with corresponding decrease in emitter voltage, exhibiting negative resistance. This takes place until the valley point is reached. This region between the peak point and valley point is called negative resistance region.

Part - B

1. Describe the construction of PN junction diode and explain the forward and reverse characteristics of PN junction diode and obtain its VI characteristic curve.
2. What is meant by transistor? Explain the symbol, Construction and working of NPN & PNP transistor with neat diagram.
3. With neat diagram explain the input and output characteristics of a transistor in CE configuration.
4. Explain the construction and principle of operation of Depletion MOSFET with the help of suitable diagram.
5. Explain the construction and principle of operation of enhancement MOSFET with the help of suitable diagram.
6. Draw the basic structure of UJT and explain V-I characteristics of UJT with the help of equivalent circuit.
7. Illustrative the V-I characteristic curve and explain the operation of zener diode.
8. Draw the circuit diagram of half-wave rectifier and explain its operation with necessary waveform.
9. Draw the circuit diagram of full-wave rectifier and explain its operation with necessary waveform.

UNIT-II AMPLIFIERS
PART-A

1. What is an amplifier?

An amplifier is a circuit, which can be used to increase the amplitude of the input current or voltage at the output by means of energy drawn from an external source.

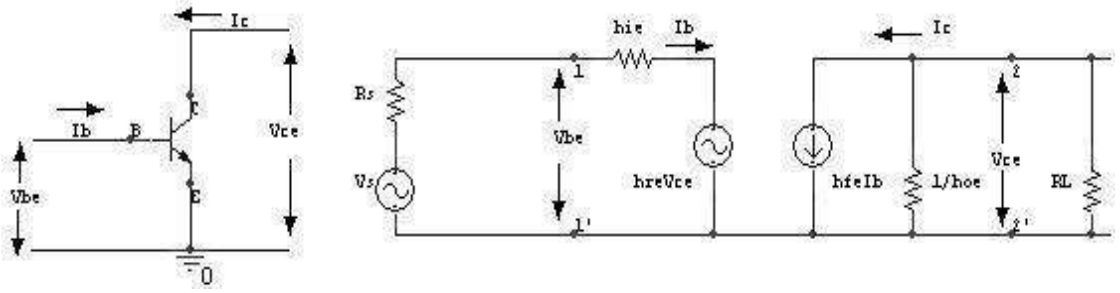
2. Why do we choose Q point at the center of the load line?

The operating point of a transistor is kept fixed usually at the center of the active region in order that the input signal is well amplified. If the point is fixed in the saturation region or the cut off region the positive and negative half cycle gets clipped off respectively.

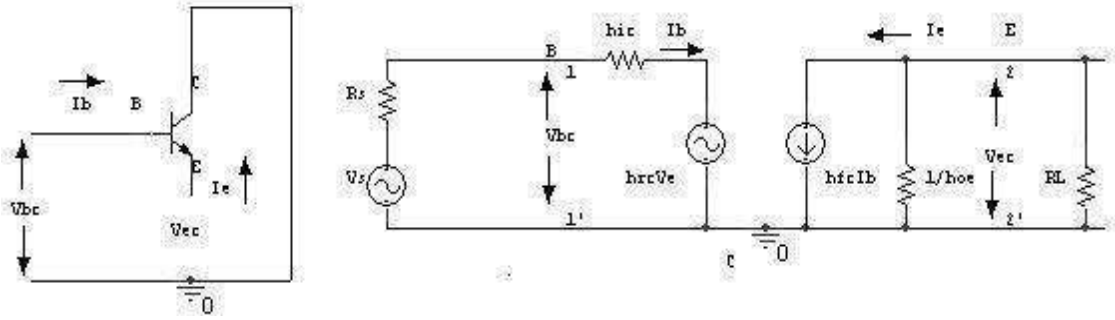
3. When does a transistor act as a switch?

The transistor acts as a switch when it is operated at either cutoff region or saturation region.

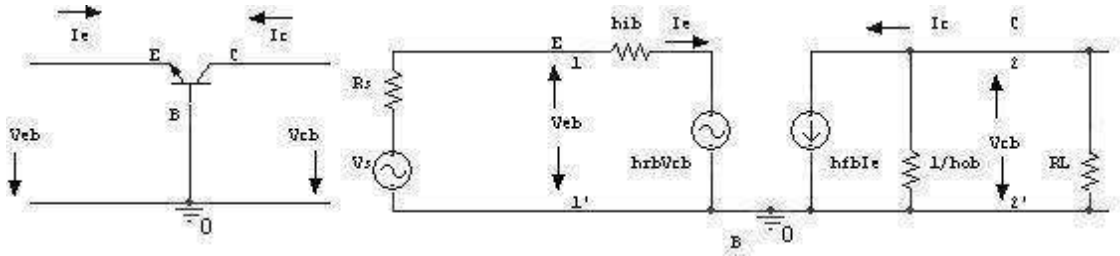
4. Draw a CE amplifier & its hybrid equivalent circuit.



5. Draw a CC amplifier & its hybrid equivalent circuit.



6. Draw a CB amplifier & its hybrid equivalent circuit



7. Which amplifier is called as voltage follower? Why?

The common collector transistor amplifier configuration is called as voltage follower. Since it has unity voltage gain and because of its very high input impedance. It doesn't draw any input current from the s output circuit without making any distortion.

The h parameters has the following limitations,

- The accurate calculation of h parameters is difficult.
- A transistor behaves as a two port network for small signals only, hence h parameters can be used to analyze only the small signal amplifiers.

8. Why N-channel FET's have a better response than P-channel FET's?

N- Channel FET have a better high frequency response than P-channel FET due to the following reason. Mobility of electrons is large in N-channel FET whereas the mobility of holes is poor in P-channel FET. The input noise is less in N-channel FET that that of the P-channel FET. The trains conductance is larger in N-channel FET that that of P-channel FET.

9. Define Miller effect in input capacitance?

For any inverting amplifier, the input capacitance will be increased by a miller effect capacitance, sensitive to the gain of the amplifier and the inter electrode capacitance connected between the input and output terminals of the active device.

$C_{Mi} = (1-A_v) C_{bc}$ $C_{Mo} = (1-1/A_v) C_{bc}$

C_{bc} -Inter electrode capacitance between input and output.

10. What is the purpose of input capacitor, Cin in single stage common source JFET amplifier?

An ac signal is supplied to the gate of the FET through an electrolytic capacitor called input capacitor Cin. This capacitor allows only ac signal enter the gate but isolates the signal source from RG. If this capacitor is not used, the signal source resistance will come across the resistor RG and thus changing the biasing conditions.

11. What is the purpose of Biasing Network (Rs and Cs) in single stage common source JFET amplifier?

The JFET is self-biased by using the biasing network Rs- Cs. The desired bias voltage is obtained when dc component of drain current flows through the source-biasing resistor Rs. whereas, the capacitor Cs bypasses the ac component of drain current.

12. What is the purpose of Coupling Capacitor (Cc) in single stage common source JFET amplifier?

It is an electrolytic capacitor used to couple one stage of amplification to the next stage or load. It allows only amplified ac signal to pass to the other side but blocks the dc voltage. If this capacitor is not used, the biasing conditions of the next stage will be drastically changed due to the shunting effect of Rd.

13. Define operating point.

The zero signal values of I_C & V_{CE} are known as operating point. It is also called so because the variations of I_C and V_{CE} take place about this point, when the signal is applied.

14. Why the operating point is selected at the centre of the active region?

The operating point of a transistor is kept fixed usually at the center of the active region in order that the input signal is well amplified. If the point is fixed in the saturation region or the cut off region the positive and negative half cycle gets clipped off respectively.

15. What is DC load line?

It is the line on the output characteristics of a transistor circuit which gives the Values of I_C & V_{CE} corresponding to zero signal (or) DC Conditions.

16. What is the need for biasing in transistor amplifier?

The proper flow of zero signal collector current and the maintenance of proper Collector emitter voltage during the passage of signal is known as transistor biasing. When a transistor is biased properly, it works efficiently and produces no distortion in the output signal and thus operating point can be maintained stable.

17. What are the factors to be considered to design a biasing circuit?

- It should ensure proper zero signal collector current.
- The emitter base junction must be forward biased and collector base junction must be reversing biased.
- The transistor should be operated in the middle of the active region or operation point should be fixed at the centre of the active region.
- The operating point should be made independent of the transistor parameters (such as β).
- It should ensure that VCE does not fall below 0.5 V for *Ge* transistors and 1 V for Silicon transistors at any instant.

18. List out different type of biasing.

a. Voltage divider bias
b. Fixed bias
c. Emitter feedback bias
d. Collector feedback bias

19. Define stability factor of an amplifier. What is ideal value?

The rate of change of collector current IC w.r.t. the collector leakage current *ICO at constant β and IB is called **stability factor** i.e.

Stability factor, $S = dI_C / dI_{CO}$ at constant I_B and β

20. What is thermal run away in a transistor?

The collector current, being equal increases with increase in temperature. This leads to increased power dissipation with further increase in temperature. .Being accumulative process it can lead to thermal runaway resulting in burn out of transistor. Self destruction of an un-stabilized transistor is called thermal runaway.

21. Why thermal runaway is not there in FETs?

The FET has a positive temperature coefficient of resistivity. In FET, as temperature increases its drain resistance also increases, reducing the drain current. Thus, unlike BJT, thermal runaway does not occur with FET.

22. What are the advantages and disadvantages of fixed bias circuits?

Merits:

a. It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
b. A very small number of components are required.

Demerits:

c. The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
d. Changes in V_{BE} will change I_B and thus cause R_E to change. This in turn will alter the gain of the stage.
e. When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.
f. For small-signal transistors (e.g., not power transistors) with relatively high values of β (i.e., between 100 and 200), this configuration will be prone to thermal runaway. In particular, the stability factor, which is a measure of the change in collector current with changes in reverse saturation current, is approximately β+1. To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small-signal transistors have large stability factors.

23. How self-bias circuit is used as constant current source?

In the self-bias circuit if Ic tends to increase because of ICO has increasing as a result of temperature, the current in RE increases. As consequences of the increase in voltage drop across RE that provides negative feedback, the base current is decreased. Hence constant IC value is maintained in the self-bias circuit.

24. How FET is known as Voltage variable resistor?

In the region before pinch off, where VDS is small, the drain to source resistance rd can be controlled by the bias voltage VGS. Therefore FET is useful as voltage variable resistor (VVR)or Voltage dependent Resistor (VDR)

25. Why do we choose q point at the center of the loadline?

The operating point of a transistor is kept fixed usually at the center of the active region in order that the input signal is well amplified. If the point is fixed in the saturation region or the cut off region the positive and negative half cycle gets clipped off respectively.

26. Name the two techniques used in the stability of the q point .explain.

Stabilization technique: This refers to the use of resistive biasing circuit which allows IB tovary so as to keep IC relatively constant with variations in Ico, β, &VBE.
Compensation techniques: This refers to the use of temperature sensitive devices such as thermostats diodes. They provide compensating voltages &currents to maintain operating point constant.

27. What is heat sink?

A heat sink is an environment or object that absorbs and dissipates heat from another object using thermal contact (either direct or radiant). Heat sinks are used in a wide range of applications wherever efficient heat dissipation is required; major examples include refrigeration, heat engines and cooling electronic devices.

Part - B

1. Analyze a BJT amplifier with a voltage divider bias (Self bias) circuit and derive an expression for stability factors.
2. Draw the a.c equivalent circuit (small signal equivalent) of a CE amplifier with voltage divider bias and derive the expression for voltage gain (Av), Current gain (Ai),input impedance (Rin), output admittance (Ro).
3. Explain the Common Collector (Emitter follower) circuit and derive the expression for Av, Ai, Rin, Ro.
4. Derive the expressions for the voltage gain, current gain, input and output impedance of Common Base amplifier.
5. Explain about common source self- bias & voltage divider bias for FET.
6. Derive gain, input and output impedance of common source MOSFET amplifier with neat circuit diagram.
7. Explain the operation of common drain (source follower) MOSFET and also derive gain, input & output impedance with neat circuit diagram.
8. Explain the operation of common gate MOSFET and also derive gain, input & output impedance with neat circuit diagram.
9. Explain the fixed bias method & derive an expression for stability factors.
10. Explain the collector feedback bias amplifier & derive an expression for stability factors.

UNIT III MULTISTAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIER

Part - A

1. Define Common Mode Rejection Ratio.

Common Mode Rejection Ratio is the figure of merit of a differential amplifier to reject common mode signal and is given by,

$$CMRR = \frac{\text{Gain of the amplifier for a difference mode input signal}}{\text{Gain of the amplifier for a common mode input signal}}$$

$$C = \left| \frac{A_d}{A_c} \right|$$

2. State Miller's Theorem.

It states that the effect of resistance Z on the input circuit is a ratio of input voltage to the current which flows from the input to the output.

$$Z1 = \frac{Z}{1-K}$$

It states that the effect of resistance Z on the output circuit is the ratio of output voltage to the current which flows from the output to input.

$$Z2 = \frac{Z \cdot K}{K-1}$$

3. Define i) Differential gain ii) Common mode gain

The gain with which differential amplifier amplifies the difference between two input signals is called differential gain of the differential amplifier denoted as A_D.

The gain with which it amplifies the common mode signal to produce the output is called common mode gain of the differential amplifier denoted as A_C.

4. What are practical limitations in selecting very high R_E?

1. Large R_E needs higher biasing voltage to set the operating point of the transistors.
2. This increases the overall chip area. Hence practically R_E cannot be selected very high.

5. What are the limitations of h parameters?

The h parameters has the following limitations,

a. The accurate calculation of h parameters is difficult.

b. A transistor behaves as a two port network for small signals only, hence h parameters can be used to analyze only the small signal amplifiers.

6. Methods of coupling multistage amplifiers

a. RC coupling
b. Transformer coupling
c. Direct coupling

7. Features of differential amplifier.

a. High differential voltage gain
b. Low common mode gain
c. High CMRR
d. Two input terminals
e. High input impedance
f. Large bandwidth
g. Low offset voltages and currents
h. Low output impedance

8. List the configuration of differential amplifiers.

a. Dual input, balanced output differential amplifier
b. Dual input, unbalanced output differential amplifier
c. Single input, balanced output differential amplifier
d. Single input, unbalanced output differential amplifier

9. State Bisection Theorem.

A particular network which has mirror symmetry with respect to an imaginary line. If the entire network is denoted as N then it can be divided into two half networks N/2 about the line of symmetry is called bisection theorem or Bartlett's bisection theorem.

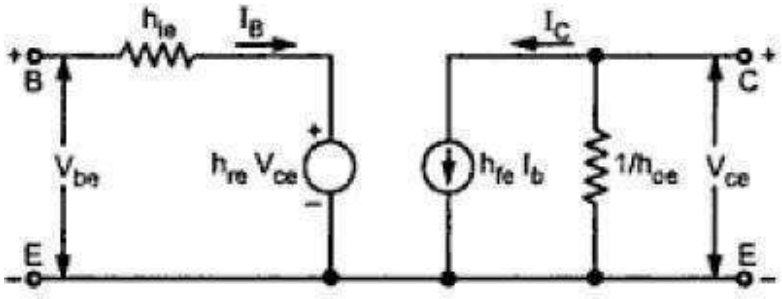
10. Methods of improving CMRR

To improve the CMRR, the common mode gain Ac must be reduced. The common mode gain Ac approaches zero as RE tends to infinity. This is because RE introduces a negative feedback in the common mode operation which reduces the common mode gain Ac. Thus higher the value of RE, lesser is the value of Ac and higher is the value of CMRR. The differential gain Ad is not dependent on RE

11. What are the other methods to improve CMRR without RE?

a. Constant current bias method
b. Current mirror circuit.

12. Draw the small signal equivalent circuit of CE amplifier.



13. Define Miller effect input capacitance.

For any inverting amplifier, the input capacitance will be increased by a miller effect capacitance, sensitive to the gain of the amplifier and the inter electrode capacitance connected between the input and output terminals of the active device.

$C_{Mi} = (1-A_v)\,C_{bc}$ $C_{Mo} = (1-1/A_v)\,C_{bc}$

C_{bc} -Inter electrode capacitance between input and output.

14. Define Q.

Q is Quality factor. It is defined as the measure of the quality of the tuned circuit and is the ratio of inductive reactance to the resistance of the coil at resonance.

15. Comment on Gain-Bandwidth product of a tuned amplifier.

This is the figure of merit defined in terms of mid band gain and the bandwidth of the tuned amplifier.

16. Differentiate between single and stagger tuned amplifier.

Single tuned amplifier uses one parallel tuned circuit as the load impedance in each stage and all these tuned circuits in different stages are tuned to the same frequency but the staggered tuned amplifier uses a number of single tuned stages in cascade, the successive tuned circuits being tuned to slightly different frequencies.

17. What is effective Quality factor?

The effective quality factor or the circuit magnification factor of the output circuit at resonantfrequency ωr is given by

$$Q_{eff} = \frac{\text{Susceptance of inductance L or Capacitance C}}{\text{Conductance of shunt resistance}} = \frac{R_t}{\omega_f L} = \omega_r C_{eq} R_t$$

18. Define loaded and unloaded Q.

Unloaded Q: It is the ratio of energy stored to the energy dissipated in a reactor.
Loaded Q: It is defined as how tightly the resonator is coupled with the terminations.

19. What is a stagger-tuned amplifier?

If two or more tuned circuits are cascaded and are tuned to slightly different frequencies, it is possibleto obtain an increased bandwidth with flat pass band with steep sides. The tuned amplifier used to do thisis called as stagger tuned amplifier.

20. What is a synchronous tuned amplifier?

A number of amplifiers can be cascaded in order to achieve high gain. All stages are assumed to be identical and to be tuned to the same frequency. This is termed as synchronously tuned amplifier which has increased gain and band width which is narrower than the band width of each of the stages.

21. What is the effect of 'Q' on stability?

Higher the value of Q, provides better stability, but smaller bandwidth and larger gain. Hence it provides less stability.

22. Define coil losses.

Copper loss, Eddy current loss and hysteresis loss are called coil losses.

23. What is the instability of tuned amplifiers?

Due to the internal capacitance between the input and output there will be feedback in the circuit. If the feedback is positive then the circuit starts oscillating instead of amplifying.

24. What are the techniques of stabilizing a band pass amplifier?

(i) Neutralization, (ii) Unilaterization, (iii) Mismatching technique.

25. What is Neutralization?

At high frequencies the various capacitances of the transistor circuits play an important role. If some feedback signal manages to reach the input terminal as a positive feedback, the stability of the circuit is affected. To avoid this, a capacitance is connected in the feedback circuit to neutralize the effect of other capacitances. This is called Neutralization.

26. Write the disadvantages of tuned amplifier.

(1) Since they use inductors & capacitors as tuning elements, the circuit is bulky and costly, (2) If the band of frequency is increased, design becomes complex. (3) They are not suitable to amplify audio frequency.

27. Write the advantages of tuned amplifier.

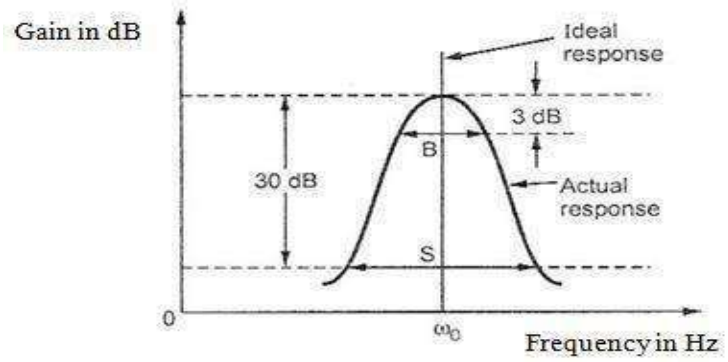
They amplify desired frequencies.

a. Signal to noise ratio at output is good.
b. They are well suited for radio Transmitters and receivers.
c. The band of frequencies over which amplification is required can be varied.

28. What are tuned amplifiers? What are the various types of Tuned simplifiers?

Amplifiers which amplify a specific frequency or narrow band of frequencies are called tuned amplifiers. The types are (i) Single tuned amplifiers, (ii) Double tuned amplifiers and (iii) Stagger tuned amplifiers.

29. Draw the frequency response of single tuned amplifier.



30. What are the applications of tuned amplifiers?

(i) Selection of a desired radio frequency signal. (ii) Amplification of the selected signal to a suitable voltage level.

31. Determine the bandwidth of two stage synchronous tuned amplifier. Assume the bandwidth ofindividual stage is 310 kHz.

$BW2 = BW \sqrt{2^{1/N} - 1} = 310 \sqrt{2^{1/2} - 1} = 200$

32. Define Q factor of the capacitor.

The Q-factor or the quality factor of a capacitor at the operating frequency **ω** is defined as the ratio of the reactance of the capacitor to its series resistance. Quality factor $Q = 1/ \omega CR$

33. What is the effect of Q on the resonance circuit?

Q factor is a dimensionless parameter that describes how under - damped an oscillator or resonator is, and characterizes a resonator's bandwidth relative to its center frequency. Higher *Q* indicates a lower rate of energy loss relative to the stored energy of the resonator; the oscillations die out more slowly. Resonators with high quality factors have low damping so that they ring or vibrate longer.

34. A 3μH coil used in tuned amplifier tunes to 1050 Khz has Rs of 50Ω.If the load resistance of theamplifier is R_L=5k.Calculate the loaded and unloaded Q of the tank circuit. (Dec 15)

Unloaded $Q = \omega_0 L / R_S$ $R_S = 50\ \Omega$; $L = 3\mu H$

$\omega_0 = 2\pi \times 1050 \times 10^3 = 6597$Khz

Loaded $Q = \omega_0 L / R$ $R = R_S \parallel R_L$; $R_L = 5k$

Part - B

1. Draw the single tuned amplifier and explain the frequency response. Derive the expression for its gain and cutoff frequency.
2. Draw the double tuned amplifier and explain the frequency response. Derive the expression for its gain and cutoff frequency.
3. Discuss briefly the need for neutralization in tuned amplifiers. Explain Hazeltine and Neutrodyne Neutralization methods with relevant circuit diagrams.
4. Derive the expression of R_i, A_V and R_O for two-stage Cascode CE amplifier also draw the equivalent circuit.
5. Draw the circuit diagram for an emitter coupled differential amplifier using BJTs. Describe common mode and differential mode working.
6. Derive the expressions of A_d and A_{cm} amplifier for BJT Differential amplifier and its equivalent circuit.

UNIT IV - FEEDBACK AMPLIFIERS AND OSCILLATORS

Part A

1. Define feedback factor. (or) What is meant by feedback?

The process of combining a fraction or part of output energy back to the input is known as feedback.

Or

Feedback factor is defined as the ratio feedback voltage or feedback current to the output voltage or current of a feedback amplifier.

It is given by $\beta=V_f/V_o$

2. What is meant by positive feedback? (or) Define direct feedback. (or) Define Regenerative feedback.

If feedback signal applied is in phase with the input signal and thus increases the input, it is called as positive feedback. it is also known as regenerative feedback.

3. What is meant by negative feedback? (or) Define inverse feedback. (or) Define degenerative feedback.

If the feedback signal applied to the input is out of phase with the input signal and thus signal decrease, it is called negative feedback. It is also known as degenerative feedback.

4. What are the effects of negative feedback? (or) What are the advantages of negative feedback?

1. It improves the stability of the circuit.
2. It improves the frequency response of the amplifier.
3. It improves the percentage of harmonic distortion.
4. It improves the signal to noise ratio (SNR).
5. It reduces the gain of the circuit.

5. Define sensitivity?

Sensitivity is defined as the ratio of percentage change in voltage gain with feedback to the percentage change in voltage gain without feedback.

Sensitivity factor (S) = $1/1+A\beta$. Where A = Amplifier gain. . β = Feedback factor.

6. Define Desensitivity D?

Desensitivity is defined as the ratio of percentage change in voltage gain without feedback to the percentage change in voltage gain with feedback.

Desensitivity factor (D) = $1+A\beta$. Where A = Amplifier gain. . β = Feedback factor.

7. Define loop gain. (or) What is meant by return ratio?

The product of open loop gain and feedback factor is called loop gain,

i.e. loop gain =$A\beta$.

8. Give the effect of negative feedback on amplifier characteristics.

Characteristics	Type of feedback			
	Current-series	Voltage-series	Voltage-shunt	Current-shunt
Voltage gain	Decreases	Decreases	Decreases	Decreases
Bandwidth	Increases	Increases	Increases	Increases
Input resistance	Increases	Increases	Decreases	Decreases
Output resistance	Increases	Decreases	Decreases	Increases

9. Give an example for voltage-series feedback.

The Common collector or Emitter follower amplifier is an example for voltage series feedback.

10. Give the properties of negative feedback.

i. Negative feedback reduces the gain
ii. Distortion is very much reduced

11. Calculate the closed loop gain of a negative feedback amplifier of its open loop gain is 100,000 and feedback factor is 0.01.

Given A=100,000
Closed loop gain A_f=?
$A_{vf} = A_v/1+A\beta$
$= 100,000/[1+ (0.01x100,000)]$
$A_{vf} = 99.9$

12. What is the effect on input and output impedance of an amplifier if it employs voltage series negative feedback?

Voltage series negative feedback
Input impedance of an amplifier – Increases by a factor of 1 + Aβ
Output impedance of an amplifier – Decreases by a factor of 1 + Aβ

13. What is the effect on input and output impedance of an amplifier if it employs current shunt negative feedback?

Current Shunt negative feedback
Input impedance of an amplifier – Decreases by a factor of 1 + Aβ
Output impedance of an amplifier – Increases by a factor of 1 + Aβ

14. List the characteristics of an amplifier which are modified by negative feedback.

Characteristics of an amplifier that are modified by negative feedback are

i. Gain decrease
ii. Bandwidth increases
iii. Noise and distortion decreases

15. In a negative feedback amplifier A=100,β=0.04,and V_S=50Mv,find(a)gain with feedback (b) feedback factor (c) (d)feedback voltage.

Given: A = 100, β=0.04, V_S=50mV

(a) Gain with feedback $A_f = A/1+A\beta$

$= 100/[1+(0.04x100)]$

$= 20$

(b) Feedback factor = 0.04

(c) Feedback voltage $V_f = \beta V_o$

$= 0.04x50mV$

$= 2mV$

16. Mention the three networks that are connected around the basic amplifier to implement feedback concept.

i. Mixing network
ii. Sampling network
iii. Feedback network

17. State the Nyquist criterion to maintain the stability of negative feedback amplifier.

The criterion of Nyquist is that the amplifier is unstable of this curve encloses the point -1+j0, and the amplifier is stable if the curve does not encloses this point.

18. What is node sampling?

When the output voltage is sampled by connecting the feedback network in shunt across the output, the connection is referred to as voltage or node sampling.

19. What is loop sampling?

When the output current is sampled by connecting the feedback network in series with the output, the connection is referred to as current or loop sampling.

20. What is the purpose of mixer network in feedback amplifier?

The mixer network is used to combine feedback signal and input at input ofan amplifier.

21. What are the advantages of introducing negative feedback?

1. Input resistance is very high.
2. Output resistance is low.
3. The transfer gain A_f of the amplifier with feedback can be stabilized against Variations of the h-parameters or hybrid π parameters of the transistors or the Parameters of the others active devices used in the amplifiers.

22. What is nyquist diagram?

The plot which shows the relationship between gain and phase-shift as a function of frequency is called as nyquist diagram.

23.Write the steps which are used to identify the method of feedback topology?

1. Identify topology (type of feedback)
   - To find the type of sampling network.
   - To find the type of mixing network
2. Find the input circuit.
3. Find the output circuit.
4. Replace each active device by its h-parameter model at low frequency.
5. Find the open loop gain (gain without feedback), A of the amplifier.
6. Indicate A_f and A_O on the circuit and evaluate $\beta = A_f/A_O$.
7. Calculate A, and β, find D, A_i,R_{if},R_{of},and R_{of}'.

24. Define Frequency compensation and its types.

If the feedback amplifier has more than two poles, it can be unstable. The technique is used to make unstable feedback amplifier to stable is called Frequency compensation. There are two types,

Dominant pole compensation: In this compensation technique if dominant pole is introduced into the amplifier so that phase shift is less than -1800 when the loop gain is unity.

Miller compensation: It is implemented by connecting a capacitor between input and output of a gain stages of a multistage amplifier.

25. Mention the three basic networks that are connected around the basic amplifier to implement feedback concept.

Mixing Network
Sampling Network
Feedback Network

26. How does an oscillator differ from an amplifier?

S.No	Oscillators	Amplifiers
1	They are self-generating circuits. They generate waveforms like sine, square and triangular waveforms of their own. Without having input signal.	They are not self-generating circuits. They need a signal at the input and they just increase the level of the input waveform.
2	It have infinite gain	It have finite gain
3	Oscillator uses positive feedback	Amplifier uses negative feedback.

27. What are the types of sinusoidal oscillator? Mention the different types of sinusoidal oscillator?

RC phase shift Oscillator.
Wein bridge Oscillator.
Hartley Oscillator
Colpitts Oscillator
Crystal Oscillator

28. What is an Oscillator?

An Oscillator is a Circuit, which generates an alternating voltage of any desired frequency. It can generate an a.c output signal without requiring any externally applied input signal.

29. What are the essential parts of an Oscillator?

i. Tank circuit (or) Oscillatory circuit
ii. Amplifier (Transistor amplifier)
iii. iii. Feedback Circuit.

30 . What is Barkhausen criterion or what are the essential conditions for oscillation?

i. The total phase shift of an oscillator should be 360^o.
ii. Magnitude of loop gain should be unity /$A\beta = 1$ /

31. List the disadvantages of crystal Oscillator.

It is suitable for only low power circuits large amplitude of vibrations may crack the crystal. It large in frequency is only possible replacing the crystal with another one by different frequency.

32. What is meant by resonant Circuit Oscillators?

LC Oscillators are known as resonant circuit oscillator because the frequency of operation of LC Oscillator is nothing but a resonant frequency of tank circuit or LC tank circuit produces sustained Oscillation at the resonant circuit oscillator.

33. Why RC phase shift is needed in a RC phase shift Oscillator?

The amplifier used causes a phase shift of 180^o than the feedback network should create phase shift of 180^o, to satisfy the Barkhausen Criterion. Hence in a phase shift oscillators, three sections of RC circuit are connected in cascade, each introducing a shift of 60^o, thus introducing a total phase shift of 180^o, due to feedback network.

34. What are the advantages of crystal Oscillators over other Oscillator?

To maintain the output frequency of an oscillator at a constant value, a crystal may be used to control the frequency of oscillation.

35. What is piezo electric effect?

The piezo electric Crystals exhibit a property that if a mechanical stress is applied across one face the electric potential is developed across opposite face. The inverse is also live. This phenomenon is called piezo electric effect.

36. What is the necessary condition for a wein bridge oscillator circuit to have sustained oscillations?

Gains of the amplifier $A \geq 3$

Feedback factor $\beta = 1/3$

So that $|A\beta| \geq 1$

37. What is frequency stability of an oscillator?

For an oscillator, the frequency of oscillations must remain constant. The analysis of the dependence of the oscillating frequency on the various factor like stray capacitance, temperature etc, is called as the frequency stability analysis.

38. What is Miller crystal oscillator? Explain its operation?

It is nothing but a Hartley oscillator with its feedback Network is replaced by a crystal. Crystal normally has higher frequency reactanceduetothe millercapacitance that are in effect between the transistor terminal.

39. List the factors that affect the frequency stability of an oscillator?

- Change in temperature
- Change in load
- Change in power supply

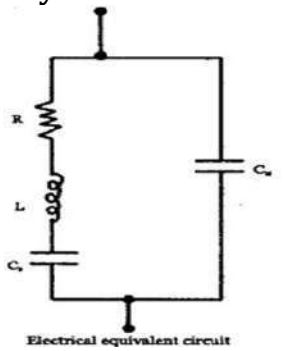
40. Wein Bridge oscillator is used for operation at 10 KHz. If the value of resistance R is 100 kΩ, Evaluate the value of C required.

$F = 1/(2\pi RC)$ $C = 159.155PF$

41. Ina RC phase shift oscillator, if R1 =R2 =R3= 200k and C1=C2=C3=100pf, Estimate the frequency of the oscillator.

The frequency of oscillator is $F = 1/(2\pi RC) = 7.957\ kHZ$

42. Draw the equivalent circuit of crystal oscillator.



Electrical equivalent circuit

Part - B

1. Draw Crystal Oscillator using BJT, explain and derive the condition for oscillation.
2. Identify the working principle of RC phase shift oscillator circuit diagram; also derive the expression for frequency of oscillation.
3. With a neat diagram explain the operation of the Wein-bridge oscillator. Also derive the expression for the frequency of oscillation.
4. Draw Hartley Oscillator using BJT, explain and derive the condition for oscillation.
5. Draw Colpitts Oscillator using BJT, explain and derive the condition for oscillation.
6. Derive the expression for an input and output resistance of a voltage series (Series-Shunt) (Voltage amplifier) feedback amplifier.
7. Derive the expression for an input and output resistance of a voltage shunt (shunt-Shunt) (Trans resistance amplifier) feedback amplifier.
8. Derive the expression for an input and output resistance of a current series (series-series) (Trans conductance amplifier) feedback amplifier.
9. Derive the expression for an input and output resistance of a current shunt (shunt-series) (current amplifier) feedback amplifier.

UNIT V POWER AMPLIFIERS AND DC/DC CONVERTERS

Part A

1. State the difference between voltage and power amplifier.

Voltage Amplifier: The input given to the transistor is in millivolts. The transistor used is a small signal transistor.

Power Amplifier: The input given to the transistor is in volts. The transistor used is a power transistor.

2. How do you bias the class A operation?

In class A mode, the output current flows throughout the entire period of input cycle and the Q point is chosen at the midpoint of AC load line and biased.

3. Which amplifier gives minimum distortion?

Class S amplifier gives minimum distortion.

4. Give the applications of class C power amplifier.

The applications of class C power amplifier are,

a. Used in radio and TV transmitters.

b. Used to amplify the high frequency signals.

c. Tuned amplifiers

5. Give the two draw backs of class C amplifier.

The drawbacks of class C amplifier are,

a. Distortion is high.

b. Figure of merit is low.

6. Define the following modes of operation (a) Class AB (b) Class C.

a. Class AB

In this mode of operation, the output current flows for more than one half cycle but less than full cycle.

b. Class C

In this mode, the level current flows for less than one half cycled i.e., $\frac{1}{4}^{th}$ of the input cycle.

7. Define Class B mode of operation and its advantages and disadvantages.

Class B mode of operation

The Biasing signal and input signal flow through the circuit for half cycle i.e., 180^{o}.

Advantages

a. Efficiency is increased from 25% to 78.5%

b. Due to push pull configuration all even harmonics are reduced. So harmonic distortions are reduced.

c. Due to centre-tapped transformer at input and output, the core saturation loss is reduced.

Disadvantages

a. Transistor is biased above the cut off region

b. Due to the centre-tapped transformer at both input and output, the circuit becomes complex

8. Why RC coupling is popular?

RC coupling is popular because it is simple, less expensive, less distortion and it provides uniform bandwidth.

9. List the advantages of transformer coupled amplifier.

The advantages of transformer coupled amplifier are,

a. it is more efficient because the low DC resistance of the primary is connected to the collector circuit.

b. It provides excellence impedance matching, thus voltage and power gains are improved.

10. What is the use of transformer coupling in the output stage of multistage amplifier?

The transformer coupling provides impedance matching between input and output. As a result the power gain is improved.

11. Where S amplifiers are used?

The class S power amplifier can be used to amplify either the constant amplitude or varying amplitude signal such as FM or AM signal.

12. Define inter modulation distortion?

Inter modulation distortion is a type of non-linear distortion. Which generate frequency components not harmonically related to the signal frequencies. It occurs when the input signal contains more than the one frequency.

13. What is the use of heat sink?

The heat sink is used to observe the heat produce in the transistor junctions while its operation. Usually power amplifiers are provided with heat sinks. The heat sink is a large, black metallic heat-conducting device placed in close contact with the transistor.

14. Define thermal resistance.

The resistance offered by the bipolar junction transistor to the flow of heat is called thermal resistance.

The thermal resistance Q = QjA = QjC+QCS+QSAo C/W

QjA = Total junction to ambient thermal resistance

QjC= Junction to case thermal resistance. QCS= Case to heat sink resistance.
QSA=Heat sink to ambient resistance.

The maximum power in class C power amplifier is, Pc max = 5/12 (T/To)(Vcc2/RL)

15. Write the advantages of heat sink?

The advantages of heat sink are,

a. The temperature of the case gets lowered.
b. The power handling capacity of the transistors can approach the rapid maximum value.

16. Write the Thermal-electric analogy parameters.

The following are the thermal-electric analogy parameters.

Tj = Junction temperature
TC = Case temperature
TA = Ambient temperature
QjA = Total thermal resistance
QjC= Transistor thermal resistance.
QCS= Insulator thermal resistance. QSA=Heat sink thermal resistance.

17. Write the maximum power handling of the class C power amplifier?

The maximum power in class C power amplifier is,

Pc max = 5/12 (T/To)(Vcc2/RL)

18. Define class A power amplifier. How do you bias class A amplifier?

It is an amplifier in which the input signal and the biasing is such that the output current flows for full cycle of the input signal. The Q point should be kept at the center of the DC load line to bias the Class A amplifier

19. Give the important features of Buck Converters.

- Gain less than unity
- Gain is independent of switching frequency as long as Ts<To
- Output voltage ripple percentage of independent of the load on the converter
- Output ripple have second order roll off with the switching frequency.
- Ideal efficiency is unity.

The input current is discontinuous and pulsating.

20. Write the important features of Boost Converters.

- Gain more than unity
- Gain is independent of switching frequency as long as Ts<RC
- Output voltage ripple percentage of dependent of the load on the converter
- Parasitic resistance degrades the gain
- Ideal efficiency is unity.

The input current is continuous.

21. List the important features of Buck-Boost Converters.

- Gain can be set below or above unity.
- Gain is independent of switching frequency as long as Ts<RC
- Output voltage ripple percentage of independent of the load on the converter & Output ripple have second order roll off with the switching frequency.
- Parasitic resistance degrades the gain
- Ideal efficiency is unity.

The input current is discontinuous and pulsating.

Part B

1. Draw the circuit diagram and explain the operation of step down switching regulator (Buck). State the advantages and disadvantages of step down switching regulator.
2. Draw the circuit diagram and explain the operation of step up switching regulator (Boost). State the advantages and disadvantages of step up switching regulator.
3. Draw the circuit diagram and explain the operation of voltage inverter type switching regulator (Buck-Boost).
4. Draw the circuit diagram of push pull class B power amplifier coupled using transformers and explain the operation. Discuss its merits and demerits.
5. Explain with neat circuit diagram, the working of transformer coupled class A power amplifier and give its advantages and disadvantages. Derive the expression for its efficiency.
6. Discuss Class AB operation of power amplifiers.
7. Draw and explain the working of class C tuned amplifier.

MADHA
Expertise | Empathy | Excellence
ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

EC3353 ELECTRONIC DEVICES AND CIRCUITS

Semester - 03

Notes

MADHA
Expertise | Empathy | Excellence
ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Vision

To excel in providing value based education in the field of Electronics and Communication Engineering, keeping in pace with the latest technical developments through commendable research, to raise the intellectual competence to match global standards and to make significant contributions to the society upholding the ethical standards.

Mission

- ✓ To deliver Quality Technical Education, with an equal emphasis on theoretical and practical aspects.
- ✓ To provide state of the art infrastructure for the students and faculty to upgrade their skills and knowledge.
- ✓ To create an open and conducive environment for faculty and students to carry out research and excel in their field of specialization.
- ✓ To focus especially on innovation and development of technologies that is sustainable and inclusive, and thus benefits all sections of the society.
- ✓ To establish a strong Industry Academic Collaboration for teaching and research, that could foster entrepreneurship and innovation in knowledge exchange.
- ✓ To produce quality Engineers who uphold and advance the integrity, honour and dignity of the engineering.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

1. To provide the students with a strong foundation in the required sciences in order to pursue studies in Electronics and Communication Engineering.
2. To gain adequate knowledge to become good professional in electronic and communication engineering associated industries, higher education and research.
3. To develop attitude in lifelong learning, applying and adapting new ideas and technologies as their field evolves.
4. To prepare students to critically analyze existing literature in an area of specialization and ethically develop innovative and research oriented methodologies to solve the problems identified.
5. To inculcate in the students a professional and ethical attitude and an ability to visualize the engineering issues in a broader social context.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Design, develop and analyze electronic systems through application of relevant electronics, mathematics and engineering principles.

PSO2: Design, develop and analyze communication systems through application of fundamentals from communication principles, signal processing, and RF System Design & Electromagnetics.

PSO3: Adapt to emerging electronics and communication technologies and develop innovative solutions for existing and newer problems.

EC3353 ELECTRONIC DEVICES AND CIRCUITS

Syllabus

UNIT I SEMICONDUCTOR DEVICES 9

PN junction diode, Zener diode, BJT, MOSFET, UJT –structure, operation and V-I characteristics, diffusion and transition capacitance - Rectifiers – Half Wave and Full Wave Rectifier, Zener as regulator

UNIT II AMPLIFIERS 9

Load line, operating point, biasing methods for BJT and MOSFET**,** BJT small signal model – Analysis of CE, CB, CC amplifiers- Gain and frequency response –MOSFET small signal model– Analysis of CS, CG and Source follower – Gain and frequency response- High frequency analysis.

UNIT III MULTISTAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIER 9

Cascode amplifier, Differential amplifier – Common mode and Difference mode analysis – MOSFET input stages – tuned amplifiers – Gain and frequency response – Neutralization methods.

UNIT IV FEEDBACK AMPLIFIERS AND OSCILLATORS 9

Advantages of negative feedback – Voltage / Current, Series , Shunt feedback Amplifiers – positive feedback–Condition for oscillations, phase shift – Wien bridge, Hartley, Colpitts and Crystal oscillators.

UNIT V POWER AMPLIFIERS AND DC/DC CONVERTERS 9

Power amplifiers- class A-Class B-Class AB-Class C-Power MOSFET-Temperature Effect- Class AB Power amplifier using MOSFET –DC/DC convertors – Buck, Boost, Buck-Boost analysis and design.

Total: 45 Periods

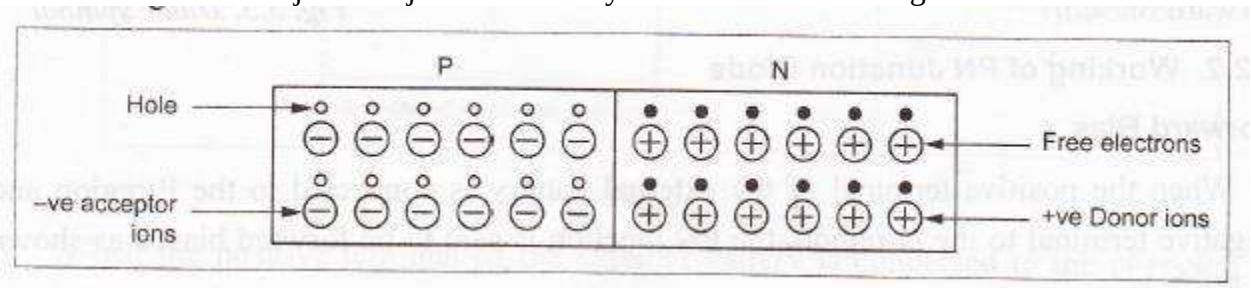
EC3353-ELECTRONIC DEVICES AND CIRCUITS
UNIT-I PN JUNCTION DEVICES
PART - B

PN junction diode: structure, operation & V-I characteristics

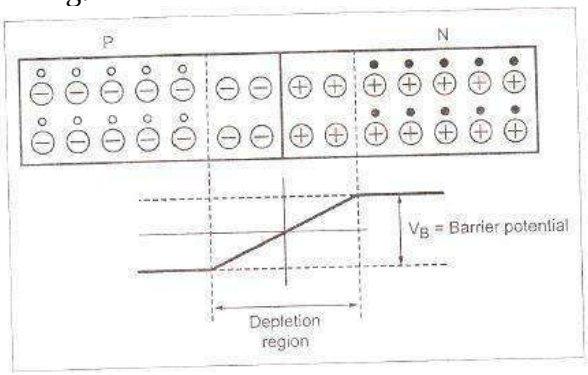
1. **With a neat diagram explain the working of a PN junction diode in forward bias And reverse bias and show the effects of temperature on its VI characteristics (NOV/DEC 2012), (May / June 2016), (Nov / Dec 2015)**
   (OR)
   Outline the charge carrier diffusion phenomenon across a PN junction. Explain the effect of forward and reverse biasing on the depletion region. (Nov/Dec 2018 R-13) (April / May 2019-R17)

A **PN junction** is formed from a piece of semiconductor (Ge or Si) by diffusing p-type material (Acceptor impurity Atoms) to one half side and N type material to (Donar Impurity Atoms) other half side. The plane dividing the two zones is known as 'Junction'.

The P-region of the semiconductor contains a large number of holes and N region, contains a large number of electrons. A PN junction just immediately formed is shown in Fig.

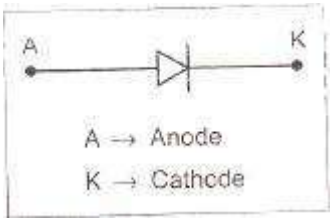


When PN junction is formed, there is a tendency for the electrons in the N-region to diffuse into the p-region, and holes from P-region to N-region. This process is called diffusion. While crossing the junction, the electrons and holes recombines with each other, leaving the immobile ions in the neighborhood of the junction neutralized as shown in Fig.



These immobile + ve and –ve ions, set up a potential across the junction. This potential is called potential barrier or junction barrier. Due to the potential barrier no further diffusion of electrons and holes takes place across the junction. Potential barrier is defined as a potential difference built up across the PN junction which restricts further movement of charge carriers across the junction. The potential barrier for a silicon PN junction is about 0.7 volt, whereas for Germanium PN junction is approximately 0.3 volt.

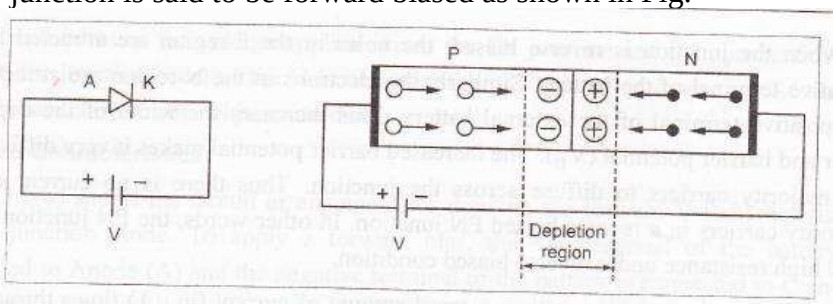
Symbol of Diode:
The symbol of PN junction diode is shown in Fig. The P-type and N-type regions are referred to as Anode and Cathode respectively. The arrowhead shows the conventional direction of current flow when the diode is forward biased.



Working of PN Junction Diode:

Forward Bias:

When the positive terminal of the external battery is connected to the P-region and negative terminal to the N-region, the PN junction is said to be forward biased as shown in Fig.

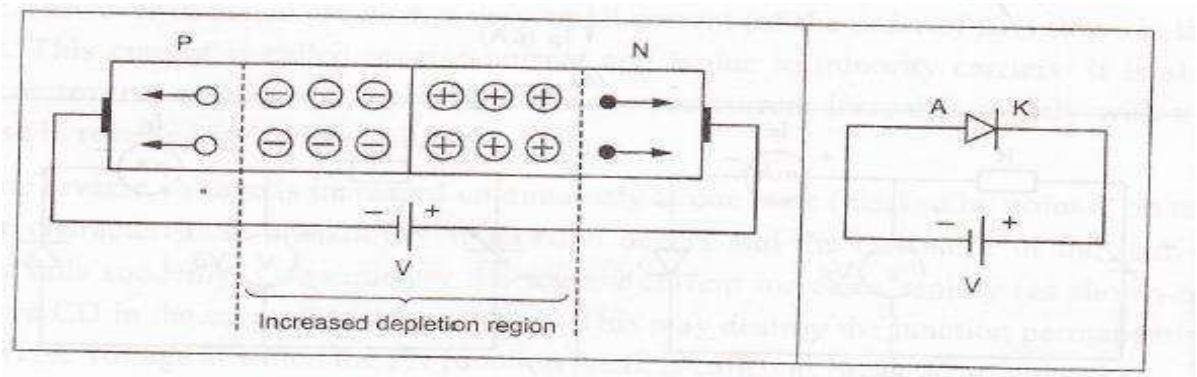


When the junction is forward biased, the holes in the p-region are repelled by the positive terminal of the battery and are forced to move towards the junction. similarly, the electrons in the N-region are repelled by the negative terminal of the battery and are forced to move towards the-junction.

This reduces the width of the depletion layer and barrier potential. If the applied voltage is greater than the potential barrier v_r, then the majority carriers namely holes in P-region and electrons in N-region, cross the barrier. During crossing some of the charges get neutralized the remaining charges after crossing, reach the other side and constitute current in the forward direction. The PN junction offers very low resistance under forward biased condition.

Since the barrier potential is very small (nearly 0.7 V for silicon and 0.3 V for Germanium junction), a small forward voltage is enough to completely eliminate the barrier. once the potential barrier is eliminated by the forward voltage, a large current start flowing through the PN junction.

Reverse Bias:



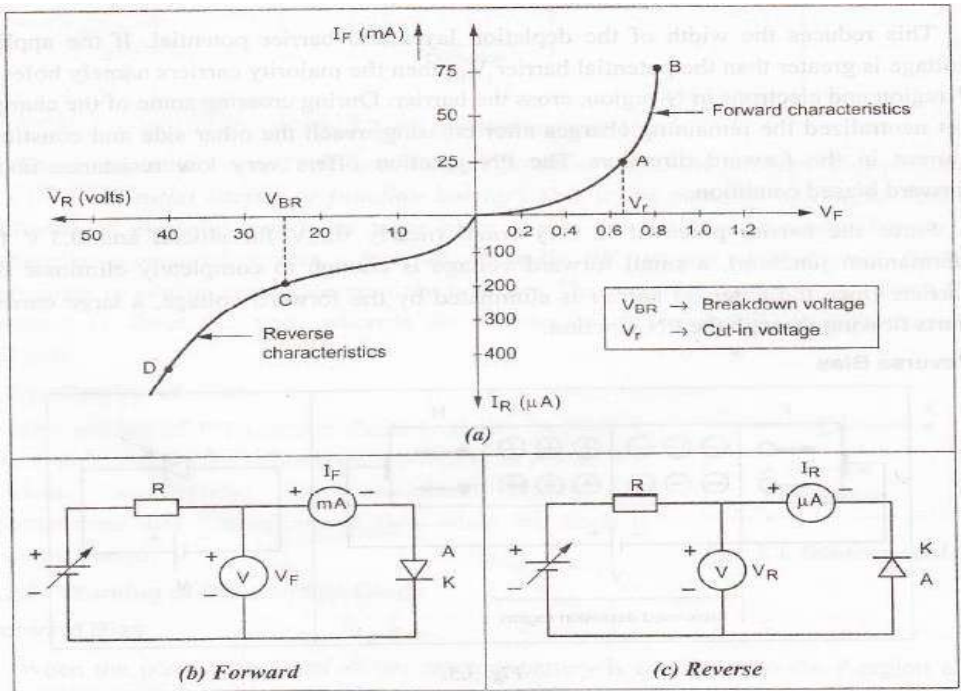
When the positive terminal of the external battery is connected to the N-region and negative terminal to the p-region, the PN junction is said to be reverse biased. When the junction is reverse biased, the holes in the P-region are attracted by the negative terminal of the battery. Similarly, the electrons in the N-region

are attracted by the positive terminal of the external battery. This increases the width of the depletion layer and barrier potential (Vs).

The increased barrier potential makes it very difficult for the majority carriers to diffuse across the junction. Thus, there is no current due to majority carriers in a reverse biased PN junction. In other words, the PN junction offers very high resistance under reverse biased condition.

In a reverse biased PN junction, a small amount of current (in μA) flows through the junction because of minority carriers. (i.e., electrons in the P-region and holes in the N region).The reverse current is small because the number of majority carrier in both regions is small.

V-l characteristics of PN-Junction Diode:



A graph between the voltage applied across the PN junction and the current flowing through the junction is called the V-I characteristics of PN junction diode. Fig. shows the V-I characteristics of PN junction diode.

Forward Characteristics:

Fig. (a) shows the circuit arrangement for drawing the forward V-I characteristics of PN junction diode. To apply a forward bias, the +ve terminal of the battery is connected to Anode (A) and the negative terminal of the battery is connected to Cathode (K). Now, when supply voltage is increased the circuit current increases very slowly and the curve is nonlinear (region-OA).

The slow rise in current in this region is because the external applied voltage is used to overcome the barrier potential (0.7 V for Si; 0.3V for Ge) of the PN junction' However once the potential barrier is eliminated and the external supply voltage is increased further, the current flowing through the PN junction diode increases rapidly (region AB). This region of the curve is almost linear. The applied voltage should not be increased beyond a certain safe limit, otherwise the diode will burnout.

The forward voltage at which the current through the PN junction starts increasing rapidly is called by **knee voltage**. It is denoted by the letter V_B.

Reverse Characteristics:

Fig (b) shows the circuit arrangement for drawing the reverse V-I characteristics of PN junction diode. To apply a reverse bias, the +ve terminal of the battery is connected to cathode (K) and - ve terminal of the battery is connected to anode (A).

Under this condition the potential buried at the junction is increased. Therefore, the junction resistance becomes very high and practically no. current flows through the circuit. However, in actual practice, a very small current (of the order of μA) flows in the circuit. This current is called reverse current and is due to minority carriers. It is also called as reverse saturation current (I). The reverse current increases slightly with the increase in reverse bias supply voltage.

If the reverse voltage is increased continuously at one state (marked by point C on the reverse characteristics) breakdown of junction occurs and the resistance of the barrier regions falls suddenly. Consequently, the reverse current increases rapidly (as shown by the curve CD in the current) to a large value. This may destroy the junction permanently. The reverse voltage at which the PN junction breaks is called as break down voltage.

Temperature effects

The cut in voltage decreases as the temperature increases. The reverse saturation current increases.

$I_{02} = 2^{(\Delta T/10)} I_{01}$

I_{01},I_{02} are the reverse current at $T_1^{\circ}C$, $T_2^{\circ}C$

$\Delta T = T_2 - T_1$.

The voltage equivalent of temperature V_T also increases. The reverse breakdown voltage increases.

2. Derive the PN diode current equation.

The applied voltage and current though diode are related by the equation

$$I = I_0 \left(e^{V/yV_T} - 1\right)$$

Where,

Io = Reverse saturation current
V = Applied voltage
I = Diode current
VT = Volt equivalent temperature

$$V_T = \frac{kT}{q}$$

$k = 1.38*10^{-23}$ J/K
T = temperature of the diode junction
I = diode current
Q = change of electron $1.602*10^{-19}$ C
At any temperature

$$V_T = \frac{\bar{k}T}{q} = \frac{1.38 \times 10^{-23}}{1.602 \times 10^{-19}} = \frac{T}{11600}$$

At room temperature

$$V_T = \frac{300}{11600} = 26mV$$

The value of η=1 for germanium and 2 for silicon.

For forward bias voltage the current equation reduces to

$$I = I_0 \left(e^{V/yV_T}\right)$$

At room temperature for germanium transistor

$$I = I_0(e^{40})$$

When the diode is reverse biased

$$I = I_0 \left(e^{V/yV_T} - 1\right)$$

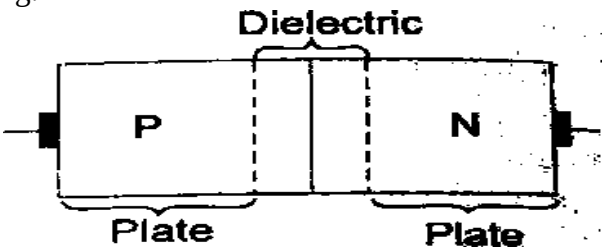
$$I \cong I_0$$

Diffusion and transient capacitance

3. Explain diffusion and transition capacitance of diode

Depletion layer capacitance (or) transition capacitance (or) space charge capacitance (May / June 2016)(Nov/Dec 2016)(May 2017)

• When a PN junction is reverse biased, a layer of positive and negative immobile ions, called depletion layer, is formed on either side of the junction. It is also known as depletion-region, space-charge region or transition region. The depletion-layer acts as a dielectric *(i.e.*, non-conductive) medium between P-region and N-region. We know that the P-region and N-region on either side of the junction, has a low resistance. Therefore, these regions act as two plates of a capacitor, separated by a dielectric *(i.e.*, depletion layer) as shown in Fig.



The capacitance formed in a junction area is called depletion layer capacitance. It is also called depletion region-capacitance, space charge capacitance, transition region capacitance or simply junction capacitance.

• Since the depletion layer width *(d)* increases with the increase in reverse bias voltage, the resulting depletion layer capacitance will decrease with the increased reverse bias.

• The depletion layer capacitance depends upon the nature of a PN junction, semiconductor material and magnitude of the applied reverse voltage. It is given by the relation,

$$C_T = \frac{K}{(V_B - V)^n}$$

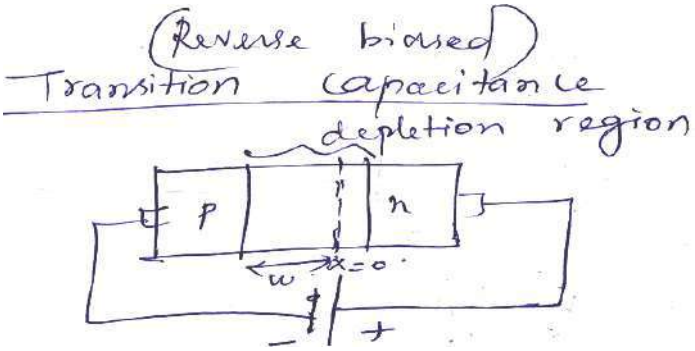
Where
K = A constant, depending upon the nature of semiconductor material
VB = barrier voltage. 0.6V for silicon and 0.3V for germanium
V = applied reverse voltage
n a constant depending upon the nature of junction.
The value of the K is

$$K = A \times \frac{\epsilon.q}{2}\left(\frac{N_A.N_D}{N_A+N_D}\right)$$

• The value of 'n' is taken as 1/2 for step or abrupt junction, 1/3 for linearly graded junction.

• It is the evident from the above relation that the value of depletion layer capacitance (CT) can be controlled by varying the applied reverse voltage. This property of variable capacitance, possessed by reverse biased PN junction, is used in the concentration of a device called varactor.
Reverse biased.

Derivation:



Connection P side is less
Doping less in P side (N_A)
N side (N_D)
Potential & change density Relation

$$N_A < N_D \frac{d^2V}{dx^2} \text{----------1}$$

X – distance measured from junction

$$N_A < N_D \frac{d2V}{dx^2} = \frac{qND}{s} \text{----------} \quad \varepsilon \rightarrow \varepsilon_o\varepsilon_r \quad 2$$

Integrating 2

$$\int \frac{d^2V}{dx^2} = \int \frac{qN_D}{\varepsilon}$$

$$\frac{dv}{dx} = \frac{qN_AX}{\varepsilon}$$

To get potential from 0 to w

$$\int_o^{V_B} \frac{dv}{dx} = \int_o^{w} \frac{qN_AX}{\varepsilon} dx$$

Where $V=V_B$

X=w

$$V_B = \frac{qN_A}{s} \times \frac{w^2}{2} \quad \text{----------} 3$$

$$W = \sqrt{V_B}$$

Q=No of change particle × change on each particle

$=(N_A \times \text{volume}) \times q$

$Q = qN_AAW$ 2

Diff 3 w.r.to V

$$V_B = \frac{qN_A}{\varepsilon} \times \frac{w^2}{2}$$

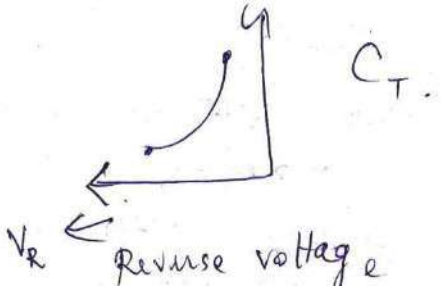
$$1 = \frac{qN_A}{s} \times \frac{1}{2}\frac{dw}{dv} 2w$$

$$\frac{dw}{dv} = \frac{\varepsilon}{qN_Aw}$$

Diff 2

$$\frac{dQ}{dv} = qN_AA\frac{dw}{dv}$$

$$C_T = qN_AA\frac{\varepsilon}{qN_Aw} = \frac{A\varepsilon}{w}$$



Ex : Varactor diode (or) Tuning diode

Diffusion capacitance C_D:(May 2017)

The junction behaves like a capacitor. The capacitance, which exists in a forward-biased junction is called a *diffusion* or *storage capacitance.* It is different from the transition or depletion layer capacitance, which exists in a reverse-biased junction. The diffusion capacitance arises due to the arrangement of minority carrier density. And its value is much larger than the depletion layer capacitance.

Width of depletion region ↓ As applied voltage ↑, the concentration of injected charged particle also increases. This rate of change of injected change with applied voltage is capacitance.

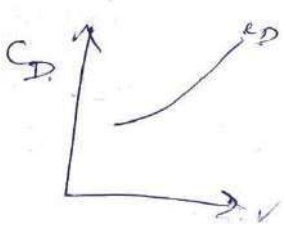
r = mean lifetime of the carrier

I = value of forward current

η = A constant (1 for Ge and 2 for Si)

V_T=volt equivalent of temperature.

$$C_D = \frac{dQ}{dv}$$



$C_D$is $> C_T$

$I = I_{pn(0)} + I_{np(0)}$

$I_{pn(0)}$ → hole diffusion current n region

$I_{np(0)}$ → electron diffusion current in p region

$$I_{np\,(0)} \backsimeq 0$$

P side heavily doped

$$J_{p(X)} = -qD_p \frac{dp_n}{dx}$$

$$J = \frac{I}{A}$$

$I_p(X) = -qAD_p \frac{dp_n}{dx}$ ----------1

$P_n(X) = P_{n(0)} e^{-X/LP}$----------2

Hole concentration in the right side of p material $P_{n(0)}$ ie junction

Diff 2

$$\frac{dp_n(x)}{dx} = P_{n(0)} e_{-X/L^P} \left(\frac{1}{L_P}\right)$$

$I_p(X) = -qAD_pP_{n(0)}e^{-X/LP}$. -1/L_P

At x=0 $I_p(X) = I_{pn(0)} = I$

$$I = \frac{QAD_P}{L_P} Pn\,(0)$$

$Pn(0) = \frac{I\,L_P}{QAD_P}$----------A

Now the excess minority charge exists only on n side and given by

$Q = \int_0^\infty Aq\,Pn(0)e^{-X/LP}dx$

$= AqPn(0)\left[\frac{e^{-X/L_P}}{\frac{-1}{L_P}}\right]_0^\infty$

$= AqLpPn(0)[e^{-\infty} - e^{-0}]$

$Q = -AqLpPn(0)$

$Q = AqLpPn(0)$----------B

Put A in B

$Q = \frac{AqLpIL_P}{qADp} = \frac{L_P^2}{Dp}.I$

Assume

$$\frac{L_P^2}{Dp} = r$$

$Q = rI \Rightarrow \frac{dQ}{dI} = r$

W.K.T

$$C_D = \frac{dQ}{dI} \cdot \frac{dI}{dV}$$

$$C_D = r.\frac{dI}{dV}$$

$$I = I_o(e^{V/DVT})$$

$$\frac{dI}{dV} = I.\frac{1}{\eta V_T}$$

$$C_D = r.\frac{I}{\eta V_T}$$

It is evident from the above relation, that diffusion capacitance is directly proportional to the forward current *(I).*

Rectifiers – Half Wave and Full Wave

Half Wave

4. What is halfwave rectifier? Explain the working principle with neat sketch? (Nov / Dec 2015) (Nov/Dec 2016)

Rectifiers *are a class of circuits whose purpose is to convert ac waveforms (usually sinusoidal and with zero average value) into a waveform that has a significant non-zero average value (dc component)*. Simply stated, rectifiers are ac-to-dc energy converter circuits. Most rectifier circuits employ diodes as the principal elements in the energy conversion process; thus, the almost inseparable notions of diodes and rectifiers.

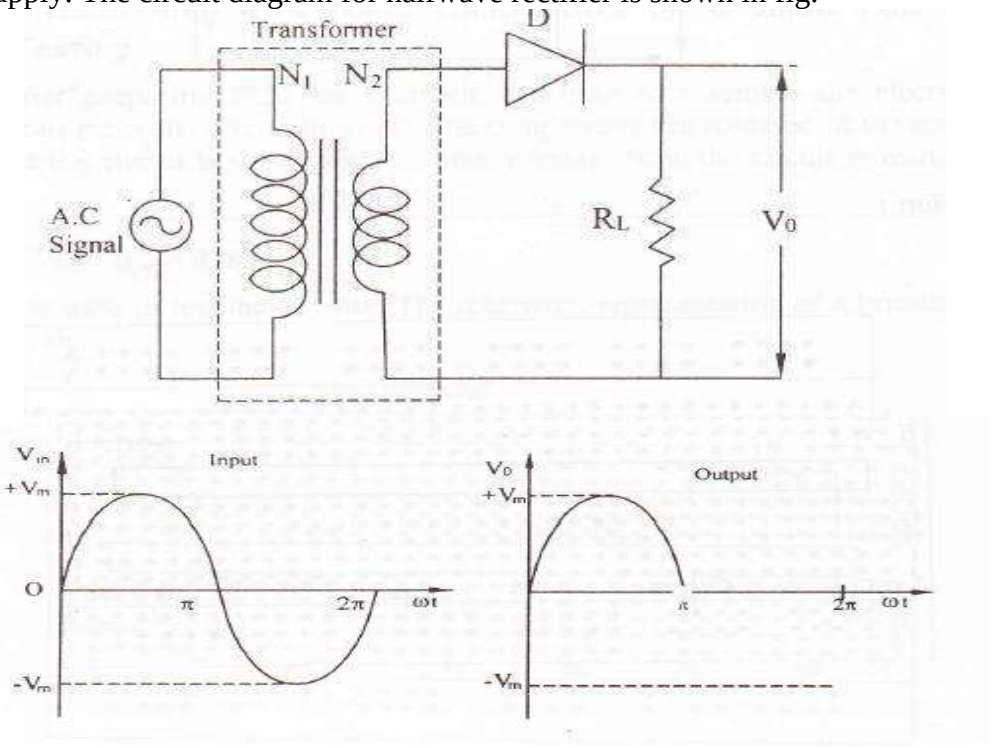
Uncontrolled rectifier: *uncontrolled* refers to the absence of any control signal necessary to operate the primary switching elements (diodes) in the rectifier circuit. (The discussion of controlled rectifier circuits, and the controlled switches themselves, is more appropriate in the context of power electronics applications). Rectifiers are the fundamental building block in dc power supplies of all types and in dc power transmission used by some electric utilities.

There are two types of rectifiers:

(a) Half Wave (HW) rectifier (b) Full Wave (FW) rectifier

Half -wave Rectifier:

It consists of a single diode in series with a load resistor. The input to half wave rectifier is supplied from the 50 Hz a.c supply. The circuit diagram for halfwave rectifier is shown in fig.



Positive half cycle:

During the positive half cycle of the input signal the *anode of the diode becomes positive with respect to the cathode* and hence the diode D conducts. For an ideal to the cathode and hence the diode D conducts. For an ideal diode, the forward voltage drop is zero. So the whole-input voltage will appear across load resistance R_L.

Negative half cycle:
During negative half cycle of the input signal, the *anode of the diode becomes negative with respective to the cathode* and hence the diode D does not contact. For an ideal diode the impedance by the diode is infinity. So the whole input voltage appears across the diode D. hence the voltage drop across R, is zero.

Analysis of Half wave rectifier:

Let Vi be the input voltage to the rectifier

$$V_i = V_m sin\omega t$$

Where,
V_m = Maximum value of the input voltage.
Let I be the current flowing though the circuit when the diode is conducting.

$$i = \begin{cases} I_m sin\omega t & For\ 0 \le \omega t \le \pi \\ 0 & For\ \pi \le \omega t \le 2\pi \end{cases}$$

Where

$$I_m = Maximum\ value\ of\ the\ current$$

$$I_m = \frac{V_m}{R_F + R_L}$$

Where
R_F-Forward dynamic resistance of diode.
R_L-Load resistance.

(a) Average or DC value of output current (I_{dc}):
From Fig., it is seen that the output current is not steady but contains fluctuations even though it is DC current. The average value of this fluctuating current is called DC current (I_{dc}). It can be calculated as follows.

Average value = (Area under the curve / Period)

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i\, d(\omega t)$$

$$I_{dc} = \frac{1}{2\pi}\left[\int_0^{\pi} I_m * \sin\omega t\, d(\omega t)\right]$$

$$I_{dc} = \frac{1}{2\pi}[-\cos\omega t]_0^{\pi} = \frac{I_m}{2\pi}[-\cos\pi - (-\cos 0)] = \frac{I_m}{2\pi}[-(-1) - (-1)] = \frac{I_m}{\pi}$$

$$I_{dc} = \frac{V_m}{\pi(R_F + R_L)}$$

(b) Average or DC output voltage (V_o):

$$V_{dc} = \frac{I_m}{\pi} \times R_L = \frac{V_m}{\pi}$$

(c) RMS value of output current (I_{rms}):

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} i^2 d(\omega t)} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2\omega t * d(\omega t)} = \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi} \left(\frac{1-\cos 2\omega t}{2}\right) * d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{4\pi}\int_0^{\pi} d(\omega t) - \int_0^{\pi} \cos 2(\omega t) * d(\omega t)} = \sqrt{\frac{I_m^2}{4\pi}\left[\omega t_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]}$$

$$= \sqrt{\frac{I_m^2}{4\pi}\left[(\pi - 0) - \left(\frac{\sin 2\pi}{2} - \frac{\sin 0}{2}\right)\right]} = \sqrt{\frac{I_m^2}{4\pi}[(\pi - 0) - 0]} = \sqrt{\frac{I_m^2}{4\pi}} = \frac{I_m}{2}$$

(d) Rectification Efficiency (η):

Rectification efficiency **(η)** $= \frac{I_{dc}^2 \times R_L}{I_{rms}^2 \times R_L} = \frac{\frac{I_m^2}{\pi^2} \times R_L}{\frac{I_m^2}{2} \times R_L} = \frac{I_m^2/\pi^2 \times R_L}{I_m^2/4 \times R_L} = \frac{4}{\pi^2} = 0.406$

(e) Ripple Factor (γ):

$$y = \frac{I'_{rms}}{I_{dc}} = \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I_{dc}^2}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{I_{rms}/2}{I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1} = \mathbf{1.21}$$

(f) Peak inverse Voltage (PIV):

Peak inverse voltage is defined as the maximum voltage that is applied across the Diode when the diode is reverse biased. [n case of half wave rectifier, maximum Voltage across the diode when it is not conducting is equal to V_m.

$$\boldsymbol{PIV = V_m}$$

(g) From factor:

$$FF = \frac{rms\ value}{average\ value} = \frac{\pi}{2} = 1.57$$

(h) Peak factor:

$$PF = \frac{V_m}{\left(\frac{V_m}{2}\right)} = 2$$

(i) Transformer utilization factor:

$$TUF = \frac{P_{dc}}{P_{ac}}(Transformer\ secondary\ rated) = 0.287$$

Disadvantages of HWR:

- Low output because one half cycle only delivers output
- A.C. component more in the output
- Requires heavy filter circuits to smooth out the output **Peak inverse Voltage.**

Rectifiers – Full Wave using center tap Transformer

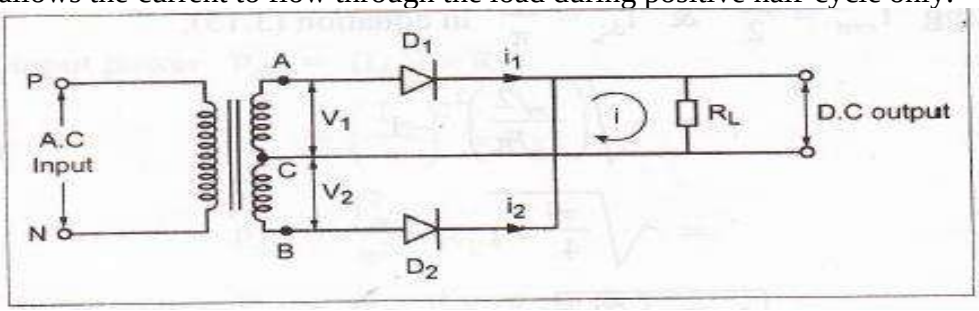
5. Explain the operation of full wave rectifier with center tap transformer. Also derive the following for this rectifier. (Apr/May 2018)

i) DC output voltage (average value) ii) DC output current (average value) iii) RMS output voltage.

In FWR, current flows through the load during both half cycles of the input a.c. supply. Like the half wave circuit, a *full wave rectifier circuit produces an output voltage or current which is purely DC or has some specified DC component*. Full wave rectifiers have some fundamental advantages over their half wave rectifier counterparts. The average (DC) output voltage is higher than for half wave, the output of the full wave rectifier has much less ripple than that of the half wave rectifier producing a smoother output waveform.

Full Wave Rectifier:

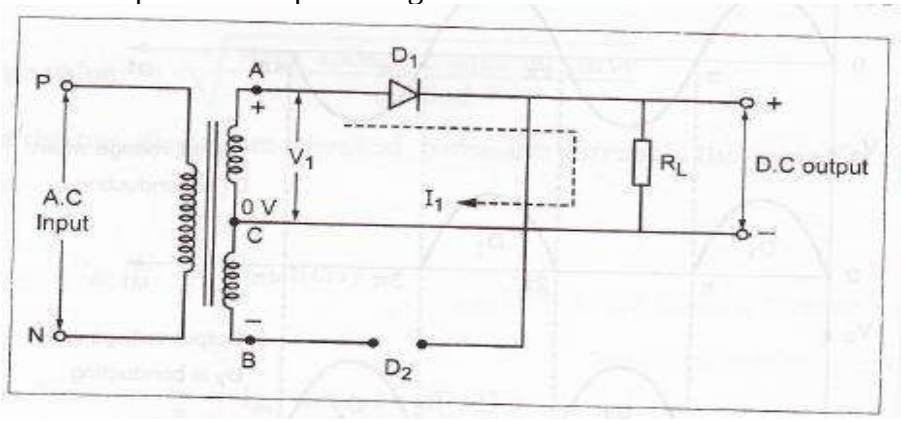
A full wave rectifier is an electronic circuit which converts AC voltage into a pulsating DC voltage using both half cycles of the applied AC voltage. A full wave rectifier is a circuit which allows a unidirectional current to flow through the load during the entire input cycle as shown in fig. The result of full wave rectification is a d.c. output voltage that pulsates every half-cycle of the input. On the other hand a half wave rectifier allows the current to flow through the load during positive half-cycle only.



Positive half cycle:

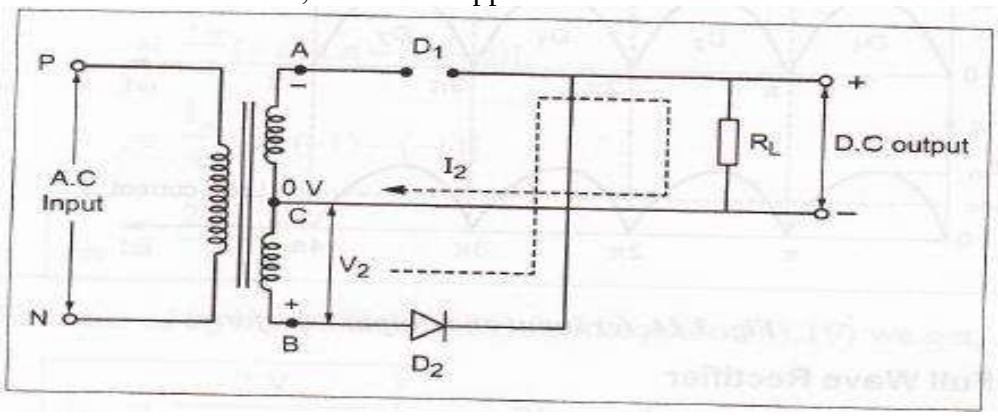
The circuit uses two diodes which are connected to secondary winding of the transformer. The input signal is applied to the primary winding of the transformer. During the positive input half cycle, the polarities of the secondary voltage is shown in fig. This forward bias the diode D, and reverse biases the diode D_1. As a result of this, the diode D, conducts some current whereas the diode D, is off.

The current through load R1 is as indicated in through D_1, and the voltage Drop across R_L will the fig. The load current flows be equal to the input voltage.



Negative half cycle:

During the negative input half cycle, the polarities of the secondary voltage are interchanged. The reverse-bias the diode D, and forward Biases the diode D_2. As a result of this, the diode D_1 is OFF and the diode D_2 conducts some current. The current through the load R, is an indicated in the fig. The load current flows through D_2 and the voltage drop across R_1 will be equal to the input voltage. The maximum efficiency of a fall-wave rectifier is 8l,2%Vo and ripple factor is 0.48.



Analysis of Full Wave Rectifier:

Let Vi be the input voltage to the rectifier, $V_i = V_m sin\omega t$

Where, V_m = Maximum value of the input voltage.

Let I be the current flowing though the circuit when the diode is conducting.

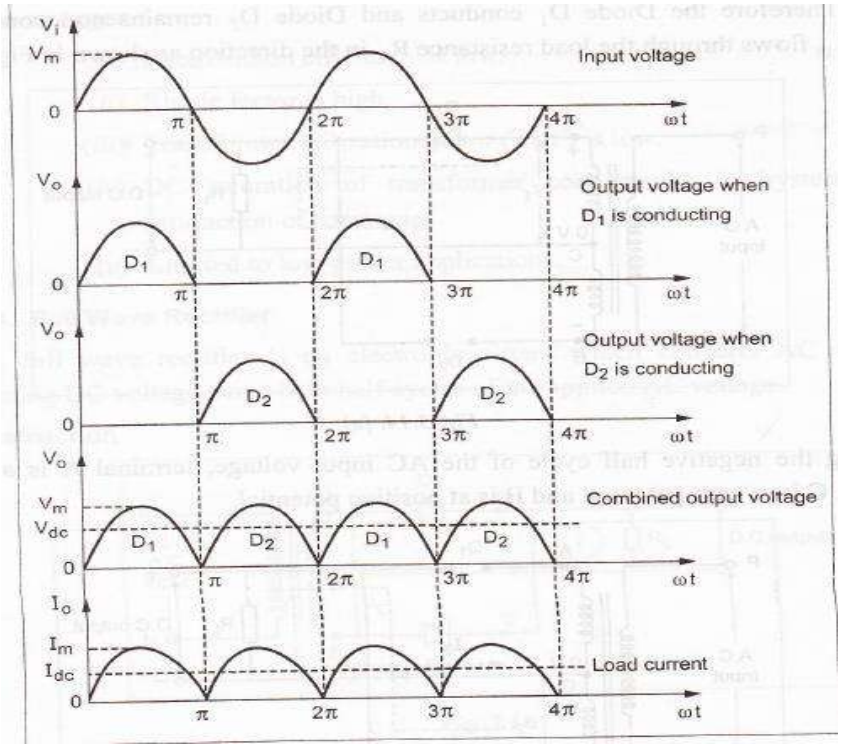
$$i = \begin{cases} I_m sin\omega t & For\ 0 \le \omega t \le \pi \\ 0 & For\ \pi \le \omega t \le 2\pi \end{cases}$$

Where, $I_m = Maximum\ value\ of\ the\ current; = \frac{V_m}{R_F + R_L}$

I_m

Where, R_F-Forward dynamic resistance of diode; R_L-Load resistance.

Input and output waveforms:



(a) Average or DC value of output current (I_{dc}):

Average value = (Area under the curve / Period)

$$I_{dc} = \frac{1}{\pi}\int_0^{\pi} i\, d(\omega t)$$

$$I_{dc} = \frac{1}{\pi}\left[\int_0^{\pi} I_m * \sin\omega t\, d(\omega t)\right]$$

$$I_{dc} = \frac{1}{\pi}[-\cos\omega t]_0^{\pi} = \frac{I_m}{\pi}[-\cos\pi - (-\cos 0)] = \frac{I_m}{\pi}[-(-1) - (-1)] = \frac{2I_m}{\pi}$$

$$I_{dc} = \frac{2V_m}{\pi(R_F + R_L)}$$

(b) Average or DC value of output voltage (V_{dc}) :

$$V_{dc} = \frac{2I_m}{\pi} \times R_L = \frac{2V_m}{\pi}$$

(c) RMS value of output current (I_{rms}):

$$I_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i^2 d(\omega t)} = \sqrt{\frac{1}{\pi}\int_0^{\pi} I_m^2 \sin^2\omega t * d(\omega t)} = \sqrt{\frac{I_m^2}{\pi}\int_0^{\pi} \left(\frac{1-\cos 2\omega t}{2}\right) * d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi} d(\omega t) - \int_0^{\pi} \cos 2(\omega t) * d(\omega t)} = \sqrt{\frac{I_m^2}{2\pi}\left[\omega t_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\left[(\pi - 0) - \left(\frac{\sin 2\pi}{2} - \frac{\sin 0}{2}\right)\right]} = \sqrt{\frac{I_m^2}{2\pi}[(\pi - 0) - 0]} = \sqrt{\frac{I_m^2}{2}} = \frac{I_m}{\sqrt{2}}$$

(d) Rectification Efficiency (η):

Rectification efficiency **(η)** $= \frac{I_{dc}^2 \times R_L}{I_{rms}^2 \times R_L} = \frac{\frac{2I_m}{\pi}^2 \times R_L}{\frac{I_m^2}{\sqrt{2}} \times R_L} = \frac{4I_m^2/\pi^2 \times R_L}{I_m^2/2 \times R_L} = \frac{0.812}{(1+\frac{R_F}{R_L})} = 81.2\%$

(e) Ripple Factor (γ):

$$y = \frac{\text{RMS value of Ac component}}{\text{Dc value of wave}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = \mathbf{0.48}$$

(f) Peak inverse Voltage (PIV):

Peak inverse voltage is the maximum possible voltage across a diode when it is not conducting. During positive half cycle of the AC input voltage Diode D1, is conducting and Diode D, is not conducting. In this case a voltage V, is developed across the load resistor R_1. Now the voltage across the non-conducting Diode D, is the sum of the voltage across R1 and voltage across the lower half of transformer secondary V_m.

Hence, PIV of Diode D2 = $V_m + V_m = 2V_m$

Similary, PIV of Diode D1 = $V_m + V_m = 2V_m$

Advantages:
1. The D.c load voltage and current are more than halfwave.
2. No D.c current thro transformer windings hence no possibility of saturation.
3. TUF is better.
4. Efficiency is higher.
5. Ripple factor less.

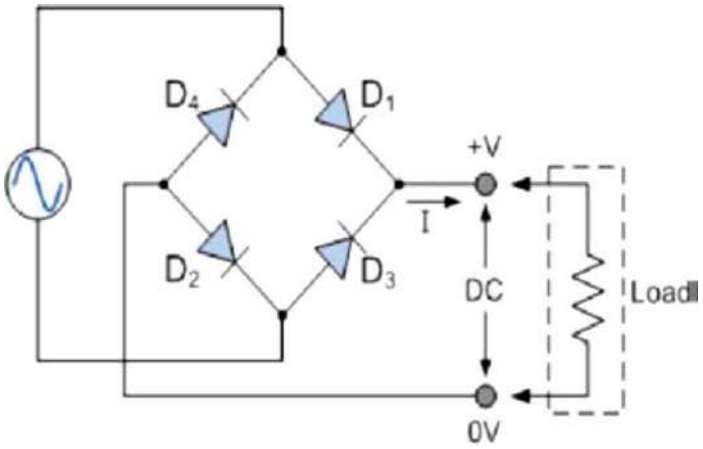
Disadvantages:
1. PIV rating of diode is higher
2. Higher PIV diodes are larger in size ad costlier.
3. Cost of transformer is high.

Rectifiers – Full Wave Bridge type

6. (a) Draw the circuit diagram and explain the working of full wave bridge rectifier & derive the expansion for average amount current & rectification efficiency. (May 2017) (Nov/Dec 2017) (Nov/Dec 2018)

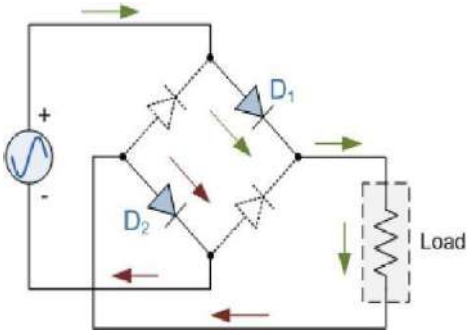
Bridge rectifier (Full Wave Bridge rectifier):

Another type of circuit that produces the same output waveform as the full wave rectifier circuit above is that of the **Full Wave Bridge Rectifier**. This type of single-phase rectifier uses four individual rectifying diodes connected in a closed loop "bridge" configuration to produce the desired output. The main advantage of this bridge circuit is that it does ***not require a special center tapped transformer***, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown below.

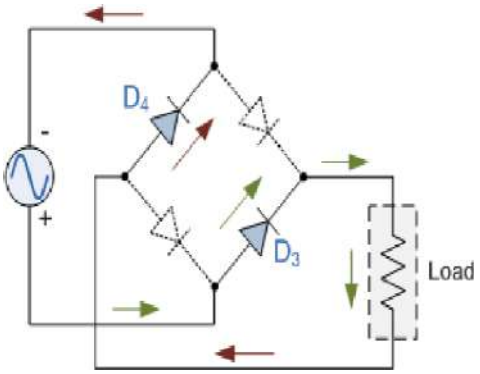


The four diodes labeled D1 to D4 are arranged in "series pairs" with only two diodes conducting current during each half cycle. *During the positive half cycle of the supply, diodes D1 and D2 conduct* in series while diodes D3 and D4 are reverse biased and the current flows through the load as shown below.

During the negative half cycle of the supply, diodes D3 and D4 conduct in series, but diodes D1 and D2 switch of as they are now reverse biased. The current flowing through the load is the same direction as before. As the current flowing through the load is unidirectional, so the voltage developed across the load is also unidirectional the same as for the previous two diode full-wave rectifier.

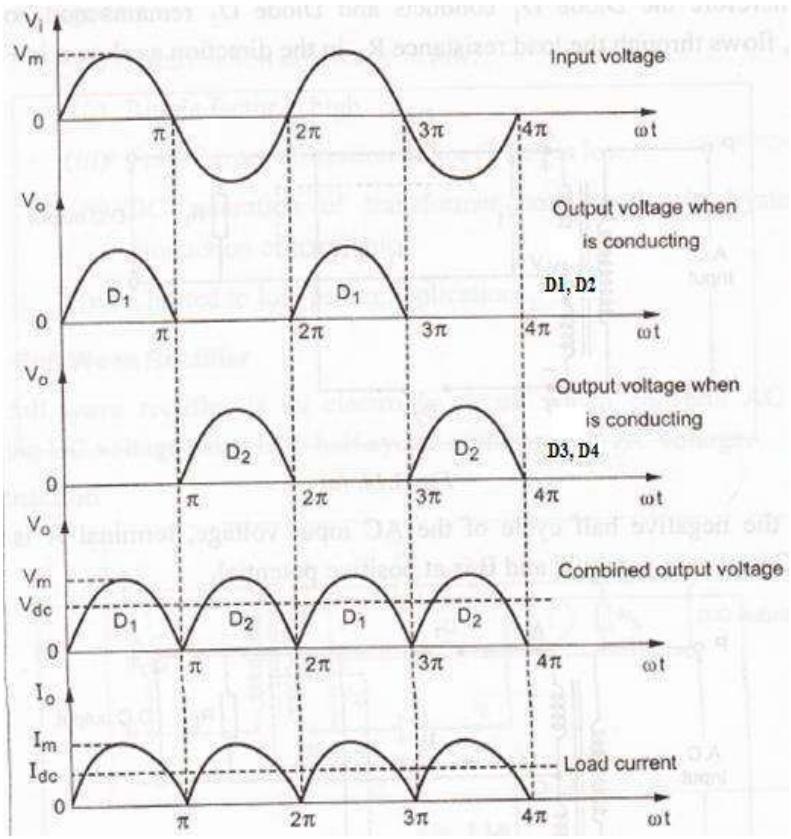


Positive half cycle



Negative half cycle

Waveform:



Analysis of Full Wave Rectifier:

Let Vi be the input voltage to the rectifier, $V_i = V_m sin\omega t$
Where,
V_m = Maximum value of the input voltage.
Let I be the current flowing though the circuit when the diode is conducting.

$$i = \begin{cases} I_m sin\omega t & For\ 0 \le \omega t \le \pi \\ 0 & For\ \pi \le \omega t \le 2\pi \end{cases}$$

Where

$$I_m = Maximum\ value\ of\ the\ current$$

$$I_m = \frac{V_m}{R_F + R_L}$$

Where, R_F-Forward dynamic resistance of diode; R_L-Load resistance.

(a) Average or DC value of output current (I_{dc}):

Average value = (Area under the curve / Period)

$$I_{dc} = \frac{1}{\pi}\int_0^{\pi} i\, d(\omega t) \qquad I_{dc} = \frac{1}{\pi}[\int_0^{\pi} I_m * \sin\omega t\, d(\omega t)]$$

$$I_{dc} = \frac{1}{\pi}[-\cos\omega t]_0^{\pi} = \frac{I_m}{\pi}[-\cos\pi - (-\cos 0)] = \frac{I_m}{\pi}[-(-1) - (-1)] = \frac{2I_m}{\pi}$$

$$I_{dc} = \frac{2V_m}{\pi(R_F + R_L)}$$

(b) Average or DC value of output voltage (V_{dc}): $V_{dc} = \frac{2I_m}{\pi} \times R_L = \frac{2V_m}{\pi}$

(c) RMS value of output current (I_{rms}):

$$I_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i^2 d(\omega t)} = \sqrt{\frac{1}{\pi}\int_0^{\pi} I_m^2 \sin^2\omega t * d(\omega t)} = \sqrt{\frac{I_m^2}{\pi}\int_0^{\pi} \left(\frac{1-\cos 2\omega t}{2}\right) * d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi} d(\omega t) - \int_0^{\pi} \cos 2(\omega t) * d(\omega t)} = \sqrt{\frac{I_m^2}{2\pi}[\omega t_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}]}$$

$$= \sqrt{\frac{I_m^2}{2\pi}[(\pi - 0) - \left(\frac{\sin 2\pi}{2} - \frac{\sin 0}{2}\right)]} = \sqrt{\frac{I_m^2}{2\pi}[(\pi - 0) - 0]} = \sqrt{\frac{I_m^2}{2}} = \frac{I_m}{\sqrt{2}}$$

(d) Rectification Efficiency (η):

Rectification efficiency **(η)** $= \frac{I_{dc}^2 \times R_L}{I_{rms}^2 \times R_L} = \frac{\frac{2I_m}{\pi}^2 \times R_L}{\frac{I_m}{\sqrt{2}}^2 \times R_L} = \frac{4I_m^2/\pi^2 \times R_L}{I_m^2/2 \times R_L} = \frac{0.812}{(1+\frac{R_F}{R_L})} = 81.2\%$

(e) Ripple Factor (γ):

$$y = \frac{\text{RMS value of Ac component}}{\text{Dc value of wave}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = \mathbf{0.48}$$

(f) Peak inverse Voltage (PIV):

Peak inverse voltage is the maximum possible voltage across a diode when it is not
Conducting. During positive half cycle of the AC input voltage Diode D1, is conducting and Diode D, is not conducting. In this case a voltage V, is developed across the load resistor R_1. Now the voltage across the non-conducting Diode D, is the sum of the voltage across R1 and voltage across the lower half of transformer secondary V_m.
Hence, PIV of Diode D2 = $V_m + V_m = 2V_m$
Similary, PIV of Diode D1 = $V_m + V_m = 2V_m$

Advantages:

1. The D.c load voltage and current are more than half wave.
2. No D.c current thro transformer windings hence no possibility of saturation.
3. TUF is better.
4. Efficiency is higher.
5. Ripple factor less.
6. No centre tapped is required.

Disadvantages:

4 diodes are used therefore voltage drop across the diode is increased. This reduces output voltage.

Applications:
1. In power supply circuits.
2. Used as rectifier in power circuits to convert A.C to D.C

(b) In a bridge rectifier circuit, input supply is 230V, 50 Hz. Primary to secondary turns ratio is 4:1, load resistance is 200 Ω. The diodes are ideal. Find DC output voltage, PIV and output signal frequency. (Nov / Dec 2018-R17)

Solution: $E_{py}(rms) = 230V, \frac{N_2}{N_1} = \frac{1}{4}, R_L = 200\Omega \quad R_f = R_s = 0\Omega \; as \; ideal$

$$\frac{E_{py}(rms)}{E_{sy}(rms)} = \frac{N_1}{N_2}, \; E_{sy}(rms) = \frac{N_1}{N_2} X E_{py}(rms) = \frac{1}{4} X 230 = 57.5 V,$$

$$E_{sy\,(max)} = \sqrt{2}\, E_{py\,(rms)} = \sqrt{2}\, X\, 57.5 = 81.31 V$$

$$I_m = \frac{E_{sm}}{R_s + 2R_f + R_L} = \frac{81.31}{200} = 0.4065 A \quad I_{DC} = \frac{2 I_m}{\pi} = \frac{2 X 0.4065}{\pi} = 0.2587 A$$

$$E_{DC} = I_{DC} R_L = 0.2587 X 200 = 51.74 V$$

PIV = E_{sm} = 81.31V (for full wave rectifier)

Output signal frequency = $2f_s$ = 2 X 50 = 100Hz

$$\text{Ripple Factor (for Full Bridge Rectifier)} = 0.482,$$

$$\text{Ripple Factor} = \frac{AC\ rms\ output}{DC\ output} = \frac{Ripple\ Voltage}{E_{DC}} \quad 0.482 = \frac{Ripple\ Voltage}{51.74}$$

i.e. Ripple voltage = 51.74 X 0.482 = 24.94 V

7. Compare different types of rectifiers?

Type	HW	CT FW	FW BR
No of diodes used	1	2	4
Need of transformer	Not necessary	Necessary	Not necessary
Ripple factor	1.21	0.48	0.48
Efficiency	40.6%	81.2%	81.2%
PIV	V_m	$2V_m$	V_m
TUF	0.287	0.812	0.693
From factor	1.57	1.11	1.11
Peak factor	2	$\sqrt{2}$	$\sqrt{2}$
Ripple frequency	f	2f	2f

Display devices- LED

8. Discuss the working principle, characteristics and application of LED in detail. (NOV/DEC 2012) (Apr/May 2018)

Explain the principle and operation of light emitting diode (LED) with necessary expressions for current densities and efficiency of light generation. (April / May 2019-R17)

A **light-emitting diode**(LED) is a semiconductor light source LEDs are used as indicator lamps in many devices and are increasingly used for other lighting. Introduced as a practical electronic component in 1962, early LEDs emitted low-intensity red light, but modern versions are available across the visible, ultraviolet, and infrared wavelengths, with very high brightness.

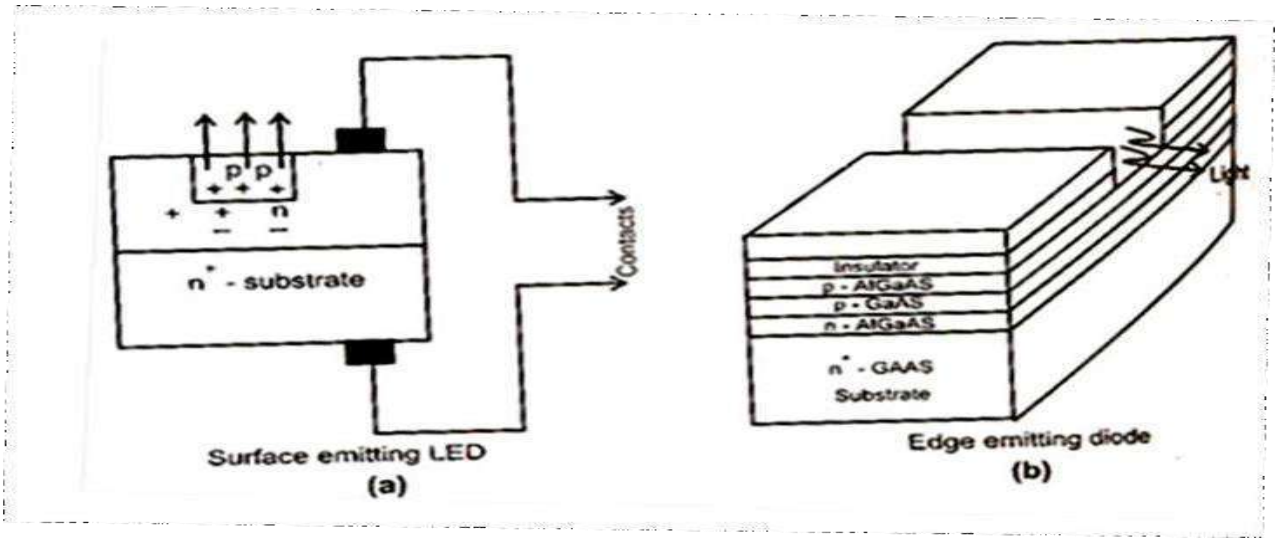
When a light-emitting diode is forward-biased (switched on), electrons are able to recombine with electron holes within the device, releasing energy in the form of photons. This effect is called electroluminescence and the color of the light (corresponding to the energy of the photon) is determined by the energy gap of the semiconductor.

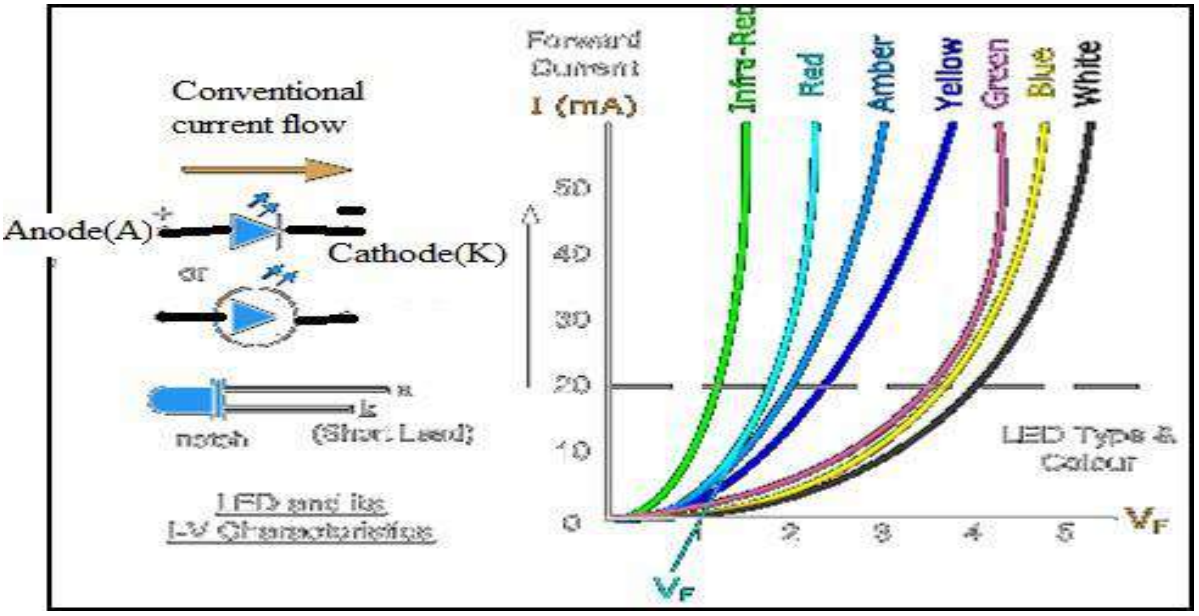
LEDs are often small in area (less than 1 mm^2), and integrated optical components may be used to shape its radiation pattern.[5] LEDs present many advantages over incandescent light sources including lower energy consumption, longer lifetime, improved robustness, smaller size, and faster switching. LEDs powerful enough for room lighting are relatively expensive and require more precise current and heat management than compact fluorescent lamp sources of comparable output.

Light Emitting Diodes are made from exotic semiconductor compounds such as Gallium Arsenide (GaAs), Gallium Phosphide (GaP), Gallium Arsenide Phosphide (GaAsP), Silicon Carbide (SiC) or Gallium Indium Nitride (GaInN) all mixed together at different ratios to produce a distinct wavelength of colour.

Different LED compounds emit light in specific regions of the visible light spectrum and therefore produce different intensity levels.

- Gallium Arsenide Phosphide (GaAsP) - red to infra-red, orange
- Aluminium Gallium Arsenide Phosphide (AlGaAsP) - high-brightness red, orange-red, orange, and yellow
- Gallium Phosphide (GaP) - red, yellow and green
- Aluminium Gallium Phosphide (AlGaP) - green
- Gallium Nitride (GaN) - green, emerald green
- Gallium Indium Nitride (GaInN) - near ultraviolet, bluish-green and blue
- Silicon Carbide (SiC) - blue as a substrate
- Zinc Selenide (ZnSe) - blue
- Aluminium Gallium Nitride (AlGaN) - ultraviolet





Light-emitting diodes are used in **applications** as diverse as aviation lighting, automotive lighting, advertising, general lighting, and traffic signals. LEDs have allowed new text, video displays, live video, and sensors to be developed, while their high switching rates are also useful in advanced communications technology. Infrared LEDs are also used in the remote control units of many commercial products including televisions, DVD players, and other domestic appliances.

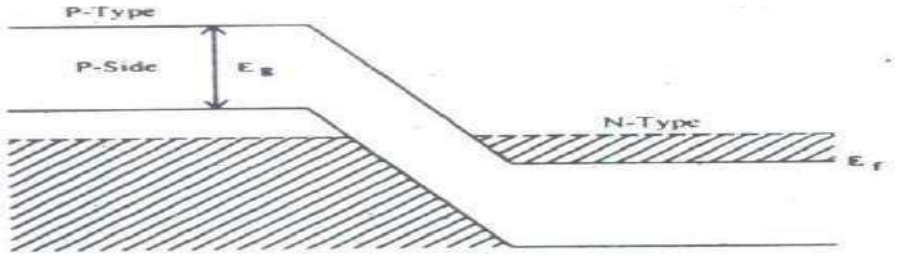
Laser diodes

9. Explain in detail about LASER DIODE? (May / June 2016) (April/May 2018)

The term laser comes from the acronym for light amplification for stimulated emission of radiation. The laser medium can be a gas, liquid, amorphous solid or semiconductor.

Laser Action

The light travelling through a semiconductor, then a single photon is able to generate an identical second photon. This photon multiplication is the key physical mechanism of lasing. The carrier inversion is the first requirement of lasing. It is achieved at the PN junction by providing the conduction bandwith electrons from the N-doped side and the valence band with holes from the P-doped side as shown in Fig. The photon energy is given by the band gap, which depends on the semiconductor material. The optical feedback and the confinement of photon in an optical resonator are the second basic requirement of lasing.



PN Homojunction Laser

It has the material GaAs on both sides of the junction. A pair of parallel planes perpendicular to the plane of the junction are cleared and polished under appropriate biasing in off condition, laser light is emitted from these planes. The other two sides are deliberately roughened to prevent lasing in those directions. Such a cavity is called a Fabryperot resonant cavity with a typical cavity length of 300 |**J**.m. It is a thin layer of material with a narrow band gap. GaAs is sandwiched between layers of a material with band gap. This is usually realized by epitaxy. In such a structure the carrier are better confined in the active region due to the heterojunction barriers. Optical confinement is also better in ***DH*** laser. The propagation of the electromagnetic radiation is confined in a direction parallel to the

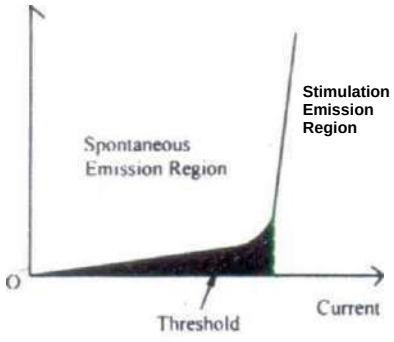
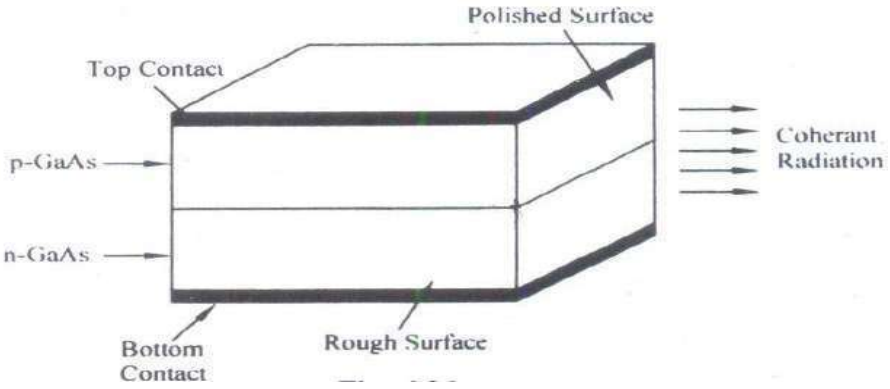
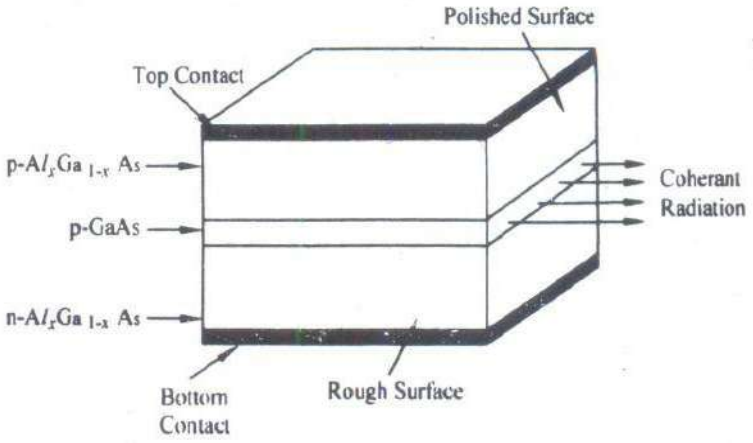


Fig. 4.28

layer interface. The current density required for lasing in lower for ***DH*** lasers compared to homojunction lasers. The double preferred for continuous operation at room temperature.



Double Hetrostructure Laser



Characteristics of Laser Diode

The Ideal light output against current characteristics for semiconductor laser is shown in Fig.4.28. The solid line represents the laser characteristics. It may be observed that the device gives low light output in the region, the threshold with corresponds to spontaneous emission only within the structure. After the threshold current value the light output increases substantially for small increases in current through the device.

ZENER DIODE

10. Explain the construction & working principle of Zener diode.
Explain the Break down mechanisms in semiconductor devices. (May/June 2016), (Nov / Dec 2015)
(OR) Explain the Concept of Zener Breakdown and its VI characteristics. (Nov/Dec 2018-R-13)

ZENER DIODE:
The Zener Diode is a PN junction semiconductor device.
It is fabricated with precise breakdown voltages, by controlling the doping level during manufacturing.
Practically, Zener Diodes are operated in reverse biased mode.

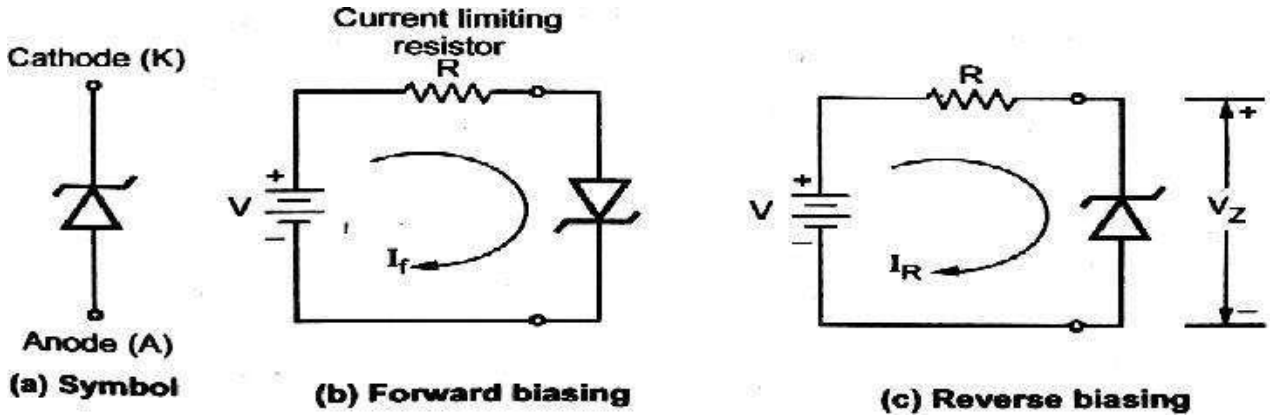


Fig.20 *Zener Diode*

CHARACTERISITCS OF ZENER DIODE:

FORWARD CHARACTERISITCS:

In forward biased condition, the normal rectifier diode and the Zener diode operate in similar fashion.
(Refer: PN diode forward characteristics)

Zener reverse characteristics

REVERSE CHARACTERISITCS:

Zener diode is designed to operate in the reverse biased condition.

In reverse biased condition, the diode carries ***reverse saturation current*** till the reverse voltage applied is less than the reverse breakdown voltage.

When the reverse voltage exceeds reverse breakdown voltage, the current through it changes drastically but the voltage across it remains almost constant.

Such a breakdown region is a normal operating region for a Zener diode.

The normal operating regions for both diode and Zener are shown in below Fig.

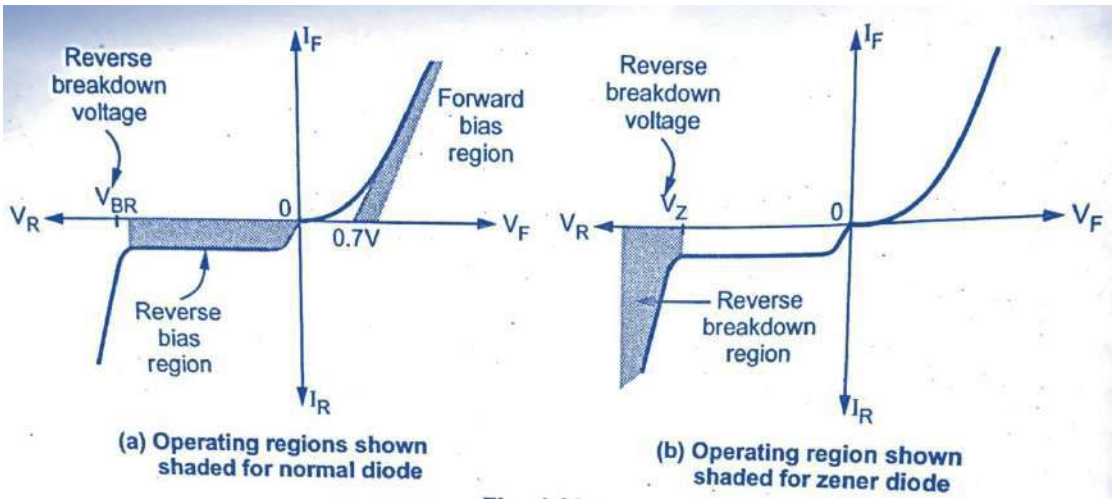


Fig. *The normal operating region for a rectifier diode and Zener diode*

When the applied reverse voltage is increased then, the current through it is very small (few μA) and it is called Reverse Leakage Current (I_o)
At certain reverse voltage, the current will increase rapidly. The breakdown occurs and the current at this point (***knee or Zener knee***) is called ***Zener knee current (I_{ZK} or I_{Zmin}).***
Zener knee current is the minimum Zener current which is must to carry out the operate in Reverse Breakdown Region.
The reverse voltage at which the breakdown occurs is called ***Zener Breakdown Voltage or Zener Voltage (V_Z)***.
The V_Z is set by controlling the doping level during manufacturing process.

Below the knee, the **reverse breakdown voltage** increases slightly as Zener current (I_Z) increases but, remains almost ***CONSTANT***.
The current at which the nominal Zener breakdown voltage is specified is called ***Zener Test Current (I_{ZT}).***

As the current increases, the power dissipation ($P_Z = V_Z I_Z$) will be increased and if this power dissipation is increased beyond a certain current value, the Zener diode may get damaged. So, there is a maximum current that a Zener diode can carry safely is called ***Zener Maximum Current (I_{ZM} or I_{Zmax}).***

In practical circuits, a current limiting resistor is used in series with Zener diode in order to limit the current between I_{Zmin} to I_{Zmax}.

The complete VI characteristics of Zener Diode is shown in Fig.

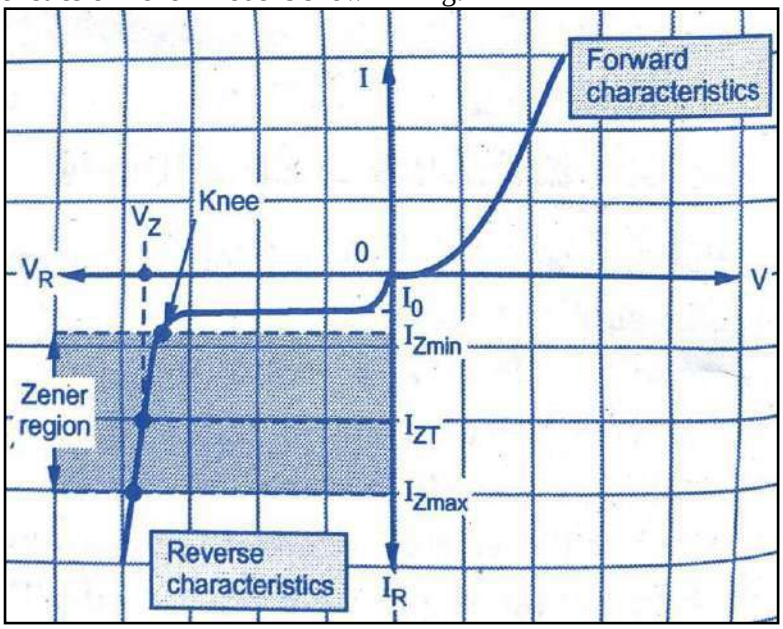


Fig. *VI characteristics of Zener Diode*

EQUIVALENT CIRCUIT OF ZENER DIODE:

When the breakdown occurs then I_Z may increase from I_{Zmin} to I_{Zmax} but voltage across Zener remains almost constant. The internal impedance decreases as current increases in Zener region. But this impedance is very small and hence ideally Zener diode is indicated by a battery of voltage V_Z. This V_Z remains almost constant in the Zener region which is shown in Fig.

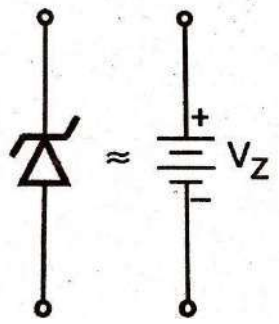


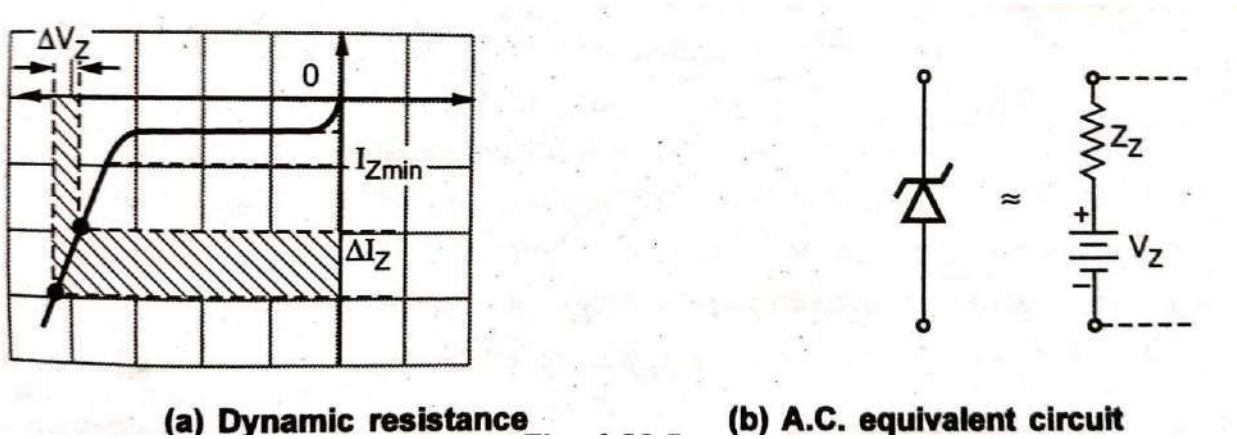
Fig. *Ideal equivalent circuit of Zener diode*

In practical circuit, the Zener internal resistance is to be considered (even though it is very small) and called as ***Zener Dynamic Resistance*** Z_Z. Due to this resistance the Zener region is not exactly vertical, i.e., for the small change in the Zener current ΔI_Z produces a small change in Zener voltage ΔV_Z. The ratio of V_Z to I_Z is called ***Zener resistance*** Z_Z.

Hence, the practical Zener diode equivalent circuit should be indicated with a battery of V_Z along with series resistance Z_Z as shown in Fig.

Dynamic Resistance, $Z_Z = \frac{\Delta V_Z}{\Delta I_Z} = \frac{1}{[\frac{\Delta I_Z}{\Delta V_Z}]}$

$$Z_Z = \frac{1}{[slope\ of\ the\ reverse\ characteristics\ in\ zener\ region]}$$



(a) Dynamic resistance **(b) A.C. equivalent circuit**

BREAKDOWN MECHANISM IN ZENER DIODE:

Two distinct breakdown mechanism:

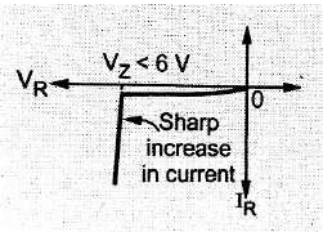
- ✓ Zener Breakdown
- ✓ Avalanche Breakdown

For devices with breakdown voltage ***less than 5V - Zener Breakdown***
For devices with breakdown voltage ***between 5V and 8V - Zener Breakdown and Avalanche Breakdown***
For devices with breakdown voltage ***above 8V - Avalanche Breakdown***

ZENER BREAKDOWN:

Zener breakdown occurs at Reverse biased condition because of heavy doping;
*Practically, **Zener breakdown** is observed in the Zener diodes with breakdown voltage **less than 6V**.*
In Zener breakdown, the value of the breakdown voltage decreases as PN junction temperature increases, i.e. Negative Temperature Coefficient (NTC)

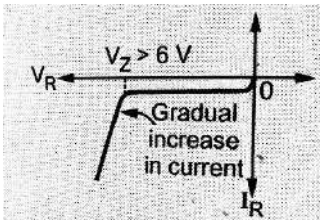
For applied reverse biased voltage of less than 6V causes a high magnitude electric field (3 X 10^5 V/cm) across the depletion region, at the PN junction.
This electric field applies a large force on the valence electron of the atom, tending it to separate them from their respective nuclei. Electron-hole pairs are generated in large numbers and there will be a sudden increase in current. *(To limit this current, a **current limiting resistor** is used in order to protect the Zener diode from being destroyed because of excessive heating at the junction)*



AVALANCHE BREAKDOWN:

Avalanche Breakdown occurs at Reverse biased condition due to ionization of electron and hole pairs
*Practically, **Avalanche breakdown** is observed in the Zener diodes with breakdown **voltage greater than 6V.***
In avalanche breakdown, the value of the breakdown voltage increases as PN junction temperature increases, i.e. Positive Temperature Coefficient (PTC)

For applied reverse biased voltage of greater than 6V causes increased acceleration of minority charge particles. Thus, collision between accelerated charge particles with high velocity and kinetic energy with adjacent atom is involved in breaking the covalent bonds of the crystal structure. This process is called **Carrier Multiplication**.
At this stage, junction is said to be in breakdown and current starts increasing rapidly. *To limit this current below I_{Zmax}, a **current limiting resistor is necessary.***



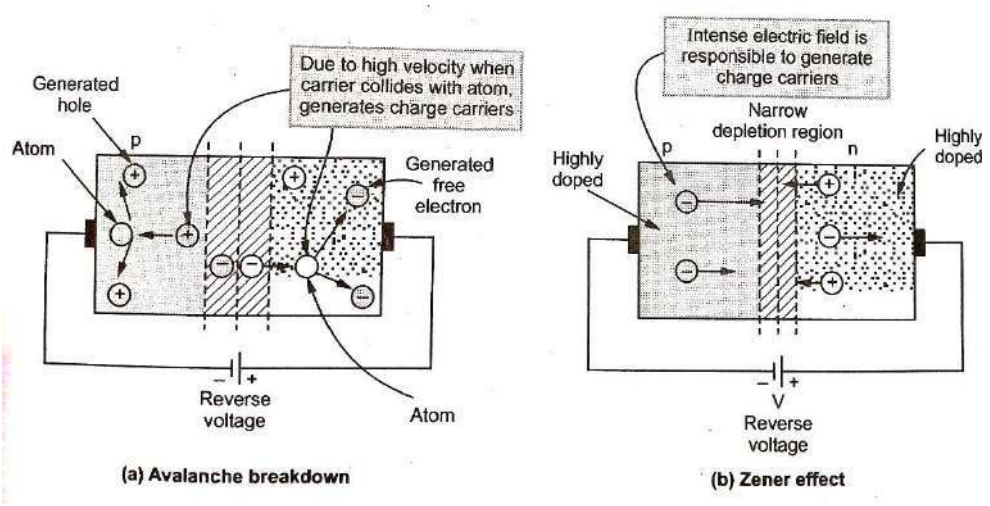


***Fig.** Breakdown Mechanism in Zener Diode*

ZENER AS REGULATOR

11. (a) Explain the working of a Zener diode as a regulator? (May 2017) (Nov/Dec 2017) (Nov/Dec 2018 – R17)

The Zener Diode is used to regulate the *Load Voltage*. Here, the Zener is used in reverse biased condition.

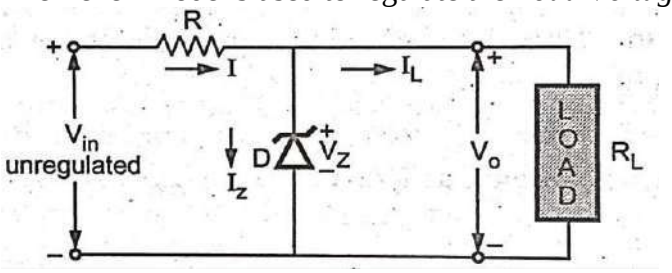


Fig. *Zener Diode as a shunt regulator*

{Under reverse biased condition, the current through the zener diode is very small of the order of few µA, up to certain limit. When enough reverse bias voltage is applied, electrical breakdown occurs and large current flows through the zener diode. The voltage at which the breakdown occurs is called **Zener Voltage (V_Z)**.

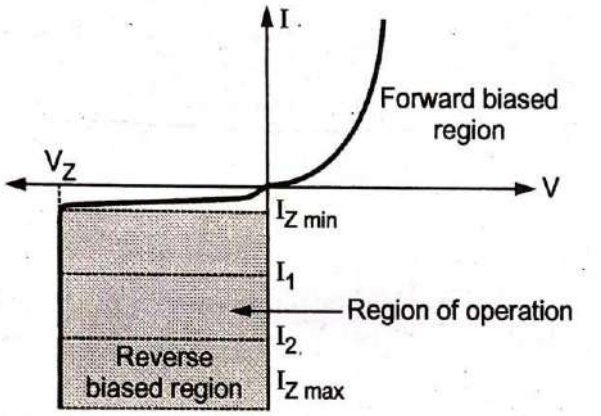


Fig. *VI characteristics of Zener Diode*

Under this condition, whatever may be the current, the **voltage** across the Zener is **constant** and **equal to V_Z**}

Since, voltage across the Zener Diode is *CONSTANT* & *equal to* V_Z, it is connected across the load.
∴ The Load Voltage (Vo) is equal to Zener Voltage (V_Z).
i.e. *The Zener Diode acts as an ideal voltage source which maintains a constant load voltage, independent of the current.*

REGULATION WITH VARYING INPUT VOLTAGE *(Line Regulation)*

Zener Regulator under varying input voltage condition is shown in Fig.

$V_o = V_Z$ is constant

$I_L = \frac{V_o}{R_L} = \frac{V_Z}{R_L} = constant$

And $I = I_Z + I_L$

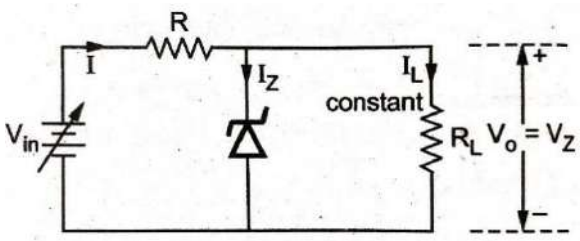


Fig. *Varying input condition*

V_{in} increases	⇒ $I = I_L + I_Z$ increases	⇒ I_L is constant (V_Z/R_L)	⇒ So I_Z increases ($I_Z = I - I_L$)	⇒ As long $I_Z < I_{Zmax}$, V_Z is constant i.e. output voltage is constant
V_{in} decreases	⇒ $I = I_L + I_Z$ decreases	⇒ I_L is constant (V_Z/R_L)	⇒ So I_Z decreases ($I_Z = I - I_L$)	⇒ As long $I_Z > I_{Zmin}$, V_Z is constant i.e. output voltage is constant

As long I_Z is between I_{Zmin} and I_{Zmax} , the V_Z i.e. output voltage V_o is constant. Thus, the changes in the input voltage is get compensated and output is maintained constant.

The **maximum power dissipation** for the zener diode is fixed, $P_D = V_Z\, I_{Zmax}$

REGULATION WITH VARYING LOAD *(Load Regulation)*

Zener Regulator under varying load condition (R_L is variable) and constant input voltage (V_{in} is constant) is shown in Fig.

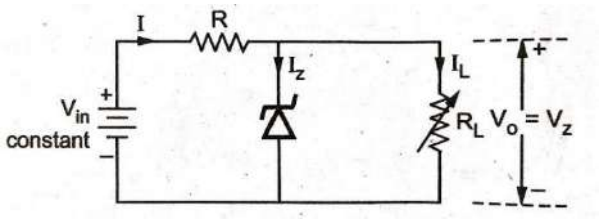


Fig. *Varying load condition*

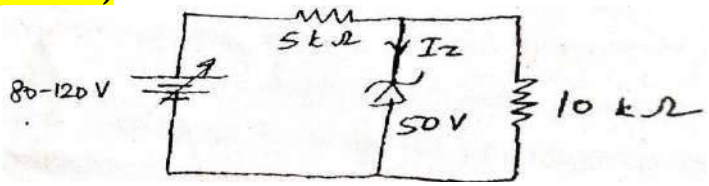
$V_o = V_Z$ is constant and **V_{in}** is Constant, then for constant R, the current (I) is constant.

$I = \frac{V_{in} - V_Z}{R}$ (constant); $I = I_L + I_Z$

R_L increases I_L decreases	→	$I = \frac{V_{in} - V_Z}{R}$ constant	→ $I_Z = I - I_L$ increases	→ As long $I_Z < I_{Zmax}$, V_Z is constant i.e. output voltage is constant
R_L decreases I_L increases	→	$I = \frac{V_{in} - V_Z}{R}$ constant	→ $I_Z = I - I_L$ decreases	→ As long $I_Z > I_{Zmin}$, V_Z is constant i.e. output voltage is constant

As long I_Z is between I_{Zmin} and I_{Zmax} , the V_Z i.e. output voltage V_o is constant. Thus, the changes in the load is get compensated and output is maintained constant.

(b) For the following circuit, find the maximum and minimum values of Zener diode current. (Nov/Dec 2018 – R17)



Solution: $V_{in\,(min)} = 80V, V_{in\,(max)} = 120V,\ V_Z = 50V,\ R_L = 10K\Omega,\quad R = 5K\Omega$

$$I_L = \frac{V_Z}{R_L} = \frac{50}{10\ X\ 10^3} = 5\ X\ 10^{-3} = 5mA$$

$$V_{in\,(min)} = V_Z + IR \quad V_{in\,(max)} = V_Z + IR$$

$$I = \frac{V_{in\,(\min)} - V_Z}{R} \quad I = \frac{V_{in\,(\max)} - V_Z}{R}$$

$$I_{(min)} = \frac{80 - 50}{5\ X\ 10^3} = 6mA \quad I_{(max)} = \frac{120 - 50}{5\ X\ 10^3} = 14mA$$

$$I_{Z\,(min)} = I_{(min)} - I_L \qquad I_{Z\,(max)} = I_{(max)} - I_L$$

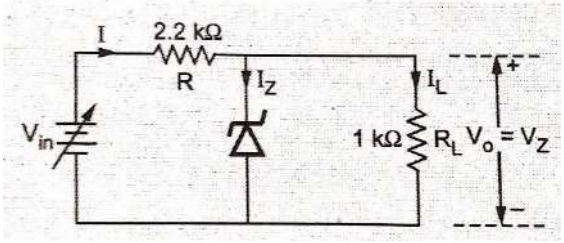
$$I_{Z\,(min)} = 6\ X\ 10^{-3} - 5\ X\ 10^{-3} = 1mA \qquad I_{Z\,(max)} = 14\ X\ 10^{-3} - 5\ X\ 10^{-3} = 9mA$$

$\therefore$ ***Minimum zener current,*** $I_{Z\,(min)} = \mathbf{1mA}$ $\therefore$ ***Maximum zener current,*** $I_{Z\,(max)} = \mathbf{9mA}$

Problems: (Anna University Exam - Solved Problems)

1. **For the zener regulator shown in Fig. 5, calculate the range of input voltage for which output will remain constant.**

$$I_{Z\,(min)} = 2.5mA, \quad I_{Z\,(max)} = 25mA, \quad V_Z = 6.1V, \quad r_Z = 0\ K\Omega$$



Solution:

$I_{Z\,(min)} = 2.5mA, I_{Z\,(min)} = 25mA, \quad V_Z = 6.1V, \quad r_Z = 0\ K\Omega, \quad R = 2.2\ K\Omega, \quad R_L = 1\ K\Omega$

$$I_L = \frac{V_Z}{R_L} = \frac{6.1}{1\ X\ 10^3} = 6.1\ X\ 10^{-3} = 6.1mA \quad (\boldsymbol{CONSTANT})$$

$For\ V_{in\,(min)}; \quad I_{(min)} = I_{z(min)} + I_L$

$I = 2.5\ X\ 10^{-3} + 6.1\ X\ 10^{-3} = 8.6mA$

$V_{in\,(min)} = V_Z + IRV_{in\,(max)} = V_Z + IR$

$V_{in\,(min)} = 6.1 + 8.6\ X\ 10^{-3}X\ 2.2\ X\ 10^{-3} = 25.02V$

$\therefore \boldsymbol{V_{in\,(min)} = 25.02V}$

$For\ V_{in\,(mzx)}; \quad I_{(max)} = I_{Z(max)} + I_L$

$I = 25\ X\ 10^{-3} + 6.1\ X\ 10^{-3} = 31.1mA$

$V_{in\,(min)} = 6.1 + 31.1\ X\ 10^{-3}X\ 2.2\ X\ 10^{-3} = 74.52V$

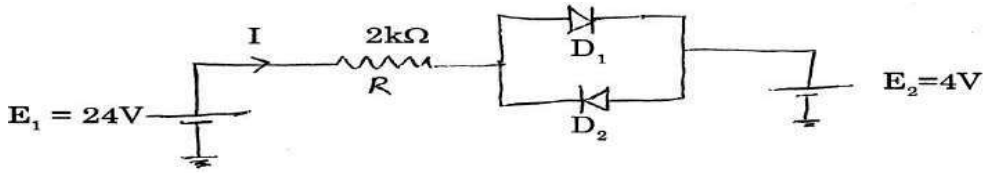
$\therefore \boldsymbol{V_{in\,(max)} = 74.52V}$

2. **A silicon diode has a saturation current 7.5μ A at room temperature 300K.Find the saturation current at 400k. I_{o1}=7.5 x 10-6 A at T_1=300° K=27° C and T_2=400 °K=127° C.** **(Nov/Dec 2016 – R13)**

Solution: The saturation current at 400°K is

$I_{02}=I_{01} \times 2^{\frac{\Delta T}{10}}$ =7.5 X 10^{-6} X $2^{(127\text{-}27)/10}$ =7.68mA

3. **Find the current I in the following circuit. (Nov/Dec 2017 – R13)**



Assume the diodes to be of silicon and forward resistance of diodes to be zero.

I = (E1-E2)/R I = (24-4)/2000

I = 1 mA **Current I is 1mA.**

4. **An AC voltage of peak value 20V is connected in series with a silicon diode and load resistance of 500Ω. If the forward resistance of diode is 10Ω find the peak current through the diode.** **(Nov/Dec 2018-R17)**

Solution: $E_m = 20V, \quad R_L = 500\Omega, \quad R_f = 10\Omega$

$$I_m = \frac{E_m}{R_f + R_L} \qquad I_m = \frac{20}{500 + 10}$$

$$\therefore I_m = 39.22\ mA$$

5. **(a) Determine the peak output voltage of a half wave rectifier, if the diode has V_F = 0.7V and the AC input is 22V. (April / May 2019-R17)**

Solution: $V_{po} = V_{pi} - V_F$

$V_F = 0.7\,V$, $V_{pi} = \sqrt{2}V_i = \sqrt{2}\,X\,22$, $V_{pi} = 31.1\,V$

$V_{po} = 31.1 - 0.7$, $V_{po} = 30.4\,V$

(b) If load resistance is given as 500Ω, calculate peak output current of the above given half wave rectifier.

Solution: $R_L = 500\Omega$ $I_p = \frac{V_{po}}{R_L} = \frac{30.4}{500}$ $I_p = 60.8\,mA$

(c) Determine the diode peak reverse voltage (PIV). PIV = V_{pi} = 31.1 V

6. **What value of series resistor is required to limit the current through a LED to 20 mA with a forward voltage drop of 1.6 V when connected to a 10V supply? (Nov/Dec 2017)**

Series resistor, $R_S = \frac{V_S - V_D}{I_F}$

$V_S = 10$ V; $V_D = 1.6$ V; $I_F = 20$ mA $= 20 \times 10^{-3}$ A

$\therefore \quad R_S = \frac{10 - 1.6}{20 \times 10^{-3}} = 420\ \Omega$

7. **In a semiconductor at room temperature(300°K), the intrinsic carrier concentration and resistivity are1.5 * 10^{16}/cm^3 and 2 *10^3Ω-mrespectively. It is to an extrinsic semiconductor with a doping concentration of 10^{20}/cm^3 for the extrinsic semiconductor.**
Calculate (a) Majority carrier concentration, (b) Shift in fermilevel due to doping (c) Minority carrier concentration when its temperature is increased to a value at which the intrinsic concentration 'n$_i$' doubles. (NOV/DEC 2012)

Assume the mobility of majority and minority carriers are same and **KT=26 meT** at room temperature.

a) Minority carrier concentration=$\frac{n_i^2}{\text{Doping concentration}}$

$= \frac{(1.5\times10^{16})}{10^{20}} = 2.25 \times 10^{12} \frac{\text{atoms}}{\text{m}^3}$

We know $\sigma = nq(\mu_n + \mu_p)$

or $(\mu_n + \mu_p) = \frac{\sigma}{nq} = \frac{1}{\rho nq}$

$= \frac{1}{(2\times10^3)(1.5\times10^{16})(1.6\times10^{-19})} = \frac{1}{4.8}$

In this case the concentration of majority and minority carriers are same, thus

$$\mu_n + \mu_p = 2\mu_n = \frac{1}{4.8} \text{ or } \mu_n = o.1042 \frac{\text{m}^2}{\text{Volt} - \text{sec}}$$

b) Because of doping concentration>> minority concentration conductivity.

$\sigma = qn\,\mu_n = (1.6 \times 10^{-19})(10^{20})(0.10242)$=1.6672

Thus resistivity R=$\frac{1}{\sigma} = 0.599\Omega$cm

Shift interm level $E_F$computed as follows

C) $E_A - E_i = KT\ \log_e \frac{n_o}{n_i} = 0.026\log_e (\frac{10^{20}}{10^{16}\times15})$

$=0.229_e$V.

Thus E_F lies0.229_eV above from fermilevel.

d) Minority carrier concentration=$\frac{(2ni)^2}{\text{doping concentration}}$ $= \frac{[2(1.5\times10^{16})^2]}{10^{20}}$ $= \frac{9\times10^{32}}{10^{20}}$ =9× 10^{12}atoms/cm^3.

Additional Questions: PART-A

1. **Define valence electron.**

   Electrons that are in shells close to nucleus are tightly bounced to the atom and have low energy. Whereas electrons that are in shells farther from the nucleus have large energy and less tightly bound to the atom. Electrons with highest energy level exist in the outermost shell of an atom. These electrons determine the electrical and chemical characteristic of each particular type of atom. These electrons are known as valence electrons.

2. **What is meant by energy band?**

   In a single isolated atom, the electron in any orbit possesses define energy. Due to an interaction between atoms the electrons in a particular orbit of one atom have slightly different energy levels from electrons in the same orbit of an adjoining atom. This is due to the fact that no two electrons see exactly the same pattern of surrounding charges. Since there are billions of electrons in any orbit, slightly different energy levels form a cluster or band known as energy band.

3. **Define conduction band & valence band.**

   - The conduction band is defined as the range of energies possessed by conduction electrons.
   - Valence band is defined as the range of energies possessed by valence electros.

4. **What are conductors, Insulators and semiconductors?**

   - A conductor is a material, which easily allows the flow of electric current. The best conductors are copper, silver, gold and aluminum.
   - An Insulator is a material that does not conduct electric current. In these materials valence electrons are tightly bound to the atoms.
   - A semiconductor is a material that has an electrical conductivity that lies between conductors and insulators. A semiconductor in it's pure state is neither a good conductor not a good insulator. The most common semiconductors are silicon, Germanium, and carbon.

5. **What are the classifications of semiconductors?**

   Semiconductors are classified as intrinsic and extrinsic semiconductors. A pure semiconductor is called intrinsic semiconductor. A doped semiconductor is called extrinsic semiconductor.

6. **What is meant by doping? How the extrinsic semiconductors are classified?**

   The process of adding impurities to a semiconductor is known as doping.
   - n-type semiconductor
   - p-type semiconductor

7. **How a *n*-type semiconductor & p-type semiconductor can be obtained?**

   - A n-type semiconductor can be obtained by adding pentavalent impurities to an intrinsic semiconductor. These are atoms with five valence electrons. Typical examples for pentavalent atoms are Arsenic. Phosphorous, Bismuth and Antimony.

   - A p-type semiconductor can be obtained by adding trivalent impurities to an intrinsic semiconductor. These are atoms with three valence electrons. Typical examples for trivalent atoms are boron(B), indium (In) and gallium (Ga).

8. **Define Fermi level.**

   Fermi level is the energy at which the probability of occupation by an electron is exactly 0.5.

9. **What is the energy band gap of silicon and Germanium at 300°*K*?**

   For Germanium: 0.66_e and for Silicon: 1.12_ev

10. **What are the different types of voltage regulators?**

    Based on how regulating element is connected to the load, voltage regulators are classified as
    - Series regulator
    - Shunt regulator
    - Switch-mode regulators or switched mode power supply (SMPS)

Additional Questions (PART-B)

1. Draw and explain the energy band diagram for the following

(i) conductors (ii) Insulators (iii) semiconductors

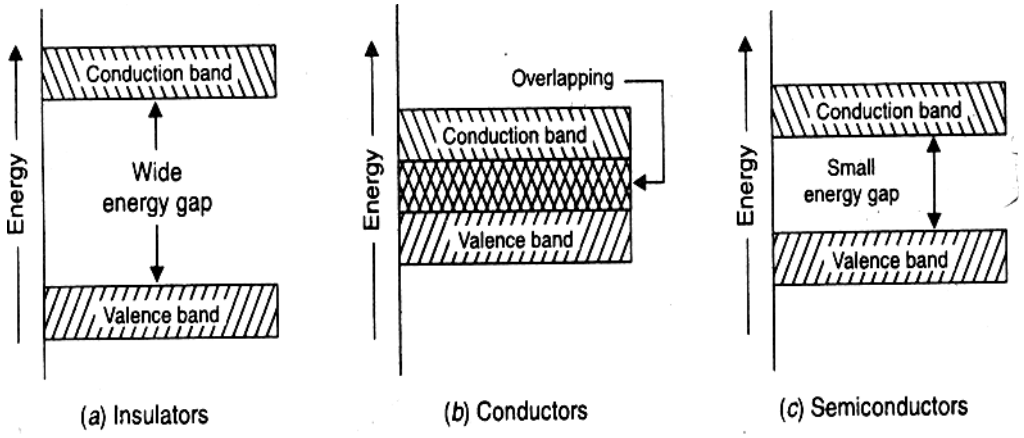
Insulators :

The materials in which the condition band and valence bands are seperated by a wide energy gap (≈ 15 eV) as shown in figure.

A wide energy gap means that a large amount of energy is required, to free the electrons, by moving them from the valence band into the condition band ;

Since at room temperature, the valence electrons of an insulator do not have enough energy to jump in to the condition, therefore insulator do not have an ability to conduct current. Thus insulators have very high resistively (or extremely low conductivity) at room temperatures.

However if the temperature is raised, some of the valence electrons may acquire energy and jump in to the conduction band. It causes the resistively of insulators to decrease.Therefore an insulator have negative temperature co-efficient of resistance.



Conductors :-

The materials in which conduction and valence bands overlap as shown in figure are called conductors. The overlapping indicates a large number of electrons available for conduction.Hence the application of a small amount of voltage results a large amount of current.

Semiconductors :-

The materials, in which the conduction and valence bands are separeated by a small energy gap (1eV) as shown in figure are called semiconductors.

Silicon and germanium are the commonly used semiconductors.

A small energy gap means that a small amount of energy is required to free the elctrons by moving them from the valence band in to the conduction band.

The semiconductors behave4 like insulators at 0K, because no electrons are available in the conduction band.

If the temperature is further increased, more valence elctrons will acquire energy to jump into the conduction band.Thus like insulators, semiconductors also have negative temperature co-efficient of resistance. It means that conductivity of semiconductors increases with the increases tempertature.

2. Explain the classification of semi-conducteurs.

Classification of semi-conducteurs :-

Semiconductors are classified in to two types

- Intrinsic Semiconductors
- Exterinsic semi-conducteurs
  - n-type semi-conductor
  - p-type semi-conductor

- **Intrinsic seiconductor**

A semiconductor in an extremely pure form is known as an intrinic semiconductor. An Intrinsic semiconductor, even at room temperature, hole-electron pairs all created. When electric field is applied across an semiconductor intrinisic semiconductor, the current conduction takes place by two process, namely by free electrons and holes.

Free electrons are produced due to the breeding up of fome co-valent bonds by thermal energy. At the same time holes are created in the co-valent bond itself.When electric field is applied across the semi-conducteurs material electrons will move towards the positive terminal of supply, holes will move towards negative terminal of the supply.

Thus current conduction inside this intrinisic semiconductor material is due to movement of holes & electrons.

But the current in the external wire is only because of electrons. Since while applying electric field, holes are attracted towards negative terminal. There one new electron is introduced. This electron will combine with the hole, thus cancelling them.

At the same time electrons are moving towards positive terminal, while leacing from this intrinisic material it leaves a hole. Again this holes are attracted towards negative terminal.

- **Extrinisic semiconductor :**

The current conduction capability of intrinisic semiconductor is very low at rom temperature. So we can not use it in electric devices.

Hence the current conduction capability must be increased. This can be achieved by adding impurities to the intrinisic semiconductor. So that it become impurity semiconductor (or) Extrinisic semiconductor.The process of adding impurity is known as doping.

The amount & type of impurities have to be closely controlled during the preparation of extrinisic semiconductor. Generally, for 10^8 atoms of semiconductor, one impurity atom is added.

The purpose of adding impurity is to increase either the number of free electrons or holes in the semiconductor crystal. If the pentavalent impurity is adding to the semiconductor, a large number of free electrons are produced in the semiconductor.

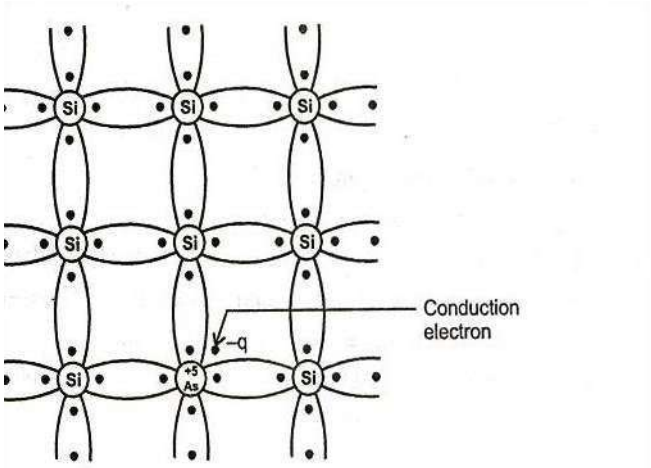
On the other hand if the trivalent impurtiy is added it introdued large number of holes. Depending upon the type of impurity added, extrisic semiconductors are classified into

- n – type Semiconductor
- p – type Semiconductor

n – type Semiconductor :

The number of free electrons in an instrinsic silicon can be increased by adding a pentavalent atom to it. These are atoms with five valence electrons. Typical example for pentavalent atoms are Arsenic, Phosphorous, Bismuth and Antimony.

Four of the pentavalent atoms valence electrons form covalent bond with the valence electrons of Silicon atom, leaving an extra electron. Since valence orbit cannot hold no more than eight electrons the extra electron becomes a conduction electron.



Crystal lattice of a Si atom displaced by arsenic atom

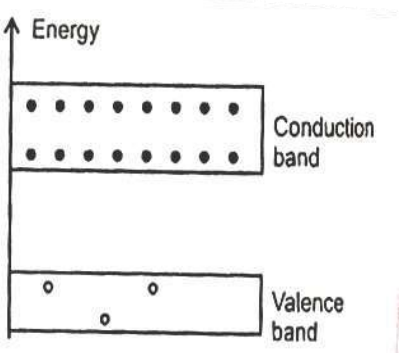
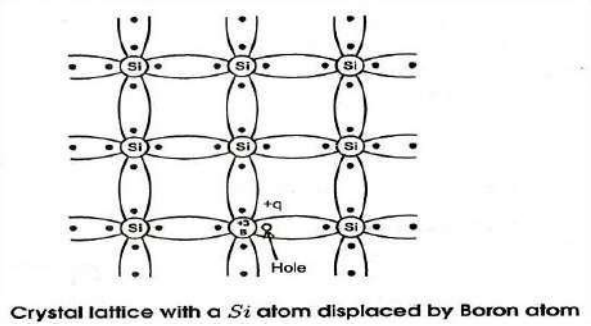


Fig. 1.12 Energy band diagram of a n-type semiconductor

Since the pentavalent atom donnates this extra conduction electron it is often called as a donor atom. For each pentavalent atom added, one free electron exists in a silicon crystal. A small amount of pentavalent impurity is enough to get more number of free electrons is greater than the nuumber of holes this extrinsic semiconductor is known as an n type semiconductor.

When a pentavalent atom is added a number of conduction band electrons are produced. Only a few holes exist in the valence band, created by thermal energy. Therefore in an n-type semiconductor, electrons are majority carriers and holes are minority carriers.

p-type semiconductor



Crystal lattice with a Si atom displaced by Boron atom

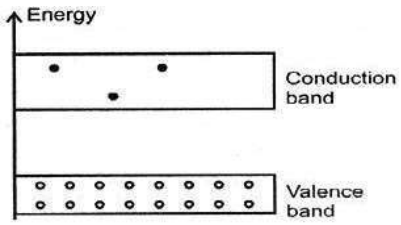


Fig. 1.14 Energy band diagram of a p-type semiconductor

A p-type semiconductor (p for Positive) is obtained by carrying out a process of doping by adding a certain type of atoms (acceptors) to the semiconductor in order to increase the number of free charge carriers (in this case positive holes).

When the doping material is added, it takes away (accepts) weakly bound outer electrons from the semiconductor atoms. This type of doping agent is also known as an acceptor material and the vacancy left behind by the electron is known as a hole.

The purpose of p-type doping is to create an abundance of holes. In the case of silicon, a trivalent atom (typically from Group 13 of the periodic table, such as boron or aluminium) is substituted into the crystal lattice. The result is that one electron is missing from one of the four covalent bonds normal for the silicon lattice. Thus the dopant atom can accept an electron from a neighboring atom's covalent bond to complete the fourth bond. This is why such dopants are called acceptors.

The dopant atom accepts an electron, causing the loss of half of one bond from the neighboring atom and resulting in the formation of a "hole". Each hole is associated with a nearby negatively charged dopant ion, and the semiconductor remains electrically neutral as a whole. However, once each hole has wandered away into the lattice, one proton in the atom at the hole's location will be "exposed" and no longer cancelled by an electron.

This atom will have 3 electrons and 1 hole surrounding a particular nucleus with 4 protons. For this reason a hole behaves as a positive charge. When a sufficiently large number of acceptor atoms are added, the holes greatly outnumber thermal excited electrons. Thus, holes are the majority carriers, while electrons become minority carriers in p-type materials.

EC8353-ELECTRONIC DEVICES AND CIRCUITS

UNIT-II TRANSISTORS & THYRISTORS
PART – A

BJT (Bipolar Junction Transistor)

1. **What is transistor** (BJT)**? What are the types of circuit connections known as configurations, for operating a transistor?**
   Transistor (BJT) is a three-terminal device: ***Base (B), Emitter (E) & Collector (C)***.
   Transistor can be operated in three configurations ***C**ommon **B**ase (**CB**), **C**ommon **E**mitter (**CE**) & **C**ommon **C**ollector (**CC**).*
   According to configuration it can be used for ***voltage*** as well as ***current amplification***.

2. **Brief the types of transistors?**
   1. **UJT** *(**U**nipolar **J**unction **T**ransistor*): In unipolar transistor, the current conduction is only due to one type of charge carriers (majority carriers).
   2. **BJT** *(**B**ipolar **J**unction **T**ransistor)*: In bipolar transistor, the current conduction is only due to both the types of charge carriers *(Holes and Electrons).*

3. **Why an ordinary transistor is called bipolar?**
   Because the transistor operation is carried out by two types charge carriers (both majority and minority carriers).

4. **What are the types of BJT?**
   Types of BJT:
   1. NPN
   2. PNP

5. **Brief the construction of BJT. Draw the symbol and structure and of BJT.**
   BJT is a three- layer semiconductor device consisting of two PN junctions.
   If a layer of P-type material is sandwiched between two layers of N-type the transistor is known as **NPN transistor**.

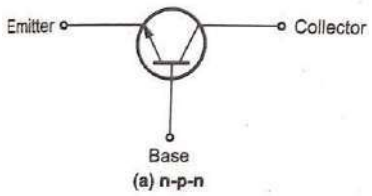


Fig. *Symbol of BJT (NPN type)*

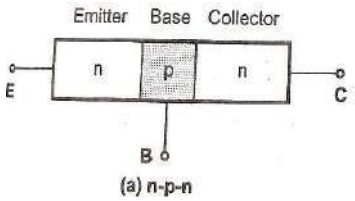


Fig. *Structure of BJT (NPN type)*

On the other hand, if a layer of N-type material is sandwiched between two layers of P-type, the transistor is known as **PNP transistor.**

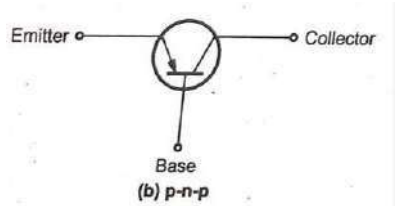


Fig. *Symbol of BJT (PNP type)*

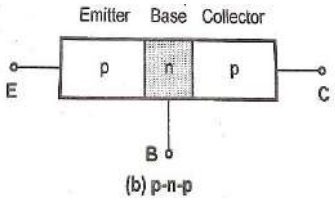


Fig. *Structure of BJT (PNP type)*

6. **Why collector is made larger than emitter and base?**
   Collector is made physically larger than emitter and base because collector is to dissipate much power.

7. **Why the width of the base region of a transistor is kept very Small as compared to other regions?**
   Base region of a transistor is kept very small and lightly doped so as to pass most of the injected charge carriers to the collector.

8. How transistor is used as an amplifier? (OR) Explain the word transistor.

The amplification in the transistor is achieved by passing input current signal from a region of low resistance to a region of high resistance.

{This concept of transfer of resistance has given the TRANSfer-resISTOR (TRANSISTOR)}

9. Why silicon is preferred to germanium while manufacturing semiconductor devices?

As the knee voltage of silicon is higher (0.7V) than the knee voltage of germanium (0.3V), silicon will be more stable for temperature variation than germanium.

10. Why transistor (BJT) is called current controlled device?

The output voltage, current or power is controlled by the input current in a transistor. So, it is called the Current Controlled device.

11. State the advantages of a transistor.

1. Low operating voltage
2. Higher efficiency
3. Small size and ruggedness
4. 4. Does not require any filament power

12. Compare the performance of a transistor in three different configurations. (Nov/Dec 2012) *(OR)* Compare the input resistance, output resistance and voltage gain of CB, CC and CE configuration. (OR) Compare the performance of CE and CC configuration. (May 2017)

Property	CB	CE	CC
Input resistance	Low (about 100Ω)	Moderate (about 750 Ω)	High (about 750 kΩ)
Output resistance	High (about 450 Ω)	Moderate (about 45 Ω)	Low (about 25Ω)
Current gain	1	High	High
Voltage gain	About 150	About 500	Less than 1
Phase shift	0 or 360°	180°	0 or 360°
Between input & output voltages Applications	For high frequency circuits	For audio frequency circuits	For impedance matching

13. Define Early effect? (Nov/Dec 2016)

As the collector voltage V_{CC} is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This known as early effect or base width modulation.

14. What is peak point Voltage?

When V_{EE} exceeds the value ($V_D+\eta V_{BB}$), the diode is forward biased and starts to conduct. The value of emitter voltage which makes diode to conduct is called **Peak Point Voltage**.

$$V_p=(V_D+\eta V_{BB})$$

<u>JFET (Junction Field EffectnTransistor)</u>

15. What are the different types of FET?

Types of FET:

1. Junction Field Effect Transistor (JFET)
2. Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

16. Draw the symbol and structure of JFET.

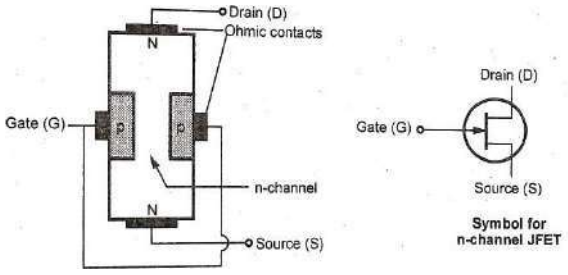


Fig. Structure and for n-channel JFET

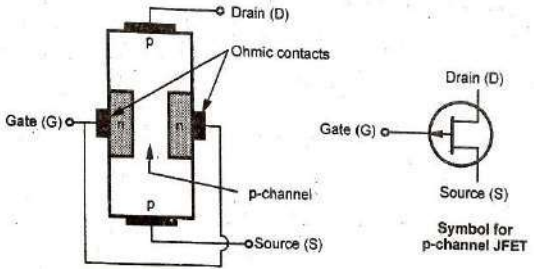


Fig. Structure and for p-channel JFET

17. What are the features of JFET?

a) The operation of JFET depends upon the flow of majority carriers only.
b) The input impedance of JFET is very high, in the order of MΩ.
c) The JFET is less noisy than BJT.
d) It exhibits no offset voltage at zero drain current.
e) It is simple to fabricate.
F) It occupies less space in an integrated circuit.

18. Draw the transfer and drain characteristics curves of JFET? (May / June 2016)

Drain Characteristics:

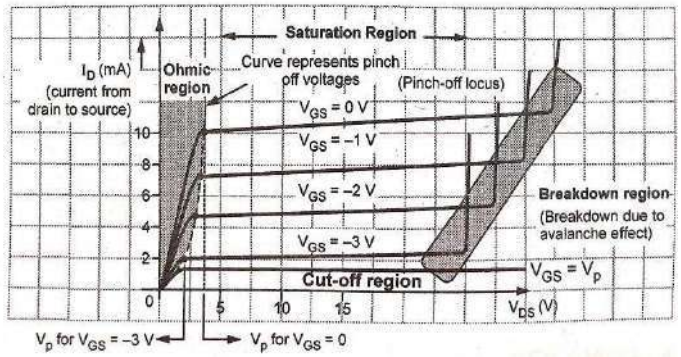


Fig. Drain VI characteristics of n-channel JFET

Transfer Characteristics:

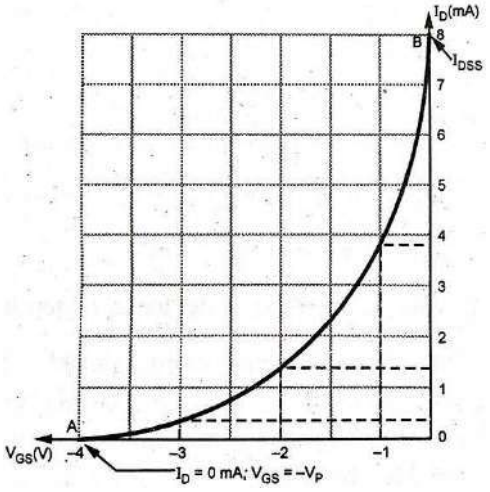


Fig. Transfer characteristics of n-channel JFET

Drain Characteristics:

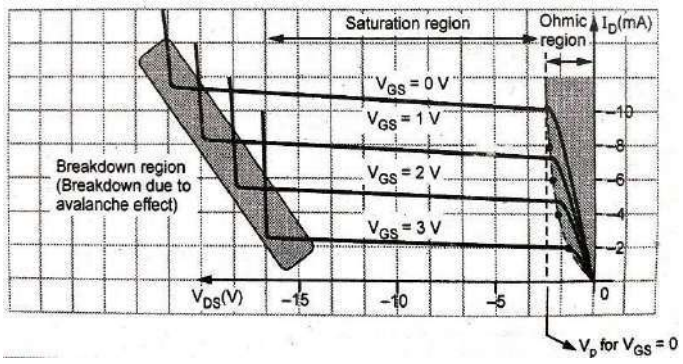


Fig. Drain VI characteristics of p-channel JFET

Transfer Characteristics:

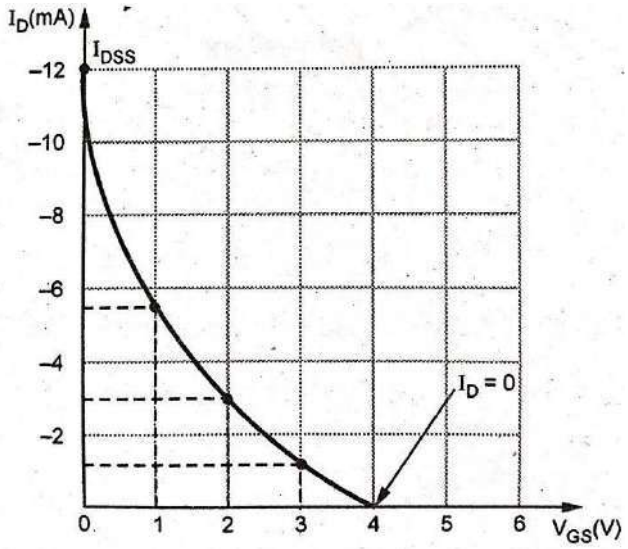


Fig. Transfer characteristics of p-channel JFET

19. Define pinch-off voltage of a FET? (Nov/Dec-2012, May/June-2013)

Pinch-off voltage (V_P) is defined as the drain to source voltage above which drain current becomes almost constant.

20. Mention the disadvantages of FET compared to BJT. (Nov/Dec-2012)

Gain bandwidth product of FET is relatively small as compared to BJT.

21. Define drain resistance.

The drain resistance or output (r_d) is defined as the ratio between change in drain-source voltage (V_{DS}) and change in drain current (I_D) at constant gate-source voltage (V_{GS}).

$$r_d = \frac{\partial VDS}{\partial i_D} V_{GS}$$

22. Differentiate FET and BJT (Nov/Dec 2018)

S.No	FET	BJT
1	Unipolar device (that is current conduction by only one type of either electron or hole).	Bipolar device (current conduction by both electron and hole).
2	High input impedance due to reverse bias.	Low input impedance due to forward bias.
3	Gain is characterized by trans conductance	Gain is characterized by voltage gain.
4	Low noise level	High noise level

23. What are the applications of JFET?

a) JFET is used as a buffer in measuring instruments since it has high input impedance and low output impedance.

b) JFET is used in RF amplifier in FM tuners and communication equipment.

c) JFET is used in digital circuit's ii computers and memory circuits because of its small size.

d) It is used oscillators because the frequency drift is low.

24.* FET has lower thermal noise than BJT - Justify. *(April / May 2019-R17)

The FET has high gate-to-main current resistance, on the order of 100MΩ or more providing a high degree of isolation between control and flow. Because base current noise will increase with shaping time, a FET typically produces less noise than a Bipolar Junction Transistor (BJT).

Thus, found in noise-sensitive electronics such as tuners and low noise amplifiers for VHF and satellite receivers. It is relatively immune to radiation.

25.* What is the difference between BJT and JFET? *(Nov/Dec 2017) (Apr/May 2018) (Nov/Dec 2018-R17)

S. No.	Bipolar junction transistor (BJT)	Junction field effect transistor (JFET)
1	Bipolar device (current conduction is by both electrons and holes)	Unipolar device (current is by only one type of carrier-either electrons or holes)
2	Low input impedance due to forward bias	High input impedance due to reverse bias
3	Current control device	Voltage control device
4	Gain is characterized by voltage gain	Gain is characterized by Tran conductance.
5	High noise level	Low noise level

MOSFET

26. What are the different types of MOSFET? (May/June-2012, 2013)

The modes of operation of the MOSFET are divided into two types.

a) Depletion mode MOSFET

b) Enhancement mode MOSFET

27. What is the other name for MOSFET? (May/June-2012, 2013)

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is also called as I**nsulated Gate** Field Effect Transistor **(IGFET)**

28. **If the gate-to-source voltage in an Enhancement MOSFET is zero, what is the current from drain to source?**
In an Enhancement MOSFET if the gate-to-source voltage is zero, then the current from drain to source is also zero.

29. **What is the major difference in construction of the D-MOSFET and the E-MOSFET?**
The depletion MOSFET has a structural channel, whereas the enhancement-MOSFET does not.

30. **If the gate-to-source voltage in depletion MOSFET is zero, what is the current from drain to source?**
When gate –source voltage is zero for depletion MOSFET, the drain-source current is equal to I_{DSS}. (I_D_I_{DSS})

31. **What are the precautions to be taken when handling MOSFET?**
a) MOSFET should be shipped and stored in a conduction foam rubber.
b) Prior to soldering, the technician should use a shorting strap to discharge his static electricity.
c) The soldering iron tip to be grounded. d) MOSFETs should never be inserted into or removed from a circuit with the power on.
e) The assembler should wear antistatic clothes and ground wrist beads.
f) All the instruments and metal benches used to test the MOS devices should be connected to ground.
g) Always avoid touching the device terminals and pick up the transistor by its casing.

32. **What are the applications of MOSFET?**
a) It can be used as input amplifiers in oscilloscope, electric voltmeters etc.
b) It is used in logic circuits.
c) It is used in computer memories.
d) It is used in phase shift oscillators.
e) It is used in FM and TV receivers.

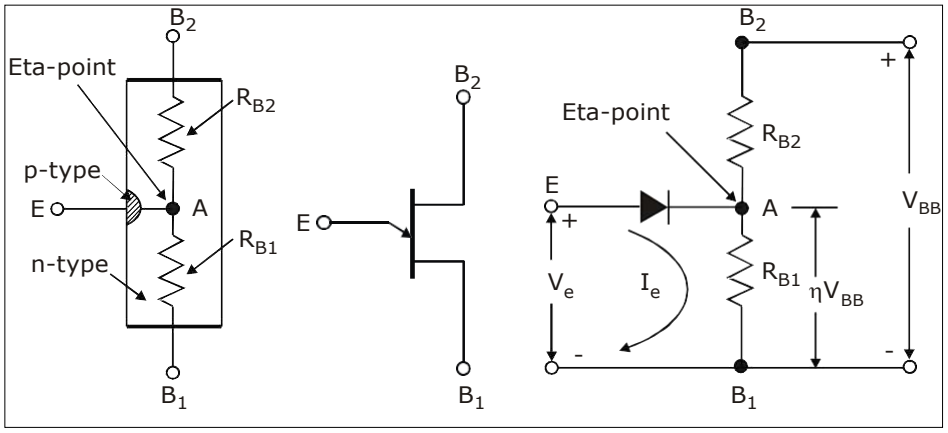
33. **Depletion MOSFET is commonly known as "Normally-ON" MOSFET why?**
The depletion MOSFET can conduct even if the gate to source voltage (V_{GS}) is zero. Because of this reason depletion MOSFET is community known as "Normally-ON" MOSFET.

34. **What is the difference between JFET and MOSFET? (May / Jun 2016)**

S. No.	JFET	MOSFET
1	Reverse bias for gate	Positive or negative gate voltage
2	Gate is formed as a diode	Gate is formed as a capacitor
3	Operation only depletion mode	Can be operated either in depletion mode or in enhancement mode.
4	High input impedance	Very high input impedance due to capacitive effect.

UJT

35. **Draw the structure of UJT. (Nov/Dec 2017)**



36. What is UJT?

Uni junction transistor is a three terminal semiconductor device consisting of only one PN junction. It differs from ordinary PN diode in the sense that it has three terminals namely Emitter, Base 1 and Base 2.

37. Describe the construction of UJT?

UJT consists of lightly doped TV type is semiconductor bar with a heavily doped ***P*** type material.

N type bar is called **base** and ***P*** type region is called **emitter.** Hence ***PN*** junction is formed between emitter and base region.

Since base is lightly doped the resistivity of the base material is very high.

The direction of arrowhead in the UJT symbol represents the conventional direction of current flow when UJT is in conduction state.

38. State two applications of UJT. (Nov/Dec 2018)

1. UJT is used to trigger other devices like SCR.
2. Also used in sawtooth wave generators and some timing circuits.
3. It is used as relaxation oscillator to obtain short pulses for triggering of SCR.

39. What is intrinsic stand OFF ratio of UJT and its equivalent circuit? (May 2017)

The intrinsic stand OFF radio (r|) is defined as the ratio between the internal dynamic resistance ***(R_{B1})*** and the inter base resistance ***(R_{BB})***-

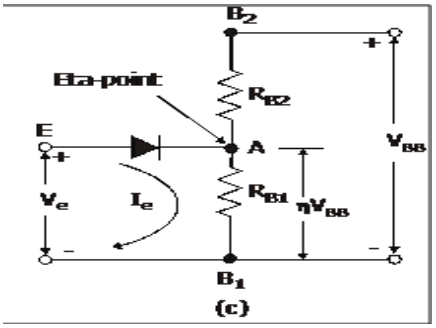
$$\eta = \frac{R_{B1}}{R_{B2}}$$

Where,

$R_{BB} = R_{B1} + R_{B2}$

R_{B1} – internal dynamic resistance

R_{B2} – inter base resistance



40. What are the different regions in characteristics of UJT?

- Cut off Region
- Negative Resistance Region
- Saturation Region

THYRISTOR

41. Describe the basic structure of SCR?

SCR consist of four semiconductor layers forming a PNPN structure. It has three PN junctions namely J_1 , J_2 anode (A), cathode ***(K)*** and the gate (G).

42. What are the different methods used to turn ON SCR?

1. Gate triggering
2. Forward break over voltage
3. Light triggering
4. Rate - effect (or) triggering

43. What is forward break over voltage? (Apr/May 2018)

SCR is forward bias with a small voltage, it is in 'OFF' and no current flows through the SCR. The applied forward voltage is increased, a certain critical voltage called forward break over voltage ***(V_{B0})***.

44. Define holding current? What is the latching current in SCR? (April / May 2019-R17)

Holding current is the current below which the SCR switches from the conduction state (ON state) to ***the forward blocking state.***

Latching Current is the minimum current required to trigger the device from its OFF state to ON state.

45. What is the forward blocking region?

This region corresponding to the OFF condition of the SCR when anode is positives.

46. What is the turn OFF mechanism used for SCR?

To turn OFF a SCR, the following methods are applied.

(i) Reversing polarity of anode-to-cathode voltage called as Gate turn OFF switch (GTO).

(ii)The second method is anode current interruption. Changing anode current by means of momentarily series or parallel switching arrangement.

(iii)Third method is forced commutation. In this, the current through SCR is reduced below the holding current

47. Give the applications of SCR.

Main applications of an SCR are as a power control device. Common areas of applications include

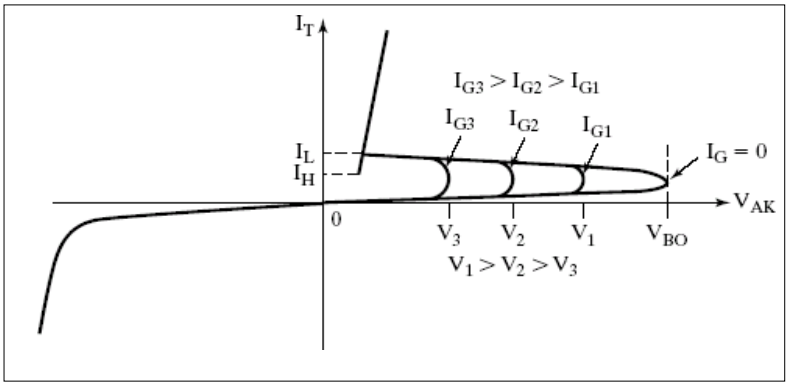
(a). As over light detector
(b). Relay control
(c). Regulated power supplies
(d). Static switches
(e). Motor control
(f). Battery charges
(g). Heater controls
(h). Phase controls
(i). For speed control of DC shunts motor.

48. What are the advantages of SCR?

- SCR controls large current in the load by means of a small gate current.
- SCR size is very compact.
- Switching speed is high.

49. Show how an SCR can be triggered on by the application of a pulse to the gate terminal. (Nov / Dec 2015)

SCR is forward bias with a small voltage, it is in 'OFF' and no current flows through the SCR. The applied forward voltage is increased, a certain critical voltage called forward break over voltage ***(V_{B0}).*** *The forward break over voltage is reduced by application of gate pulses.*



<u>IGBT, DIAC & TRIAC</u>

50. IGBT is a voltage controlled device. Why?

Because the controlling parameter is gate-emitter voltage.

51. Why IGBT is very popular nowadays? MAY/JUNE-2012

1. Lower gate requirements 2. Lower switching losses 3. Smaller snubbed circuit requirements

52. What is DIAC?

A DIAC is two terminal semiconductor device and three-layer bidirectional device, which can be switched from of its OFF to ON state for either negative or positive polarity of applied voltage.

53. What are the applications of DIAC?

The DIAC is used as a triggering device; it is not a control device. It is used in.

- Temperature control
- Triggering of TRIAC
- Light diming circuits
- Motor speed control

54. What is TRIAC?

TRIAC is a three terminal semiconductor switching device which can conduct in either forward or reverse direction. The TRIAC is the combination of two SCR's connected in parallel but in opposite direction.

55. What are the applications of TRIAC?

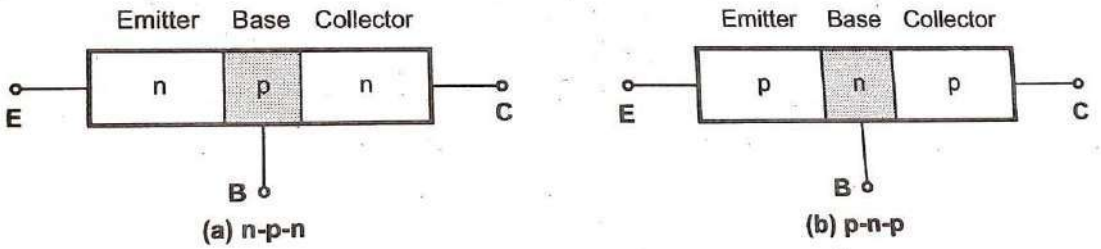
- Heater control
- Phase control
- Light dimming control
- Static switch to turn A.C power ON and OFF.
- Speed control of motor.

PART-B

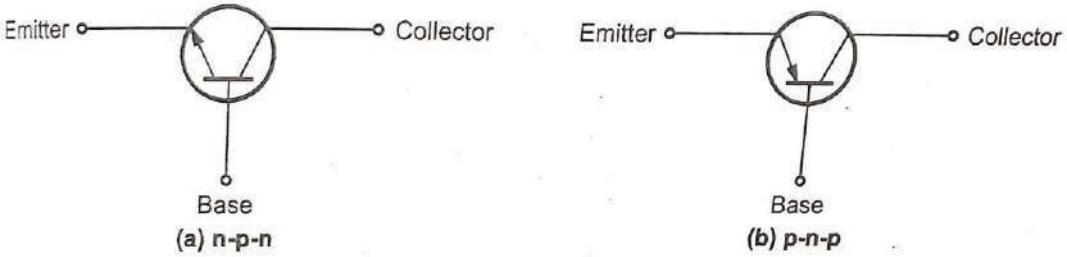
BJT-Structure, Operation & Characteristics

1. Explain about the transistor (BJT) operation.

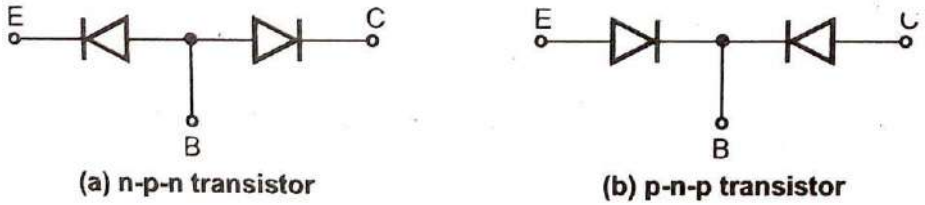
Structure:



Symbol:



Two-diode transistor analogy

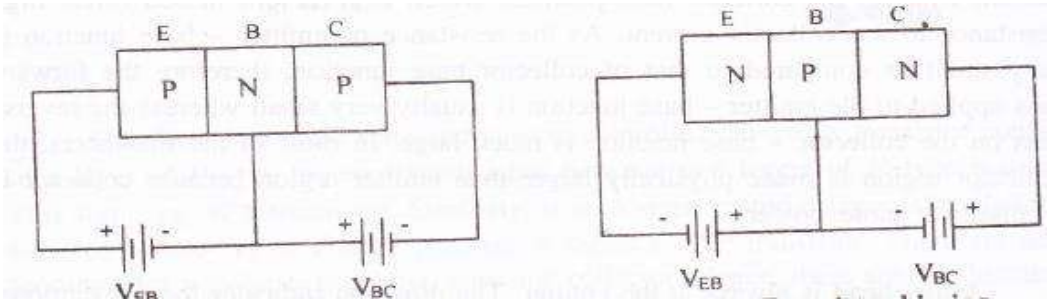


Applying external voltage to a transistor is called biasing. In order to operate transistor properly as an amplifier, it is necessary to correctly bias the two PN junctions with external voltages. Depending upon external bias voltage polarities used, the transistor works in one of the three regions.

1. Active region ***2. Cut-off region*** ***3. Saturation region***

S. No.	Region	Emitter Base	Collector Base	Operation of a transistor
1	Active	Forward biased	Reverse biased	Acts as an amplifier
2	Cut off	Reverse biased	Reverse biased	Acts as an open switch
3	Saturation	Forward biased	Forward biased	Acts as a closed switch

To bias the transistor in its active region the emitter base junction is forward biased, while the collector-base junction in reverse-biased as shown in Fig. The Fig. shows the circuit connections for active region for both NPN and PNP transistors.



Operation of NPN transistor:

As shown in fig. the forward bias applied to the emitter base junction of an NPN transistor causes a lot of electrons from the emitter region to cross over to the base region. As the base is lightly doped with P-type impurity, the number of holes in the base region is very small and hence the number of electrons that combine with holes in the P – type base region is also very small. Hence a few electrons combine with holes to constitute a base current I_B. The remaining electrons (more than 95%) crossover into the collector region to constitute a collector current I_C. Thus the base and collector current summed up give the emitter current i.e. $I_E=-(I_C+I_B)$.

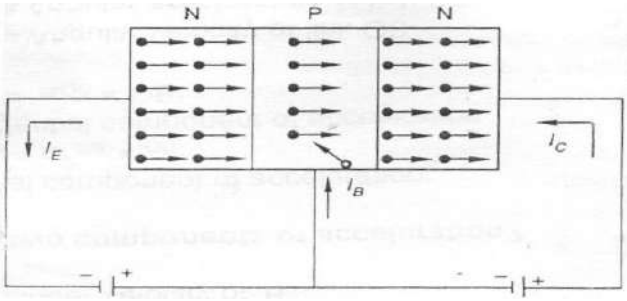


Fig. Current in NPN transistor

In the external circuit of the NPN bipolar junction transistor, the magnitudes of the emitter current I_E, the base current I_B and the collector current I_C are related by $I_E=I_C+I_B$.

Operation of PNP transistor:

As shown in fig. the forward bias applied to the emitter – base junction of a PNP transistor causes a lot of hoses from the emitter regions to cross over to the base region as the base is lightly doped with N-type impurity. The number of electrons in the base regions is very small and hence the number of holes combined with electrons in the N – type base region is also very small. Hence a few holes combined with electrons to constitute a base current I_B.

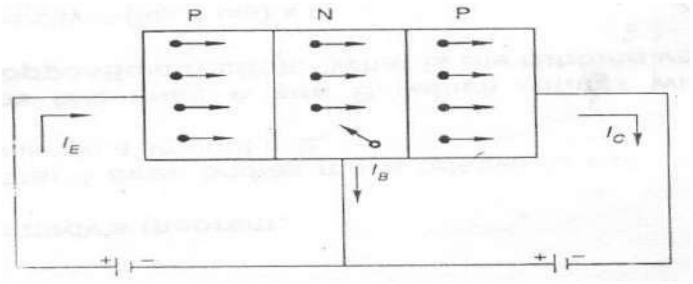


Fig. Current in PNP transistor

The remaining holes (more than 95%) cross over into the collector region to constitute a collector current I_C. Thus, the collector and base current when summed up gives the emitter current.

i.e. $I_E = -(I_C + I_B)$.

In the external circuit of the PNP bipolar junction transistor, the magnitudes of the emitter current I_E, the base current I_B and the collector current I_C are related by

$$I_E = I_C + I_B$$

The equation gives the fundamental relationship between the currents in a bipolar transistor circuit. Also, this fundamental equation shows that there are current amplification factors α and β in common base transistor configuration and common emitter transistor configuration respectively for the static (d.c) currents, and for small changes in the currents.

Large – signal current gain (α). The large signal current gain of a common base transistor is defined as the ratio of the negative of the collector – current increment to the emitter – current change from cut off ($I_E=0$) to I_E,i.e.

$$\alpha = -\frac{(I_c - I_{CBO})}{I_E - 0}$$

where I_{CBO} (or I_{CO}) is the reverse saturation current flowing through the reverse biased collector – base junction. i.e. the collector to base leakage current with emitter open. As the magnitude of I_{CBO} is negligible when compared to I_E, the above expression can be written as

$$\alpha = \frac{I_C}{I_E}$$

Since I_C and I_E are flowing in opposite directions, α is always positive. Typical value of α ranges from 0.90 to 0.995. Also, α is not a constant but varies with emitter current I_E, collector voltage V_{CB} and the temperature.

2. (a) Explain various characteristics of BJT in Common Base configuration with neat diagram.

Common Base Configuration (CB configuration):

This configuration is also called the grounded base configuration. In this case the input is connected between emitter and base while the output is taken across the collector and base. Thus the base of the transistor is common to both input and output circuits and hence the name, common base configuration. The common base circuit arrangement for NPN transistors is shown in Fig.

Current Amplification Factor (α):

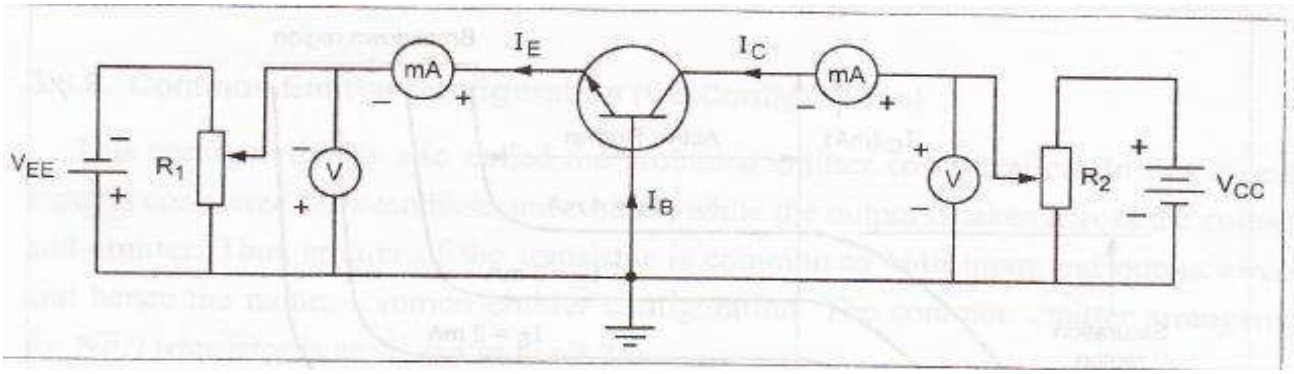
The current amplification factor is defined as the ratio of changes in Collector current (ΔI_C) to the change in emitter current (ΔI_E) when the collector to base voltage (V_{CB}) is maintained at a constant value.

$$\alpha = (\Delta I_C)/(\Delta I_E) \text{ (at constant } V_{CB})$$

The value of α is always less than unity. The practical value of transistors lie between 0.95 and 0.99.

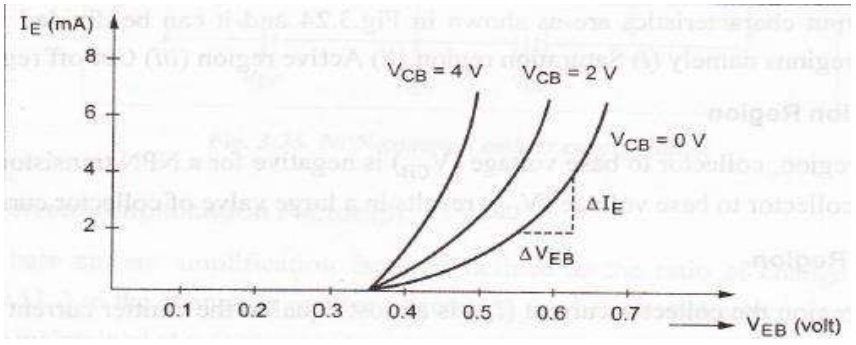
Characteristics of Common Base Configuration:

The circuit arrangement for determining the characteristics of a common base NPN transistors is shown in Fig.In this circuit, the collector to base voltage (V_{CB}) can be varied by adjusting the potentiometer R_2. The emitter to base voltage (V_{EB}) can be varied by adjusting the potentiometer R_l. The DC voltmeters and DC milliammeters are connected in the emitter and collector circuits to measure the voltages and currents.



a). Input Characteristics:

The curve plotted between the emitter current (I_E) and the emitter to base voltage (V_{EB}) at constant collector to base voltage (V_{CB}) are known as input characteristics of a transistor in common base configuration.



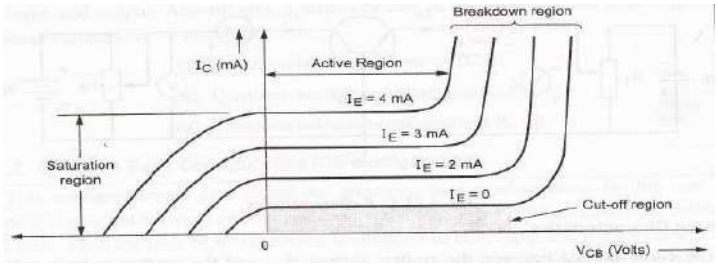
Input Resistance (R_i):

It is the ratio of change in emitter to base voltage (ΔV_{EB}) to the corresponding change in emitter current (ΔI_E) for a constant collector to base voltage (V_{CB}).

$$R_i = \frac{\Delta V_{EB}}{\Delta I_E} \quad \text{(at constant } V_{CB})$$

b). Output Characteristics:

The curve plotted between the collector current (I_C) and the collector to base voltage (V_{CB}) at constant emitter current (I_E) are known as output characteristics of a transistor is common base configuration.



The output characteristics are as shown in Fig. and ***it can be divided into three important regions namely (i) Saturation region (ii) Active region (iii) Cut-off region.***

(i). Saturation Region:

In this region, collector to base voltage (V_{CB}) is negative for a NPN transistor. A small change in collector to base voltage (V_{CB}) results in a large valve of collector current.

(ii). Active Region:

In this region the collector current (I_C) is almost equal to the emitter current (I_E). The transistor is always operated in this region. In the active region, the curves are almost flat. A very large change in V_{CB} produces only a very small change in I_C. It means that the circuit has very high output resistance about 500 K Ω.

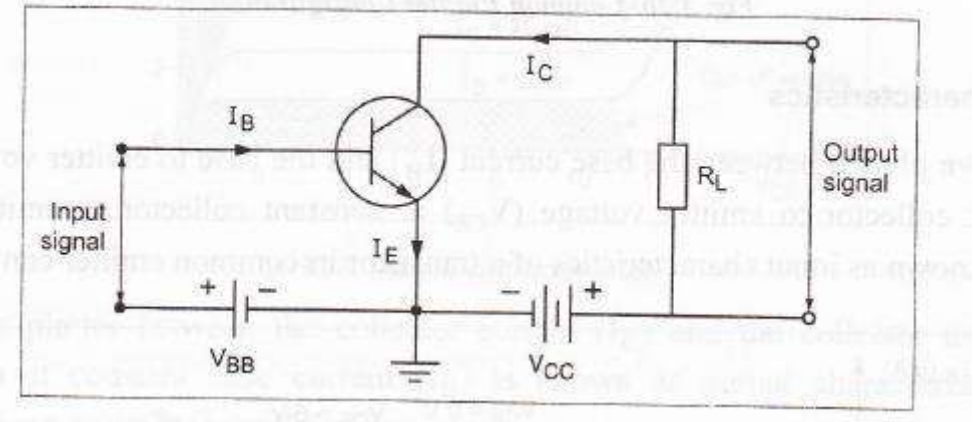
(iii). Cut-off Region:

It is the region along the X-axis as shown by shaded or dotted portion. This corresponds to the curve marked I_E=0. In the cut-off region both the junctions of a Transistor are reverse biased. A small collector current flows even when the emitter Current (I_E) is equal to zero.
If the collector to base voltage (V_{CB}) is increased beyond a certain large value, the collector current (I_C) increases rapidly due to avalanche breakdown and the transistor action is lost. This region is called breakdown region.

(b) For a transistor connected in CE configuration, sketch the typical output and input characteristics and explain the shape of characteristics.

Common Emitter Configuration (CE Configuration):

This configuration is also called the grounded emitter configuration. In this case the input is connected between base and emitter, while the output is taken across the collector and emitter. Thus emitter of the transistor is common to both input and output circuits and hence the name, common emitter configuration. The common emitter arrangement for NPN transistor is as shown in Fig.



Base Current Amplification Factor (β):

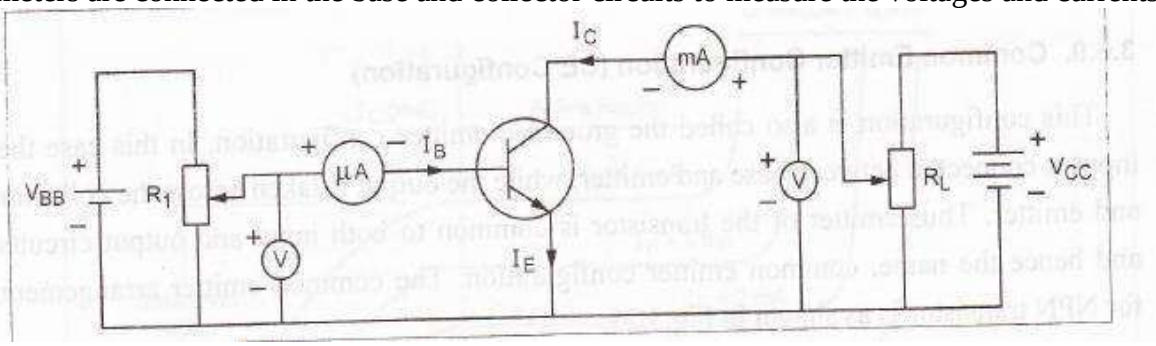
The base current amplification factor is defined as the ratio of change in collector current (ΔI_C) to the change in emitter current (ΔI_E) when the collector to emitter voltage(V_{CE}) is maintained at a constant value.

$$\beta = \frac{\Delta I_C}{\Delta I_B} \text{ (at constant } V_{CE})$$

The value of β is always greater then unity. Practical value of β in commercial transistors lie between 20 to 500.

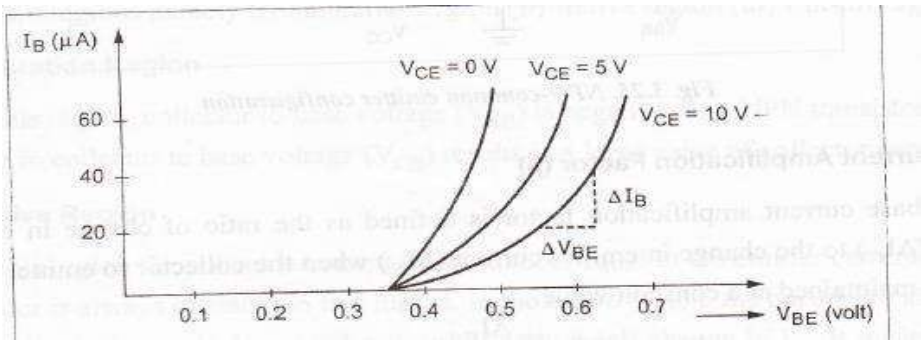
Characteristics of common Emitter configuration:

The circuit arrangement for determining the characteristics of a common emitter NPN transistor is shown inFig.In this circuit, the collector to emitter voltage (V_{EC}) can be varied by adjusting the potentiometer R_2. The base to emitter voltage (V_{BE}) can be varied by adjusting the potentiometer R_1. The DC voltmeters and milliammeters are connected in the base and collector circuits to measure the voltages and currents.



1. **Input Characteristics:**

   The curve plotted between the base current (I_B) and the base to emitter voltage (V_{BE}) at constant collector to emitter voltage (V_{CE}) at constant collector to emitter voltage (V_{CE})are known as input characteristics of a transistor in common emitter configuration.

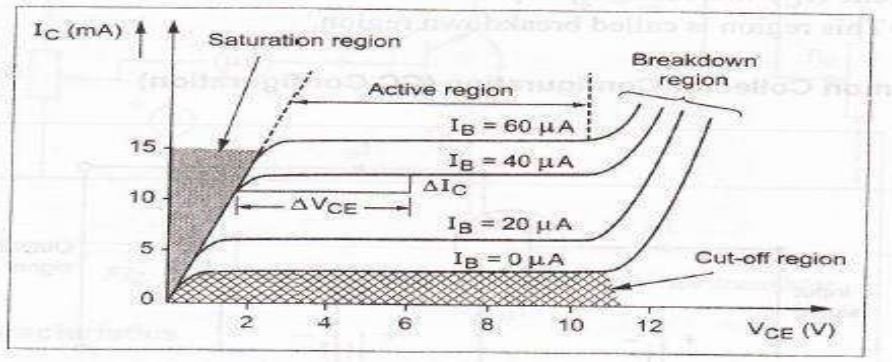


Input Resistance (R_i): It is the ratio of change in base to emitter voltage (V_{BE}) to the Corresponding change in base current (ΔI_B) for a constant collector to emitter voltage (v_{CE}).

$$R_i = \frac{\Delta V_{BE}}{\Delta I_B} \quad \text{(at constant } V_{CE})$$

When the collector to emitter voltage (V_{CE}) is increased, the value of base current (I_B) decreased slightly as shown in Fig.

2. Output Characteristics:



The curves plotter between the collector current (I_C) and the collector to emitter Voltage (V_{CE}) at constant base current (I_B) is known as output characteristic of a transistor in common emitter configuration.
The output characteristic may be divided into three important regions namely saturation region, active region, and cut-off region.

(i) Saturation Region:

In this region (shown by dotted area) a small change in collector to emitter voltage (V_{CE}) results in a large value of collector current.

(ii) Active Region:

It is the region between saturation and cut-off region. In this region the curves are almost flat. When the collector to emitter voltage (V_{CE}) is increased. Further, the collector current I. slightly increases. The slope of the curve is little bit more than the output characteristics of common base configuration. Therefore, the output resistance (R_o) of this configuration is less as compared to common base configuration.

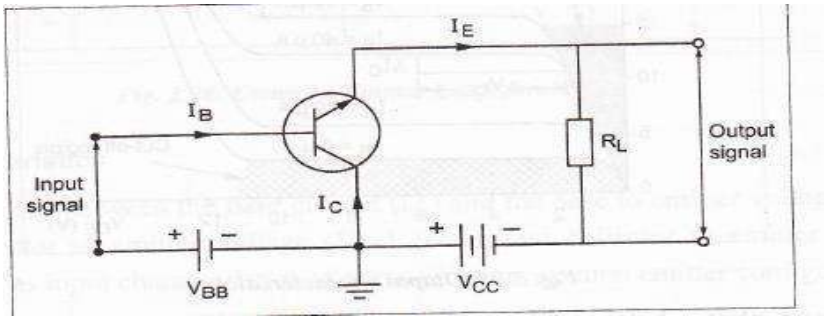
(iii) Cut-off Region:

It is the region along the X-axis is shown by shaded area. This corresponds to the curve marked $I_B = 0$. In the cut-off region both the junctions of a transistor are reverse biased. A small collector current flows even when the base current (I_B) is equal to zero. It is the reverse leakage current (I_{CEo})that flows in the collector circuit.

If the collector to emitter voltage (V_{CE}) is increased beyond a certain large collector current (I_C) increases rapidly due to avalanche breakdown and the action is lost. This region is called breakdown region.

(c) Explain various characteristics of BJT in Common Collector configuration with neat diagram.

Common collector configuration (CC configuration):



This configuration is also called the grounded collector configuration' In this case the input is common between base and Collector. While the output is taken across the emitter and collector. Thus the collector of the transistor is common to both input and output circuits and hence the name common collector configuration. The common collector circuit arrangement for NPN transistor as shown in Fig.

Current Amplification Factor (γ):

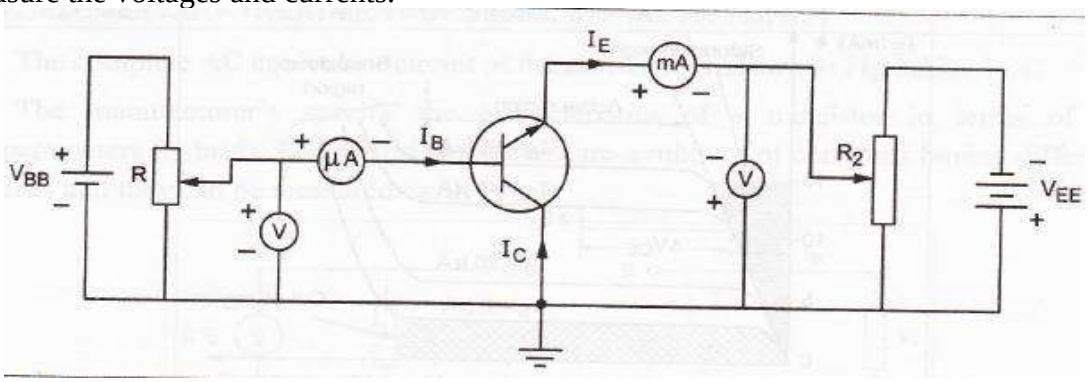
The current amplification is defined as the ratio of change in emitter current (ΔI_E) to the change in base current (ΔI_B). It is generally denoted by γ.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

The value of γ is nearly equal to β.

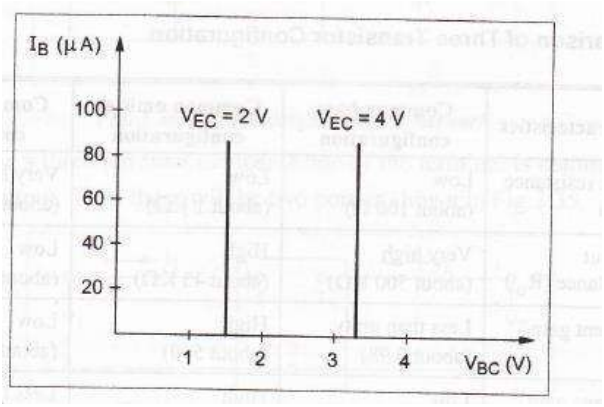
Characteristics of common Collector configuration:

The circuit arrangement for determining the characteristics of a common collector NPN transistor is shown in Fig. In this circuit, the emitter to collector voltage (V_{EC}) can be varied by adjusting the potentiometer R_2. The base to collector voltage (V_{BC}) can be varied by adjusting the potentiometer R_1. The DC voltmeter and millimeters are connected in the base and emitter circuits to measure the voltages and currents.



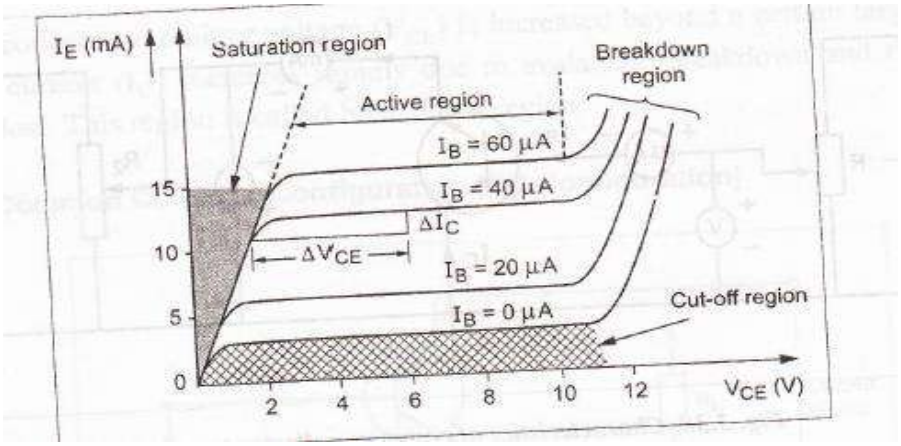
1. Input Characteristics:

The curves plotted between the base current (I_B) and the base to collector voltage (V_{BC}) at constant emitter to collector voltage (V_{EC}) are known as input characteristics of a transistor in common collector configuration.



2. Output Characteristics:

The curves plotted between the emitter current (I_E) and the emitter to collector voltage (V_{EC}) at constant base current (I_B) are known as output characteristics of a transistor is common collector configuration.

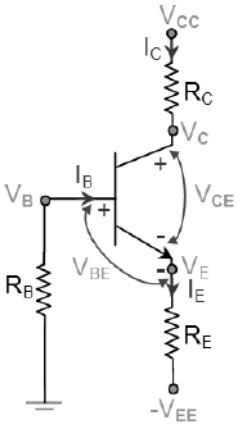


3. Explain the emitter bias method used in transistor amplifier circuits. (Nov/Dec 2017)

Emitter Bias

This biasing network uses two supply voltages, V_{CC} and V_{EE}, which are equal but opposite in polarity. Here V_{EE} forward biases the base-emitter junction through R_E while V_{CC} reverse biases the collector-base junction. Moreover

$$V_E = -V_{EE} + I_E R_E$$
$$V_C = V_{CC} - I_C R_C$$
$$V_B = V_{BE} + V_E$$
$$I_C = \beta I_B$$
$$I_E \approx I_C$$



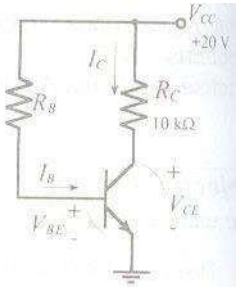
Emitter Bias Circuit

In this kind of biasing, I_C can be made independent of both β and V_{BE} by choosing $R_E >> R_B/\beta$ and $V_{EE} >> V_{BE}$, respectively; which results in a stable operating point.

4. Explain the selection of Q point for transistor bias circuits and discuss the limitations on the output voltage swing. (Nov / Dec 2015)

The dc load line for a transistor circuit is a straight line drawn on the transistor output characteristics. For a common emitter CE circuit. The load line is a graph of collector current versus collector emitter voltage for a given value of collector resistance and a given supply voltage. The load lines show all corresponding levels of I_c and V_{CE} that can exist in a particular circuit.

Consider the common emitter circuit in fig. Note that the polarities of the transistor terminal voltage are such that the base emitter junction is forward biased and the collector base junction is reverse biased. These are the normal bias polarities for the transistor junctions. The dc load line for the circuits in fig drawn on the device common emitter characteristics in fig.



V_{CE} = (Supply voltage) – (Voltage drop across R_C)

$V_{CE} = V_{CC} - I_C R_C$

If the base emitter voltage is zero, the transistor is not conducting and IC = 0. Substituting the V_{CC} and R_C values from fig into equal 5-1

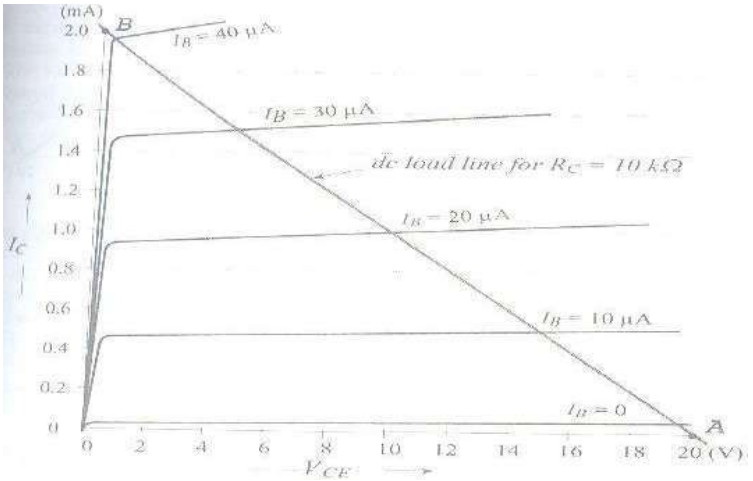
V_{CE} = 20V – (0*10k ohms) =20V

Plot point A on the common emitter characteristics in fig. 5-2 at I_c = 0 and V_{CE} = 20V. This is one point on the dc load line.

Now assume a collector current of 2mA, and calculate the corresponding collector emitter voltage level.

V_{CE} = 20V-(2mA*10k ohms) =0V

Plot point B fig 5-2 at VCE = 0 and I_C = 2mA. The straight line drawn though point A and point B is the dc load line for R_C = 10kohms and V_{CC} = 20V. If either of these two quantities is changed, a new load line must be drawn.



As already stated the dc load line represents all corresponding I_C and V_{CE} levels that can exist in the circuit as represented by Eq. 5-1 for example a point plotted at V_{CE} = 16V and I_C = 1.5mA on fig 5-2 does not appear on the load line. This combination of voltage and current cannot exist in this particular circuit. Knowing any one of I_B, I_C, or V_{CE}, it is easy to determine the other two from a dc load line drawn on the device characteristics. It is not always necessary to have the device characteristics in order to draw the dc load line. A simple graph of I_C versus V_{CE} can be used as demonstrated in example 5-1.

Limitation on the output voltage swing:

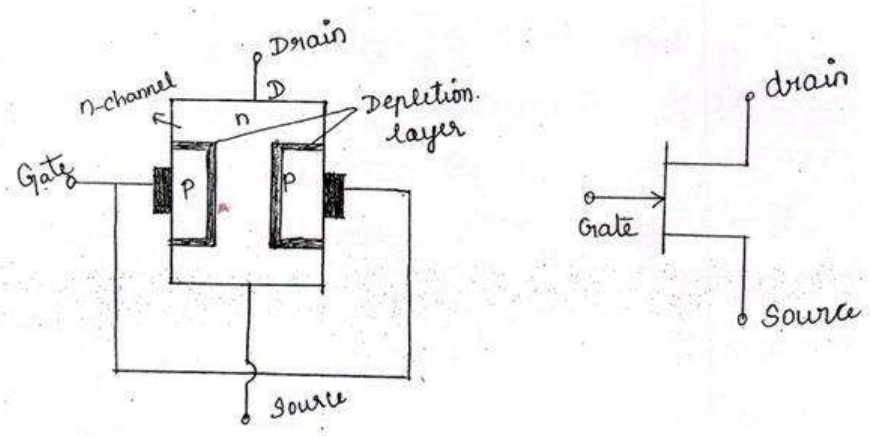
The maximum possible transistor collector emitter voltage swing for a given circuit can be determined without using the transistor characteristics. For convenience, it may be assumed that I_c can be driven to zero at one extreme and to V_{cc} / R_c at the other extreme, [see fig]. This changes the collector emitter voltage from $V_{CE} = V_{cc}$ to $V_{CE} = 0$, as illustrated in fig. thus with the Q point at the center of the load line, the maximum possible collector voltage swing is seen to be approximately $\mp V_{cc}/2$.

JFET- Structure, Operation & Characteristics

5. (a) Explain construction and operation of Junction Field Effect Transistor (JFET)? (NOV/DEC 2012) (May/June-2012)
(b) Explain drain and transfer characteristics of JFET? (May 2017)

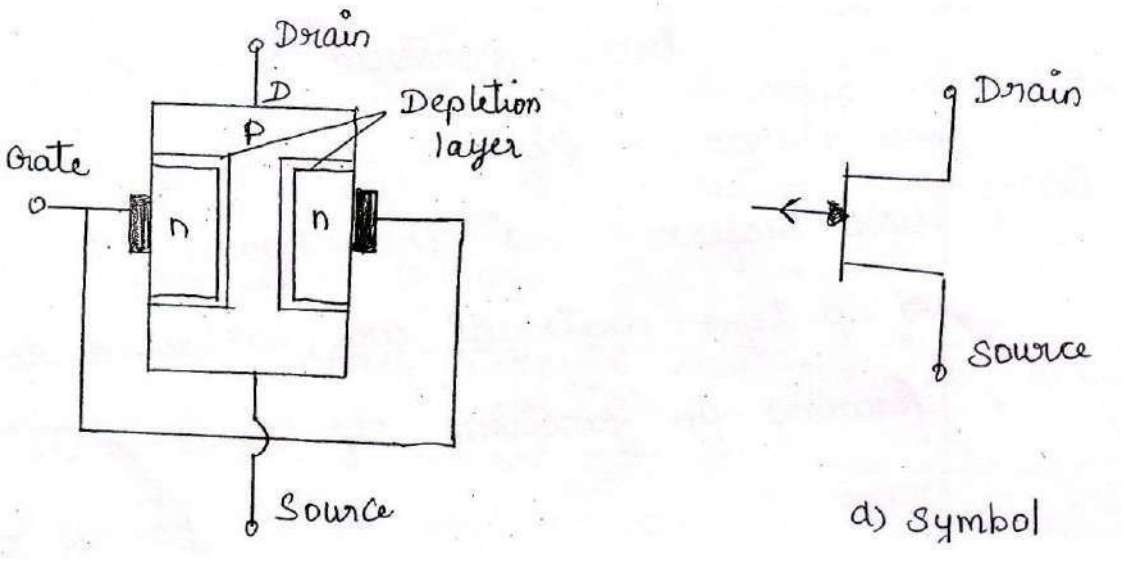
(a) Construction and operation:

The basic construction of an n-channel JFET is shown in fig. It consists of an n-type silicon bar referred as the channel. Two small pieces of p-type material are attached to its sides forming pn junctions. If the bar is of n-type the JFET is called as on n-channel JFET, and if the bar is of p-type it is called a p-type channel JFET fig shows schematic diagram of both types of FET's with their symbols.



N-channel JFET **Symbol**

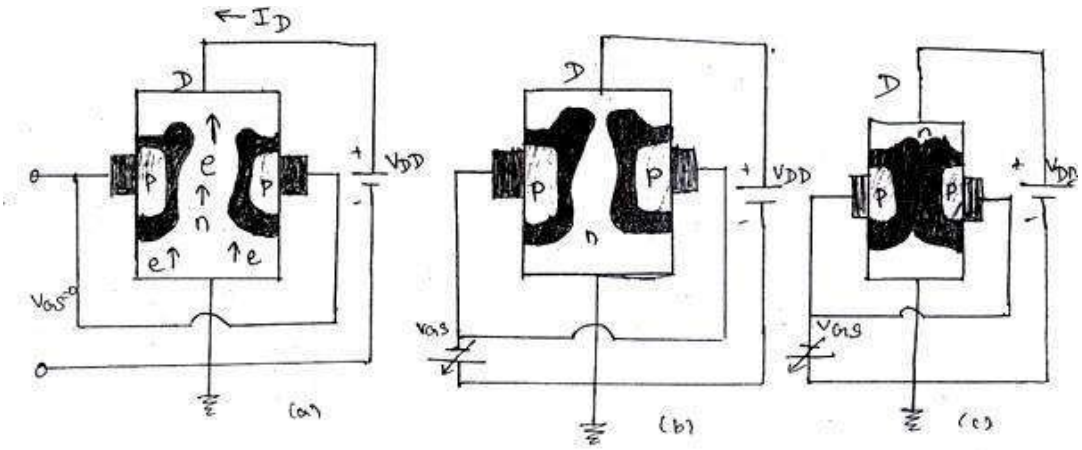
The channel ends are designated as source(S) and drain (D). The source S is the terminal through which the majority carriers enters the bar and drain D is the terminal through which the majority carriers leave the bar. The two p-regions, which are formed by alloying or by diffusion, are connected together and their terminal is called gate. When no bias applied to JFET, depletion regions are formed at two pn junctions as shown in fig. Recall that depletion region is a region depleted of charge carriers and therefore behaves insulators



P-channel JFET

Operation of N-channel JFET

When Vds is of some fixed positive value and reverse bias on Vgs increasing.



Operation of N-channel JFET

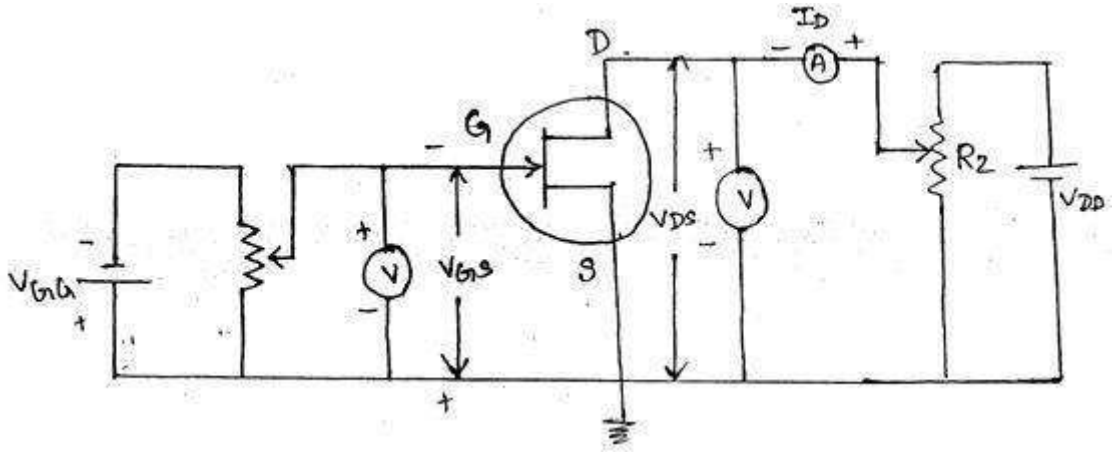
Let us assume that the gate is not biased and a fixed positive voltage is applied between the drain and source terminals as shown in fig. Due to this applied voltage will move through the n-type channel from source to drain. When the gate is negative biased with respect to source, the pn junction are reverse biased and the depletion region are formed. Since the channel is lightly doped compared to heavily doped p-region, the depletion region penetrates deeply into the channel. As a result, the effective channel resistance significantly and reduces the drain current I_D. If the reverse biased on the gate is increased further the depletion will cover the entire width of the channel and ID is cut off completely fig.

2.V_{GS}=0, V_{DS} is varied

First assume that the gate source voltage (V_{GS}) is set to the zero. When the drain source voltage V_{DS} is also zero, the current flowing through FET is also zero that is I_D=0.The instant the voltage V_{DS} is applied, electrons starts flowing from source to drain terminals establishing the current I_D under this condition the channel between drain and source act as a resistance.

(b) Characteristics of JFET:-

The circuit diagram to obtain the characteristics of JFET is shown in fig.



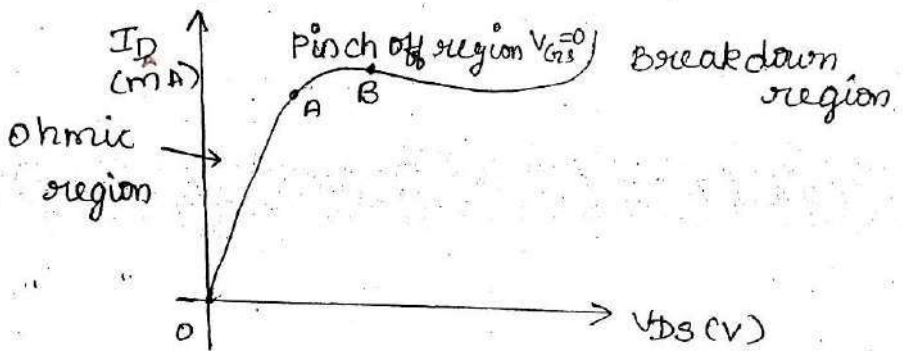
The characteristics that we consider are

i) Drain characteristics ii) Transfer characteristics

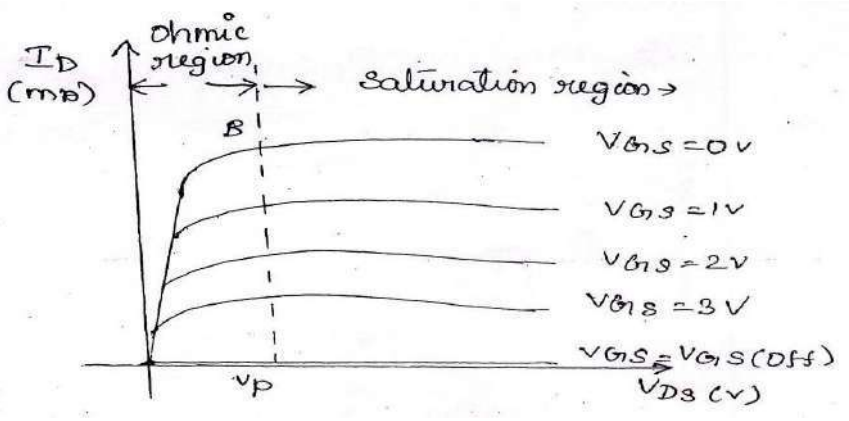
In drain characteristics the relation between Id and VDS for different values of VGS is plotted. In transfer characteristics the relation between ID and VDGS for constant is plotted.

(i) Drain characteristics with V_{GS}=0 (May 2017)

The drain characteristics for V_{GS}=0 is shown in fig. To plot this characteristic the gate to source voltage is kept at zero and V_{DS} is varied from zero. When V_{DS} is zero the drain current I_D is also zero. When V_{DS} is increased the drain, current starts flowing through the channel and FET behaves like a resistor till point A. That is for low values of V_{DS}, current varies directly with voltage following ohm's law. The portion of characteristics where the FET behaves like a resistor is known as ohms region. The FET can be used as a voltage variable resistor in this region if we increase V_{DS}, a stage is reached at which pinch off occurs and the drain current reaches a saturation level. The drain to source voltage at which pinch off occurs is known as pinch off voltage V_P, and corresponding I_D is known as I_{DSS}. The point B at which pinch-off occurs is shown in fig. Even if we increase V_{DS} above V_P the drain current V_{DS} above Vp the drain current does not increase. The region where the drain current is constant inspite of the variation in V_{DS} is known as pinch-off region. If we increase V_{DS} for there a stage is reached at which the gate channel junction FET breakdown and increase rapidly. This region in the characteristics is known as breakdown region. When a bias (-1V) is applied between gate source the pinch off occurs at less drain current less than I_{DSS}. The drain characteristics for different values of V_{GS} shown fig.



Characteristics of JFET for VGS=0



Characteristics of JFET for different values of V_{GS}

(ii) Transfer characteristics

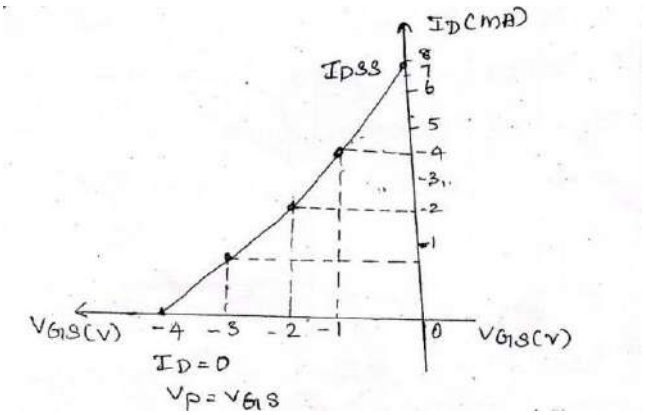
It is a plot of drain current Id versus V_{GS} constant values. To plot the characteristics V_{DS} is kept constant and V_{GS} is varied. When V_{GS}= the current flowing the FET is Equal to I_{DSS} and when V_{GS}=V_{GS} (off), the drain current is zero.

Shockley's equation:-

The relation between V_{GS} and I_D can be represented by Shockley's equation

$I_D = I_{DSS}(1-V_{GS}/Vp)^2$ 3.1

Using this mathematically expression, we can develop the plot of I_D versus V_{GS} for any JFET, provide the two parameters I_{DSS} and Vp are known.



Transfer characteristics of JFET.

MOSFET- Structure, Operation & Characteristics

6. **With neat diagram explain the construction & working of depletion MOSFET and enhancement MOSFET with its necessary characteristics curve.** ***(Nov/Dec 2018 R-13)*** ***(May/June 2016)*** ***(Apr/May 2018)***

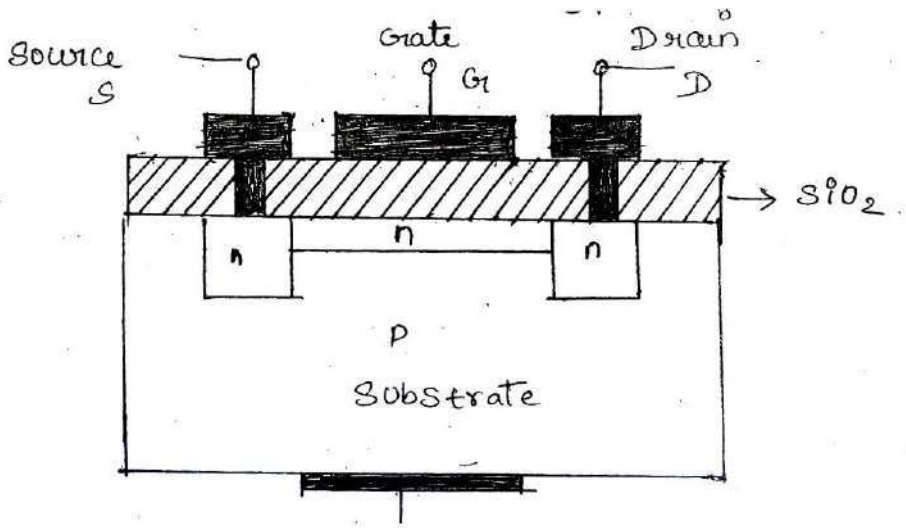
OR

Brief about the construction and operation of *n-channel depletion type MOSFET* with a neat diagram. Enumerate the characteristics of *depletion type* MOSFET with a suitable graph. (April/May 2019-R17)

Depletion MOSFET:

- The construction of an N-channel depletion MOSFET is shown in fig. If consists of a lightly doped p-type substrate in which two highly doped n-regions are diffused. The two heavily doped n-

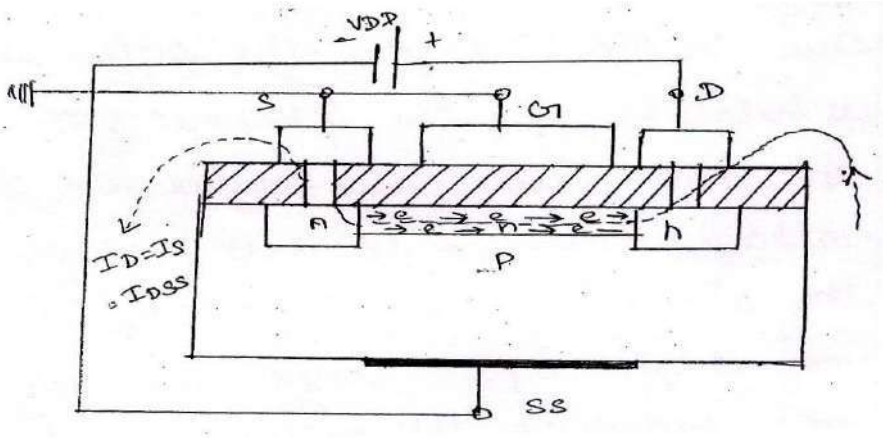
regions act as the source and drain. A lightly doped n-type channel is introduced between the two heavily doped source and drain. A thin layer of (1µm thick) silicon dioxide is coated on the surface. Holes are cut in the oxide layer to make contact with n-regions due to sio_2 layer the gate is completely insulated from the channel. This permits operation with gate source or gate channel voltages above and below zero. In addition the insulated layer of sio_2 accounts for very high input impedance of MOSFET. In some MOSFETS the p-type substrate is internally connected to source, whereas in many discrete devices an additional terminal is provided for substrate labeled SS.



SS substrate

Basic operation:

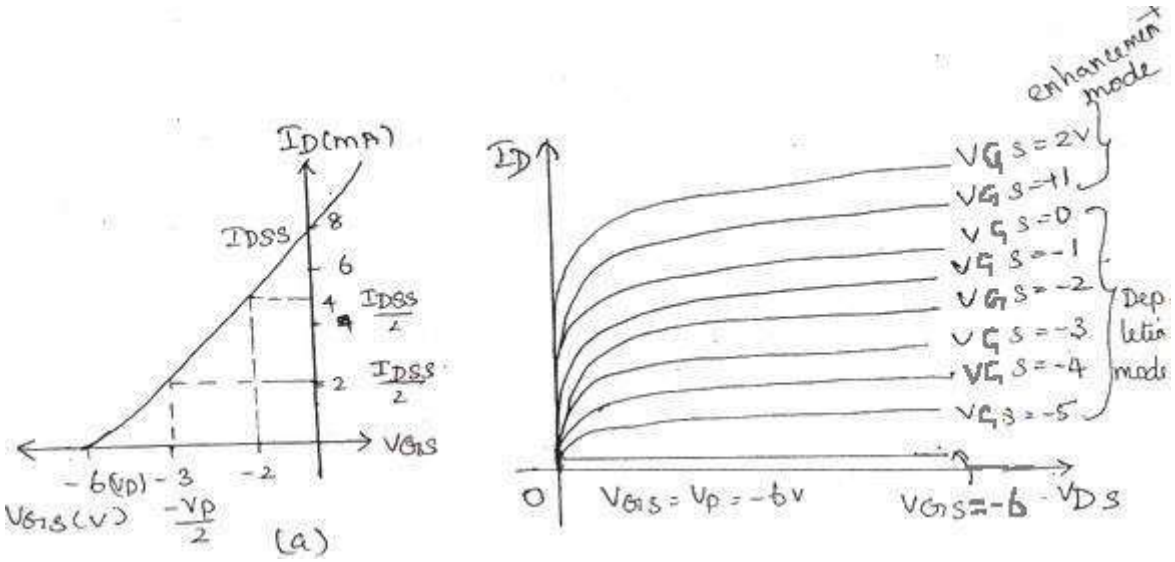
In fig a voltage VDS is applied between the drain and source terminals and the gate to source voltage is set to zer. As a result, current is established from drain to source (conventional direction) similar to JFET like in JFET, the satuarated drain current IDSS flow during pinch-off and it is labeled as IDSS.



If a negative voltage is applied to gate with repeat to source. These holes recombine with electrons and reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, lesser the number of free electrons in the channel. Since the negative voltage on the gate deplete channel, the device is referred to as depletion MOSFET. The depletion mode of operation is similar to JFET operation. When sufficient negative voltage is applied to gate the channel may be completely cut off and the corresponding V_{GS} is called (V_{GS} (OFF)).

If a positive voltage is applied to gate with respect to source then the electrons are induced in the channel. The induced electrons constitute additional current from source to drain. If we increase V_{GS} more in positive direction more number of electrons is induced and hence the drain current increases.

That is, the application of a positive gate –to –source voltage has enhanced the number of charge carriers compared to that of when V_{GS}=0v. For this reason the mode in which the MOSFET. Operates for positive values of gate-to-source voltage is known as enhancement mode.

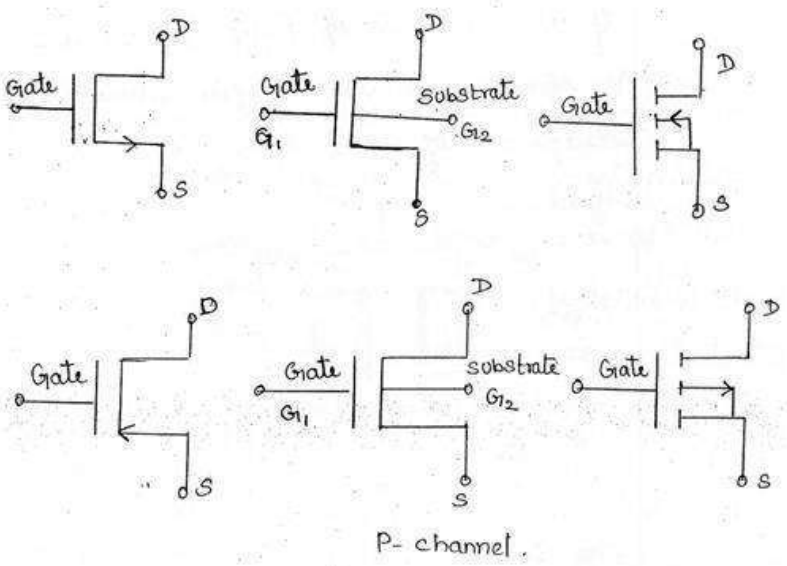


It is a plot of drain current versus drain source voltage for various value of gate-source voltage. The drain characteristics of depletion MOSFET is shown ii fig. Note that for negative of V_{GS} the characteristics of depletion MOSFET is similar to those N-channel JFET. If the gate is made positive additional carrier are introduced in the channel and the channel conductivity increases. Therefore the depletion MOSFET consists of two regions of operation

.

The transfer characteristics of deletion MOSFET is shown in fig. The general shape of the transfer characteristics is similar to those for the JFET. However the deletion MOSFET can be operated with V_{GS}>0. As a result IDSS is not maximum drain current as it is for JFET. The equation fior transfer characteristics curve of depletion MOSFET is same as that of JFET.

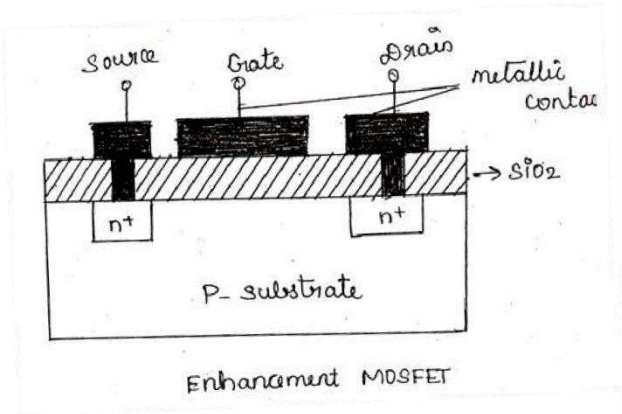
The three circuit symbols for n-channel MOSFET and p-channel MOSFET are shown in fig.



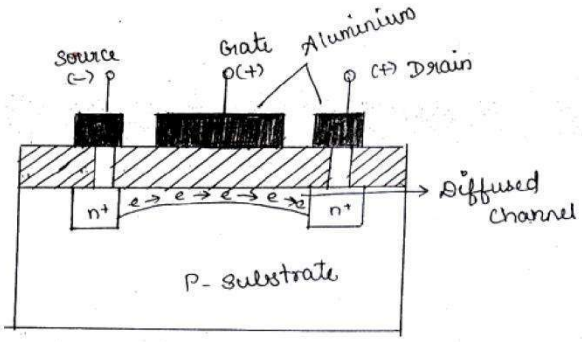
Symbol of N-channel and P-channel MOSFET'S

N-channel enhancement MOSFET ***(May/June-2013), (May/June2016), (Nov/Dec2015) (May 2017) (Apr/May 2018)***

• The construction of *n-channel enhancement MOSFET* is shown in fig. like depletion MOSFET it also consists of a p-type substrate and two heavily doped n-regions that act as source and drain. The sio_2 layer is present to isolate the gate from the region between the drain and source. The source and drain terminals are connected through metallic contacts to n-doped regions. But the enhancement MOSFET does not contain diffused channel MOSFET does not contain diffused channel between the source and drain



Enhancement MOSFET



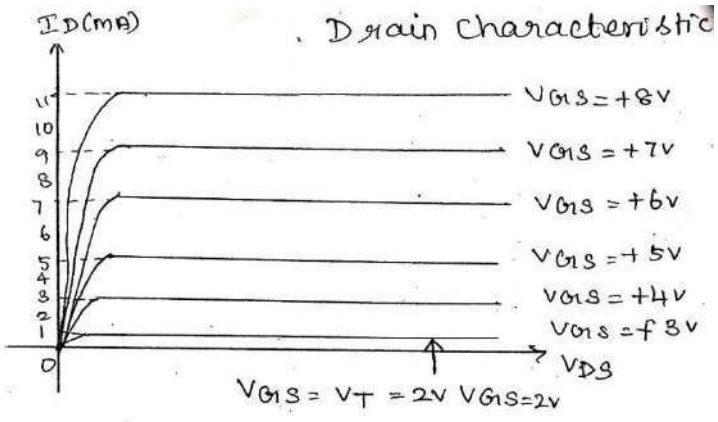
working of N- channel enhancement MOSFET

When the drain is made positive with repeat to source and no potential is applied to gate due to absence of the channel, a small drain current (ie., a reverse leakage current) flows. The we apply a positive voltage to that gate with respect to source and substrate, negative charge carriers are induced in the substrate the negative charge carriers which are minority carriers in the p-type substrate form an "inversion layer". As the gate potential is increased more and more negative charge carriers are induced. There negative carriers that are accumulated between source and drain current flows from source to drain through the induced channel. The magnetized of the drain current depends on the gate potential. Since the conduction of the channel is enhanced by the positive bias voltage on the gate the device known as enhancement MOSFET.

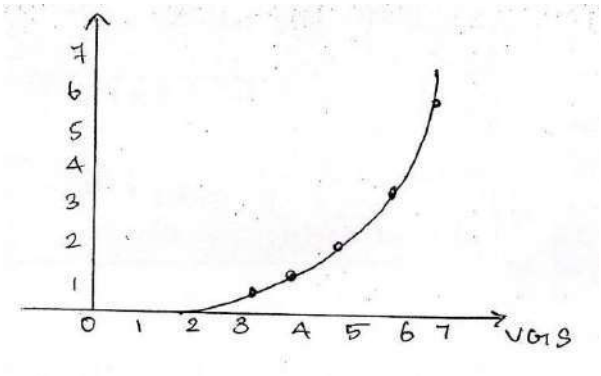
Drain characteristics :

The drain characteristics of enhancement MOSFET is shown in fig.

The current IDSS for VGS=0 is very small of the order of nano amperes shown in fig. Note that the drain current increases with positive increases with positive increase in gate source have voltage.



Transfer characteristics:



The n-channel enhancement MOSFET requires a positive gate to source voltage for its operation fig shows the general transfer characteristics of an n-channel MOSFET. Since the drain current is zero for VGS=0, the IDSS is zero for this device. As VGS is made positive the current ID increases slowly at first and then more rapidly with an increase in VGS. The gate source voltage at which there is significant increase in drain current is called the threshold voltage and is referred to as VT or VGS the equation for the transfer characteristics of enhancement MOSFET differs as the curve states at VGS(th) rather than at VGS. The equation for transfer characteristics is I_D=K(V_{GS}–$V_{GS(th)}$)^2

<u>UJT (UNIJUNCTION FIELD EFFECT TRANSISTOR)</u>

7. (a) Explain the construction operation and characteristics of UJT? (May/June2016), (Nov/Dec2015) (Nov/Dec 2018)
(b) Describe the operation of UJT as a relaxation oscillator and derive its frequency of oscillation? (Nov/Dec 2016)

(A) UNI-JUNCTION TRANSISTOR (UJT)

Construction:

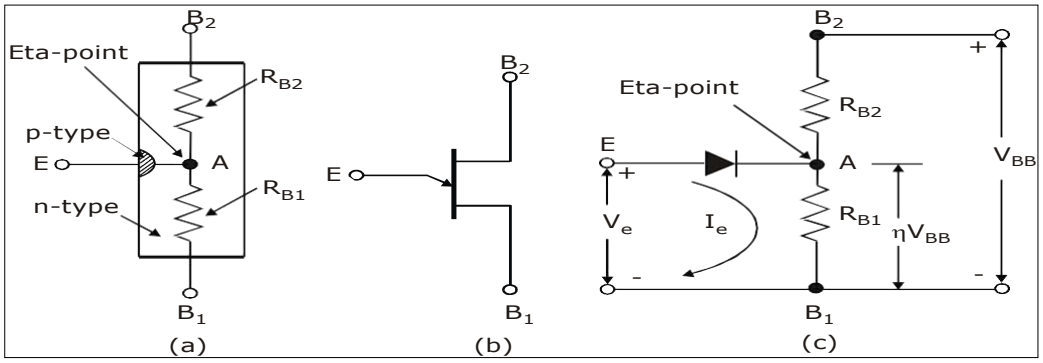


Fig.: (a) Basic structure of UJT (b) Symbolic representation (c) Equivalent circuit

UJT is an n-type silicon bar in which p-type emitter is embedded. It has three terminals base1, base2 and emitter 'E'. Between B_1 and B_2 UJT behaves like ordinary resistor and the internal resistances are given as R_{B1} and R_{B2} with emitter open $R_{BB} = R_{B1} + R_{B2}$. Usually the p-region is heavily doped and n-region is lightly doped. The equivalent circuit of UJT is as shown. When V_{BB} is applied across B_1 and B_2, we find that potential at A is

$$V_{AB1} = \frac{V_{BB}R_{B1}}{R_{B1}+R_{B2}} = \eta V_{BB} \quad \left[\eta = \frac{R_{B1}}{R_{B1}+R_{B2}}\right]$$

η is intrinsic standoff ratio of UJT and ranges between 0.51 and 0.82. Resistor R_{B2} is between 5 to 10KΩ.

OPERATION

When voltage V_{BB} is applied between emitter 'E' with base 1 B_1 as reference and the emitter voltage V_E is less than $(V_D + \eta V_{BE})$ the UJT does not conduct. $(V_D + \eta V_{BB})$ is designated as V_P which is the value of voltage required to turn on the UJT. Once V_E is equal to $V_P \equiv \eta V_{BE} + V_D$, then UJT is forward biased and it conducts.

The peak point is the point at which peak current I_P flows and the peak voltage V_P is across the UJT. After peak point the current increases but voltage across device drops, this is due to the fact that emitter starts to inject holes into the lower doped n-region. Since p-region is heavily doped compared to n-region. Also holes have a longer life time, therefore number of carriers in the base region increases rapidly. Thus potential at 'A' falls but current I_E increases rapidly. R_{B1} Acts as a decreasing resistance.

The negative resistance region of UJT is between peak point and valley point. After valley point, the device acts as a normal diode since the base region is saturated and R_{B1} does not decrease again.

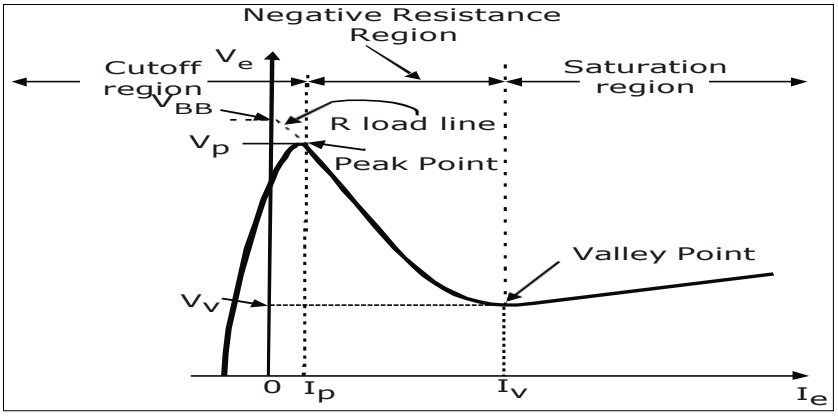


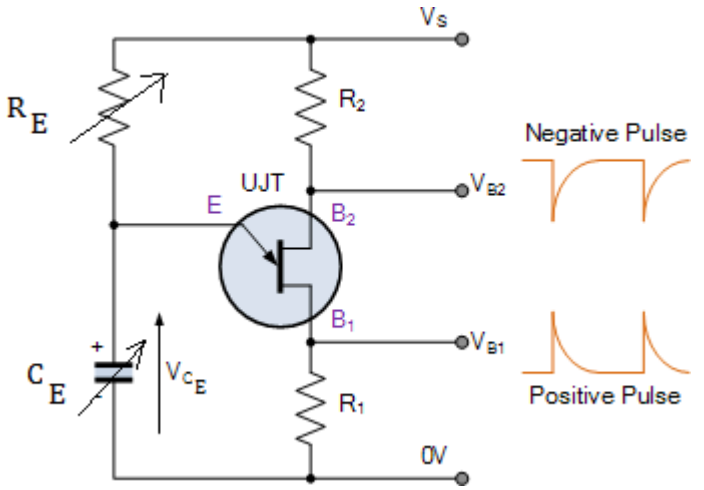
Fig.: V-I Characteristics of UJT

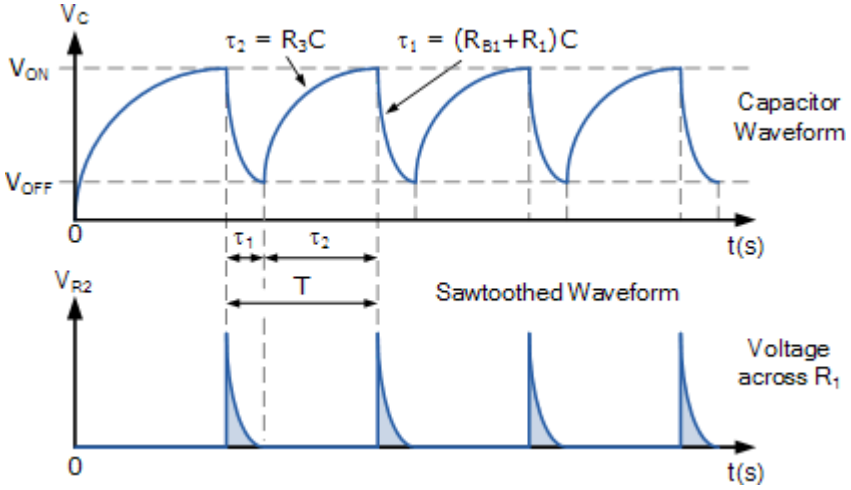
(B)* Operation of UJT as a relaxation oscillator and its derivation- frequency of oscillation.** ***(Nov 2016)

UJT as a relaxation oscillator consists of UJT and a capacitor C_E which is charged through R_E as the supply voltage V_{BB} is switched ON. The voltage across the capacitor increases exponentially and when the capacitor voltage reaches the peak point voltage V_p, the UJT starts conducting and the capacitor voltage is discharged rapidly through EB_1 and R_1.After the peak point voltage of UJT is reached, it provides negative resistance to the discharge path which is useful in working of the relaxation oscillator. As the capacitor voltage reaches zero the device then cuts off and capacitor C_E starts to charge again. This cycle is repeated continuously generating a saw tooth waveform across C_E.

The inclusion of external resistors R_2 and R_1 in series with B_2 and B1 provides spike waveform. When the UJT fires, the sudden surge of current through B_1 causes drop across R1,which provides positive spikes. At the time of firing fall of V_{EB1} causes I_2 to increases rapidly which generates negative going spikes across R_2.

By changing the value of R_E and C_E the frequency of oscillation changes.





Frequency of oscillation:

Voltage across the capacitance prior to breakdown is given by

$V_c=V_{BB}(1- e^{-t/R_EC_E})$

R_EC_E- Charging time constant

Discharge of capacitor occurs when V_C is equal to the peak point voltage V_p,

$V_p= \eta V_{BB}=V_{BB}(1- e^{-t/R_EC_E})$

Where $\eta =(1- e^{-t/R_EC_E})$

$e^{-t/R_EC_E} =1- \eta$

Taking Log on both side

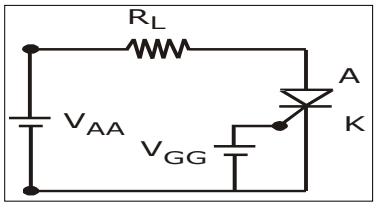
$$\frac{t}{R_EC_E} = \log_e \frac{1}{(1-\eta)}$$

$$t = R_EC_E \ln \frac{1}{(1-\eta)}$$

$$f = 1/t = \frac{1}{R_EC_E \ln \frac{1}{(1-\eta)}}$$

THYRISTOR (SCR)

8. DRAW AND EXPLAIN THE V-I CHARACTERISTICS OF THYRISTOR (SCR) (or) DISCUSS THE DIFFERENT MODES OF OPERATION OF THYRISTOR WITH THE HELP OF ITS STATIC V-I CHARACTERISTICS. (Nov/Dec 2017) (Apr/May 2018) (OR)
Outline the structure of SCR and explain its operation. Also, illustrate its V-I characteristics. (Apr/May 2019-R17)



Circuit diagram

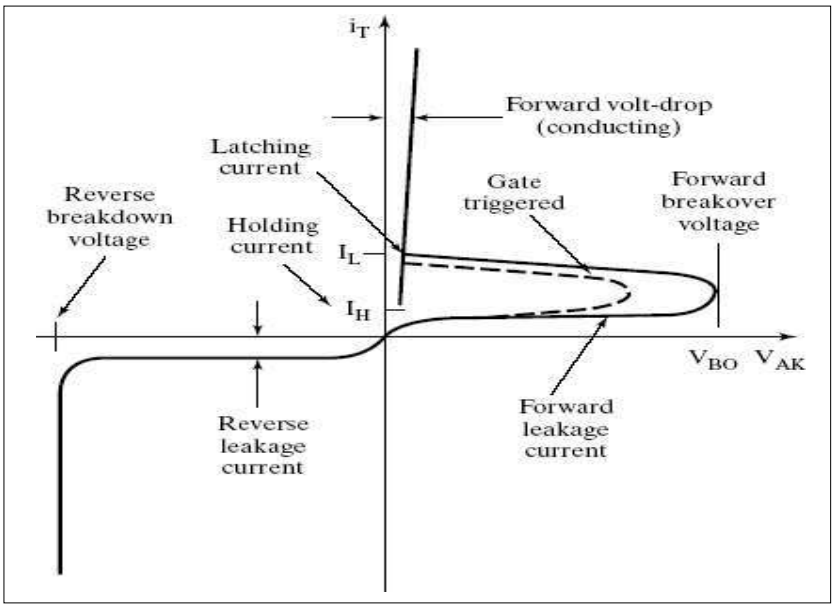


Fig: V-I Characteristics of SCR

A typical V-I characteristics of a thyristor is shown above. In the reverse direction the thyristor appears similar to a reverse biased diode which conducts very little current until avalanche breakdown occurs. In the forward direction the thyristor has two stable states or modes of operation that are connected together by an unstable mode that appears as a negative resistance on the V-I characteristics. The low current high voltage region is the forward blocking state or the off state and the low voltage high current mode is the on state. For the forward blocking state the quantity of interest is the forward blocking voltage V_{BO} which is defined for zero gate current. If a positive gate current is applied to a thyristor then the transition or break over to the on state will occur at smaller values of anode to cathode voltage as shown. Although not indicated the gate current does not have to be a dc current but instead can be a pulse of current having some minimum time duration. This ability to switch the thyristor by means of a current pulse is the reason for wide spread applications of the device.

However once the thyristor is in the on state the gate cannot be used to turn the device off. The only way to turn off the thyristor is for the external circuit to force the current through the device to be less than the holding current for a minimum specified time period.

HOLDING CURRENT I_H

After an SCR has been switched to the on state a certain minimum value of anode current is required to maintain the thyristor in this low impedance state. If the anode current is reduced below the critical holding current value, the thyristor cannot maintain the current through it and reverts to its off state usually I_μ is associated with turn off the device.

LATCHING CURRENT I_L

After the SCR has switched on, there is a minimum current required to sustain conduction. This current is called the latching current. I_L associated with turn on and is usually greater than holding current.

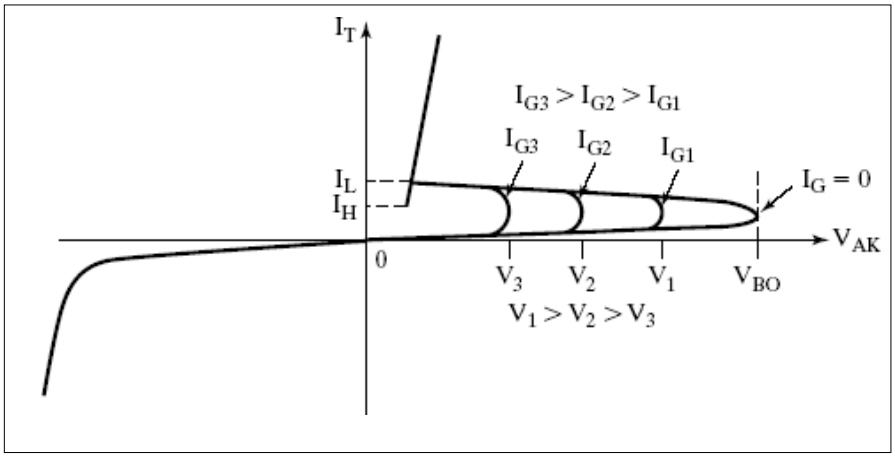


Fig.: Effects on gate current on forward blocking voltage

9. Sketch the four layer construction of an SCR and the two transistor equivalent circuit explains the device operation. (Non / Dec 2016)(May 2017)

A thyristor is the most important type of power semiconductor devices. They are extensively used in power electronic circuits. They are operated as bi-stable switches from non-conducting to conducting state.

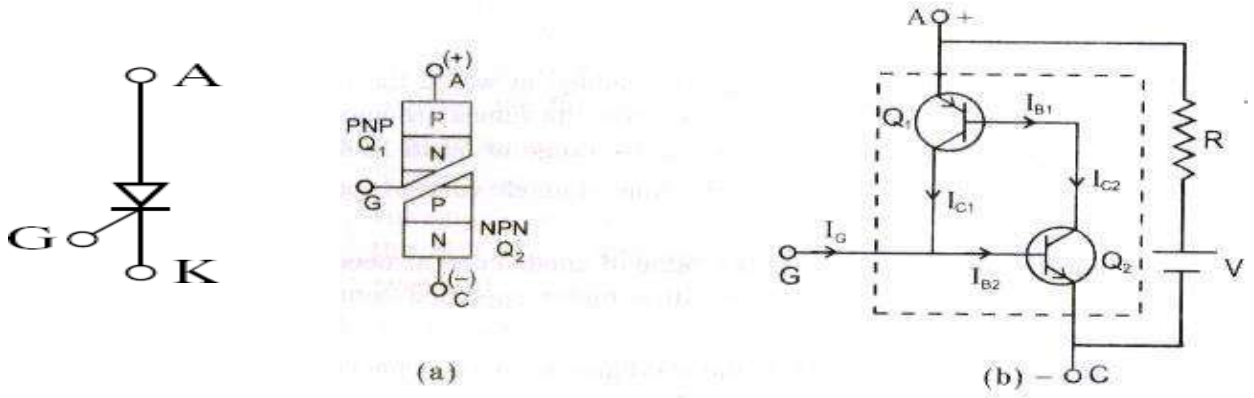
A thyristor is a four layer, semiconductor of p-n-p-n structure with three p-n junctions. It has three terminals, the anode, cathode and the gate.

The word thyristor is coined from thyratron and transistor. It was invented in the year 1957 at Bell Labs. The Different types of Thyristors are

- Silicon Controlled Rectifier (SCR).
- TRIAC
- DIAC
- Gate Turn Off Thyristor (GTO)

SILICON CONTROLLED RECTIFIER (SCR)

The SCR is a four layer three terminal device with junctions J_1, J_2, J_3 as shown. The construction of SCR shows that the gate terminal is kept nearer the cathode. The approximate thickness of each layer and doping densities are as indicated in the figure. In terms of their lateral dimensions Thyristors are the largest semiconductor devices made. A complete silicon wafer as large as ten centimeter in diameter may be used to make a single high power thyristor.



Two transistor model of SCR

OPERATION

When the anode is made positive with respect the cathode junctions J_1& J_3 are forward biased and junction J_2 is reverse biased. With anode to cathode voltage V_{AK} being small, only leakage current flows through the device. The SCR is then said to be in the forward blocking state. If V_{AK} is further increased to a large value, the reverse biased junction J_2 will breakdown due to avalanche effect resulting in a large current through the device. The voltage at which this phenomenon occurs is called the forward breakdown voltageV_{BO}. Since the other junctions J_1& J_3 are already forward biased, there will be free movement of carriers across all three junctions resulting in a large forward anode current. Once the SCR is switched on, the voltage drop across it is very small, typically 1 to 1.5V. The anode current is limited only by the external impedance present in the circuit.

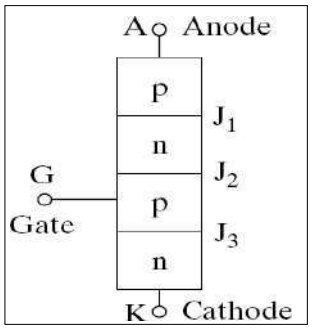


Fig.: Simplified model of a thyristor

Although an SCR can be turned on by increasing the forward voltage beyond V_{BO}, in practice, the forward voltage is maintained well below V_{BO} and the SCR is turned on by applying a positive voltage between gate and cathode. With the application of positive gate voltage, the leakage current through the junction J_2 is increased. This is because the resulting gate current consists mainly of electron flow from cathode to gate. Since the bottom end layer is heavily doped as compared to the p-layer, due to the applied voltage, some of these electrons reach junction J_2 and add to the minority carrier concentration in the p-layer. This raises the reverse leakage current and results in breakdown of junction J_2 even though the applied forward voltage is less than the breakdown voltageV_{BO}. With increase in gate current breakdown occurs earlier.

DIAC

10. Explain in detail about DIAC and its characteristics?

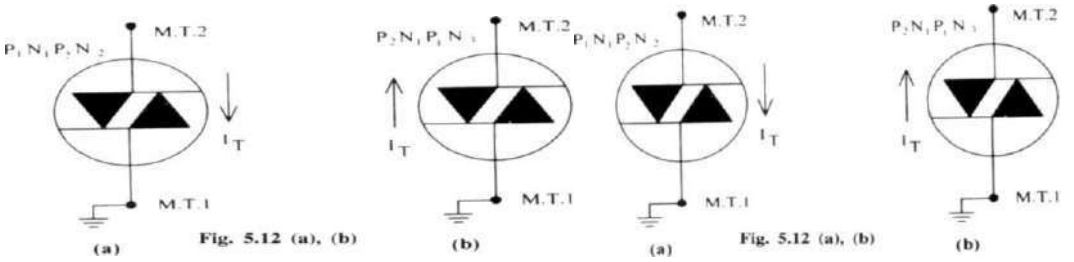


Fig. 5.12 (a), (b)

Fig. 5.12 (a), (b)

- The DIAC can be turned ON only when the applied voltage across it is main terminal reaches the break - over voltage.
- The M.T.2 is positive with respect to M.T.1, the DIAC passes current through the DIAC $P_1N_1P_2N_2$from M.T.2 to
- M.T.1 as shown in Fig. 5.12 (a). The DIAC turn 'ON' the applied voltage makes M.T.2 negative with respect to the M.T.1, the DIAC current through the diode
- When the current drops below the holding value. It is used as a triggering device.

Characteristics of a DIAC

The DIAC is operated with M.T.2 positive with respect to M.T.1, the V I characteristics obtained is as shown in Fig. 5.13 by the curve marked *OAB.* Similarly the DIAC is operated with its M.T.2 negative with respect to M.T.I, the V-l characteristics obtained as shown in Fig. 5.13 by the curve marked *OCD.*

Applications

The DIAC is used as a triggering device; it is not a control device. It is used in,

- Temperature control
- Triggering of TRIAC
- Light diming circuits
- Motor speed control

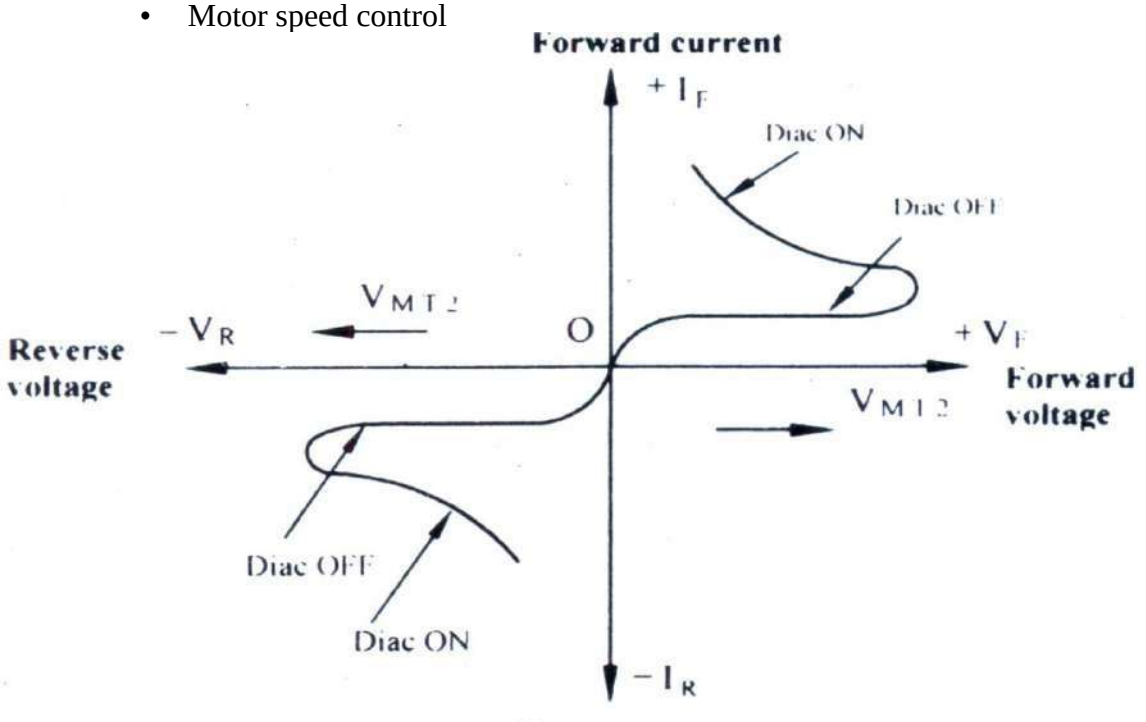


Fig. 5.13

TRIAC

11. EXPLAIN THE CONSTRUCTION, OPERATION & STATIC CHARACTERISTICS OF TRIAC

A triac is a three terminal bi-directional switching thyristor device. It can conduct in both directions when it is triggered into the conduction state. The triac is equivalent to two SCRs connected in anti-parallel with a common gate. Figure below shows the triac structure. It consists of three terminals viz., MT_2, MT_1 and gate G.

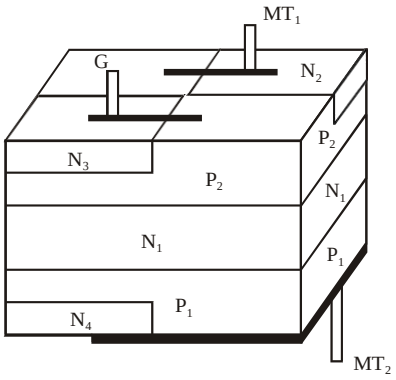


Fig. TRIAC Structure

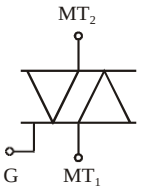


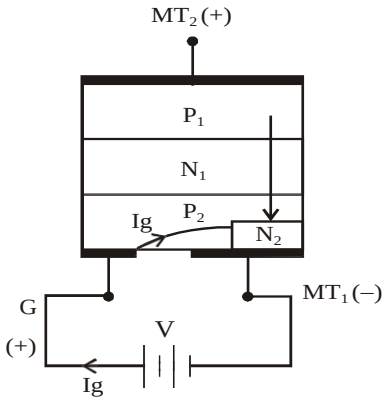
Fig. TRIAC Symbol

The gate terminal G is near the MT_1 terminal. Figure above shows the triac symbol. MT_1 is the reference terminal to obtain the characteristics of the triac. A triac can be operated in four different modes depending upon the polarity of the voltage on the terminal MT_2 with respect to MT_1 and based on the gate current polarity.

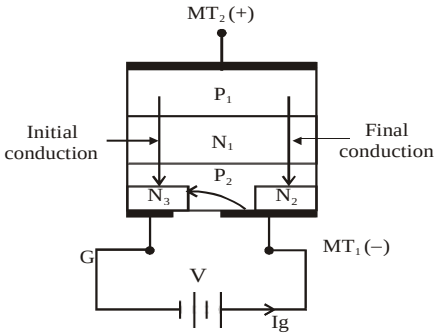
The characteristics of a triac are similar to that of an SCR, both in blocking and conducting states. A SCR can conduct in only one direction whereas triac can conduct in both directions.

MODE 1: MT_2 *positive, Positive gate current* (I^+ *mode of operation)*

When MT_2 and gate current are positive with respect to MT_1, the gate current flows through P_2-N_2 junction as shown in figure below. The junction P_1-N_1 and P_2-N_2 are forward biased but junction N_1-P_2 is reverse biased. When sufficient number of charge carriers is injected in P_2 layer by the gate current the junction N_1-P_2 breakdown and triac starts conducting through $P_1N_1P_2N_2$ layers. Once triac starts conducting the current increases and it's V-I characteristics is similar to that of thyristor. Triac in this mode operates in the first-quadrant.



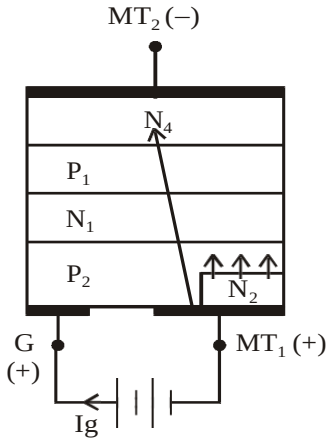
MODE 2: ***MT_2 positive, Negative gate current*** *(I^- mode of operation)*



When MT_2 is positive and gate G is negative with respect to MT_1 the gate current flows through P_2-N_3 junction as shown in figure above. The junction P_1-N_1 and P_2-N_3 are forward biased but junction N_1-P_2 is reverse biased. Hence, the triac initially starts conducting through $P_1N_1P_2N_3$ layers. As a result the potential of layer between P_2-N_3 rises towards the potential of MT_2. Thus, a potential gradient exists across the layer P_2 with left hand region at a higher potential than the right hand region. This results in a current flow in P_2 layer from left to right, forward biasing the P_2N_2 junction. Now the right hand portion P_1-N_1 - P_2-N_2 starts conducting. The device operates in first quadrant. When compared to Mode 1, triac with MT_2 positive and negative gate current is less sensitive and therefore requires higher gate current for triggering.

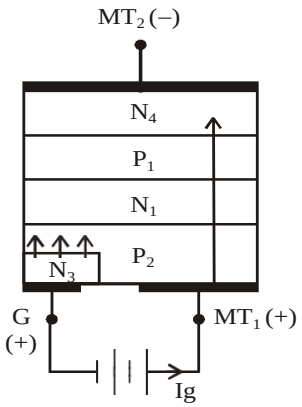
MODE 3: ***MT_2 negative, Positive gate current*** ***(III^+ mode of operation)***

When MT_2 is negative and gate is positive with respect to MT_1 junction P_2N_2 is forward biased and junction P_1-N_1 is reverse biased. N_2 layer injects electrons into P_2 layer as shown by arrows in figure below. This causes an increase in current flow through junction P_2-N_1. Resulting in breakdown of reverse biased junction N_1-P_1. Now the device conducts through layers $P_2N_1P_1N_4$ and the current starts increasing, which is limited by an external load.



The device operates in third quadrant in this mode. Triac in this mode is less sensitive and requires higher gate current for triggering.

MODE 4: ***MT_2 negative, Negative gate current*** *(III^- mode of operation)*



In this mode both MT_2 and gate G are negative with respect to MT_1, the gate current flows through P_2N_3 junction as shown in figure above. Layer N_3 injects electrons as shown by arrows into P_2 layer. These results in increase in current flow across P_1N_1 and the device will turn ON due to increased current in layer N_1. The current flows through layers $P_2N_1P_1N_4$. Triac is more sensitive in this mode compared to turn ON with positive gate current. (Mode 3).

Triac sensitivity is greatest in the first quadrant when turned ON with positive gate current and also in third quadrant when turned ON with negative gate current. When MT_2 is positive with respect to MT_1 it is recommended to turn on the triac by a positive gate current. When MT_2 is negative with respect to MT_1 it is recommended to turn on the triac by negative gate current. Therefore Mode 1 and Mode 4 are the preferred modes of operation of a triac (I^+ mode and III^- mode of operation are normally used).

TRIAC CHARACTERISTICS

Figure below shows the circuit to obtain the characteristics of a triac. To obtain the characteristics in the third quadrant the supply to gate and between MT_2 and MT_1 are reversed.

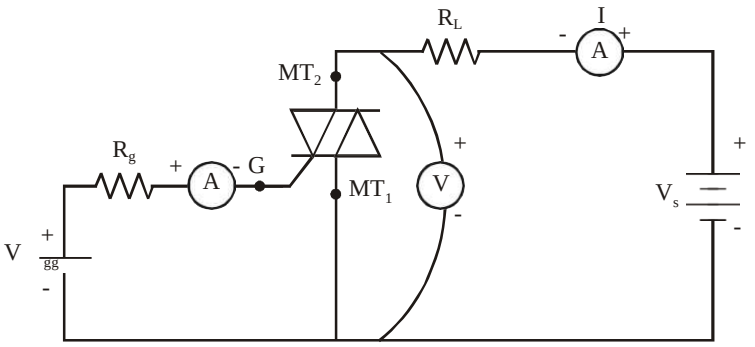


Figure below shows the V-I Characteristics of a triac. Triac is a bidirectional switching device. Hence its characteristics are identical in the first and third quadrant. When gate current is increased the break over voltage decreases.

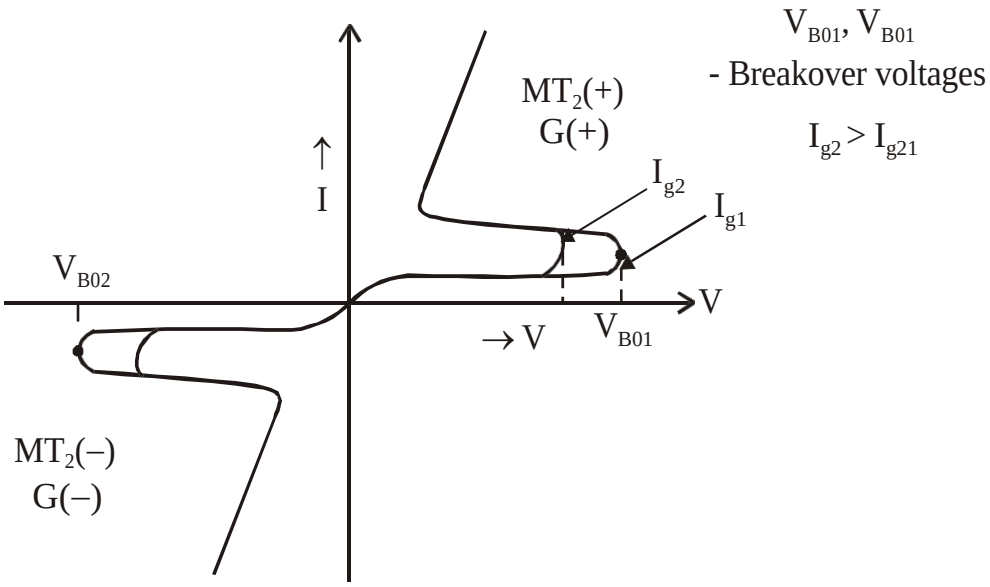


Fig.: Triac Characteristic

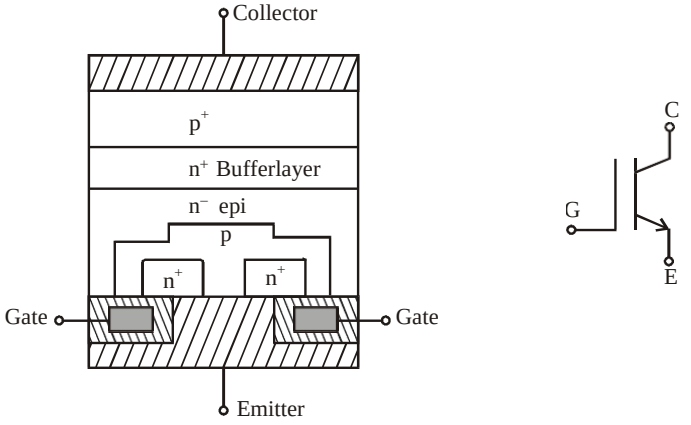
Triac is widely used to control the speed of single-phase induction motors. It is also used in domestic lamp dimmers and heat control circuits, and full wave AC voltage controllers.

IGBT-Structure, Operation & Characteristics

12. EXPLAIN THE CONSTRUCTION, OPERATION & STATIC CHARACTERISTICS OF INSULATED GATE BIPOLAR TRANSISTOR (IGBT). ***(NOV/DEC-2012) (May/June2016) (May 2017) (Nov/Dec 2018 R-13)***

IGBT is a voltage-controlled device. It has high input impedance like a MOSFET and low on-state conduction losses like a BJT.

Figure below shows the basic silicon cross-section of an IGBT. Its construction is same as power MOSFET except that n^+ layer at the drain in a power MOSFET is replaced by P^+ substrate called collector.



Structure **Symbol**

Fig.: Insulated Gate Bipolar Transistor

IGBT has three terminals gate (G), collector (C) and emitter (E). With collector and gate voltage positive with respect to emitter the device is in forward blocking mode. When gate to emitter voltage becomes greater than the threshold voltage of IGBT, a n-channel is formed in the P-region. Now device is in forward conducting state. In this state p^+ substrate injects holes into the epitaxial n^- layer. Increase in collector to emitter voltage will result in increase of injected hole concentration and finally a forward current is established.

CHARACTERISTIC OF IGBT

Figure below shows circuit diagram to obtain the characteristic of an IGBT. An output characteristic is a plot of collector current I_C versus collector to emitter voltage V_{CE} for given values of gate to emitter voltage V_{GE} .

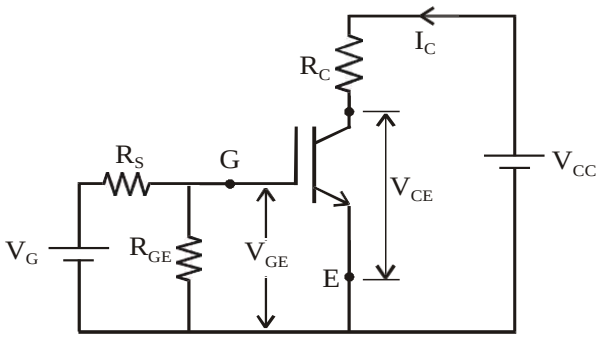


Fig.: Circuit Diagram to Obtain Characteristics

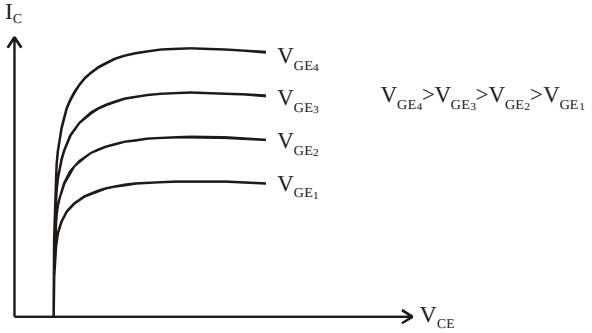


Fig. Output Characteristics

A plot of collector current I_C versus gate-emitter voltage V_{GE} for a given value of V_{CE} gives the transfer characteristic. Figure below shows the transfer characteristic.

Note

Controlling parameter is the gate-emitter voltage V_{GE} in IGBT. If V_{GE} is less than the threshold voltage V_T then IGBT is in OFF state. If V_{GE} is greater than the threshold voltage V_T then the IGBT is in ON state.

IGBTs are used in medium power applications such as ac and dc motor drives, power supplies and solid state relays.

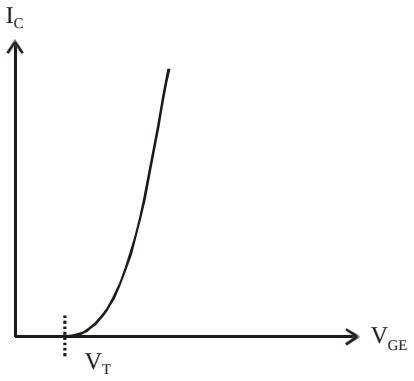
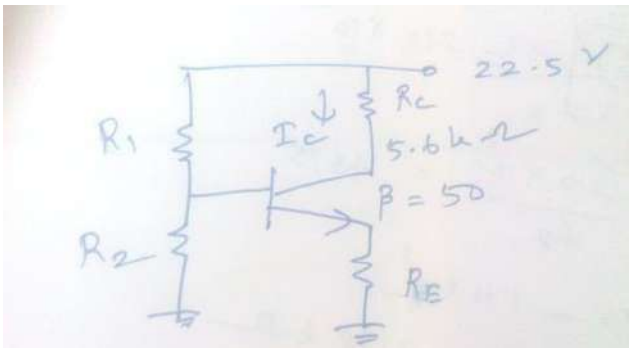


Fig. Transfer Characteristic

Solved Problems:

1. **Design a voltage divider bias circuit for transistor to establish the quiescent point V_{CE}=12v, Ic = 1.5mA, Stability factor S $\leq$ 3, $Q = 50, V_{BE} = 0.7V, V_{CC} = 22.5\ V$ and $Rc = 5.6\ K\Omega$.**

(May 2017) (Nov/Dec 2017)



$\beta = 50, \quad V_{BE} = 0.7\ V, \qquad V_{CC} = 22.5\ V, \qquad R_C = 5.6\ k\Omega, \qquad V_{CE} = 12\ V, \qquad I_C = 1.5\ mA, \qquad S \leq 3$

$Emitter\ Resistance\ (R_E)$

$V_{CE} = V_{CC} - I_C(R_C + R_E)$

$12 = 22.5 - (1.5 \times 10^{-3})\ (5.6 \times 10^3 + R_E) = 14.1 - 1.5 \times 10^{-3} R_E$

$R_E = 1.4 \times 10^3 \Omega = 1.4k\ \Omega$

$Resistances\ R_1\ and\ R_2$

Stability factor (s)

$$3 = \frac{\beta + 1}{1 + \beta\ (\frac{R_E}{R_{th} + R_E})} = \frac{50 + 1}{1 + 50 \times \frac{1.4 \times 10^3}{R_{th} + 1.4 \times 10^3}} = \frac{51}{1 + \frac{70 \times 10^3}{R_{th} + 1.4 \times 10^3}}$$

$$3\ [\frac{(R_{th} + 1.4 \times 10^3) + 70 \times 10^3}{R_{th} + 1.4 \times 10^3}] = 51$$

$3[(R_{th} + 1.4 \times 10^3)] + (70 \times 10^3) = 51\ (R_{th} + 1.4 \times 10^3)$

$48[R_{th} + (1.4 \times 10^3)] = 210 \times 10^3$

$$R_{th} + 1.4 \times 10^3 = \frac{(210 \times 10^3)}{48} = 4375$$

$R_{th} = 4375 - 1.4 \times 10^3; R_{th} = 2975\ \Omega; R_{th} = 2.98\ k\Omega$

For good voltage divider the value of resistor

$R_2 = 0.1\beta . R_E = 0.1 \times 50 \times (1.4 \times 10^3) = 7 \times 10^3 \Omega = 7k\Omega$

Thevenin's Resistance (R_{th})

$$2.98 = R_1 \| R_2 = \frac{R_1 . R_2}{R_1 + R_2} = \frac{7R_1}{R_1 + 7}$$

$2.98(R_1 + 7) = 7R_1; \qquad 4.02R_1 = 20.86$

$$R_1 = \frac{20.86}{4.02} = 5.2\ k\Omega$$

2. **For an n channel silicon FET with a = 3*10^{-4} cm and N_D = 10^{15} electronics/cm^3 find (a) the pinch off voltage and (b) the channel half width for V_{GS} = ½ VP and I_D = 0. (May / Jun 2016)**

Solution:

The relative dielectric constant of silicon is given in table 5-1 as 12, and hence $\epsilon = 12\epsilon_0$. Using the value of e and ϵ_0 from appendixes A and B, we have from Eq expressed in mks units,

$$V_P = \frac{1.60 \times 10^{-19} \times 10^{21} \times (3 \times 10^{-6})^2}{2 \times 12 \times (36\pi \times 10^9)^{-1}} = 6.8V$$

b. Solution Eq for b, we obtain for V_{GS} = ½ V_P

$$b = a\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{1/2}\right] = (3 \times 1^{-4})\left[1 - \left(\frac{1}{2}\right)^{\frac{1}{2}}\right] = 0.87 \times 10^{-4}\,cm$$

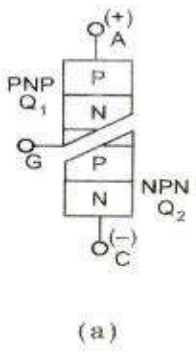
Hence the channel width has been reduced to about one third its value for V_{GS} = 0

3. **Determine the base current for the CB transistor circuit if I_C =80 mA and Q = 170. (Nov/Dev 2016)**

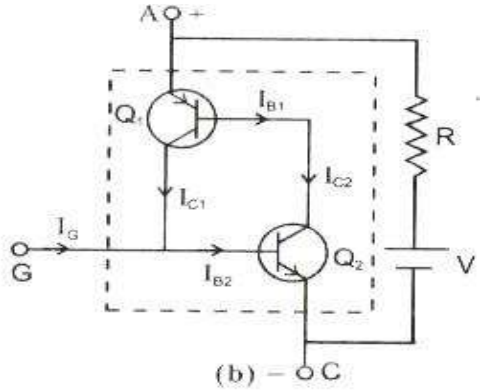
Given
I_C =80 mA
β = 170.

$$\beta = \frac{I_c}{I_B} = \frac{80 \times 10^{-3}}{I_B} = 170 \therefore I_B = \frac{I_c}{\beta} = \frac{80 \times 10^{-3}}{170} = 0.4706 \text{ mA}$$

4. **Draw the two-transistor equivalent circuit of SCR? (May 2017)**



(a)



5. **A transistor has a typical Q = 100. If the collector current is 40 mA. What is the value of emitter current?** ***(May 2017)***

Given: I_C =40 mA β = 100 $\beta = \frac{I_c}{I_B}$

$$\therefore I_B = \frac{I_c}{\beta} = \frac{40 \times 10^{-3}}{100} = 0.0004 \text{ A}$$

$I_E = I_B + I_C$ $I_E = 0.0004 + 40 \times 10^{-3} = 0.0404$ A

6. If the collector current is 2mA and the base current is 25μA, what is the emitter current?

Solution: $I_C = 2mA$, $I_B = 25\mu A$,

$I_E = I_B + I_C = 2mA + 25\mu A$ **$\therefore I_E = 2.025mA$**

7. Calculate I_C and I_E for a transistor that has $\alpha = 0.99$ and $I_B = 150\mu A$. Determine the value of Q_{dc} for the transistor? (Nov / Dec 2015)

Solution: $\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-099} = 99$

$\beta = \frac{I_C}{I_B}$; $I_C = \beta \times I_B = 99 \times 150\ \mu A = 14\ mA$

$\alpha = \frac{I_C}{I_E}$; $I_E = \frac{Ic}{\alpha} = \frac{14}{0.99} = 14.14mA$

8. **A germanium transistor is to be operated at zero signal I_C = 1mA. If the collector supply voltage V_{CC} = 12V, what is the value of R_B in the base resistor method? Assume β = 100. If another transistor of same batch with β = 50 is used, what will be new value of zero signal I_C for same R_B? Comment on the results.** ***(Nov/Dec 2018-R17)(13 Marks)***

Solution:

$V_{CC} = 12\ V, \quad \beta = 100$

$V_{BE} = 0.3\ V$ ∵ Germanium transistor

Zero signal $I_C = 1\ mA$

$\therefore$ Zero signal $I_B = \frac{I_C}{\beta} = \frac{1\ mA}{100} = 0.01\ mA$

Using the relation, $V_{CC} = I_B R_B + V_{BE}$ we have

$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12 - 0.3}{0.01\ mA} = 1170\ k\Omega$

ii) $\beta = 50$

Using the relation, $V_{CC} = I_B R_B + V_{BE}$ we have

$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.3}{1170\ k\Omega} = 0.01\ mA$

$\therefore$ Zero signal $I_C = \beta I_B = 50 \times 0.01\ mA = 0.5\ mA$

Comment: It is clear from the above example that with the change in transistor parameter β, the zero-signal collector current has changed from 1mA to 0.5 mA. Therefore, the base resistor method cannot provide stabilization.

9. **The intrinsic stand-off ratio for a UJT is 0.6. If the inter base resistance is 10KΩ, what are the value of R_{B1} and R_{B2}?** ***(Nov/Dec 2018-R17) (4 Marks)***

Sol. : $\eta = 0.6, \quad R_{BB} = 10\ k\Omega$

$\eta = \left.\frac{R_{B1}}{R_{BB}}\right|_{I_E = 0}$ i.e. $0.6 = \frac{R_{B1}}{10}$

$\therefore \quad R_{B1} = 6\ k\Omega$

$R_{BB} = R_{B1} + R_{B2}$ i.e $10 = 6 + R_{B2}$

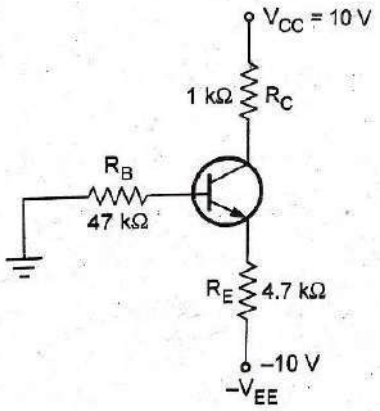
$\therefore \quad R_{B2} = 4\ k\Omega$

10. **When V_{GS} of a JFET changes from -3.1 V to -3 V, the drain current changed from 1 mA to 1.3 mA. Find the value of transconductance.** ***(Nov/Dec 2018-R17) (2 Marks)***

Solution:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{(1.3-1)\times10^{-3}}{(3.1-3)} = 3\ mA/V$$

11. **Find the Q point of the transistor shown below. Also draw the DC load line. Give β = 100 and V_{BE} = 0.7V.** ***(Nov/Dec 2018-R17) (15 Marks)***



Sol. :

$$I_B = \frac{V_{EE}-V_{BE}}{R_B+(1+\beta)R_E} = \frac{10-0.7}{47K+(1+100)4.7K} = \mathbf{17.83\ \mu A}$$

$$I_C = \beta I_B = 100\times17.83\mu A = \mathbf{1.783\ mA}$$

$$I_E = I_C + I_B = 1.783\ mA + 17.83\ \mu A = \mathbf{1.8\ mA}$$

$$V_C = V_{CC} - I_C R_C = 10-(1.783\times10^{-3}\times1\times10^{3})$$

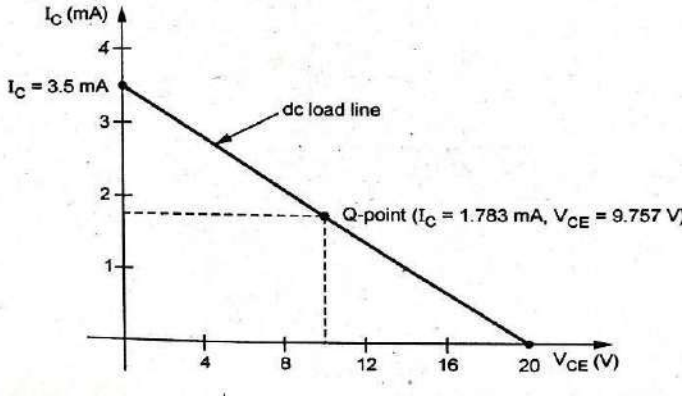
$$= \mathbf{8.217\ V}$$

$$V_E = -V_{EE} + I_E R_E = -10\ V + (1.8\times10^{-3}\times4.7\times10^{3})$$

$$= \mathbf{-1.54\ V}$$

$\therefore$ $V_{CE} = V_C - V_E = 8.217 - (-1.54) = \mathbf{9.757\ V}$

$\therefore$ The Q point of the circuit is $\mathbf{V_{CE}}$ = **9.757 V** and $\mathbf{I_C}$ = **1.783 mA**

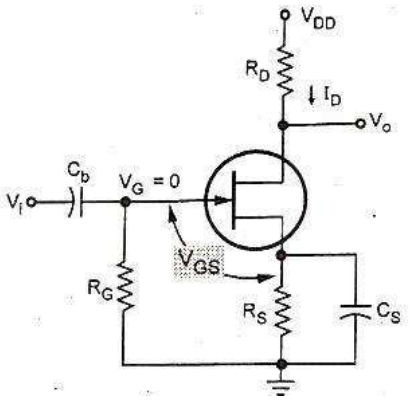


when $V_{CE} = 0$, $I_C = \frac{V_{CC}-(-V_{EE})}{R_C+R_E}$

$$= \frac{10+10}{1K+4.7K} = \mathbf{3.5\ mA}$$

when $I_C = 0$, $V_{CE} = V_{CC}-(-V_{EE}) = 10 + 10 = 20\ V$

12. **In a self-bias n-channel JFET, the operating point is to be set at I_D = 1.5mA and V_{DS} =10V. The parameters are I_{DSS} = 5mA and V_{GS} (off) = -2V. Find the values of R_S and R_D if V_{DD} = 20V.** ***(Nov/Dec 2018-R17) (9 Marks)***



Given : $I_D = 1.5$ mA, $I_{DSS} = 5$ mA,

$V_{GS(OFF)} = -2\text{ V} = V_p$, $V_{DD} = 20$ V and $V_{DS} = 10$ V

Step 1 : Calculate V_{GS}

We have $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_p}\right]^2$

$$\therefore \quad V_{GS} = V_p\left[1-\sqrt{\frac{I_D}{I_{DSS}}}\right] = -2\left[1-\sqrt{\frac{1.5}{5}}\right] = -0.9\text{ V}$$

Step 2 : Calculate R_s

$$V_{GS} = V_G - V_S = 0 - V_S = -0.9\text{ V}$$

$$\therefore \quad V_S = 0.9\text{ V}$$

$$\therefore \quad R_S = \frac{V_S}{I_D} = \frac{0.9\text{V}}{1.5\text{ mA}} = 600\ \Omega$$

EC8353-ELECTRONIC DEVICES AND CIRCUITS

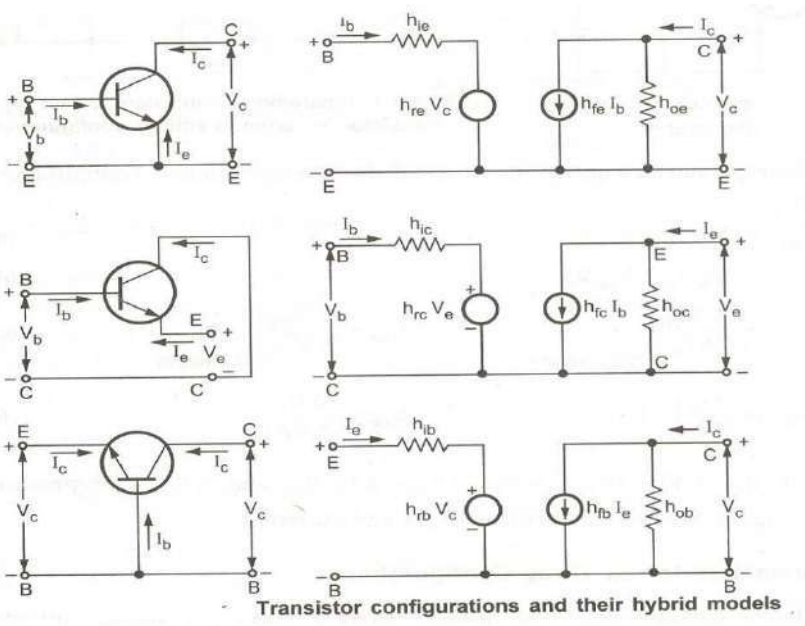
UNIT-III AMPLIFIERS

PART-A

BJT Small Signal Model

1. **Which is the BJT configuration is suitable for impedance matching application and why?**
   CC configuration is suitable for impedance matching application because of very high input impedance and low output impedance.

2. **Draw the hybrid small signal model of BJT device. (MAY/JUNE2016)**



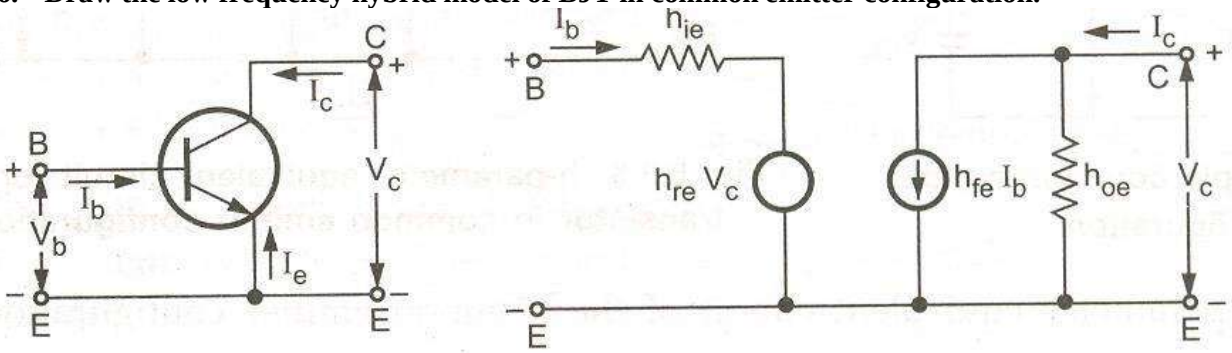
Transistor configurations and their hybrid models

3. **What are the tools used for small signal analysis of BJT?**
   - h – Parameter circuit model.
   - z – Parameter circuit model.
   - y – Parameter circuit model.
   - Trans-conductance parameter circuit model.
   - Physical model
   - T-model

4. **What are the steps used for small signal analysis of BJT?**
   - Draw the actual circuit diagram
   - Replace coupling capacitors and emitter bypass capacitor by short circuit.
   - Replace dc source by a short circuit. In other words, short V_{CC} and ground lines.

5. **State the phase relationship between input / output currents and phase relationship between the input / output voltages of various transistors configurations. (Nov/Dec 2018)**
   For all the transistor configurations, input and output currents are in phase.
   The input and output voltages of both CB and CC configuration are in phase. But in common-emitter amplifier the input and output voltages are 180^0 out of phase.

6. Draw the low frequency hybrid model of BJT in common emitter configuration.

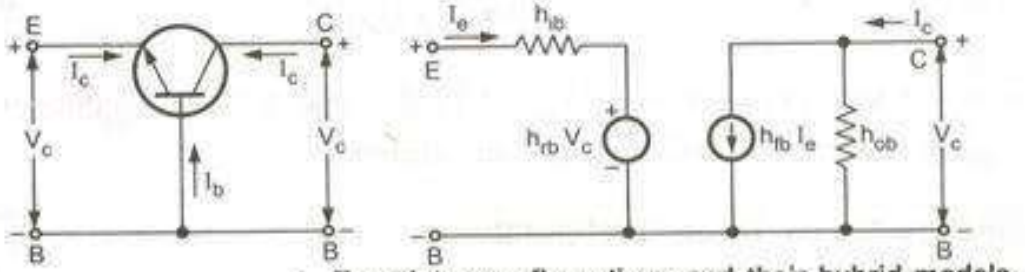


$V_b = h_{ie}I_b + h_{re}V_c$

$I_c = h_{fe}I_b + h_{oe}V_c$

<u>CE, CB, CC Amplifiers</u>-<u>Gain and frequency response</u>

7. Draw the hybrid small signal model of CB configuration? (Apr/May 2018)



Transistor configurations and their hybrid models

8. Why emitter is always forward biased and collector is always reverse biased with respect to base?

To supply majority charge carrier to base and to remove the charge carriers away from the collector-base junction.

9. Why CE configuration is most popular in amplifier circuits?

Because it's current, voltage and power gain are quite high and the ratio of output impedance and input impedance are quite moderate.

10. Give the voltage gain for CE configuration including source resistance.

$A_{vs} = A_i \times R_L / R_S + R_i$

$= (- h_{fe} / 1 + h_{oe} R_L) \times R_L / (R_S + R_i)$

11. Define the h_{ie} and h_{fe} for a common emitter transistor configuration.

From the h – parameter equivalent circuit of the common emitter configuration.

$H_{ie} = \Delta V_{BE} / \Delta I_B \mid V_{CE}$ constant

$H_{fe} = \Delta I_C / \Delta I_B \mid V_{CE}$ constant

12. Give the current gain expression for a common emitter transistor configuration.

Current gain for common emitter configuration:

$A_i = - I_C / I_b = - h_{fe} / 1 + h_{oe} R_L$

MOSFET small signal model

13. What is trans-conductance? Give its expression for MOSFET. (Nov/Dec 2017)

The trans-conductance is a ratio of output current to input voltage and hence it represents the gain of the MOSFET.

Tran conductance expression for MOSFET

$g_m = 2 \sqrt{(KI_{DQ})}$

$I_{DQ} = K (V_{GSQ} – V_T)^2$

14. State the values of C_{gd} and C_{gs} in various operating regions of MOSFET.

Values of gate capacitances in Triode Region:

$C_{gs} = C_{gd} = (WL\ C_{ox})$ ½

Values of gate capacitances in Saturation Region:

$C_{gs} = (WL\ C_{ox})$ 2/3

$C_{gd} = 0$

Values of gate capacitances in Cut - off Region:

$C_{gs} = C_{gd} = 0$

$C_{gd} = WL\ C_{ox}$

C_{ox} – Gate Capacitance.

15. List various gate capacitances in MOSFET.

There are three gate capacitances in MOSFET:

C_{gs} – gate source capacitance,

C_{gd} – gate drain Capacitance, and

C_{gb} - gate body Capacitance.

CS and Source follower

16. Explain the effect of source resistor on CS MOSFET amplifier.

The source resistor is introduced to stabilize the Q – point against variations in the MOSFET parameters. In BJT circuits, a source resistor reduces the small gain.

17. What is source follower? (Apr/May 2018)

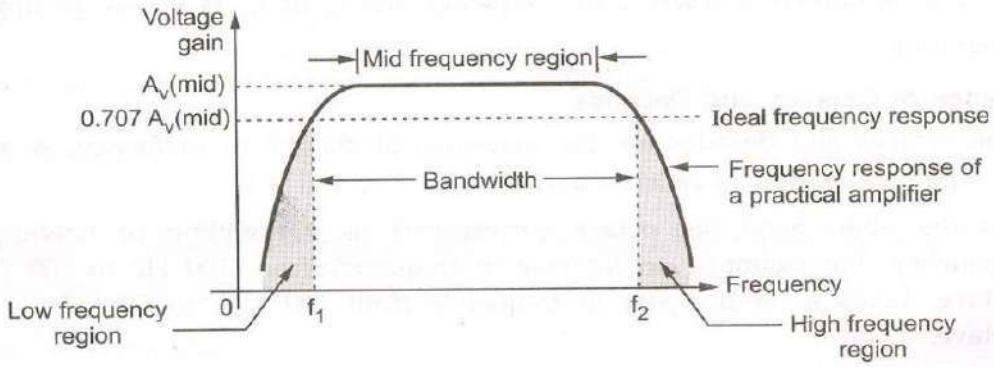
A common-drain amplifier, also known as a source follower, is one of three basic single-stage field effect transistor (FET) amplifier topologies, typically used as a voltage buffer.

Gain and frequency response

18. What is the significance of octaves and decades in frequency response?

- Octaves and Decades are the measure of change in frequency.
- Ten times change in frequency is called a Decade. On the other hand, an Octave corresponds to a doubling of the frequency.
- For example, an increase in frequency from 100Hz to 200Hz is an octave. Likewise, a decrease in frequency from 100Hz to 50Hz is also an octave.
- If the frequency is reduced to one hundredth of fc (from fc to 0.01fc), the drop in the voltage gain is – 40 dB. In each decade the voltage gain drops by – 20 db.

19. Draw *general frequency response* curve (or) *half-power frequencies* of an amplifier.



Frequency response of an RC coupled amplifier

- In the above diagram the frequency f_2 lies in high frequency region, while the frequency f_1 lies in low frequency region.
- These two frequencies are also referred to as half power half – power frequencies since gain or output voltage drops to 70.7% of maximum value and this represents a power level of one half the power at the reference frequency in mid – frequency region.

Additional Questions

20. What is the relation between α and β of the transistor?

$$\alpha = \frac{\beta}{\beta+1}$$

21. Why must the base be narrow for the transistor action?

β is the ratio of IC to IB. IB becomes less if the base width is narrow. Higher value of β can be obtained with lower value of base current.

22. What are emitter efficiency and base transport factor of a transistor?

The ratio of current of injected carriers at emitter junction to the total emitter current is called the emitter injection efficiency.
Transport Factor, β= IC / IB

23. What is the relation between the current of a transistor?

$I_E = I_B + I_C$

24. How many h-parameters are there for a transistor?

- h_r–reverse voltage gain
- h_o–output admittance.
- h_i,-input impedance
- h_f-forward current gain

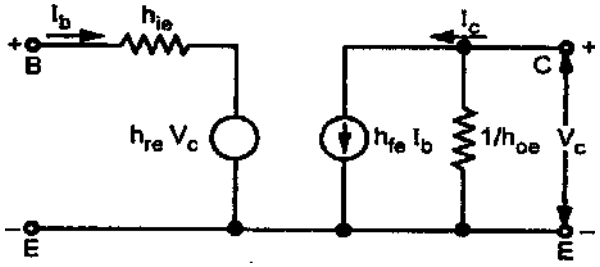
25. Why h-parameters are called hybrid parameters?

Because they have different units are mixed with other parameters.

26. What are the advantages of the h-parameters? (Apr/May 2011)

(1) Real numbers up to radio frequencies
(2) Easy to measure
(3) Determined from transistor static characteristics curve
(4) Convenient to use in the circuit analysis and design
(5) Easily convertible from one configuration to other

27. Draw the hybrid model for a transistor. (Nov/Dec 2012)



28. What are h-parameters? Define the four h-parameters.

One of a set of four transistor equivalent circuit parameters that conveniently specify transistor performance for small voltage and current in a particular circuit also known as hybrid parameter.

Input resistance with output short – circuited, in Ω.

$h_{11} = V_i / I_i \,|\, V_o = 0$

Fraction of output voltage at input with input open circuited. This parameter is ratio of similar quantities, hence unitless.

$h_{12} = V_i / V_o \,|\, I_i = 0$

Forward current transfer ratio or current gain with output short circuited.

$h_{21} = I_o / I_i \,|\, V_o = 0$

This parameter is a ratio of similar quantities, hence unitless. Output admittance with input open – circuited, in mhos.

$h_{22} = I_o / V_o \,|\, I_i = 0$

29. State Miller's theorem. (Nov/Dec 2016)

Miller's theorem states that, if Z is the impedance connected between two nodes node 1 and node 2, it can be replaced by two separate impedance Z_1 and Z_2; where Z_1 is connected between node - 1 and ground, and node Z_2 is connected between node -2 and ground.

The Vi and Vo are the voltages at the node – 1 and node – 2 respectively, The values of Z_1 an d Z_2 can be derived from the ratio of Vo and Vi, denoted as K. Thus it is not necessary to know the values of Vi and Vo to calculate the values of Z_1 and Z_2

The values of impedance Z_1 and Z_2

$Z_1 = Z / (1 - K)$; $Z_2 = Z \times K / (K - 1)$

30. What do you mean by faithful amplification?

During the process of raising the strength of the input signal if the shape of the output voltage is exactly same as that of the input signal, the amplification is called faithful amplification.

31. Define the various h-parameters for a common emitter transistor.

From the h – parameter equivalent circuit of the common emitter configuration.

$V_{be} = h_{ie} I_b + h_{re} V_{ce}$

$I_c = h_{fe} I_b + h_{oe} V_{ce}$

Where, $h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right| V_{CE}$ constant

$h_{re} = \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right| I_B$ constant

$h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right| V_{CE}$ constant

$h_{oe} = \left.\frac{\Delta I_C}{\Delta V_C}\right| I_B$ constant

32. State the advantages of using h-parameters for analyzing transistor amplifiers.

i.) Real numbers at audio frequencies
ii.) Easy to measure
iii.) Can be obtained from the transistor static characteristics curves,
iv.) Convenient to use in circuit analysis and design,
v.) Most of the transistor manufacturers specify the h – parameters.

33. What is bandwidth of an amplifier.

The bandwidth of an amplifier is defined as the difference between the lower cut - off frequency and upper cut off frequency.

$BW = f_2 – f_1$

34. State the effect of coupling and bypass capacitors on the frequency response of amplifier.

Reactance of a capacitor is given by $X_c = 1 / 2\pi fc$. At medium and high frequencies, the factor f makes X_c very small, so that all coupling capacitors behave as short circuits. At low frequencies, X_c increases. This increase in X_c drops the signal voltage across the capacitor and reduces the circuit gain. As signal frequencies decrease, the capacitor reactance's increase and circuit gain continues to fall, reducing the output voltage.

35. State the effect of internal transistor capacitance on the frequency response of amplifier.

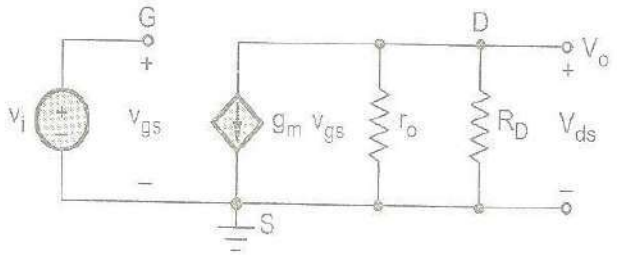
At high frequencies, the reactance of the junction capacitance are low. As frequency increases, the reactance of junction capacitances fall. When these reactance become small enough, they provide shunting effect as they are in parallel with junctions. This reduces the circuit gain and hence the output voltage.

36. Give the expression for r_o of NMOS transistor.

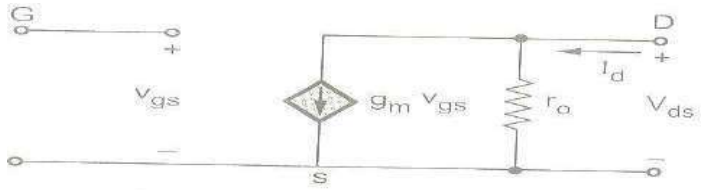
$r_o = (\partial i_D / \partial v_{DS})^{-1} \big|_{v_{GS} = V_{GSQ} = \text{const.}}$

$r_o = [\lambda K [(v_{GSQ} – V_T)^2]^{-1} \approx [\lambda I_{DQ}]^{-1}$

37. Draw the small signal equivalent circuit of CS JFET (Nov/Dec2015).



Small signal equivalent circuit of common-source circuit with NMOS transistor model

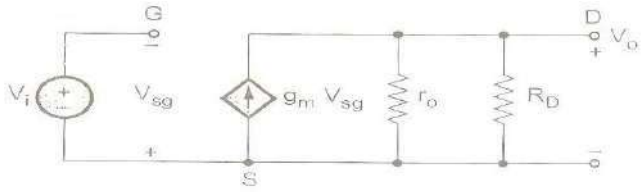


Expanded small signal equivalent circuit, including output resistance, for NMOS transistor

38. What is Gate capacitance in MOSFET.

Gate capacitance is a parallel – plate capacitance formed by a gate electrode with the channel, with the oxide layer acts as a capacitor dielectric. It is denoted as C_{ox}.

39. Draw the small signal equivalent circuit of PMOS transistor.



Small signal equivalent circuit of common source amplifier with PMOS transistor model

40. Explain the loading effect.

The small signal overall voltage gain is,

$$G_v = v_o / v_s = - g_m(r_o \parallel R_D)(R_i / R_i + R_{si}) = A_v (R_i / R_i + R_{si})$$

Since Rsi is not zero, the amplifier input signal v_i is less than the signal voltage, This is known as **loading effect**. It reduces the voltage gain of the amplifier.

41. What do you mean by drain diffusion and source diffusion capacitance?

Drain and Source capacitances are due to the reverse – biased pn junctions formed by the n^+ source region and the p – type substrate, and the n^+ drain region and the p- type substrate. These are denoted as **source diffusion capacitance** and **drain diffusion capacitance** respectively.

42. Give the expression of unity gain frequency (f_T)for MOSFET amplifier?

Unity gain frequency for MOSFET:

$f_T = g_m / 2\pi (C_{gs} + C_{gd})$

From the above expression we can say that f_T is proportional to gm and inversely proportional to the internal capacitances.

43. Compare different amplifiers.

COMMON SOURCE AMPLIFIER	Good voltage amplifier and better trans conductance amplifier	• Large Voltage gain • High input resistance • High output resistance
COMMON DRAIN AMPLIFIER	Good voltage buffer	• Voltage gain ≈ 1 • High input resistance • Low input resistance
COMMON GATE AMPLIFIERS	Good current buffer	• Current Gain ≈ 1 • Low input resistance • High output resistance

44. What is the need of coupling capacitors in amplifier design? (Aril/May 2019) (Nov / Dec 2015)

Coupling capacitors isolates the DC condition of one stage from the following stages.

It is used to couple output of one stage to another stage.

45. Differentiate between power transistor and signal transistor. (May / Jun 2016)

S.No	Power transistor	Small signal transistor
1	n^{-1} drift layer is present	110 n^{-1} drift layer
2	Secondary breakdown occurs	No secondary breakdown
3	Used in power circuits	Used in amplifying circuits

PART-B

BJT Small signal Model-Analysis of CE, CB, CC amplifiers

1. **Draw the small signal model of BJT device (OR) Draw the parameters equivalent circuit or small signal model of a transistor in CE, CB, CC configuration? (Apr/May 2018). (OR)**

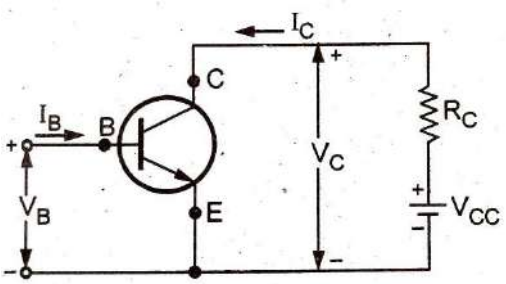
Draw the hybrid model of BJT in CE, CC and CB configuration.

h – Parameter model for CE, CC and CB configuration

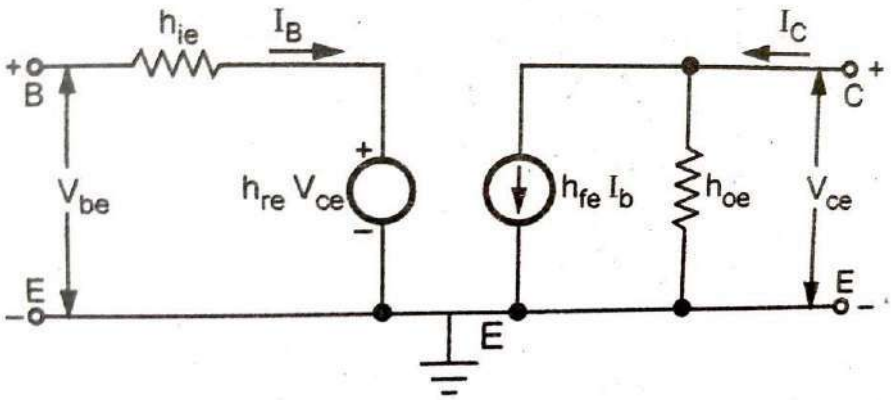
The variable I_b, I_c, V_b, and V_c represent total instantaneous current and voltage.

I_b – Input current; I_c – Output current; V_{be} – Input voltage; V_{ce} – Output voltage

CE Configuration



h– Parameter equivalent circuit



$V_{be} = h_{ie}I_b + h_{re}V_{ce}$ --- (1)

$I_c = h_{fe}I_b + h_{oe}V_{ce}$ --- (2)

Where, $h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \Big|_{V_{CE}} -$ constant------(3)

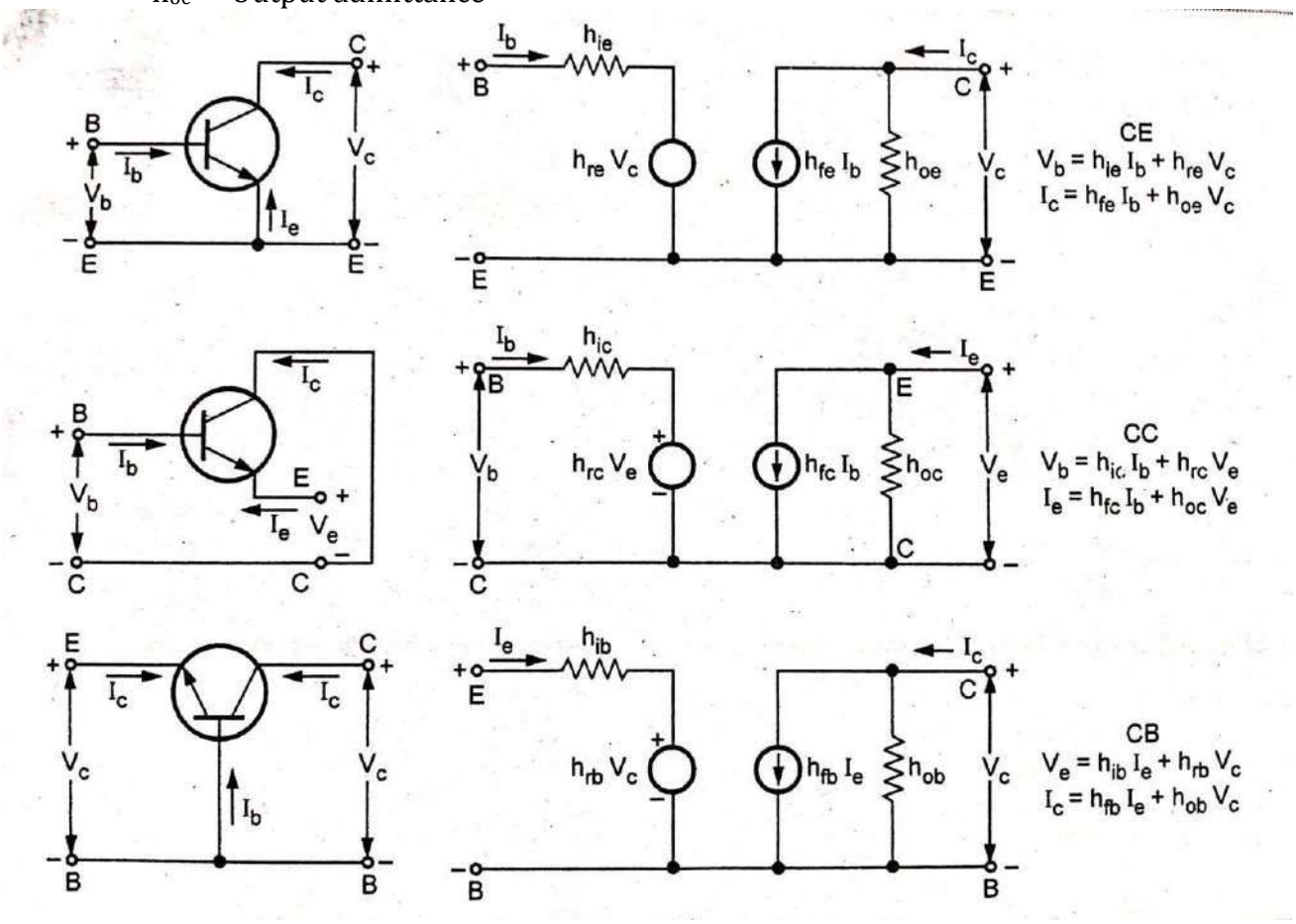
$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \Big|_{I_B} -$ constant---- (4)

$h_{fe} = \frac{\Delta I_c}{\Delta I_B} \Big|_{V_{CE}} -$ constant ----(5)

$h_{oe} = \frac{\Delta I_c}{\Delta V_C} \Big|_{I_B} -$ constant -----(6)

h_{ie} – Input resistance;

h_{re} – Reverse voltage gain;
h_{fe} – Forward transfer gain;
h_{oe} – Output admittance



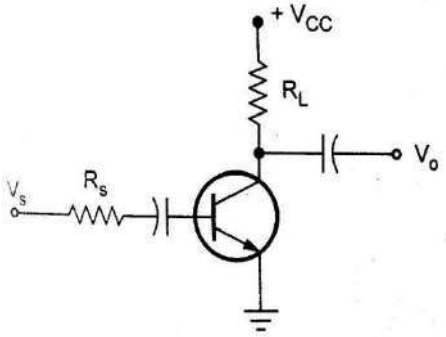
Relationship between h-parameters of different transistor configuration:

CE to CB conversion formulae	CE to CC conversion formulae
$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$	$h_{ic} = h_{ie}$ *
$h_{rb} = \frac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}$	$h_{rc} = 1 - h_{re} \approx 1$ *
$h_{fb} = -\frac{h_{fe}}{1 + h_{fe}}$	$h_{fc} = -(1 + h_{fe})$ *
$h_{ob} = \frac{h_{oe}}{1 + h_{fe}}$	$h_{oc} = h_{oe}$ *

2. (A) Derive the expressions for current gain (A_I), voltage gain(A_V), input resistance (R_i) and output resistance (R_O) for CE amplifier using h – parameter model. ***(April/May 2015 & 18) (Nov / Dec' 2014& 16)***

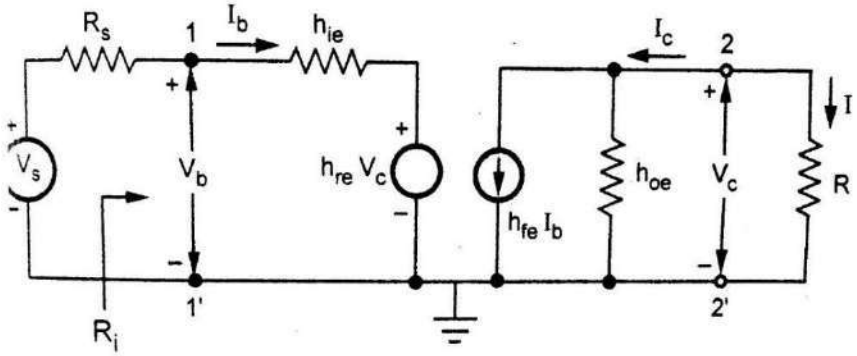
Illustrate the steps involved in analyzing a BJT amplifier circuit using small signal model. (April/May 2019) (5 Marks)

Circuit diagram



(a) CE amplifier

h – Parameter model



(b) CE amplifier in its h-parameter model

Current gain $[A_I]$ $A_I = \frac{I_L}{I_b}$

$I_C = h_{fe}I_b + h_{oe}V_c;\ I_C = h_{fe}I_b + h_{oe}(-I_cR_L);$ $\{since, V_c = -I_cR_L\}$

$I_C + h_{oe}R_LI_c = h_{fe}I_b;\ I_C(1 + h_{oe}R_L) = h_{fe}I_b$

$$\frac{I_C}{I_b} = \frac{h_{fe}}{1 + h_{oe}R_L}$$

$$A_I = \frac{-I_C}{I_b} = -\frac{h_{fe}}{1 + h_{oe}R_L}$$

Input Resistance $(R_i) R_i = \frac{V_b}{I_b}$

$V_b = h_{ie}I_b + h_{re}V_C$

$V_C = -I_CR_L;\ V_C = A_II_bR_L$

Now $R_i = \frac{V_b}{I_b} = \frac{h_{ie}I_b + (A_I I_b R_L)}{I_b} = h_{ie} + h_{re} A_I R_L$

Substituting, $A_I = \frac{-h_{fe}}{1+h_{oe}R_L}$ to the above equation

$$R_i = h_{ie} + h_{re}\left(\frac{-h_{fe}}{1 + h_{oe}R_L}\right) \times R_L$$

$$R_i = h_{ie} - \frac{h_{re}h_{fe}R_L}{1 + h_{oe}R_L}$$

Voltage gain $(\mathbf{A_V})$ $A_V = \frac{V_c}{V_b} = \frac{A_I I_b R_L}{V_b}$ $\because \frac{I_b}{V_b} = \frac{1}{R_i}$

$$A_V = \frac{A_I R_L}{R_i}$$

Output admittance $(\mathbf{Y_o})$ $Y_o = \frac{I_c}{V_c}$ with $V_s = 0$

$I_c = h_{fe}I_b + h_{oe}V_c$ (divide this equation by V_C)

$$\frac{I_c}{V_c} = \frac{h_{fe}I_b + h_{oe}V_c}{V_c}$$

$$Y_o = \frac{h_{fe}I_b}{V_c} + h_{oe}$$

From h parameter circuit with $\mathbf{V_s = 0}$

$R_s I_b + h_{ie}I_b + h_{re}V_c = 0$ *(Apply KVL)*

$(R_s + h_{ie})I_b = -h_{re}V_c$

$$\frac{I_b}{V_c} = \frac{-h_{re}}{R_s + h_{ie}}$$

Substitute, $\frac{I_b}{V_c} = \frac{-h_{re}}{R_s+h_{ie}}$ *in* $Y_o = \frac{h_{Fe}I_b}{V_c} + h_{oe}$

$$Y_o = \frac{I_c}{V_c} = h_{fe}\left(\frac{-h_{re}}{R_s + h_{ie}}\right) + h_{oe}$$

$$Y_o = h_{oe} - \frac{h_{Fe}h_{re}}{R_s+h_{ie}} \quad \text{and} \quad R_o = \frac{1}{Y_o}$$

(B) Draw the circuit of CE amplifier with DC sources eliminated and deduce the small signal model for amplifier operation. (April/May 2019) (8 Marks) (OR) **Approximate analysis of CE amplifier using simplified Hybrid Model.**

Analysis of CE Amplifier using simplified Hybrid Model:

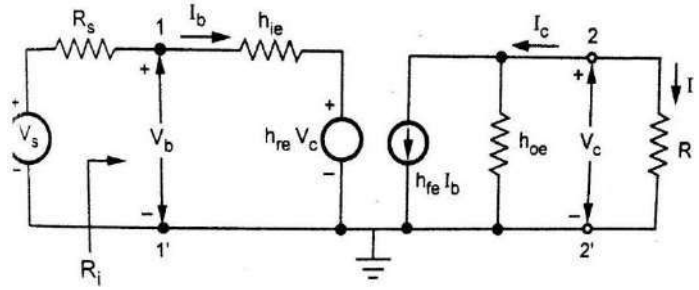


Fig. Simplified CE model

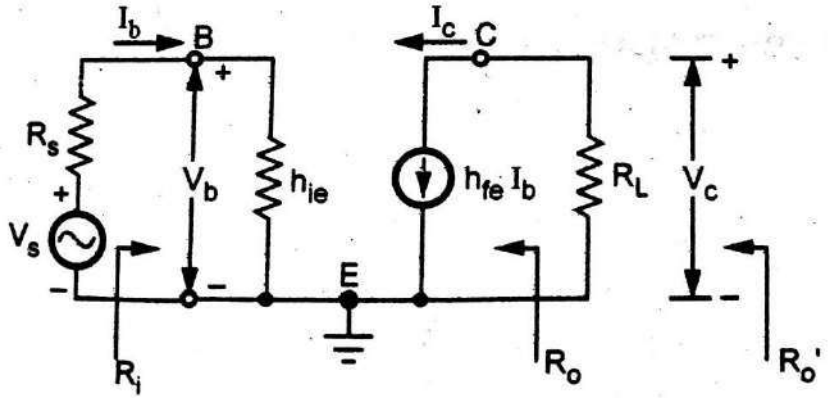


Fig. Approximate CE model

Current gain $[A_I]\ A_I = \frac{I_L}{I_b}$

$$A_I = \frac{-I_C}{I_b} = -h_{fe}$$

Input Resistance $(R_i) R_i = \frac{V_b}{I_b}$

$$R_i = h_{ie}$$

Voltage gain $(\mathbf{A_V})\ A_V = \frac{V_c}{V_b} = \frac{A_I I_b R_L}{V_b} \because \frac{I_b}{V_b} = \frac{1}{R_i}$

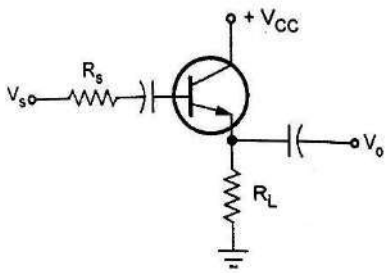
$$A_V = \frac{A_I R_L}{R_i}$$

Output admittance $(\mathbf{Y_o}) Y_o = 0$

$$R_o = 1/Y = \infty$$

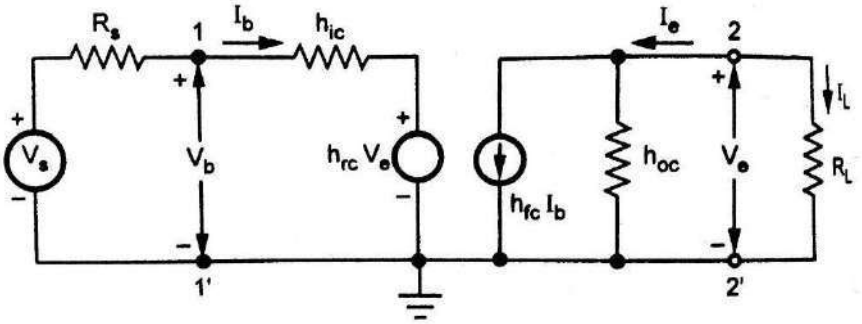
3. (A) Derive the expressions for current gain, voltage gain, input impedance and output impedance for an Emitter Follower (common collector) circuit.

Circuit diagram



(a) CC amplifier

h parameter equivalent circuit



(b) CC amplifier in its h-parameter model

Current gain (A_I) $A_I = \frac{I_L}{I_b} = \frac{-I_e}{I_b}$

Apply KCL

$I_e = h_{fc}I_b + h_{oc}V_e \quad = h_{fc}I_b + h_{oc}(-I_eR_L) \qquad (since, V_e = -I_eR_L)$

$I_e + I_eR_Lh_{oc} = h_{fc}I_b ; I_e(1 + h_{oc}R_L) = h_{fc}I_b ; \frac{I_e}{I_b} = \frac{h_{fc}}{1 + h_{oc}R_L}$

$$A_i = \frac{I_e}{I_b} = \frac{-I_L}{I_b} = \frac{-h_{fc}}{1 + h_{oc}R_L}$$

Input Resistance (R_i) $R_i = \frac{V_b}{I_b}$

Apply KVL

$V_b = h_{ic}I_b + h_{rc}V_e (\ V_e = -I_eR_L)$

$V_e = A_II_bR_L \qquad \{A_I = \frac{-I_e}{I_b}\}$

Now

$R_i = \frac{h_{ic}I_b + h_{re}(A_II_bR_L)}{I_b}; \qquad R_i = h_{ic} + h_{re}A_IR_L$

$R_i = h_{ic} - h_{rc}\left(\frac{h_{Fc}R_L}{1+h_{oc}R_L}\right) \qquad \{A_I = \frac{-h_{Fc}}{1+h_{oc}R_L}\}$

Voltage gain (A_V) $A_V = \frac{V_e}{V_b}$ $\{\because V_e = -I_e R_L;\ I_e = A_I I_b;\quad V_b = I_b\ R_i\}$

$$A_V = \frac{A_I I_b R_L}{V_b} \Rightarrow \frac{A_I I_b R_L}{I_b R_i} \qquad \{\because \frac{I_b}{V_b} = \frac{1}{R_i}\}$$

$$A_V = \frac{A_I R_L}{R_i}$$

Output admittance $(\mathbf{Y_0})$ $Y_0 = \frac{I_2}{V_2}$ with $V_s = 0$

$$Y_O = \frac{I_e}{V_e} \text{ with } V_s = 0$$

$$I_e = h_{fc}\, I_b + h_{oc}\, V_e$$

Dividing the above equation by V_e, $\quad \frac{I_e}{V_e} = \frac{h_{fc} I_b}{V_e} + h_{oc} \quad ---(1)$

From circuit $V_s = 0$

Apply KVL

$$R_S I_b + h_{ic}\, I_b + h_{rc}\, V_e = 0$$

$$(R_S + h_{ic}) I_b = -h_{rc}\, V_e$$

$$\frac{I_b}{V_e} = \frac{-h_{rc}}{R_s + h_{ic}} ---(2)$$

Sub equation (2) in (1)

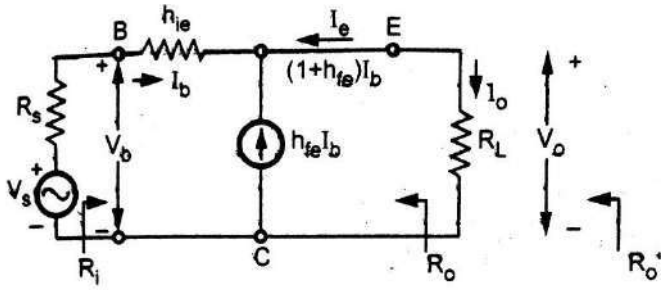
$$\frac{I_e}{V_e} = h_{fc}\left(\frac{-h_{rc}}{R_s + h_{ic}}\right) + h_{oc}$$

$$y_o = \frac{I_e}{V_e} = h_{oc} - \frac{h_{fc}\, h_{rc}}{R_s + h_{ic}} \quad and\ R_o = \frac{1}{y_o}$$

(B) Draw the circuit of CC amplifier with DC sources eliminated and deduce the small signal model for amplifier operation. (April/May 2019) (8 Marks) (OR) **Approximate analysis of CC amplifier using simplified Hybrid Model.**

In simplified CE model, the input is applied to base and output is taken from collector, and emitter is common between input and output. The same simplified model can be modified to get simplified CC model.

For simplified CC model, make collector common and take output from emitter.



The $h_{fb}I_b$ current direction is now exactly opposite that of CE model because the current $h_{fc}I_b$ always points towards emitter.

Current gain (A_I) $A_I = \frac{I_L}{I_b} = \frac{-I_e}{I_b}$

$A_i = 1 + h_{fe}$

Input Resistance (R_i) $R_i = \frac{V_b}{I_b}$

Apply KVL

$V_b = h_{ie}I_b + I_O R_L$; (divide both sides by I_b)

$\{A_I = \frac{-I_e}{I_b} = \frac{-I_O}{I_b}\}$

Now

$R_i = \frac{V_b}{I_b} = h_{ie} + (1 + I_O h_{fe})R_L$;

Voltage gain (A_V) $A_V = \frac{V_e}{V_b}$

$A_V = \frac{A_I I_b R_L}{V_b} \Rightarrow \frac{A_I I_b R_L}{I_b R_i}$ $\{\because \frac{I_b}{V_b} = \frac{1}{R_i}\}$

$A_V = \frac{A_I R_L}{R_i}$

Substituting values of A_I and R_i *we get,* $A_V = \frac{A_I I_b R_L}{V_b} \Rightarrow \frac{A_I I_b R_L}{I_b R_i}$

Output admittance (Y_0) $Y_0 = \frac{I_2}{V_2}$ with $V_s = 0$

$Y_O = \frac{I_e}{V_e}$ with $V_s = 0$

$I_e = h_{fc} I_b + h_{oc} V_e$

Dividing the above equation by V_e, $\frac{I_e}{V_e} = \frac{h_{fc}I_b}{V_e} + h_{oc} \quad ---(1)$

From circuit $V_s = 0$

Apply KVL

$R_S I_b + h_{ic} I_b + h_{rc} V_e = 0$

$(R_S + h_{ic})I_b = -h_{rc} V_e$

$\frac{I_b}{V_e} = \frac{-h_{rc}}{R_s + h_{ic}} ---(2)$

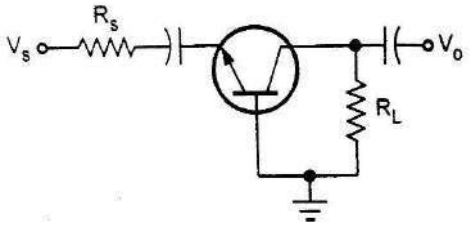
Sub equation (2) in (1)

$\frac{I_e}{V_e} = h_{fc}(\frac{-h_{rc}}{R_s + h_{ic}}) + h_{oc}$

$y_o = \frac{I_e}{V_e} = h_{oc} - \frac{h_{fc}\, h_{rc}}{R_s + h_{ic}}$ *and* $R_o = \frac{1}{y_o}$

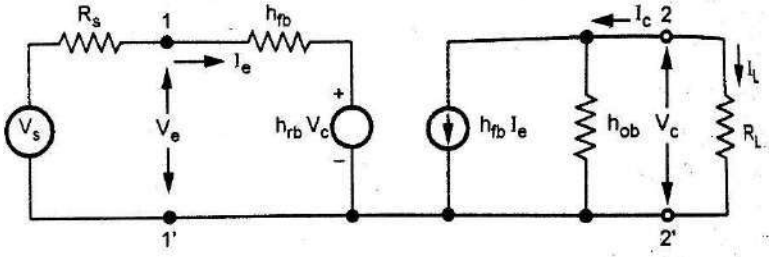
4. Derive the expression for A_i, A_v, R_c and R_o for CB amplifier using h parameter model. ***(April/May 2016)***

Circuit diagram



(a) CB amplifier

h parameter model



(b) h-parameter equivalent circuit for CB amplifier

Current gain (A_I) $A_I = \frac{I_L}{I_e} = \frac{-I_c}{I_e}$

$I_c = h_{fb}I_e + h_{ob}V_c$

$h_{fb}I_e + h_{ob}(-I_cR_L)$ $\quad \therefore V_c = -I_cR_L$

$I_c + h_{ob}I_cR_L = h_{fb}I_e$

$(1 + h_{ob}R_L)I_c = h_{fb}I_e$

$$A_I = \frac{I_c}{I_e} = -\frac{h_{fb}}{1 + h_{ob}R_L} \qquad \Rightarrow \frac{-I_L}{I_e} = -\frac{h_{fb}}{1 + h_{ob}R_L}$$

Input Resistance R_i $R_i = \frac{V_e}{I_e}$

$V_e = h_{ib}I_e + h_{rb}V_c$

$V_c = -R_LI_c$

$= A_II_eR_L$

$$R_i = \frac{V_e}{I_e} = \frac{h_{ib}I_e + h_{rb}A_II_eR_L}{I_e}$$

$R_i = h_{ib} + h_{rb}A_IR_L$

Voltage gain (A_V) $A_V = \frac{V_c}{V_e} = \frac{A_II_eR_L}{V_e}$

$$= \frac{A_I R_L}{R_c} \qquad \left| \frac{I_e}{V_e} = \frac{1}{R_i} \right.$$

Output admittance $(\mathbf{Y_0})$ $Y_0 = \frac{I_c}{V_c}$ with $V_s = 0$

$$I_c = h_{fb} I_e + h_{ob} V_c$$

$$\div V_c \quad \frac{I_c}{V_c} = \frac{h_{fb} I_e}{V_c} + h_{ob} \quad ---(1)$$

When $V_s = 0$

$$R_s I_e + h_{ib} I_e + h_{rb} V_c = 0$$

$$(R_s + h_{ib})\, I_e = -h_{rb} V_c$$

$$\frac{I_e}{V_c} = -\frac{h_{rb}}{R_s + h_{ib}} \quad ---(2)$$

Sub (2) in (1)

$$\frac{I_c}{V_c} = h_{fb}\left(\frac{-h_{rb}}{R_s + h_{ib}}\right) + h_{ob}$$

$$y_0 = \frac{I_c}{V_c} = h_{ob} - \frac{h_{fb}.\, h_{rb}}{R_s + h_{ib}}$$

$$R_o = \frac{1}{y_0}$$

5. **Explain the frequency response operation of BJT amplifier with suitable circuit diagram.**

From the fig 9.1, the capacitors C_S,C_C and C_E will determine the low-frequency response. C_s is normally connected between the applied source and active device. In fig 9.2The total resistance is now $R_S + R_i$,the cutoff frequency is established as

$$f_{LS} = \frac{1}{2M(R_S + R_i)\, C_S}$$

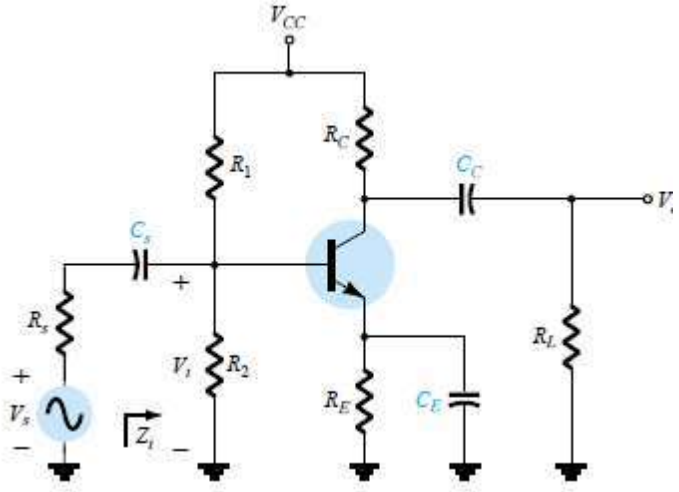


Fig Loaded BJT amplifier with capacitors that affect the low- frequency response

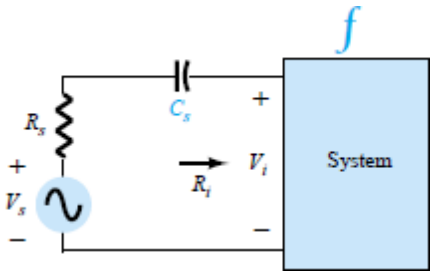


Fig Determining the effect of C_s on the low frequency response

At mid or high frequency, the reactance of the capacitor will be small to permit short circuit approximation for the element. the voltage V_i related to V_S by

$$V_i|_{mid} = \frac{R_i\ V_S}{R_i + R_S}$$

The value of R_i is determined by $R_i = R_1 \| R_2 \| \beta r_e$

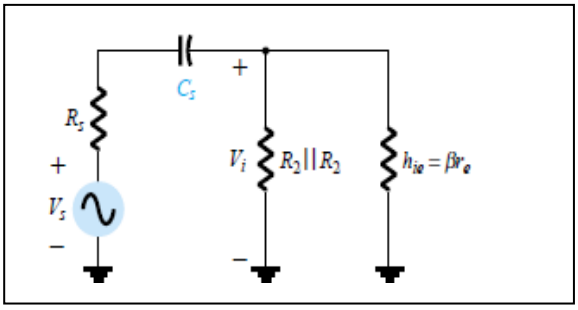


Fig Localized ac equivalent for C_s

The voltage V_i applied to the input of the active device can be calculated using the voltage divider rule: $V_i = \frac{R_i\ V_S}{R_S + R_i - jX_{Cs}}$

Since the coupling capacitor is normally connected between the output of the active device and the applied load, the R-C configuration that determines the low cutoff frequency due to C_C.

From fig 9.4 the total series resistance is now $R_0 + R_L$ and the cutoff frequency is determined by,

$$f_{LC} = \frac{1}{2M(R_{0+}\ _L)C_C}$$

The resulting value for R_0 , $R_0 = R_C \| r_0$

To determine f_{LE}, C_E must be determined from

$$f_{LE} = \frac{1}{2MR_{eC_E}}$$

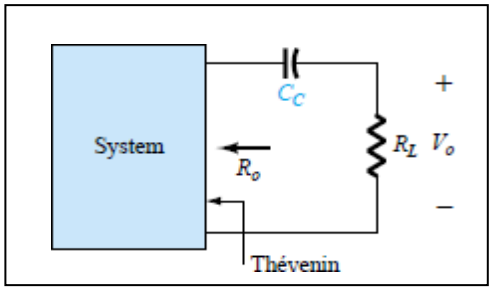


Fig determining the effect of C_c on the low freq

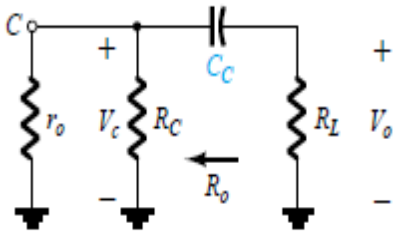


Fig Localized ac equivalent for C_c with V_i=0 V

The value of R_e is determined by $R_e = R_E \| (\frac{R_S'}{\beta} + r_e)$.where $R_S' = R_S \| R_1 \| R_2$

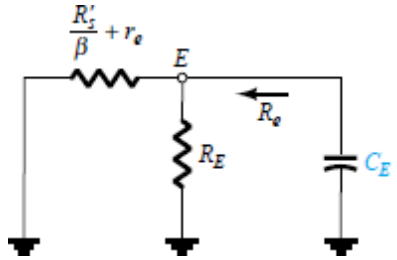


Fig .9.6 Localized ac equivalent of C_E

The effect of C_E on the gain is given by,

$$A_V = - R_C / r_e + R_E$$

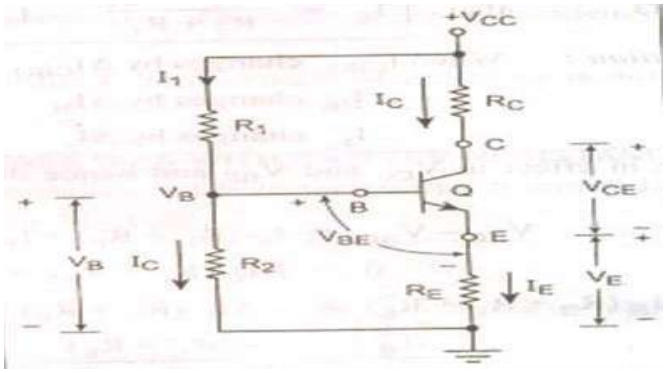
The maximum gain is available where R_E is 0Ω. At low frequency with bypass capacitor C_E in open circuit.

As the frequency increases, the reactance of the capacitor C_E will decrease, reducing the parallel impedance of R_E and C_E until R_E shorted out by C_E.

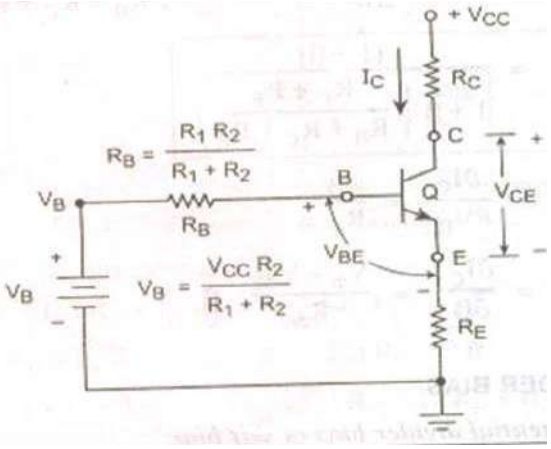
At the midband frequency level, the Short circuit equivalents for the capacitors can be inserted. The highest low frequency cutoff determined by C_S, C_C or C_E.
If there are two or more high cutoff frequencies, the effect will be to raise the lower cutoff frequency and reduce the resulting bandwidth of the system. there is an interaction between the capacitive elements that can affect the resulting low cutoff frequency.

6. Discuss the factors involved in the selection of I_C, R_C and RE for a single stage common emitter BJT amplifier circuit, using voltage divider bias (Nov/Dec2015)

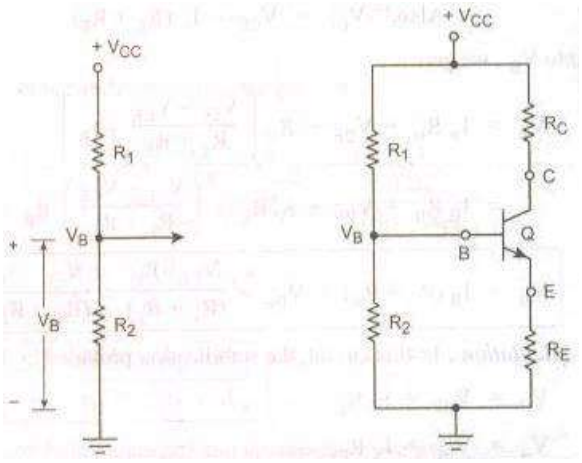
It is also called potential divider bias or self-bias.
In all D.C bias discussed in the above sections clearly states that the values of D.C bias currents and voltage of collector depends on the currents gain$\beta(\beta = \frac{IC}{IB})$. But we know it is purely a temperature sensitive one particularly in silicon type. Hence the nominal value of β is not well defined.
So it is not desirable to provide a D.C bias circuit which is independent of the transistor current gain (β). This is avoided by potential or voltage divider bias shown in the



Here R1 and R2 forms potential dividing Rc collector load resister and its equivalent thevinins circuits is as follows;



This method is widely used since its provides a stable Q-point.
In this method two resistors R1 and R2 connected across the supply voltage Vcc and it provide biasing.
Emitter resistance Re provides bias to BE junction. This causes the base current and hence collector current flows in zero signal condition.
Applying KVL law to BE junction circuit we get fig.



V_B is the voltage across R2 which is given by $V_B = VCC*(R2/ (R1+R2))$
Jut by taking this value as a source voltage and $R_B = R1 \| R2$

$$R_B = \frac{R1R2}{R1 + R2}$$

We can draw the thevinins equivalent circuit which is shown in fig
Then as per KVL law,
$V_B - I_B R_B - V_{BE} - I_E R_E = 0$
$V_B - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0$ $(I_E = I_B + I_C)$
$V_B = I_B R_B + V_{BE} + (I_C + I_B) R_E$
Then apply KVL to output side we get
$V_{CC} - I_C R_C - I_E R_E - V_{CE} = 0$ But $I_C = I_E$
$V_{CC} - I_C R_C - I_C R_E - V_{CE} = 0$
$V_{CC} - I_C (R_C + R_E) - V_{CE} = 0$
$I_C (R_C + R_E) = V_{CC} - V_{CE}$
$I_C = V_{CC} - V_{CE} / (R_C + R_E)$
Also $V_{CE} = V_{CC} - I_C / (R_C + R_E)$
Then put I_c into V_B we get
$V_B = I_B R_B + V_{BE} + R_E [V_{CC} - V_{CE} / (R_C + R_E) + I_B]$
$= I_B R_B + V_{BE} + I_B R_E + [V_{CC} - V_{CE} / (R_C + R_E)]$
$V_B = I_B(R_B + R_E) + V_{BE} + [V_{CC} * V_{CE} / (R_C + R_E)] - [V_{CE} * R_E / (R_C + R_E)]$

Gain and frequency response

7. Explain the frequency response of an amplifier with suitable characteristics.

The plot between the gain of the amplifier and frequency of the signal is known as frequency response of the amplifier. The frequency covers a wide range from 0Hz to very high frequencies(> 100MHz).

Decibels: The decibel (dB) is a measure of the difference in magnitude between two power levels. The power gain in decibel is given by,

$$G_{dB} = 10 \log_{10} \frac{P_2}{P_1} \text{ dB}$$

Where P_2 = specified terminal power; P_1 = reference power

If the power P_2 is output power (P_0) and P_1 is input power (P_i) of an amplifier. Then the power gain is given by,

$$G_{dB} = 10 \log_{10} \frac{P_0}{P_i}$$

If V_0 and V_i are output and input voltage of an amplifier then voltage gain, $G_{dB} = 20 \log_{10} \frac{V_0}{V_i}$

The frequency response is divided into three region 1) Low frequency region 2) Mid frequency region 3) High frequency region.

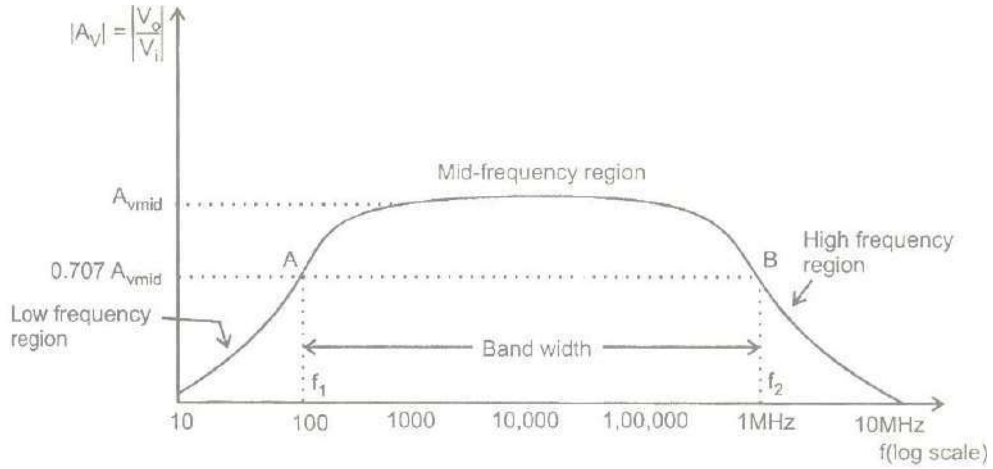


Fig: Frequency response of an amplifier

1) **Mid frequency region:** The gain of the amplifier is maximum A_{Vmid} intersecting the frequency response at point A and B. The corresponding frequencies f_1 ans f_2 are generally called corner, cutoff or half power frequencies.
If the maximum voltage gain in mid-band is $A_{Vmid} = V_0 / V_i$ then the gain at half power frequencies is $A_{Vmid} / \sqrt{2}$
The output power in mid-band is, $P_{o(mid)} = V_0^2 / R_0 = (A_{Vmid} V_i)2 / R_0$
The power at half power frequency is, $P_{o(HPF)} = V_0^2 / R_0 = (A_{Vmid} V_i / \sqrt{2})^2 / R_0$
$= P_{0(mid)} / 2$

2) **Cutoff Frequency:** The frequency at which the voltage gain is equal to 0.707 times of its maximum value is called cutoff frequency.

3) **Bandwidth:** The bandwidth of the amplifier is defined as the difference between the two half power frequencies f_1 and f_2
Bandwidth = $f_2 - f_1$
Where f_1= the lower cutoff frequency
f_2=the upper cutoff frequency

4) **Low frequency region:** In midband frequencies the coupling and bypass capacitor are replaced by short circuits.

Capacitive reactance $X_c = \frac{1}{2MfC}$

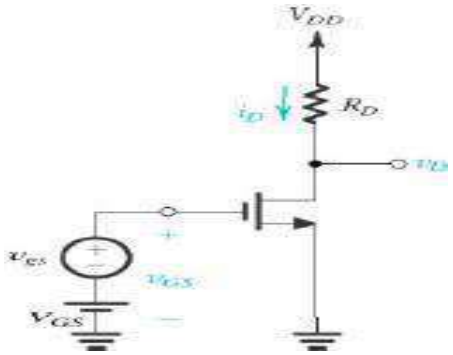
At Low frequency, the coupling and bypass capacitor are increased. Hence the voltage gain decreases.

5) **High frequency region:** Here the internal capacitance across the junction affects the performance of the amplifier.
The capacitance, $C_{b'e}$ = feedback path from bias to emitter
C_{ce} = feedback path from collector to emitter
These capacitors divert the signal to ground.
$C_{b'c}$ = feedback path from base to collector
This provides a bypass path for the input ac signal.

MOSFET-Small Signal Model

8. Draw and explain the small signal model of MOSFET.

To operate as an small signal amplifier,we bias the MOSFET in saturation region.



- The DC bias Point
- The signal current in the drain
- The voltage gain

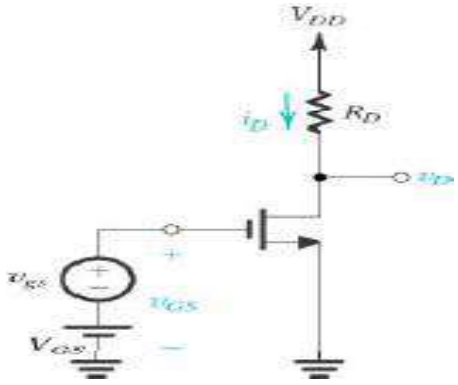
The DC bias Point: $I_D - \frac{1}{2} K_n'(W/L)(V_{GS} - V_t)^2$

$V_D = V_{DD} - I_D R_D$

$V_D \gg V_{GS} - V_t$

The required signal depends on V_D, which is sufficiently greater than $(V_{GS} - V_t)$.

The Voltage Gain:



$V_D = V_{DD} - I_D R_D$

$V_D = V_{DD} - (I_D + i_d)R_D$

$V_D = V_{DD} - I_D R_D - i_d R_D$

$V_d = - i_d R_D = - g_m v_{gs} R_D$

$A_v = V_d / V_{gs} = - g_m R_D$

In the small signal analysis, signal are superimposed on the DC quantities,

The drain current, $i_D = I_D + i_d$.

The AC drain current i_d is related to v_{gs} is so called transistor Trans conductance (g_m).

$$g_m \equiv i_d / v_{gs} = \tfrac{1}{2} K_n'(W/L)(V_{GS} - V_t)[S]$$

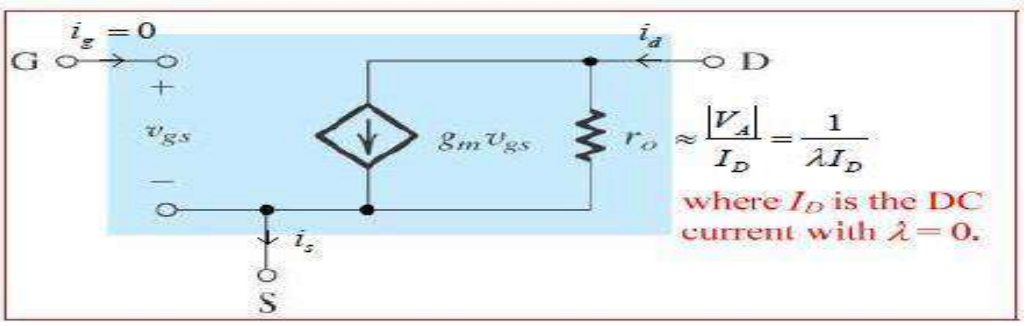
Sometimes expressed in terms of the overdrive voltage, $V_{OV} = V_{GS} - V_t$

$$g_m = K_n'(W/L) V_{OV} [S]$$

This g_m depends on the bias. The Trans conductance g_m equals the slope of i_D- v_{gs} characteristic.
Similarly drain voltage, $V_D = V_D + V_d$

In saturation mode, MOSFET acts a voltage controlled current source, The control voltage V_{gs} and output current i_D give rise to small signal Π-model.

For Operation in the saturation region $V_{GD} \leq V_t$ ==> $V_{GS} - V_{DS} \leq V_t$
Where the total drain to source voltage is $V_{DS} = V_{DS} + v_d$



- $i_g = 0$ and v_{gs} → infinite input resistance
- r_0 models the finite output resistance in the range from ≈ 10KΩ to 1MΩ and depends on bias current I_D.

$$g_m = K_n'(W/L)(V_{GS} - V_t)$$

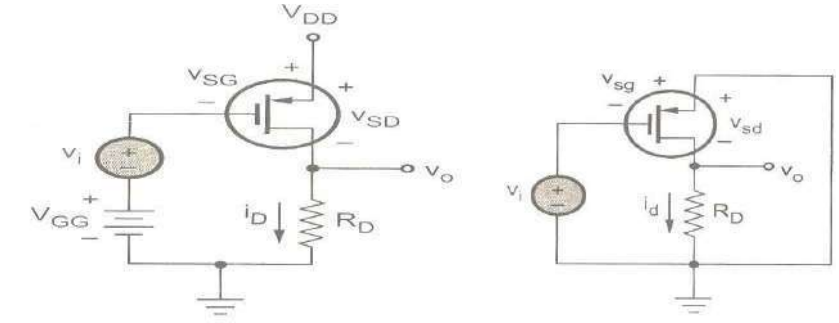
it can be, $g_m = I_D / (V_{GS} - V_t)/2$
Similar to $g_m = I_C / V_T$ for BJT. Hence the bias current $g_m$is much larger for than for MOSFET.

MOSFET have these advantages over BJT:

- ✓ High input resistance.
- ✓ Small physical size.
- ✓ Low power dissipation.
- ✓ Relative ease of fabrication.

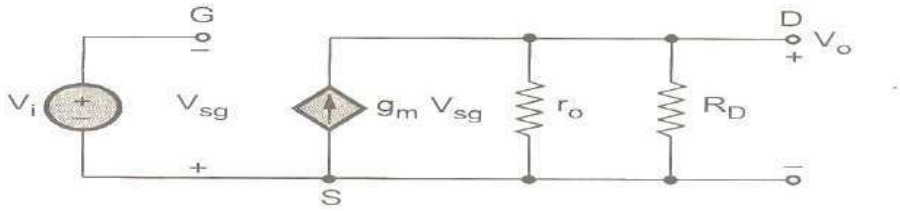
Becomes amplifiers combines the advantages of BJT and MOSFET, They provide very large input resistance from MOSFET and a large output impedance from the BJT.

9. Explain Small signal model of P Channel MOSFET.



(a) Common source circuit with PMOS transistor

(b) Corresponding a.c. equivalent circuit



Small signal equivalent circuit of common source amplifier with PMOS transistor model

The above diagram shows the common source circuit with p-channel MOSFET and its A.C equivalent circuit. The A.C equivalent circuit seen for n-channel MOSFET also applies to the p-channel MOSFET; however, there is a change in current directions and voltage polarities compared to the circuit containing the n-channel MOSFET. The above diagram shows the small signal equivalent circuit of the p-channel MOSFET amplifier.

10. Explain the Common – Source (CS) Configuration. (April/May 2019) (Nov/Dec 2017)

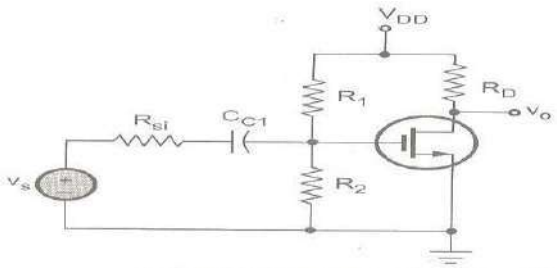
The diagram shows the common source circuit with voltage divider biasing and coupling capacitor. The MOSFET is biased near the middle of the saturation region by R1 and R2 resistors to work as an amplifier.

Assume that,the signal frequency is sufficiently large for the coupling capacitor to act essentially as a short circuit. The signal source is represented by a Thevenin equivalent circuit, in which the signal voltage source vs, is in series with an equivalent source resistance Rsi.

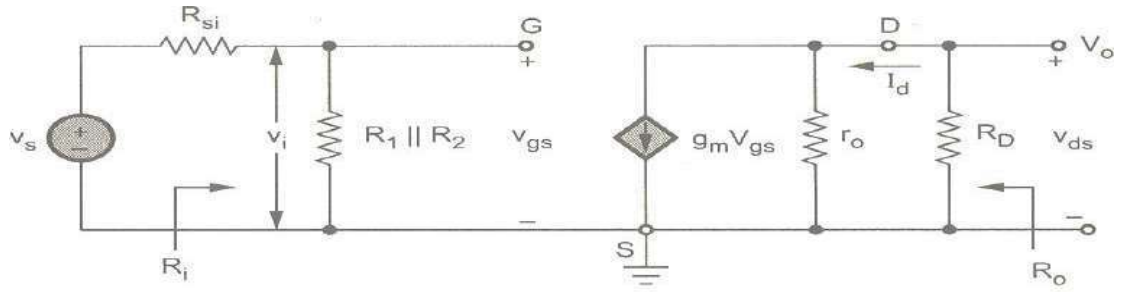
Here R_{si} should me much less than the amplifier input resistance,

$R_i = R_1 \| R_2$ in order to minimize loading effects.

The following diagram shows the resulting small- signal equivalent circuit.



Common-source circuit with voltage divider biasing and coupling



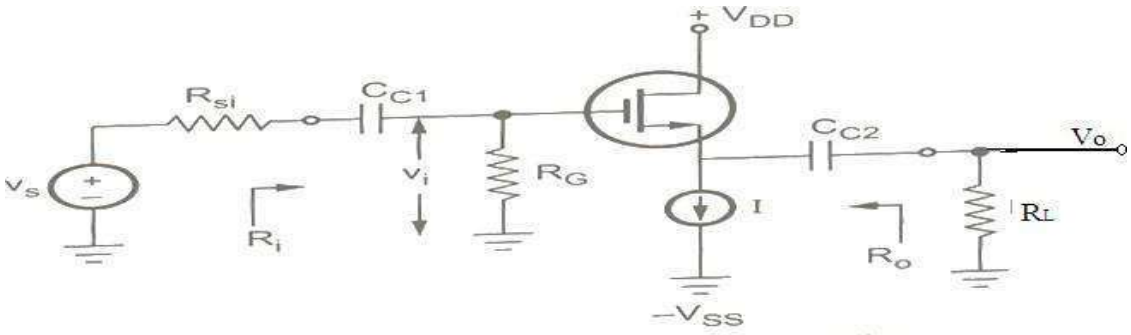
Small-signal equivalent circuit

$v_o = - g_m v_{gs} (r_o \| R_D)$
$v_i = v_{gs}$
$A_v = v_o / v_i = - g_m v_{gs} (r_o \| R_D) / v_{gs} = - g_m (r_o \| R_D)$
The input gate to source voltage is
$v_i = (R_i / R_i + R_{si})\, v_s$
So the small signal overall voltage gain is,

$G_v = v_o / v_s = - g_m (r_o \| R_D)(R_i / R_i + R_{si}) = A_v (R_i / R_i + R_{si})$

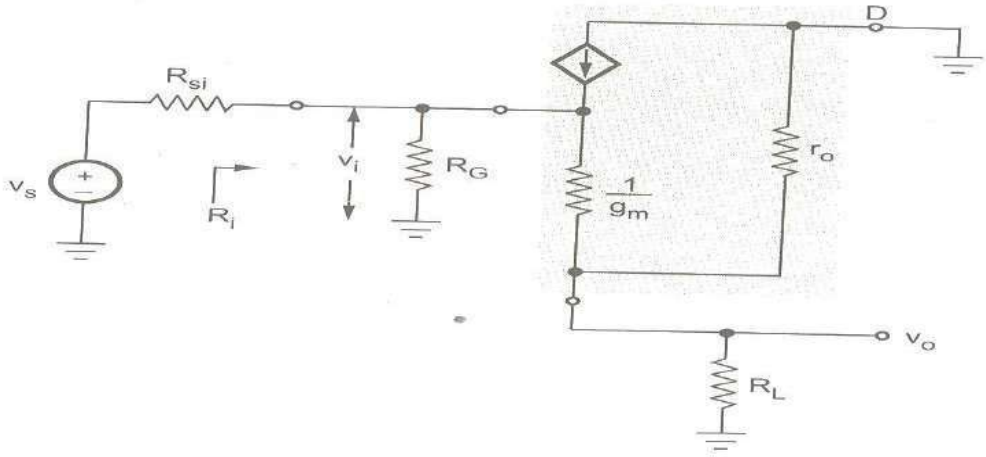
Since Rsi is not zero, the amplifier input signal v_i is less than the signal voltage, This is known as **loading effect**. It reduces the voltage gain of the amplifier.
The input resistance is $R_{is} = R_1 \| R_2$
The output resistance is $R_o = R_D \| r_o$
We can also relate the A.C drain current to the A.C drain to source voltage, as
$V_{ds} = - I_d (R_D)$

11. Analysis of Common – Drain (CD) or Source follower Amplifier.(Nov/Dec 2016)(May 2017)



Common drain amplifier

The above diagram shows the common – drain amplifier circuit. It is also known as grounded drain amplifier.
In this amplifier circuit, drain is used as a signal ground and hence RD is not needed.
The input signal is coupled to via Cc1 to the MOSFET gate and the output signal at the output signal at the MOSFET source is coupled via Cc2 to a load resistance RL.
Since RL is in effect connected in series with the source terminal of the MOSFET, it is more convenient to use the MOSFET's T model for the analysis. This is shown in the following diagram.
$R_i = R_G$
$v_i = v_s x R_i / (R_i + R_{si}) = v_s x R_G / (R_G + R_{si})$
From the following diagram it can be seen that the load resistance RL is in parallel with ro and resistance 1/gm in series with $R_L \| r_o$.



Small signal equivalent circuit for CD amplifier

The input voltage v_i appears across the total resistance and hence by applying the voltage divider rule, we have

$v_o = v_i x (R_L \| r_o) / (1/g_m) + (R_L \| r_o)$

$A_v = v_o / v_i = (R_L \| r_o) / (1/g_m) + (R_L \| r_o)$

The open circuit voltage gain A_{vo} (RL = Infinity) is given as

$A_v = r_o /(1 / g_m) + r_o$

Since $r_o >> 1 / gm$, the open circuit voltage gain tends to unity; however, it is always less than unity.

Usually, $R_L << r_o$ and hence the voltage gain given by above expression Av becomes

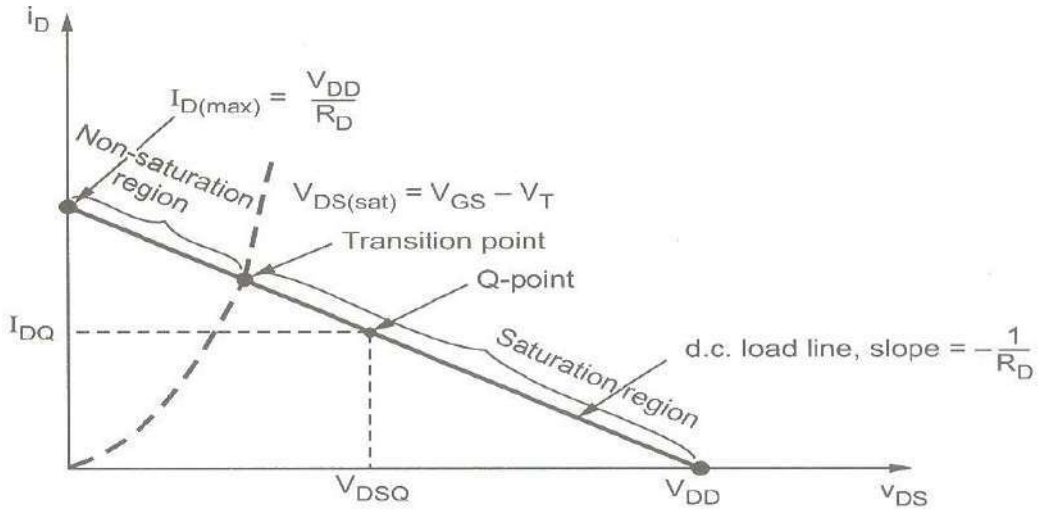
$A_v = v_o / v_i = R_L / (1 / g_m) + R_L$ $(R_L << r_o)$

$A_{vs} = G_v = v_o / v_s = v_o / v_i X v_i / v_s$

$= (R_L \| r_o) / (1 / g_m) + (R_L \| r_o) X R_G / (R_G + R_{si})$

The output resistance is given by

$R_o = 1 / g_m \| \ r_o = 1 / g_m$.



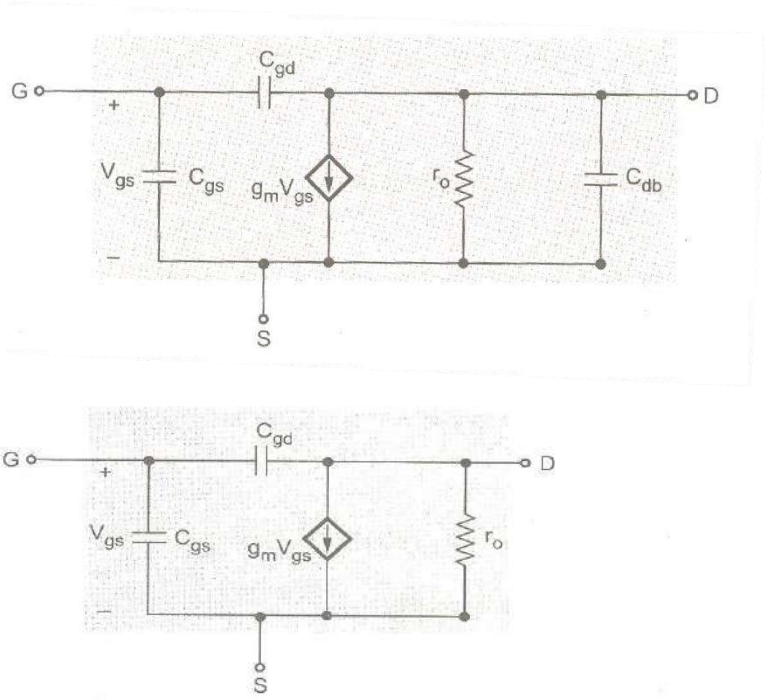
D.C. load line and transition point separating saturation and non-saturatio regions

The above diagram shows the D.C load line, the transition point, and the Q- point, which is in the saturation region.

High Frequency Analysis

12. Explain High – Frequency MOSFET Model.

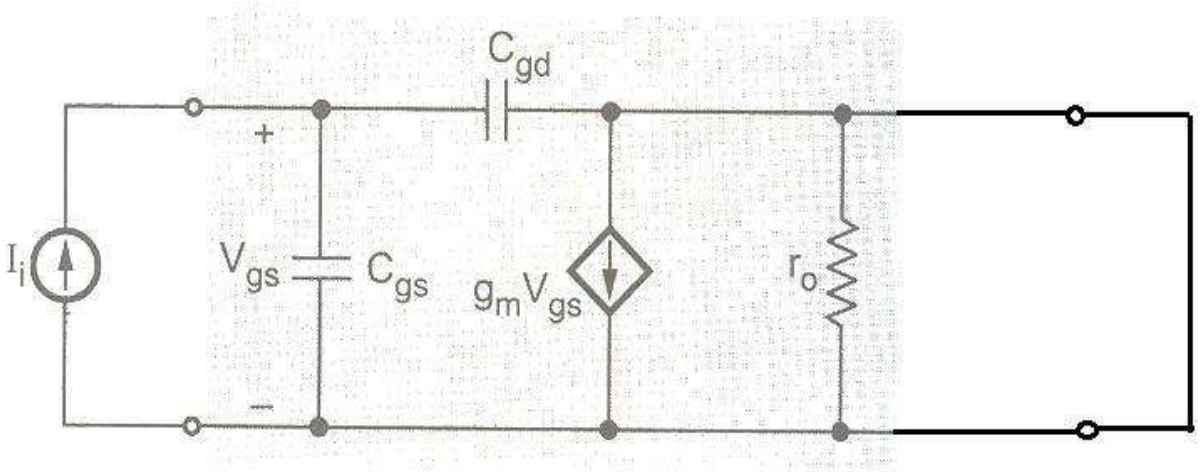
Following diagram shows the high frequency equivalent circuit model for MOSFET. In this model, capacitance C_{db} can be neglected to simplify the analysis. The resulted model is shown



High frequency equivalent circuit neglecting C_{db}

13. Calculate the current gain of high frequency model. (OR)
Derive an expression for MOSFET unity gain frequency(f_T). (April/May 2019)

The f_T is the frequency at which the short – circuit current gain of the CS MOSFET amplifier becomes unity.



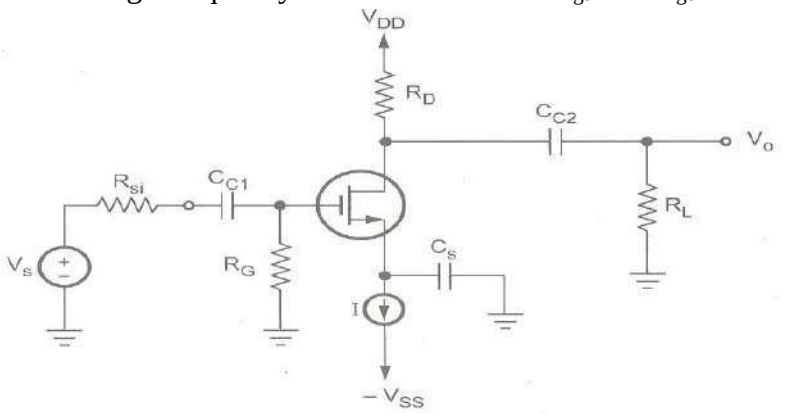
The above diagram shows the modified high – frequency equivalent circuit to determine the short – circuit current gain. Here, the input is fed with a current – source signal Ii and the output terminals are shorted.
The short circuit current Io is given by

$I_o = g_m V_{gs} – s C_{gd} V_{gs}$

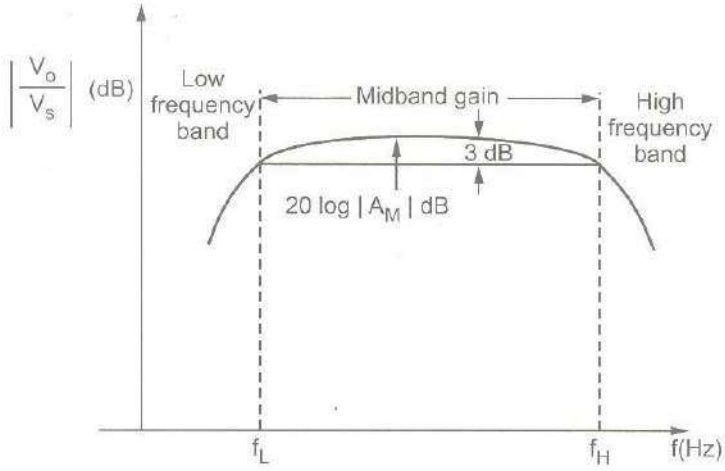
The second term in the above equation is very small and can be neglected at the frequencies of interest and thus
$I_o = g_m V_{gs}$
The Vgs in terms of Ii can be given by
$V_{gs} = I_i / s (C_{gs} + C_{gd})$
Substituting the values of I_i and I_o from the above equations we have
$I_o / I_i = g_m V_{gs} / V_{gs}.s(C_{gs} + C_{gd}) = g_m / s(C_{gs} + C_{gd})$
For physical frequencies s=jω. From above equation it can be seen that the magnitude of the current becomes unity at the frequency.
$\omega_T = g_m / C_{gs} + C_{gd}$
$f_T = g_m / 2\pi (C_{gs} + C_{gd})$
From the above expression we can say that f_T is proportional togm and inversely proportional to the internal capacitances.

14. Explain Frequency response of CS Amplifier. (Apr/May 2018) *(OR)* With neat circuit diagram, perform ac analysis for common source using equivalent circuit NMOSFET AMPLIFIER (NOV/DEC2015)

The following diagram shows the CS MOSFET amplifier. Its gain falls at low frequency due to the effect of C_{c1} and C_s and C_{c2}. Its gain falls at high frequency due to the effect of C_{gs} and C_{gd}.



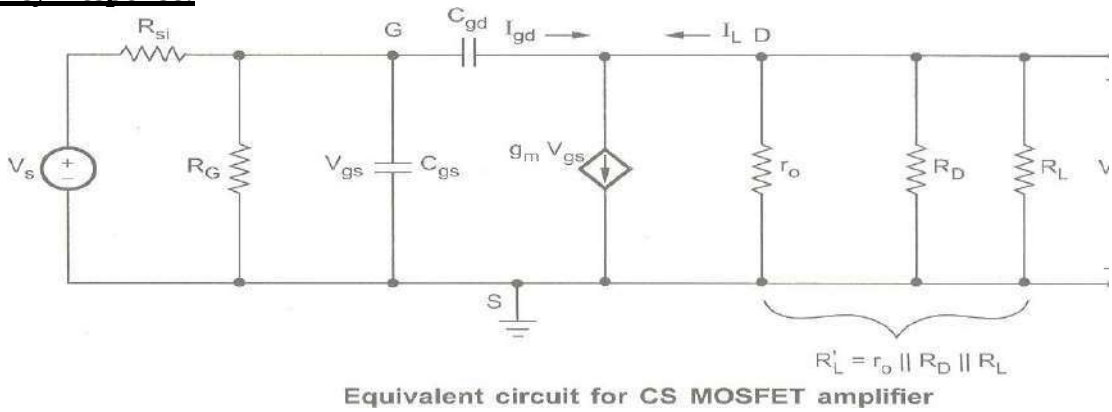
CS MOSFET amplifier



Frequency response of CS MOSFET amplifier

Above diagram shows frequency response of CS MOSFET amplifier.

High Frequency Response:



Equivalent circuit for CS MOSFET amplifier

The above diagram shows equivalent circuit for CS MOSFET amplifier.

Let us consider the output node. The load current is $g_m V_{gs} - I_{gd}$, where $g_m V_{gs}$ is the output current of the MOSFET and I_{gd} is the current supplied through the very small capacitance C_{gd}.

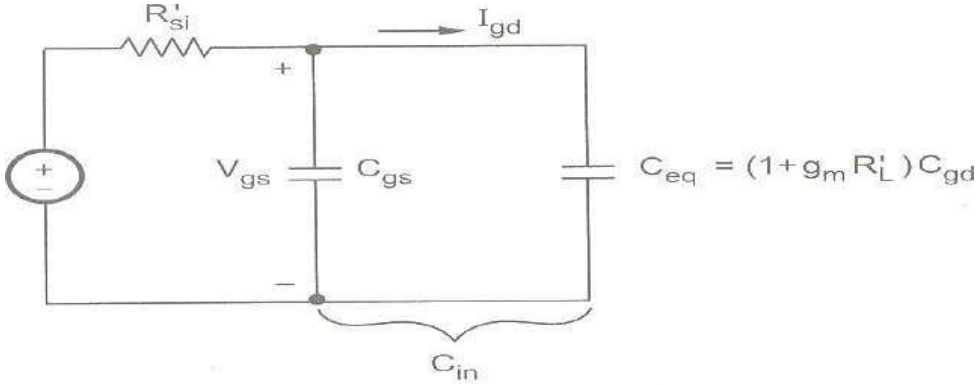
At frequencies in the vicinity of f_H, the I_{gd} is very small and can be neglected.

Hence we can write

$V_o \approx - I_L R_L = - g_m V_{gs} R_L`$

Where $R_L = r_o \| R_d \| R_L`$

Now consider the input node. We can replace Cgd at the input side with the equivalent capacitance Ceq using Miller's theorem. This is shown in the following diagram.



Input node

By Miller's theorem, equivalent capacitance is given by,

$C_{eq} = (1 + A_v)C = (1 + A_v)C_{gd}$

Since input voltage Vgs, we have

$A_v = V_o / V_i = -g_m V_{gs} R_L` / V_{gs} = - g_m R_L`$

$C_{eq} = (1 + g_m R_L`)$ = Total input capacitance Cin can be given by,

$C_{in} = C_{gs} + C_{eq} = C_{gs} + (1 + g_m R_L`)C_{gd}$

The total resistance is given by,

$R_{si}` = R_{si} \| R_G$

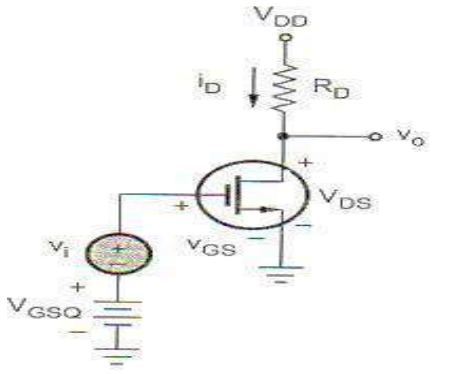
By considering input circuit as a simple- time constant circuit we have

$\tau = RC = R_{si}` C_{in}$

$\omega_H = \omega_o = 1/ \tau = 1 / R_{si}`C_{in}$

$f_H = 1 / 2\pi R_{si}`C_{in}$

15. Explain small signal model of MOSFET.



NMOS common-source circuit with time varying signal source in series with gate d.c. source

From the above diagram, we see that the output voltage is

$v_{ds} = V_o = V_{DD} - i_D R_D$

$v_o = V_{DD} - (I_{DQ} + i_d) R_D = (V_{DD} - I_{DQ} R_D) - i_d R_D$

The output voltage is also a combination of D.C and A.C values. The time – varying output signal is the time – varying drain to source voltage, or

$Vo = Vds = - i_d R_D$

We have,

$i_d = g_m V_{gs}$

In summary, the following relationships exist between the time varying signals for the circuit. The equations are given in terms of the instantaneous A.C values as well as the phasors. We have,

$v_{gs} = v_i$

(or)

$V_{gs} = V_i$ and

$I_d = g_m v_{gs}$

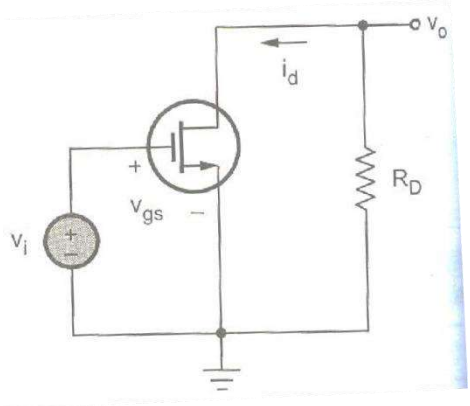
(or)

$I_d = g_m V_{gs}$ also

$v_{ds} = - i_d R_D$

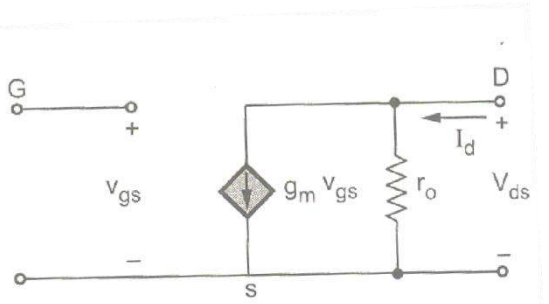
(or)

$V_{ds} = - I_d R_D$

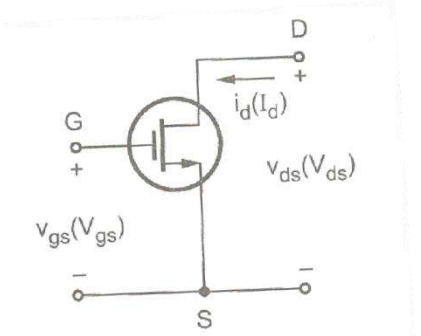


The above diagram shows the A.C equivalent circuit. Here, the D.C sources are made zero.

From the equivalent circuit for the NMOS amplifier circuit, we can draw a small signal equivalent circuit for the MOSFET.



Expanded small signal equivalent circuit, including output resistance, for NMOS transistor



Common-source NMOS transistor with small signal parameters

The above diagram shows the small signal low frequency A.C equivalent circuit for n – channel MOSFET.

The relation of I_d by V_{gs} is included as a current source gm vgs connected from drain to source.
The input impedance is represented by the open circuit at its input terminals, since gate current IG is zero.
We know that the circuit has the finite output resistance of a MOSFET biased in the saturation region because of the nonzero slope in the I_D versus V_{DS} curve.

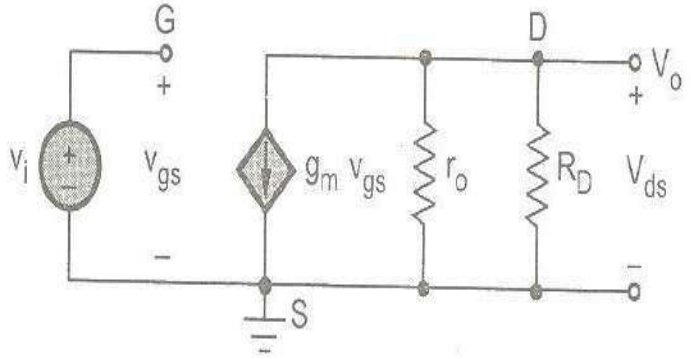
We also know that,
$i_D = K [(v_{CS} – V_T)^2(1+\lambda v_{DS})]$

where λ is the channel length modulation parameter and is a positive quantity. The small signal output resistance, is defined as,

$$r_o = (\partial i_D / \partial v_{DS})^{-1} \Big| v_{GS} = V_{GSQ} = \text{const.}$$

$$r_o = [\lambda K [(v_{GSQ} – V_T)^2]^{-1} \approx [\lambda I_{DQ}]^{-1}$$

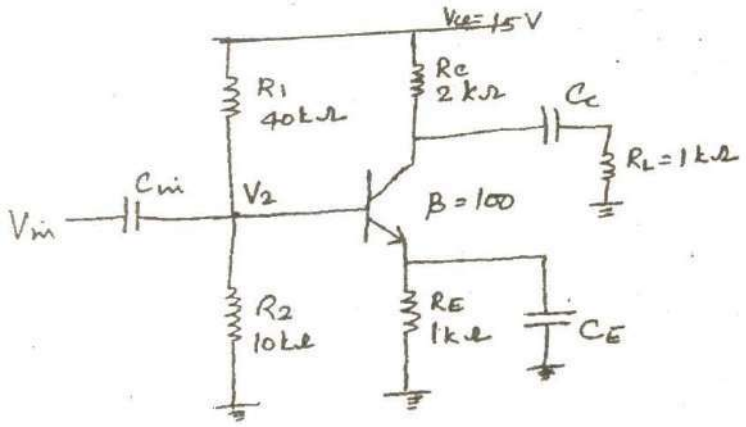
This small signal output resistance is also a function of the Q – point parameters. The following diagram shows the small signal equivalent circuit of common – source circuit.



Small signal equivalent circuit of common-source circuit with NMOS transistor model

Problems

1. **For the circuit below, find (i) dc bias levels (ii) dc voltage across the capacitors (iii) ac emitter resistance (iv) voltage gain (v) state of the transistor. (Nov/Dec 2018)**



Solution:

Given that,

Emitter resistance, R_E=1 KΩ
Collector resistance, R_C=2 KΩ
Load resistance, R_L=1 KΩ
Collector input voltage, V_{CC}=15V
Amplification factor, ß=100
Input resistance, R_1=40 KΩ and R_2=10 KΩ
Voltage gain, A_V= ?
AC emitter resistance, r_e= ?

i. **DC bias levels:** DC bias levels of CE amplifier determined by calculating various dc voltages and dc currents.

DC voltage, V_2 across resistor, R_2 is

$$V_2 = \frac{V_{CC}}{R_1 + R_2} X R_2$$

Substituting the corresponding values, V_2 is obtained as,

$$V_2 = \frac{15}{40 + 10} X 10$$

V_2= 3 V

DC emitter voltage, V_E across emitter resistor, R_E is,

$V_E = V_2 - 2V_{BE}$
= 3 V- 0.7 V
= 2.3 V

DC emitter voltage, V_E= 2.3 V

DC emitter current, I_E is given by,

$$I_E = \frac{V_E}{R_E}$$

$$I_E = \frac{2.3\ V}{1\ K\Omega} = 2.3\ mA$$

DC Collector voltage, V_C is determined as, $V_C = V_{CC} - I_C R_C$

V_C=15 V - 2.3 X 2 KΩ since $[I_E = I_C]$

V_C = 10.4 V

DC base current, I_B is obtained as,

Using the relation $I_C = ß\ I_B$

$$I_B = \frac{I_C}{ß} = \frac{2.3\ mA}{100} = 0.023\ mA$$

ii. DC voltages across the capacitors: From the above calculations, DC voltages across capacitors in the circuit is obtained as,

DC voltage across capacitor, C_{in} is, $V_2 = 3$ V

DC voltage across emitter capacitor, C_E is , $V_E = 2.3$ V

DC voltage across collector capacitor, C_C is $V_C = 1.4$ V

iii. AC Emitter Resistance: The ac emitter resistance, r_e' is given by, [$I_E = 2.3$ mA]

$$r'_e = \frac{25\text{ mV}}{I_E} = \frac{25\text{ mV}}{2.3\text{ mA}} = 10.9\ \Omega$$

iv. Voltage Gain(A_V): The voltage gain A_V of CE amplifier is defined by,

$$A_V = \frac{r_c}{r'_e}$$

Here, total ac collector resistance, r_c is determined by, $r_e = R_c \parallel R_L$

$$r_c = \frac{R_C R_L}{R_C + R_L} = \frac{2\,X\,1}{2+1}\ 10.9\Omega = 0.667\ K\Omega$$

Substituting r_c value in A_V, implies,

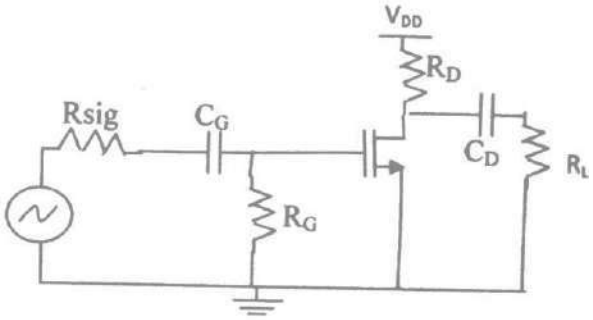
$$A_V = \frac{0.667\ K\Omega}{10.9\ \Omega}$$

Voltage gain, $A_V = 61.2$

v. State of transistor: From the above calculation it can be determined that the transistor is in active state.

Since $V_C > V_E$

2. Determine the mid band gain, the upper 3 dB frequency f_H of a CS amplifier fed with a signal source having an internal resistance R_{sig} = 100 KΩ. The amplifier has RG = 4.7 MΩ, $R_D = R_L$ = 15 KΩ gm = 1 mA/V, r_o = 150 KΩ, C_{gs} = 1 pF and C_{gd} = 0.4 pF. (May/June2016)



Solution: $A_M = \frac{R_G}{R_G + R_{Sig}} g_m R'_L$

Where $R'_L = r_0 \| R_D \| R_L = 150 \| 15 \| 15 = 7.14\text{K}\Omega$

$$g_m R'_L = 1 \times 7.14 = 7.14 V/V$$

Thus $A_M = -\frac{4.7}{4.7+0.1} \times 7.14 = -7 V/V$

The equivalent capacitance C_{eq} is found as

$$C_{eq} = (1 + g_m R'_L) C_{gd} = (1 + 7.14) \times 0.4 = 3.26 pF$$

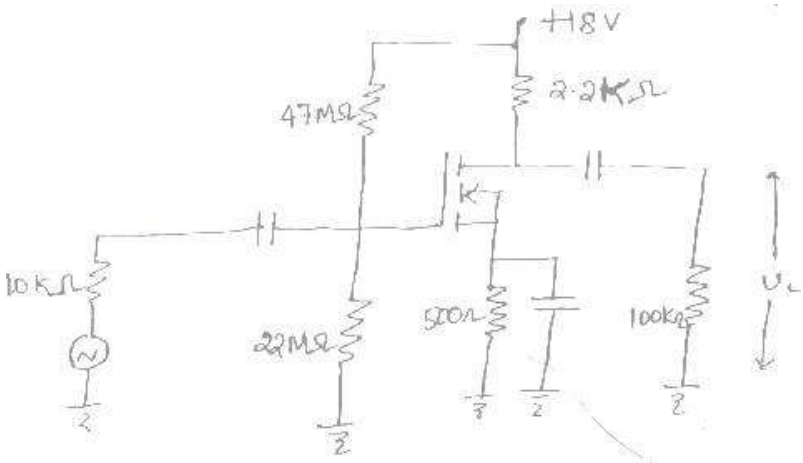
The total input capacitance C_{in} can be now obtained as

$$C_{in} = C_{gd} + C_{eq} = 1 + 3.26 = 4.26\ pF$$

The upper 3 dB frequency f_H is found from

$$f_H = \frac{1}{2\pi C_{in}(R_{sig} \| R_G)} = \frac{1}{2\pi \times 4.26 \times 1^{-12}(0.1 \| 4.7) \times 10^6} = 382\ kHz$$

3. The MOSFET shown fig has the following parameter V_T = 2V, $Q = 0.5 \times 10^{-3}$, r_d = 75KΩ. It is biased at at I_D = 1.9m A. (Nov/Dec2017)



a) Verify that the MOSFET is biased in its active region.
b) Find the input resistance.
c) Draw the small single equivalent circuit and find the voltage gain VL/VS.

Solution:

a) $V_{DS} = V_{DD} - I_D(R_D + R_S) = 18 - (1.9mA)(2.2 * 103 + 500) = 12.87V$

$$V_G = \left(\frac{22 * 10^6}{47 * 10^6 + 22 * 10^6}\right) 18 = 5.74V$$

Using equation 7.25 to find V_{GS}, we have

$V_{GS} = 5.74-(1.9)(5) = 4.79V$

$$|V_{GS} - V_T| = |4.79 - 2| = 2.79V$$

Therefore condition 8.30 is satisfied;

$$12.87 = |V_{DS}| > |V_{GS} - V_T| = 2.79$$

And we conclude that the MOSFET is biased in its active region.

b)

$$r_{in} = R_1 \| R_2 = (47M\Omega \| (22M\Omega) = 15M\Omega$$

c) From equation 8.31,

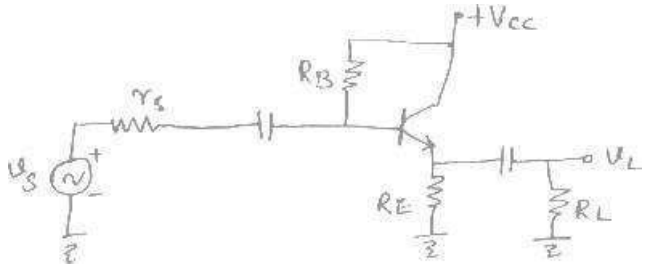
$g_m = 0.5 * 10^{-3}(4.79 - 2) = 1.4 * 10^{-3}$ S

The small single equivalent circuit is shown in fig 8.33 from equation 8.33

$$\frac{v_L}{v_s} = \left(\frac{15 * 10^6}{10 * 10^3 + 15 * 10^6}\right) * (-1.4 * 10^{-3})[(75 * 10^3 \| (2.2 * 1^3 \| (100 * 10^3)]$$

$= (0.999)(-1.4*10^{-3})(2.09*10^3) = -2.92$

4. A CC amplifier shown in below figure has V_{CC} = 15V, R_B = 75KΩ and R_E = 910 Ω the Q of the silicon transistors is 100 and the load resistor is 600 Ω find r_{in} and A_V. (Nov/Dec 2015)



Given:

V_{CC} = 15V, R_B = 75KΩ, R_E = 910 Ω, $\beta = 100$, RL = 600 Ω

To Find: r_{in} and A_V

Formulae used $I_B = \frac{V_{CC}-0.7}{R_B+(\beta+1)R_E}$, $I_E = (1+\beta)I_B$, $r_E = \frac{0.026}{I_E}$

$$r_{in}(stage) = (\beta+1)(r_e + r_L) \| R_B$$

$$V_L = R_E \| R_L$$

$$r_{in}(stage) = (\beta+1)(r_e + R_E)$$

$$r_o(stage) = R_E \| r_e \qquad (r_s = 0)$$

$$A_r = \frac{V_L}{V_S} = \frac{R_E}{r_E + R_E} \; (output\ open)$$

Calculation:

$$I_B = \frac{V_{CC}-0.7}{R_B+(\beta+1)R_E} = \frac{15-0.7}{75000+(100+1)910} = \frac{15-0.7}{75000+101*910} = \frac{143}{166910}$$

$$= 8.5674 \times 10^{-4} A$$

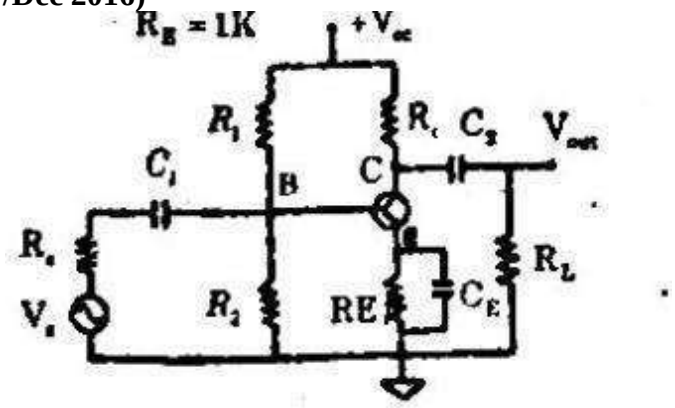
$$I_E = (1+\beta)I_B = (101) \times 8.5674 \times 10^{-4} = 0.08653A$$

$$r_E = \frac{0.026}{I_E} = \frac{0.026}{0.08653} = 0.300$$

$$r_{in}(stage) = (\beta+1)(r_e + R_E) = (101) \times (0.300 + 910) = 91940.3\ ohms$$

$$A_V = \frac{V_L}{V_S} = \frac{R_E}{r_E + R_E} = \frac{910}{910+0.300} = 0.999$$

5. Evaluate the A_I, A_V, R_i, R_o, A_{is}, A_{vs} of a single stage CE amplifier with R_s=1 KΩ R_1=22KΩ, R_2=10KΩ, R_c=2KΩ, R_L=2KΩ, h_{fe}=50,h_{ie}=1.1KΩ, h_{oe}=25μA/V and h_{re}=2.5X10^{-4}
(Nov/Dec 2016)



Given
R_s=1 KΩ R_1=22KΩ,R_2=10KΩR_c=2KΩ,R_L=2KΩ,h_{fe}=50,h_{ie}=1.1KΩ,h_{oe}=25μA/V and h_{re}=2.5X10^{-4}.

i)Current gain

$$A_i = -h_{fe} = -50$$

ii) Input impedance $R_i = h_{ie} = 1.1\ k\Omega$

$$R_i = h_{ie} \| R_1 \| R_2$$
$$= 1.1 \times 10^3 \| 22 \times 10^3 \| 10k\Omega$$
$$= 1.1 \times 10^3 \| \left[\frac{22 \times 10 \times 10^6}{32 \times 10^3}\right]$$
$$= 1.1 \times 10^3 \| \left[\frac{220 \times 10^3}{32}\right]$$
$$= 1.1 \| 6.87k$$
$$= \frac{1.1 \times 6.87 \times 10^6}{(1.1 + 6.87)10^3} = \frac{7.56 \times 10^6}{7.975 \times 10^3} = 0.947 \times 10^3 = 947\ \Omega$$

iii*)*Voltage gain

$$A_v = \frac{A_I R_L'}{R_i} = \frac{-50 \times (R_c \| R_L)}{R_i} = \frac{-50(2k \| 2k)}{1.1k} = -45.45$$

Output voltage

$$R_0 = \frac{1}{y_0} = \infty$$
$$R_0' = R_0 \| R_L' = \infty \| 2k \ \| \ 2k = 1k$$

Over all voltage gain

$$A_{vs} = A_V \times \frac{V_{in}}{V_s}$$
$$A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_b} \times \frac{V_b}{V_s}$$

$$where\ \frac{V_o}{V_b} = Av\ and \qquad \frac{V_b}{V_s} = \frac{R_1}{R_1 + R_3}$$

$$A_{vs} = \frac{AvR_L'}{R_i' + R_s} = \frac{-45.45 \times 947}{947 + 1k} = \frac{-45.45 \times 947}{1947} = -22.106$$

Overall current gain

$$A_{is} = \frac{I_L}{I_S} = \frac{I_L}{I_C} \times \frac{I_C}{I_b} \times \frac{I_b}{I_S}$$

$$\frac{I_L}{I_C} = \frac{R_c}{R_c + R_L} = \frac{-2k}{2k + 2k} = \frac{-2k}{4k} = -0.5$$

$$\frac{I_C}{I_b} = h_{fe} = 50$$

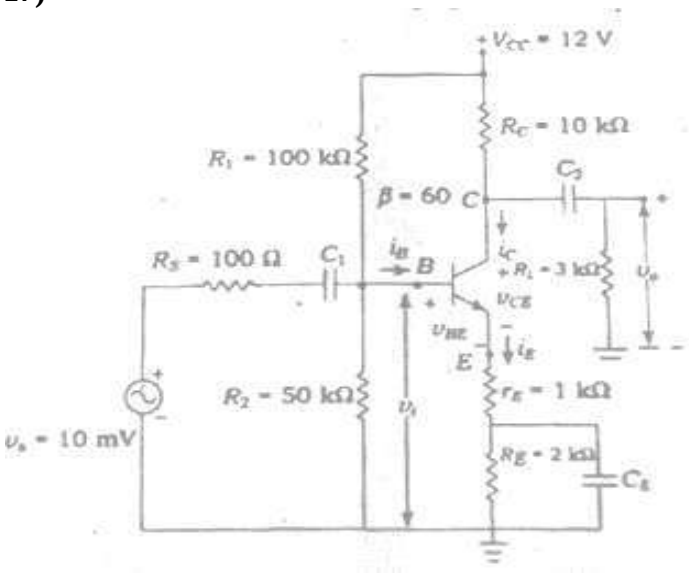
$$\frac{I_b}{I_S} = \frac{R_B}{R_B + R_i} = \frac{22\|10}{22\|10 + 11k} = \frac{6.87k}{6.87k + 11k} = \frac{6.87}{7.97} = 0.86$$

$A_I = \frac{I_L}{I_S}$

$= -0.5 \times 50 \times 0.86$

$A_{IS} = -21.54$

6. Fig shows a common emitter amplifier. Determine the input resistance, ac load resistance, voltage gain and output voltage?(May 2017)



Given:

$V_{CC} = 12\ V, R_C = 10\ k\Omega, R_\alpha = 3\ k\Omega, \beta = 60, R_1 = 100\ k\Omega, R_2 = 50\ k\Omega, r_E = 1\ k\Omega, R_{E1} = 2\ k\Omega, R_S = 100\ \Omega,$

$$V_s = 10\ mV$$

Input resistance looking directly into the base.

$$V_{th} = V_{CC}\left(\frac{R_2}{R_1 + R_2}\right) = 12\left(\frac{50 \times 10^3}{100 \times 10^3 + 50 \times 10^3}\right)$$

$$= 12\left(\frac{50}{150}\right) = \frac{12}{3} = 4\ V$$

$$R_{th} = R_1 \| R_2$$

$$= \frac{100 \times 50 \times 10^3 \times 10^3}{10^3 \times 100 + 50 \times 10^3} = \frac{100 \times 50 \times 10^3}{10^3(150)}$$

$$= \frac{500 \times 10^3}{15} = \frac{100 \times 10^3}{3} = 33.3 \times 10^3 \Omega = 33.3\ k\Omega$$

$$Emitter\ resistance\ (R_E)$$

$$R_E = R_{E1} + R_E = 1k\Omega + 2k\Omega = 3k\Omega$$

$$I_E = \frac{V_{th} - V_{BE}}{R_E + \frac{R_{th}}{\beta}}$$

$$= \frac{4 - 0.7}{3 \times 10^3 + \frac{33.3 \times 10^3}{60}}$$

$$I_E = \frac{3.3}{3555.55} = 0.000928 = .92mA$$

A.C resistance

$$r_e^1 = \frac{25}{I_E(mA)} = \frac{25}{0.92}$$

Input resistance

$$R_i = \beta(r_E + r_e^1) = 27\Omega$$
$$= 60(1 \times 10^3 + 27)$$
$$= 61620\ \Omega$$
$$= 61.6\ k\Omega$$

Input resistance of the stage

$$R_{is} = (R_1 \| R_2) \| \quad [\beta(r_E + r_e^1)]$$
$$= \frac{33.33 \times 61.6 \times 10^3 \times 10^3}{33.33 \times 10^3 + 61.6 \times 10^3}$$
$$= \frac{2053.12 \times 10^3}{94.93}$$
$$= 21.62\ k\ \Omega$$

A.C load resistance

$$r_2 = R_c \| R_L$$

$$= 10k \| 3k$$
$$= \frac{10 \times 3 \times 10^6}{13 \times 10^3} = \frac{30}{13} \times 10^3 = 2.3\ k\Omega$$
$$A_v = \frac{r_L}{r_E + \gamma_e^1} = \frac{2307}{1 \times 10^3 + 27} = 2.246$$

Overall voltage gain

W.K.T the ratio of base to source voltage

$$\frac{V_{in}}{V_s} = \frac{R_{iS}}{R_S + R_{iS}} = \frac{21.62 \times 10^3}{100 + 21.62 \times 10^3} = \frac{21.62 \times 10^3}{21720} = 0.99$$

$$\therefore over\ all\ voltage\ gain$$

$$A_{vs} = A_V \times \frac{V_{in}}{V_s} = 2.246 \times 0.99 = 2.235$$

Output voltage

$$V_O = A_{VS} \times V_S = 2.235 \times 10\ mV$$
$$V_O = 22.35\ mV$$

7. An NPN common emitter amplifier circuit has the following parameters: h_{fe}=50, h_{ie}=1KΩ and R_c=3KΩ. Find the voltage gain of the amplifier. (April/May 2019)

$$A_V = \frac{A_I R_L}{R_i}; \qquad A_I = -h_{fe}; \qquad R_i = h_{ie}; R_L = R_C;$$

$$A_V = \frac{-50\ X\ 3\ X\ 10^3}{1\ X\ 10^3}; \qquad A_I = -50; \qquad R_i = 1K; R_L = 3K;$$

$$\boldsymbol{A_V = -150}$$

8. A common emitter amplifier has an input resistance 2.5 kΩ and voltage gain of 200.If the input signal voltage is 5mV. Find the base current of the amplifier. (May 2017) (Nov/Dec 2017)

W.K.T

i_b-base current, R_i=2.5 kΩ, V_s=5mV

$2.5X10^{-3} = \frac{V_s}{i_b} = 5x10^{-3}/i_b \therefore i_b = 2 \times 10^{-6}\ A = 2\mu A$

9. For a certain D-MOSFET, I_{DSS}=10 mA and $V_{GS(off)}$= -8 V. check if it is an n-channel or p-channel device? Justify your answer. (Nov/Dec 2018)

Given that,

For a D-MOSFET,

Saturation currents, I_{DSS}=10 Ma

Gate to source cut-off voltage, $V_{GS\ (off)}$= -8V

Since the D-MOSFET has negative $V_{GS\ (off)}$. The device is n-channel D-MOSFET.

Additional Important question and answers:

1. Derive the expression for current gain, input impedance and voltage gain of a CE transistor Amplifier. (Nov/Dec 2016) (Apr/May 2018)

The ac equivalent circuit can be obtained by replacing all the capacitors and voltage sources by a short circuit.

Characteristics of CE amplifier:

A. Without Emitter Resistor

(1) It has good voltage gain with phase inversion i.e., the output voltage is 180° out of phase with input.
(2) It also has good current gain, power gain and relatively high input and output impedance.

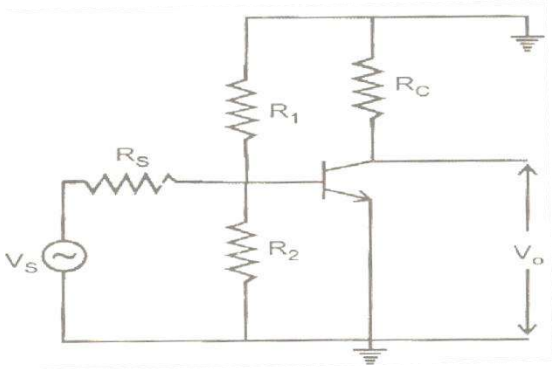


Fig. ac equivalent circuit of CE amplifier

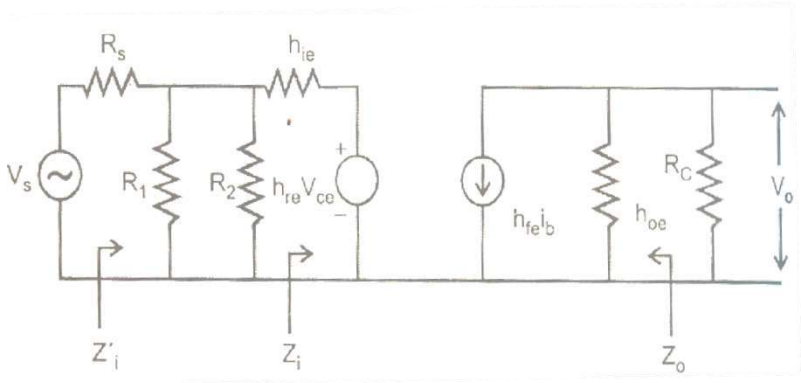


Fig. h-parameter model of CE amplifier

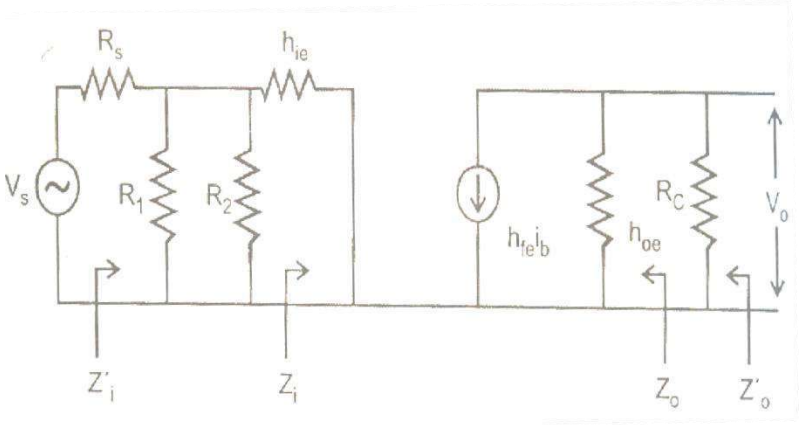
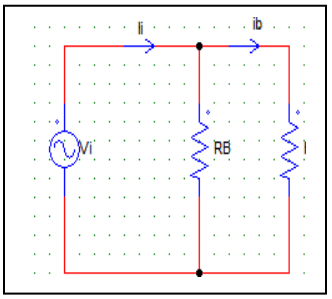


Fig Approximate hybrid model of CE amplifier

Assume $h_{re}=0$,

The input impedance: h_{ie} seen to be in series with $h_{re}V_0$.For CE circuit, h_{re} is normally a very small quantity. So that the voltage $h_{re}V_0$ fed back from the output to the input circuit is much smaller than the voltage drop across h_{ie}.

$$Z_i' = R_B \| h_{ie} \qquad \text{where } R_B = R_1 \| R_2$$



The output impedance: The output voltage variation have liitle effect upon the input of CE circuit, only the output half of the circuit need to be considered in determining the output impedance.

$$Z_0' = R_C \frac{1}{h_{oe}}$$

The voltage gain: $A_V = V_0 / V_i$

W.K.T $\quad V_0 = -i_c R_c \qquad V_i = i_b h_{ie}$

Where $h_{re} V_0$ is assumed short circuited.

$$i_c = h_{fe}\, i_b$$

$$A_V = -(h_{fe} R_C) / h_{ie}$$

Current Gain:

$$A_I = I_0 / I_i = i_c / I_i$$

$$= \frac{-ic}{ib} \cdot \frac{ib}{Ii} = -h_{fe} \frac{ib}{Ii} \qquad \frac{ib}{Ii} = R_B / (h_{ie} + R_B)$$

$$= -h_{fe} R_B / (h_{ie} + R_B)$$

B. With emitter resistor:

A common emitter amplifier with emitter resistor Re provides feedback and voltage gain stabilized in a CE amplifier But it reduces the gain.

To obtain h-parameter model of the circuit, we replace the transistor by its h-parameter model.

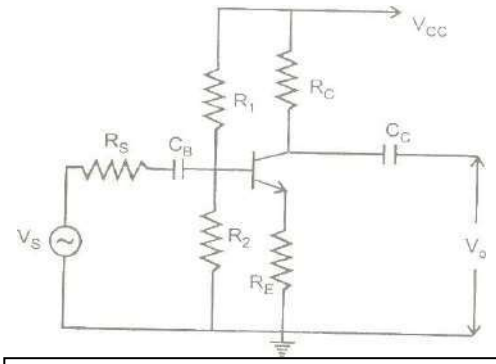


Fig. CE amplifier with Emitter resistor

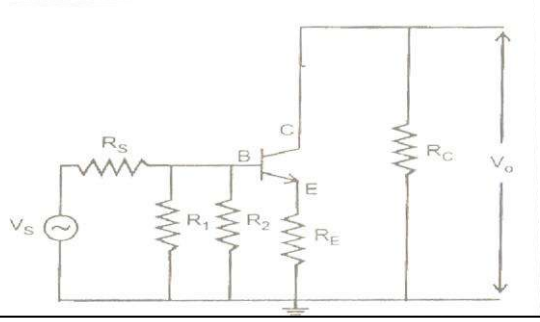


Fig. AC equivalent circuit of CE amplifier with Emitter resistor

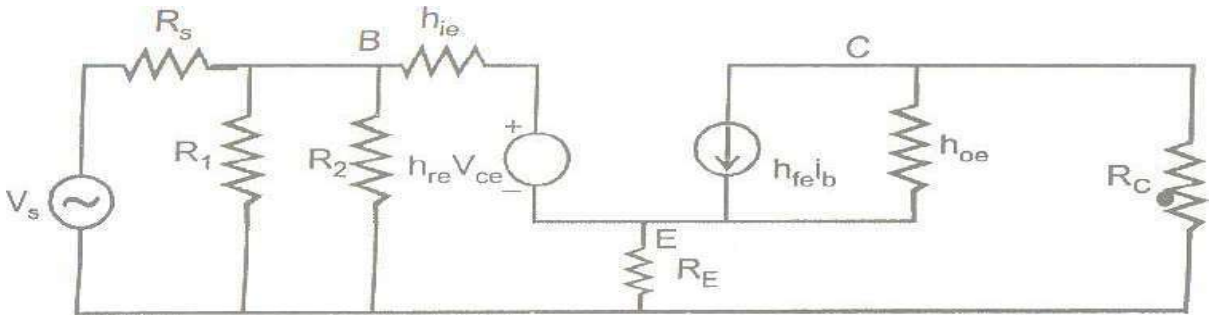


Fig .h-parameter model of a CE amplifier with emitter resistor

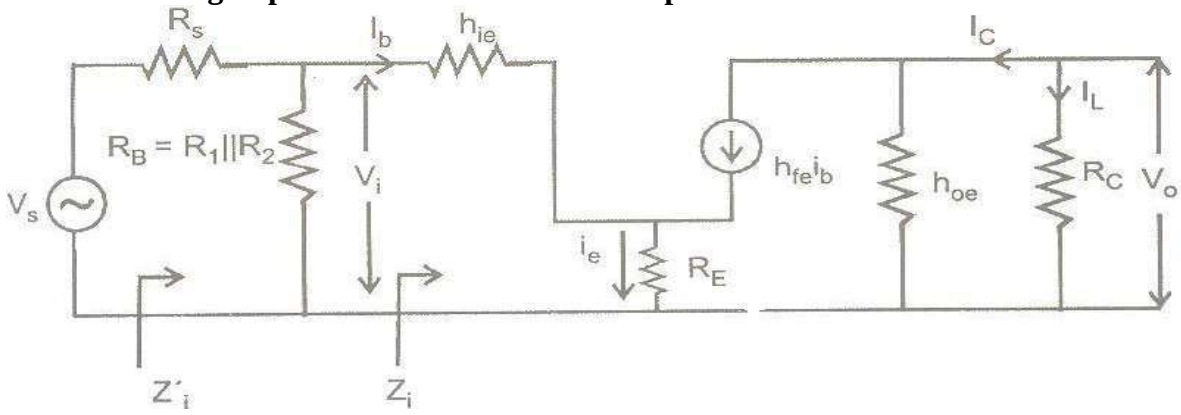


Fig .Approximate Model

Assuming h_{re} is very low, **The input impedance**

$Z_i' = R_B \| Zi$

$Z_i = V_i / I_i = V_i / i_b$ ----------1

$V_i = h_{ie}\, i_b + i_e\, R_E$ W.K.T ($i_e = i_b + i_c$)

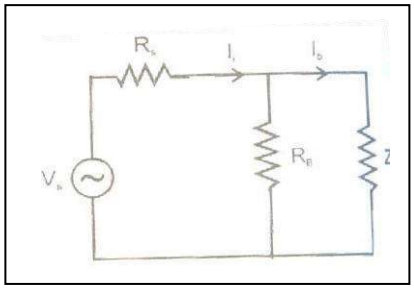
$i_e = i_b + h_{fe}\, i_b = (1+h_{fe}) i_b$ ----------2

sub eq(2) in eq(1), $V_i = i_b (h_{ie} + (1+h_{fe}) R_E)$

$Z_i = V_i / i_b = h_{ie} + (1+ h_{fe}) R_E$ -------- 3

$Z_i = R_B \| Zi$

$= R_b \| (h_{ie} + (1+h_{fe}) R_E)$---------- 4



Voltage Gain: $A_v = V_0 / V_i$ ----------5

$Vo = I_L R_C$

$= - i_c R_c$ where($i_c = h_{fe}\, i_b$)

$= -h_{fe}\, i_b R_c$

$V_i = I_i Z_i$

$= i_b (h_{ie} + (1+h_{fe}) R_E)$ ----------6

Sub eq(6) and eq(6) in eq(4)

$A_V = V_0 / V_i = - h_{fe} R_C\, i_b / (h_{ie} + (1+h_{fe}) R_E)\, i_b$

$= - h_{fe} R_C / h_{ie} (1+h_{fe}) R_E$----------7

Since $(1+h_{fe})R_E >> h_{ie}$ $A_v = - h_{fe} Rc / (1+h_{fe})R_E$ ----------8

Since $h_{fe} >> 1$ $A_v = - R_C / R_E$ ---------- 9

Output impedance: $Z_0 = R_C$---------- 10

Current gain: The current gain is defined as the ratio of output current to input current

$A_I = I_0 / I_i = I_0 / i_b \cdot i_b / I_i$

$I_0 = - i_c$

$A_I = - h_{fe} \ i_b / I_i$ 11

using voltage divider rule, $I_b / I_i = R_B / R_B + Z_i$

$A_I = - h_{fe} R_B / R_B + Z_i$----------12

Application:

It is used as voltage amplifier, among the three basic amplifier configuration CE amplifier most frequently used.

2. Derive the expression for current gain, input impedance and voltage gain of a CC transistor Amplifier.

This circuit is also known as emitter follower amplifier because its voltage gain is close to unity. Hence a change in base voltage appears as an equal change across the load.

Characteristics of CC amplifier:

(1) CC amplifier provide current gain and power gain. but no voltage gain.

(2) It has high input impedance and very low output impedance.

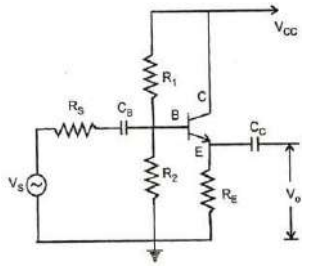


Fig . Common collector amplifier

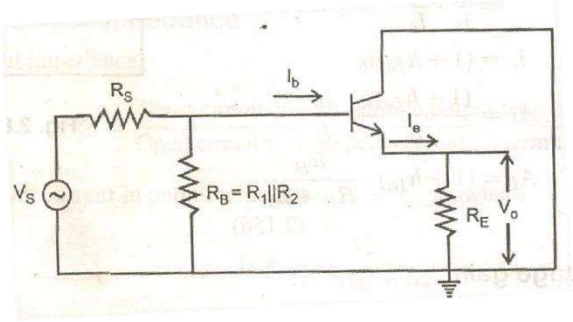


Fig . ac equivalent of CC amplifier

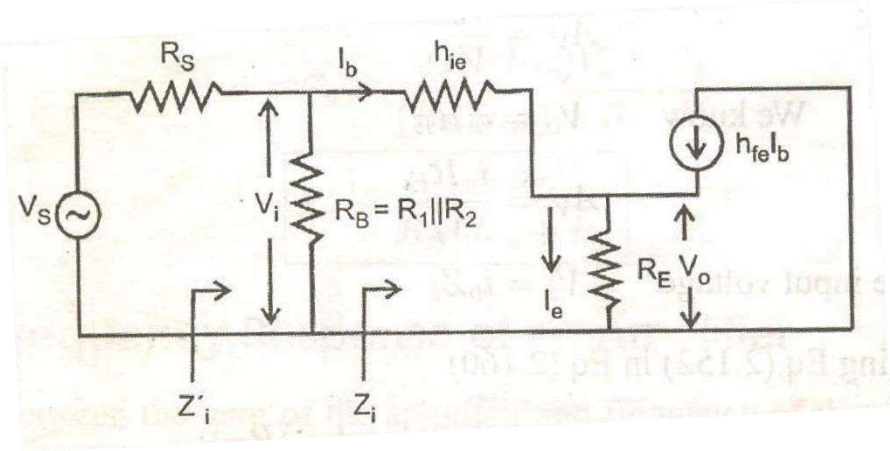


Fig .h-parameter model of a CC amplifier

The input impedance: $Z_i' = Zi \ \| \ R_B$----------1

$Z_i = V_i / i_b$

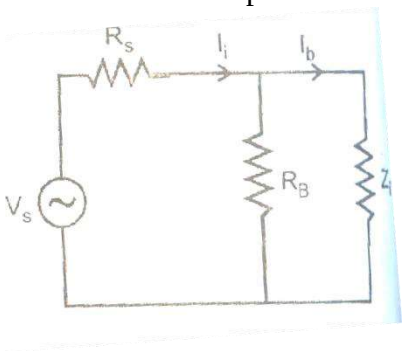
$V_i = h_{ie}\, i_b + I_e\, R_E$ -------2 W.K.T $i_e = (1+h_{fe})i_b$

sub eq(2) in eq(1), $V_i = i_b(h_{ie} + (1+h_{fe})\, R_E)$

$Z_i = V_i / i_b = h_{ie} + (1+ h_{fe})\, R_E$ ---------3

$Z_i' = R_B \| Z_i$

Current gain: The current gain is defined as the ratio of output current to input current



$A_I = i_e / I_i = I_e / i_b \,.\, i_b / I_i$ W.K.T $i_e = (1+h_{fe})i_b$

$A_I = -(1+h_{fe})i_b / i_b \,.\, i_b / I_i$

$A_I = -(1+h_{fe}).R_B / R_B + Z_i.$

Voltage Gain: $A_v = V_0 / V_i$ ---------- 4

$Vo = i_e R_E$ 5

$A_v = - i_e R_E / V_i$

The input voltage $V_i = i_b Z_i$ ----------6

Sub eq(3) in eq(6)

$= i_b (h_{ie} + (1+h_{fe}) R_E$ ----------7

$A_V = R_E i_e / (h_{ie} + (1+h_{fe}) R_E)\, i_b$ W.K.T $i_e = (1+h_{fe})i_b$

$= - (1+h_{fe}) R_E / h_{ie} + (1+h_{fe}) R_E$

$= h_{ie} + (1+h_{fe}) R_E - h_{ie} / h_{ie} + (1+h_{fe}) R_E$

$= 1 - \frac{hie}{h_{ie} + (1+h_{fe})\, R_E}$ ----------8

Since $(1+h_{fe})R_E >> h_{ie}$ and $h_{fe} >> 1$ $A_v = 1 - \frac{h_{ie}}{h_{fe} R_E}$ ---------- 9

Output impedance: $Z_0 = \frac{Short circit current through output terminal}{open\ circuit\ voltage\ between\ output\ terminals}$

Short circuit current through output terminal $i_b = V_s / h_{ie} \| R_B + R_S$ ---------- 10

Open circuit voltage between output terminals = V_s

$Z_0 = \frac{1+h_{fe}}{R_E \| h_{ie} + R_S}$ ---------- 11

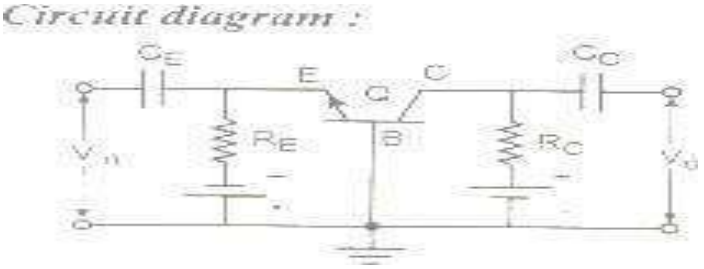
Application:

(1) The voltage gain of emitter follower as unity, thus it is used as buffer amplifier.
(2) It is used as impedance matching network.

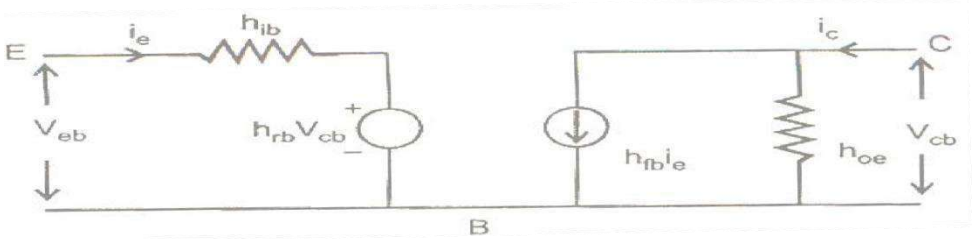
3. Derive the expression for current gain, input impedance and voltage gain of a CB transistor Amplifier. (May/June2016)

In this circuit only a fraction of output voltage is feedback to input thus h_{re} is very small. Therefore $h_{rb}V_0$ can be neglected when deriving CB gain and impedance.

Characteristics of CB amplifier:



(1) This CB circuit provides voltage gain and power gain but no current gain.
(2) It has high output impedance and very low input impedance thus it is unsuitable for most voltage amplification.



a. Input impedance: After neglecting $h_{rb}V_0$, The Z_e is given by,

Apply KVL , $V_i = I_e h_{ib} + I_e R_B - I_e R_B = I_e h_{ib} + I_e R_B - I_E h_{fb} R_B$

$I_C = I_e h_{fb} = I_e [h_{ib} + R_B - h_{fb} R_B]$ ---------- 1

$Z_e = V_i / I_e = h_{ib} + R_B(1 - h_{fb})$ ---------- 2

The actual impedance of the circuit is given by

$Z_i = Z_e \parallel R_e$ ---------- 3

b. Output impedance: The output has very less impact on the input hence the output impedance can be taken as $Z_e \cong 1 / h_{ob}$

The actual output impedance is given by, $Z_0 = R_C \parallel Z_C \cong R_C$

R_C is usually much smaller than $1/ h_{ob}$, soothe circuit impedance is approximately equal to R_C.

c. Voltage Gain: it is given by $A_v = V_0 / V_i$ ---------- 4

$V_0 = I_C (R_C \parallel R_L)$ ---------- 5

$V_i = I_e h_{ib} + I_e R_B - I_E h_{fb} R_B = I_e [h_{ib} + R_B(1 - h_{fb})]$

$A_V = I_C (R_C \parallel R_L) / I_e [h_{ib} + R_B(1 - h_{fb})]$ ---------- 6

$A_V = h_{fb} (R_C \parallel R_L) / h_{ib} + R_B(1 - h_{fb})$ ---------- 7

d. Current gain: The transfer current gain of the device is given by $h_{fc} = I_C / I_e$ ---------- 8

The signal current is divided between R_E and Z_e, and the collector current divides between R_C and R_L ,giving a lower value of current gain.

$I_L = I_C R_E / R_E + R_L$

$= h_{fc} I_e R_E / R_E + R_L$ but $I_e = I_S R_B / R_B + Z_e$

$A_i = I_L / I_S = h_{fc} R_E R_B / (R_B + Z_e)(R_C + R_L)$ ---------- 9

e. Power Gain:

The Power gain is given by $A_{PT} = A_V * h_{fb}$ ---------- 10

Where A_i is significantly different from h_{fb} $A_p = A_V * A_i$ --------- 11

f. Application:

It is used for very high frequency voltage amplifier.

EC8353-ELECTRON DEVICES AND CIRCUITS

UNIT-IV MULTISTAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIER

PART-A

BIMOS cascade amplifier, Differential amplifier

1. **What is a differential amplifier?**
   An amplifier, which is designed to give the difference between two input signals, is called the differential amplifier.

2. **What is the function of a differential amplifier?**
   The function of a differential amplifier is to amplify the difference of two signal inputs, i.e.,$V_0 = A_D(V_1 - V_2)$, where A_D is the differential gain.

3. **What is the differential-mode voltage gain of a differential amplifier?**

   It is given by $A_d = \frac{1}{2}(A_1 - A_2)$

4. **What are the ideal values of A_d and A_c with reference to the differential amplifier?**
   Ideally, Ac should be zero and A_d should be large, ideally infinite.

5. **What are advantages of differential amplifier?**
   It has high gain and high CMRR.

6. **List some applications of differential amplifiers?**
   Used in IC applications, AGC circuits and phase inverters.

Common mode and Difference mode analysis

7. **Define differential mode signals of a differential amplifier. (Nov/Dec 2018)**
   The differential mode signal is the difference between two input voltages. i.e.,
   $V_d = V_1 - V_2$
   The differential mode input signal is zero when $V_1 = V_2$

8. **When two signals V_1 and V_2 are connected to the two inputs of a difference amplifier, define a difference signal V_d and common-mode signal V_c**
   The difference signal V_d is defined as the difference of the two signal inputs,
   i.e., $V_d = V_1 - V_2$
   The common-mode signal V_c is defined as the average of the two signals,
   I.e., $V_c = (V_1 + V_2)$

9. **What is the common-mode gain A_C in terms of A_1 and A_2?**
   It is given by $A_c = A_1 + A_2$

10. **Define CMRR what its ideal value How to improve it. (Nov/Dec2015), (May/ June2016)(May 2017)**
    The common-mode rejection ratio (CMRR) of a differential amplifier is defined as the ratio of the differential-mode gain to common-mode gain.
    $\text{CMRR} = \frac{|A_d|}{|A_c|}$
    Ideal value of is Infinite.
    The improve CMRR the following circuits are used
    i) Current mirror circuit ii) Temperature compensation. iii) Differential amplifier with constant current bias.

11. **Express CMRR in dB.**

    CMRR (dB)=$20\log A_d - 20\log A_c$.

Single tuned amplifiers

12. What is meant by tuned amplifiers? (A/M 2010)

Tuned amplifiers are amplifiers that are designed to reject a certain range of frequencies below a lower cut off frequency ω_L and above a upper cut off frequency ω_H and allows only a narrow band of frequencies.

13. Classify tuned amplifiers.

1. Single tuned amplifier.
2. Double tuned amplifier.
3. Synchronously tuned amplifier.
4. Stagger tuned amplifier.

14. What is the other name for tuned amplifier?

Tuned amplifiers used for amplifying narrow band of frequencies hence it is also known as "narrow band amplifier" or "Band pass amplifier.

15. What is the application of tuned amplifiers?(N/D 2007)

The application of tuned amplifiers to obtain a desired frequency and rejecting all other frequency in
(i). Radio and T .V broadcasting as tuning circuit.
(ii). Wireless communication system.

16. What are the advantages of tuned circuit?

- High selectivity
- Smaller collector supply voltage
- Small power gain.

Neutralization methods

17. What is meant by neutralization? (N/D 2012)

It is the process by which feedback can be cancelled by introducing a current that is equal in magnitude but 180^o out of phase with the feedback signal at the input of the active device. The two signals will cancel and the effect of feedback will be eliminated. This technique is termed as neutralization.

18. What is the need for neutralization (Nov/Dec2015)

In turn RF amplifier at high frequency centered around a radio frequency the inter junction capacitance between base and collector C_{bc} of the transistor becomes dominant i.e. its reactance become low enough to be considered. As reactance of C_{bc} at RF is low enough it provides the feedback path from collector to base. If this feedback is positive the circuit is converted to an unstable one generating its own oscillations and can stop working as an amplifier. In order to prevent oscillations without redacting the stage gain neutralization is used in tuned amplifiers.

19. State the merits of using push-pull configuration. (May 2018) (Apr/May 2018)

- Efficiency is high. (78.5%)
- Figure of merit is high.
- Distortion is less
- Ripple present in the output due to power supply is multiplied.

20. List the disadvantages of push-pull amplifier.

- Two identical transistors are needed.
- Centre taping is required in transformer.
- Transformers used are bulky and expensive.
- If the parameters of the two transistors differ, there will be unequal amplification of the two halves of signal which introduces more distortion.

21. How do you bias class-A operation?

In class A mode of means, the output current flows throughout the entire period of input cycle and the Q-point is chosen at the midpoint of A.C load line and biased.

22. Give two applications of class-C power amplifier.

- Used in radio and TV transmitters.
- Used to amplify the high frequency signals.
- Tuned amplifiers.

23. What is multistage amplifier?

Multistage cascading permits several single-stage amplifiers to be combined into one circuit. Multistage cascading can produce an amplifier with large gain, high input resistance and low output resistance. The small-signal behavior of a multistage amplifier can be modeled by cascading an appropriate number of small-signal two-port amplifier models.

24. A multistage amplifier employs five stages each of which has a power gain of 30. What is the total gain of the amplifier in dB. (Nov/Dec 2018)

Given that,

The power gain of each stage in a five-stage amplifier is,

$A_{Vn} = 30$, n = 1 to 5

Total gain, A_V = ?

The overall gain, A_V of an n-stage amplifier is given as,

$A_V = A_{V1} \text{ X } A_{V2} \text{ X } A_{V3} \text{ X } \ldots\ldots A_{Vn}$

Here, n = 5

$A_V = A_{V1} \text{ X } A_{V2} \text{ X } A_{V3} \text{ X } A_{V4} \text{ X } A_{V5}$

$= 30 \text{ X } 30 \text{ X } 30 \text{ X } 30 \text{ X } 30$

$A_V = 243 \text{ X } 10^5$

Total gain, $A_V = 243 \text{ X } 10^5$

A_V = 147.71 dB

25. CMRR of an amplifier is 100dB, calculate common mode gain if the differential gain is 1000(Nov/Dec 2016)

CMRR=A_d/A_C, 100=1000/A_c, A_c=10

26. Define conversion efficiency of power amplifier? (Nov/Dec 2016)

It is a measure of an active device in converting the d.c power of the supply into the ac power delivered to load. It is also referred theoretical efficiency or collector circuit efficiency

- Mathematically, collector circuit efficiency,

$$\eta_c = \frac{\text{a.c.power delivered to the load}}{\text{power supplied by the d.c.source to output circuit}}$$

27. A tuned circuit has a resonant frequency of 1600 KHz and a bandwidth of 10 KHz. What is the value of its Q factor? (May 2017)

$$Q_{\text{factor}} = \frac{\text{resonant frequency}}{\text{bandwidth}} = \frac{1600}{10} = 160$$

28. What is thermal runaway? (Nov/Dec 2017)

Thermal runaway occurs in situations where an increase in temperature changes the conditions in a way that causes a further increase in temperature, often leading to a destructive result. It is a kind of uncontrolled positive feedback.

29. Compare the characteristics of CE, CB, CC amplifiers (May/June 2016) (Nov/Dec 2017)

30.

S.No	Common Emitter Amplifier	Common Base Amplifier	Common Collector Amplifier
1	In this case emitter is common to both input and output	In this case base is common to both input and output	In this case collector is common to both input and output
2	180^0 phase shift occurs	No phase shift occurs	No phase shift occurs
3	Input impedance: Low	Very low	Very high
4	Output impedance: High	Very high	Low

31. A multistage amplifier employs five stages each of which has a power gain of 30. What is the total gain of the amplifier in dB? (Nov/Dec 2017)

Solution:

Absolute gain of each stage = 30 No. of stages = 5

Power gain of one stage in dB = 10 log 10 30 = 14.77

∴ Total power gain = 5 ×14.77 = 73.85 dB

32. What is cross over distortion? (Apr/May 2018)

Crossover distortion is the term given to a type of **distortion** that occurs in push-pull class AB or class B amplifiers. It happens during the time that one side of the output stage shuts off, and the other turns **on**.

33. Determine the input impedance of a differential amplifier (emitter coupled) with R_B=3.9 KΩ and Z_B=2.4 KΩ. (April/May 2019)

$$Z_i = R_B \| Z_B$$

$$Z_i = \frac{R_B \times Z_B}{R_B + Z_B}$$

$$Z_i = \frac{3.9 \times 10^3 \times 2.4 \times 10^3}{3.9 \times 10^3 + 2.4 \times 10^3}$$

The input impedance of a differential amplifier (emitter coupled), $Z_i = 1.49\ \Omega$

34. A single tuned amplifier provides a band width of 10KHz at a frequency of 1MHz. Find the circuit Q. (April/May 2019)

$$f_O = BW \times Q_O$$

$$Q_O = \frac{f_O}{BW}$$

$$Q_O = \frac{1 \times 10^6}{10 \times 10^3}$$

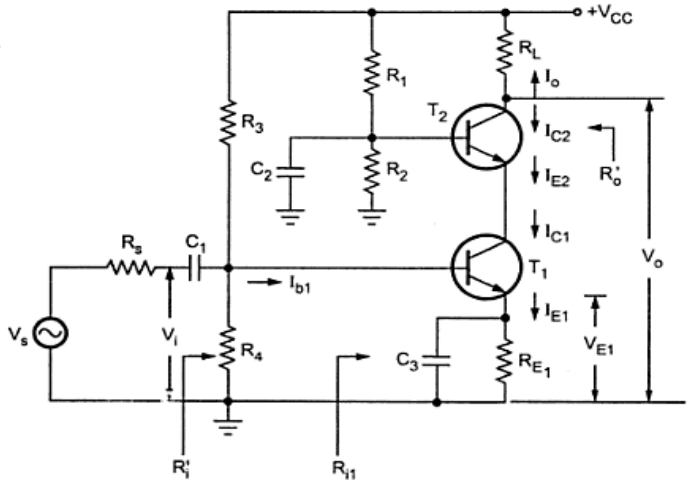
$$Q_O = 100$$

PART-B

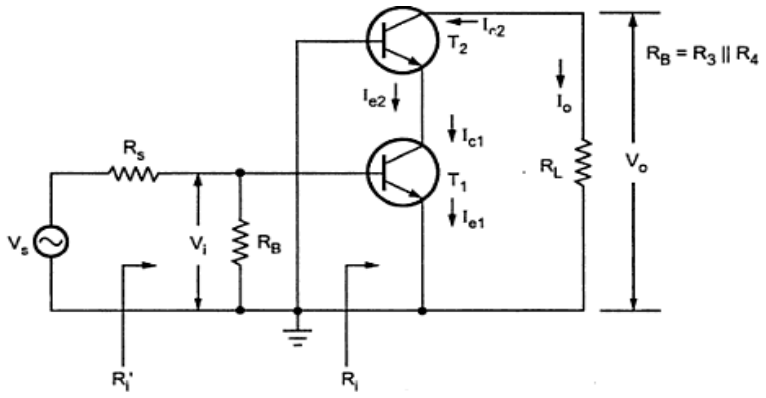
BIMOS cascade amplifier, Differential amplifier

1. Explain the operation of cascade amplifier.

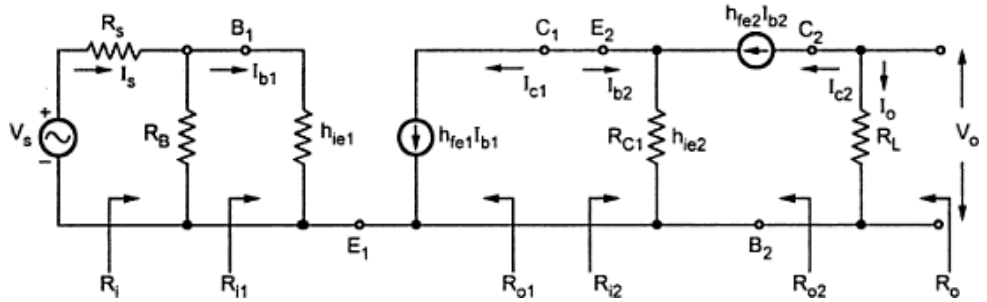
- The cascade amplifier consists of a common emitter amplifier stage in series with a common base amplifier stage.
- It solves the low impedance problem of a common base circuit.
- It gives the high input impedance of a CE amplifier as well as good voltage gain and high frequency response of CB circuit.
- For DC bias $I_{C1} = I_{E1}$, $I_{E2} = I_{C1}$



- Ac equivalent circuit for cascade amplifier is drawn by shorting dc supply and capacitors.



- A simplified h parameter equivalent circuits for cascade amplifier is drawn by replacing transistor with their equivalents



Analysis of second stage (CB)

a) Current gain (A_{i2})

$$A_{i2} = \frac{h_{fe}}{1+h_{fe}}$$

b) Input resistance (R_{i2})

$$R_{i2} = \frac{h_{ie}}{1+h_{fe}}$$

c) Voltage gain (A_{v2})

$$A_{v2} = \frac{A_{i2} R_{L2}}{R_{i2}}$$

Analysis of first stage (CE)

a) Current gain (A_{i1})

$$A_{i1} = -hfe$$

b) Input resistance (R_{i1})

$$R_{i1} = hie$$

c) Voltage gain (A_{v1})

$$A_{v1} = \frac{A_{i1} R_{L1}}{R_{i1}}$$

2. BIMOS cascade amplifier (or coupling amplifier):

- To get faithful amplification, amplifier should have desired voltage gain, current gain and it should match its input impedance with the connected source impedance. Similarly, output impedance must match with the load impedance.
- Normally, these requirements of the amplifier cannot be obtained in a single stage amplifier, which is due to the limitation of the parameters of transistor or FET or whatever device used.
- Under these situations, more than one amplifier stages are cascaded such that input and output stages provide impedance matching requirements with some amplification and remaining middle stages provide most of the amplification.

Therefore, for making cascading following reasons,

- The amplification of a single stage amplifier is not sufficient.
- When input and output impedance is not of the correct magnitude, for a particular application two or more amplifier stages are connected in cascaded fashion or coupling. This is known as multistage amplifier.

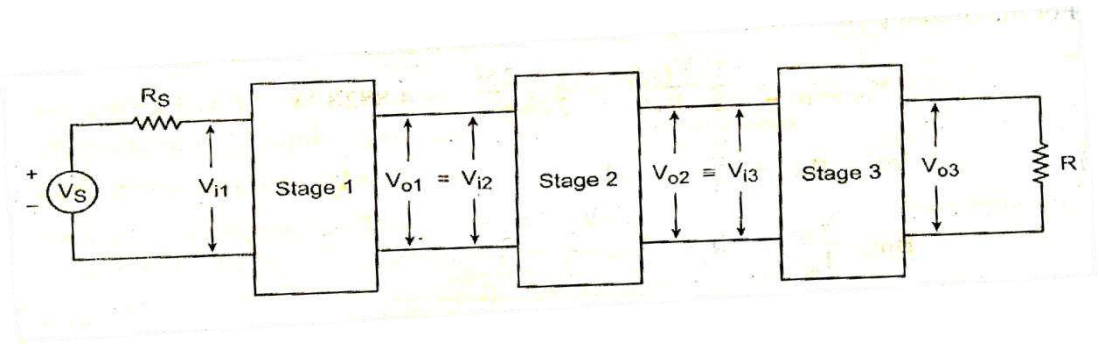


Figure: Block diagram of cascade amplifier

From the above figure, $V_{i1}, V_{i2}, V_{i3}$the input of first, second and third stages and V_{o1}, V_{o2}, V_{o3} are the output of the three stages. Therefore, $\frac{V_{o3}}{V_{i1}}$ is the overall voltage gain of 3 stage amplifier which is given as follows:

$$A_v = \frac{V_{o3}}{V_{i1}} \quad \ldots\ldots\ldots\ldots\ldots (1)$$

$$= \frac{V_{o3}}{V_{i3}} \cdot \frac{V_{i3}}{V_{i2}} \cdot \frac{V_{i2}}{V_{i1}} \quad \ldots\ldots\ldots\ldots\ldots (2)$$

From the figure, we know that,

$V_{o1} = V_{i2}$; $V_{o2} = V_{i3}$; put this into the above equation, we get

$$A_v = \frac{V_{o3}}{V_{i3}} \cdot \frac{V_{o2}}{V_{i2}} \cdot \frac{V_{o1}}{V_{i1}} \quad \ldots\ldots\ldots\ldots\ldots (3)$$

Already we know that,

$$\text{Voltage gain (A)} = \frac{Output\ voltage}{Input\ voltage} = \frac{Vo}{V_i}$$

$$A_v = A_{v3} \cdot A_{v2} \cdot A_{v1} \quad \ldots\ldots\ldots\ldots (4)$$

Therefore, the voltage gain of multistage amplifier is the product of individual gains of the each stage. Then the multistage amplifier is shown below.

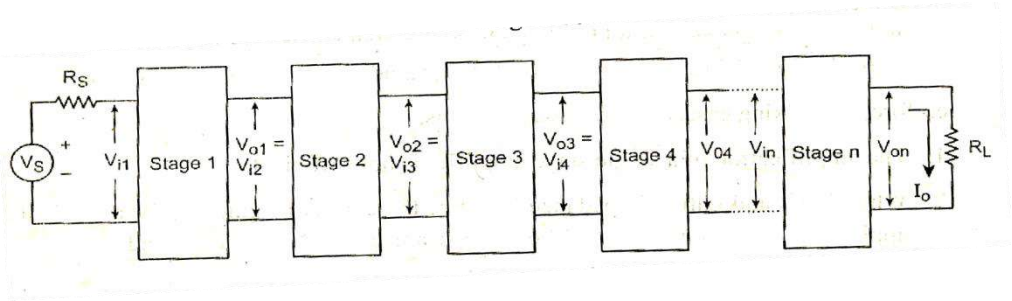


Figure: Multistage amplifier

Voltage gain: The resultant voltage gain of the multistage amplifier is the product of the voltage gains of the various stages or individual stages.

(i.e.,) $A_v == A_{v1} \cdot A_{v2} \cdot A_{v3} \cdot A_{v4} \ldots\ldots\ldots A_{vn}$ ..... (5)

= Then, Voltage gain of n^{th} stage is as follows:

$$A_{v1} = \frac{A_{in} R_{ln}}{R_{in}} \ldots\ldots\ldots\ldots (6)$$

Where, R_{ln} = Effective load resistance of n^{th} stage.

R_{in}= Input resistance / impedance of 1^{st} stage.

Selection of cascading amplifier configuration:

From the above discussion, the multistage amplifier is divided into three parts:

i) Input stage
ii) Middle stage and
iii) Output stage.

- In the above, the input stage must be designed with input impedance matches with the source impedance.
- Similarly, the output stage designed must be the output impedance matches with the load impedance.
- Then, middle stage is designed with our desired voltage and current gain.

Anyhow, to select the cascading configuration, the following considerations are important since we normally use these three configurations.

Common mode and Difference mode analysis

3. Draw the circuit diagram and explain the working of a differential amplifier using FET. Derive the expression for differential mode gain and common mode gain.(May 2017)

- Normally, analysis in amplifier depends on both AC and DC analysis.
- In the above two, the d.c signals determines the operating values for the transistors and used as biasing.
- Similarly, a.c signals are used as input signals, which determine the output of the differential amplifier.
- The dual input, balanced output differential amplifier is also called **Symmetrical Differential Amplifier.**

❖ **DC ANALYSIS:**

- DC analysis means using D.c voltage as biasing voltage and keeping it constant (to obtain suitable operating point).

❖ **AC ANALYSIS:**

- For performing AC analysis, we must apply AC input signals as an input. So, we can calculate the following:
  A. Differential mode gain (A_d).
  B. Common mode gain (A_c).
  C. Input resistance (R_i).
  D. Output resistance (R_o).

  The above can be obtained by using h-parameters.

A. Differential gain (A_d)

- To obtain the Differential mode gain, the two input signals must be different from each other.
- Here, we take the two a.c input signals as equal in magnitude but having 180° phase shift between them.
- Then, the magnitude of each a.c input voltage V_{S1} and $V_{S2}$is $\frac{V_S}{2}$.
- For the a.c purposes, emitter terminal can be grounded which is shown in figure below with small signal analysis.

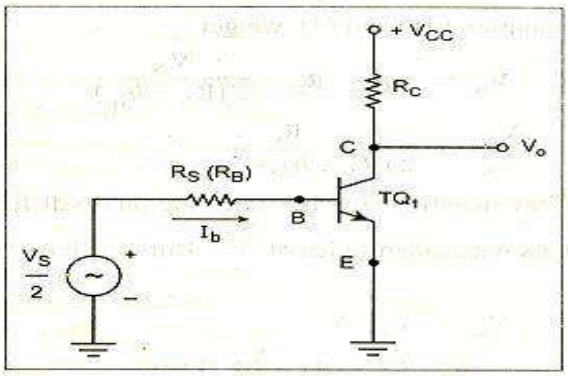
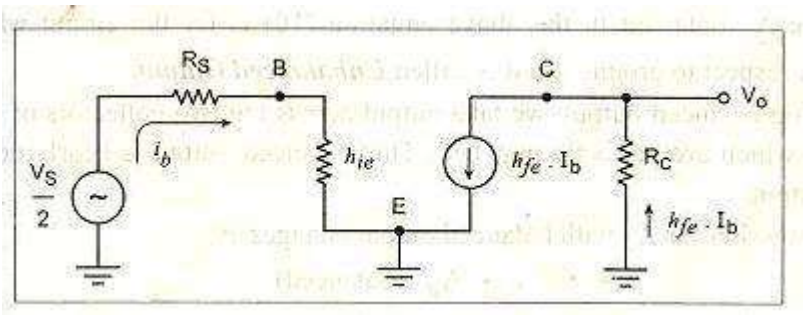


Figure (1): AC Equivalent for differential operation (half circuit concept)

- The circuit which can be analyzed by considering only one transistor is called Half circuit concept of analysis.



Figure(2): Approximate hybrid model

- For obtaining the differential mode gain (A_d) from the above hybrid model, we have to apply the Kirchhoff's voltage law in input side,

$$\frac{V_S}{2} = i_b R_S + i_b h_{ie} \quad \text{……..(1)}$$

$$\frac{V_S}{2} = i_b(R_S + h_{ie}) \quad \text{……..(2)}$$

$$i_b = \frac{V_S}{2(R_S + h_{ie})} \quad \text{……...(3)}$$

- Similarly, applying the Kirchhoff's voltage law to output loop, we get

$$V_o = - I_b h_{fe} . R_C \text{ ..... (4)}$$

- Put the value of I_b in equation (4) from (3), we get,

$$V_o = \frac{-h_{fe} V_S R_C}{2(R_S + h_{ie})} \text{ … … . . (5)}$$

- Then, $\frac{V_o}{V_S} = \frac{-h_{Fe} . R_C}{2(R_S + h_{ie})}$ ……(6)
- Negative sign indicates that 180^0 phase difference between input and output. If the input signals are equal and are out of phase by 180^0, we get
- Differential mode signal $V_d = V_1 - V_2 = (\frac{V_S}{2}) - (-\frac{V_S}{2}) = V_S$ …..(7)

  Where, $V_S$is differential input voltage.

- Differential voltage gain $A_d = \frac{V_o}{V_S}$

$$A_d = \frac{h_{fe} R_C}{2(R_S + h_{ie})} \text{ … … … . (8)}$$

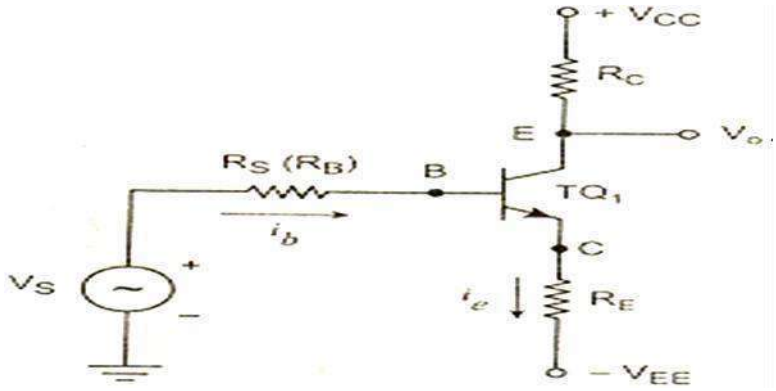
- When the output of differential amplifier is measured with reference to ground, it is called unbalanced output.
- The output across the collectors of Q_1 and Q_2 to be perfectly matched then A_d for balanced output is twice than that of A_d for unbalanced output. Therefore

$$A_d = \frac{h_{fe} R_C}{(R_S + h_{ie})} \text{ … … … … … … . (9)}$$

B. Common mode gain (A_C)

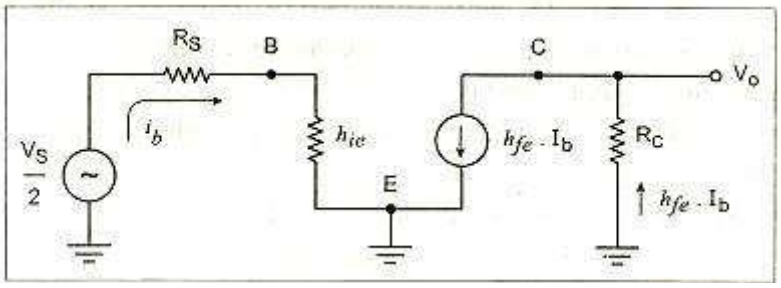
- In common mode, the both transistor's input magnitude and phases are also inphase with each other.
- Let us assume that input signals are having the same magnitude V_S and are in same phase.
- Common mode voltage $V_C = \frac{V_1 + V_2}{2} = \frac{V_S + V_S}{2} = V_S$ ……(10)
- If suppose, the output is expressed as, $V_o = A_C . V_S$ ……(11)
- Common mode gain $A_C = \frac{V_o}{V_S}$ …….(12)
- In this mode, both the emitter current $I_{e1} = I_{e2} = I_e$ of TQ_1, TQ_2 flows through R_E in the same direction, with same magnitude.

- Hence, the total current flowing through R_E is nearly $2I_e$ …..(13)



Figure(1): A.C. Equivalent Circuit for Common Mode Configuration

- Then the approximate hybrid model for the above circuit can be obtained and is used to obtain the A_d.



Figure(2): Approximate Hybrid model

- As the current through R_E is $2I_e$, for simplicity of derivation, we have to assume the I_e and effective emitter resistance as $2R_E$.
- Current through R_C = Load current I_L
- Effective emitter = 2 R_E
- Current through emitter resistance = $I_L + I_b$
- Current through $h_{oe} = (I_L – h_{fe} . I_b)$
- Now, applying Kirchhoff's voltage law to input side,

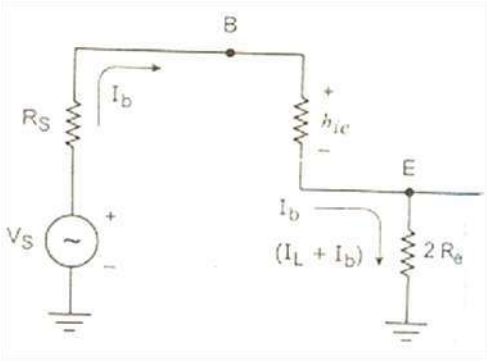


Figure (3): Input side

$-I_b R_S + I_b h_{ie} + 2R_E(I_L + I_b) = - V_S$ ……(14)

$I_b R_S - I_b h_{ie} - 2R_E(I_L + I_b) = V_S$……(15)

While, $V_o = - I_L . R_C$……(15a)

- Negative sign is due to the assumed direction of current. Similarly apply KVL to output side.

$$\frac{-(I_L - h_{Fe}I_b)}{h_{oe}} - 2R_E(I_L + I_b) - I_L R_C = 0 \ldots. (16)$$

$$\frac{-I_L}{h_{oe}} + \frac{h_{Fe}I_b}{h_{oe}} - 2I_L R_E - 2I_b R_E - I_L R_C = 0 \ldots (17)$$

$$I_b\left[\frac{h_{Fe}}{h_{oe}} - 2R_E\right] = I_L\left[\frac{1}{h_{oe}} + 2R_E + R_C\right] \ldots\ldots\ldots (18)$$

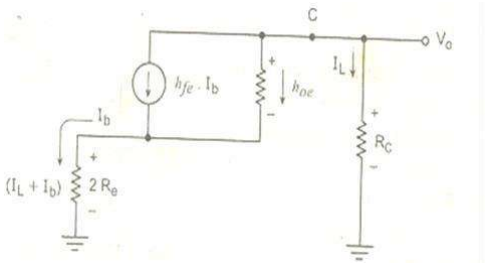


Figure (4): Output side

- Multiplying both sides by h_{oe}, then

$$I_b[h_{fe} - 2R_E h_{oe}] = I_L[\,1 + h_{oe}(2R_E + R_C)] \ldots\ldots\ldots\ldots\ldots (19)$$

$$\frac{I_L}{I_b} = \frac{[h_{fe} - 2R_E h_{oe}]}{[\,1 + h_{oe}(2R_E + R_C)]} \ldots\ldots\ldots (20)$$

$$I_b = \frac{I_L[\,1+h_{oe}(2R_E+R_C)]}{[h_{Fe}-2R_E h_{oe}]} \qquad \ldots\ldots\ldots\ldots (21)$$

- Putting this I_b in equation (15),

$$V_S = \frac{I_L[1 + h_{oe}(2R_E + R_C)][R_S + h_{ie} + 2R_E] + 2R_E}{[h_{fe} - 2R_E h_{oe}]}$$

$$\frac{V_S}{I_L} = \frac{[1 + h_{oe}(2R_E + R_C)][R_S + h_{ie} + 2R_E] + 2R_E}{[h_{fe} - 2R_E h_{oe}]} \ldots (22)$$

- Then, find LCM and adjusting the terms,

$$\frac{V_S}{I_L} = \frac{2R_E(1 + h_{fe}) + R_S(1 + 2R_E h_{oe}) + h_{ie}(1 + 2R_E h_{oe}) + h_{oe}R_C(2R_E + R_S + h_{oe})}{[h_{fe} - 2R_E h_{oe}]}$$

$$\frac{V_S}{I_L} = \frac{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe}) + h_{oe}R_C(2R_E + R_S + h_{oe})}{[h_{fe} - 2R_E h_{oe}]} \ldots . (23)$$

Actually $h_{oe}R_C \ll 1$. Neglecting the terms,

$$\frac{V_S}{I_L} = \frac{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})}{[h_{fe} - 2R_E h_{oe}]} \ldots . . (24)$$

$$I_L = \frac{V_S.\,[h_{fe} - 2R_E h_{oe}]}{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})} \ldots . . (25)$$

Putting this I_L in equation (15a),

$$V_o = -\,I_L \,.\, R_C$$

$$V_o = \frac{-V_S.[h_{Fe}-2R_E h_{oe}]R_C}{2R_E(1+h_{Fe})+(R_S+\,h_{ie})(1+2R_E h_{oe})} \ldots\ldots (26)$$

Hence the common mode gain can be written as,

$$A_C = \frac{V_o}{V_S} = \frac{[2R_E h_{oe} - h_{fe}]R_C}{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})} \ldots\ldots (27)$$

In practice, h_{oe} is neglected, because the expression for A_C can be further modified as,

$$A_C = \frac{-h_{fe}R_C}{R_S + h_{ie} + 2R_E(1 + h_{fe})} \ldots . . (28)$$

The above expression is same whether the output is balanced or unbalanced.

COMMON MODE REJECTION RATIO (CMRR):

$$\text{CMRR} = \left|\frac{A_d}{A_C}\right|$$

From equation (8) and (28),

$$\text{CMRR} = \left|\frac{\frac{h_{Fe}R_C}{2(R_S+h_{ie})}}{\frac{h_{Fe}R_C}{(R_S+h_{ie}+2R_E(1+h_{Fe})}}\right| \ldots\ldots (29)$$

$$\text{CMRR} = \left|\frac{(R_S + h_{ie} + 2R_E(1 + h_{fe})}{2(R_S + h_{ie})}\right| \quad \ldots(30)$$

This is CMRR for dual input balanced output differential amplifier circuit.

For balanced case,

$$\text{CMRR} = \left|\frac{(R_S + h_{ie} + 2R_E(1 + h_{fe})}{(R_S + h_{ie})}\right|$$

For unbalanced case,

$$\text{CMRR} = \left|\frac{(R_S + h_{ie} + 2R_E(1 + h_{fe})}{2(R_S + h_{ie})}\right|$$

C. Input Impedance (R_i):

R_i is defined as the equivalent resistance existing between any one of the input and the ground when other input terminal is grounded.

$$R_i = \frac{V_S}{I_b}$$

Put the V_S and $I_b$from the above discussion, $R_i = 2(R_S + h_{ie})$.

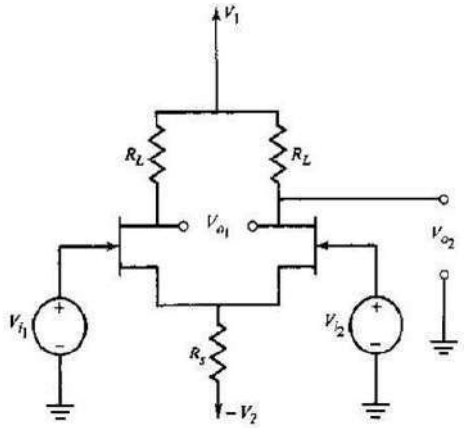
For one transistor and input pair, the resistance is $R_S + h_{ie}$.

Hence for dual input circuit, the total input resistance is $2(R_S + h_{ie})$, as the 2 circuits are perfectly matched.
This input resistance is not dependent on whether output is balanced or unbalanced.

D) OUTPUT IMPEDANCE R_O:

- It is defined as the equivalent resistance between one of the output terminals with respect to ground.
- The resistance between output terminal with respect to ground is R_C.

$R_O = R_C$



Changes to be made for FET is

BJT	FET
Rc	Rd

re= 1

$$A_d = \frac{g_m}{\frac{V0}{V_{in}}} = \frac{R_d}{V_{g_{md}}} = g_{md} R_d$$

4. Draw a differential amplifier and its ac equivalent circuit. *(OR)* **Explain the operation of basic emitter coupled differential amplifier** *(or)* **Explain the function of differential amplifier with neat circuit. (A/M 2010) (M/J 2012)** *(OR)* **Explain the common mode and differential mode operation of the differential amplifier (May/June2016 Nov/Dec-2017, May-2018)** *(OR)*
Explain the working of a single ended input differential amplifier. (Nov/Dec 2018)

❖ **DIFFERENTIAL AMPLIFIER BASIC BLOCK DIAGRAM:**

- The differential amplifier amplifies the difference between two applied input signals V_{in1} and V_{in2} (voltage signals). Hence, it is called as **Difference amplifier.**

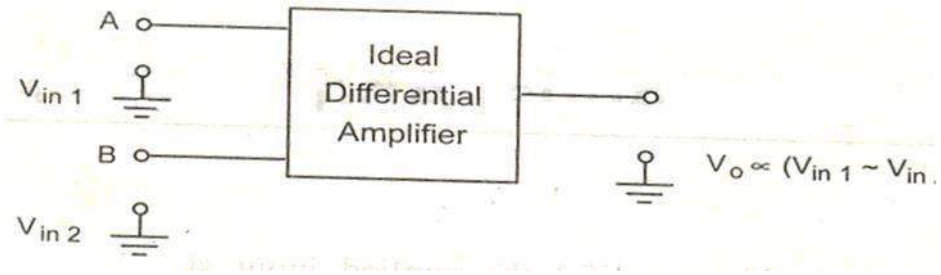


Fig: block diagram of differential amplifier

- In an ideal amplifier, the output voltage V_o is proportional to the difference between the two input signals. Therefore we can write,

$$V_o \alpha (V_{in1} - V_{in2}) \text{ .....(1)}$$

❖ **DIFFERENTIAL GAIN A_d:**

- From the above equation, we can write the differential gain A_d is [Generally gain is nothing but the output parameter (may be voltage, current, etc.) to input parameter].
- Therefore, $V_o = A_d (V_{in1} - V_{in2})$ ..... (2)

  Where A_d = Differential gain constant
- This A_d is thegain with which differential amplifier amplifies the difference between two input signal is called **Differential gain.**
- The difference between the two inputs (V_{in1}~ V_{in2}) is generally called difference voltage and denoted as V_d.
- output foreThere voltage is $V_o = A_d . V_d$.....(3)
- Therefore the differential gain can be expressed as,

$$A_d = \frac{V_o}{V_d} \quad \text{.....(4)}$$

❖ **COMMON MODE GAIN A_c :** If we apply two input voltages which are equal in all the respect to the differential amplifier i.e., $V_1 = V_2$ then, ideally the output voltage V_o is $(V_1 ~ V_2) . A_d$, must be zero.

- In this mode the applied input signals, phase and frequency must be in same.

- But the output voltage of the practical differential amplifier not only depends on the difference voltage but also depends on the average common level of the two inputs.
- Such an average level of the two input signal is called **common mode signal** which is denoted as V_c.

$$V_c = \frac{V_{1+} V_2}{2} \quad \text{.....(5)}$$

- In practical, the differential amplifier produces the output voltage proportional to each common mode signal. The gain which it amplifies the common mode signal to produce the output is called common mode gain of the differential amplifier denoted as A_c.

$$A_c = \frac{V_o}{V_c} \quad \text{.....(6)}$$

- So that total output of any differential amplifier can be expressed as,

$$V_o = A_d . V_d + A_c . V_c \text{.....(7)}$$

❖ COMMON MODE REJECTION RATIO:

- In differential amplifier, if both transistors input the same, then that differential amplifier is called as **common mode differential amplifier.**
- In common mode operation, the output is zero.
- But due to many disturbance in signals, noise signals appear as a common input signal to both the input terminals of the differential amplifier.
- Such a common signal should be rejected by the differential amplifier(CMRR).
- Thus, the ability of a differential amplifier to reject a common mode signal is expressed by a ratio called **common mode rejection ratio.**
- CMRR is defined as the ratio of the differential mode gain (A_d) to common mode voltage gain (A_c).

$$CMRR = \frac{|Ad|}{|A_c|} = \rho \text{..... (8)}$$

- In ideal case the CMRR is infinite, because the common mode gain is nearly or exactly zero. But in practical, it is not infinite.
- But ρ is very large one, since A_d is very large and A_c is very small. The CMRR can be expressed in dB also.

$$CMRR \text{ in dB} = 20 \log \frac{|Ad|}{|A_c|} \text{ dB.....(9)}$$

- The total output voltage is,

$$V_o = A_d . V_d + A_c . V_c \text{.....(10)}$$

Where, V_o = Total output voltage of differential amplifier,

A_d = Differential mode gain of differential amplifier,

A_c = Common mode gain of differential amplifier,

V_d = Differential mode voltage.

- From equation (10), V_o can be written as,

$$V_o = A_d . V_d [1 + \frac{Ac . V_c}{Ad . V_d}] \text{..... (11)}$$

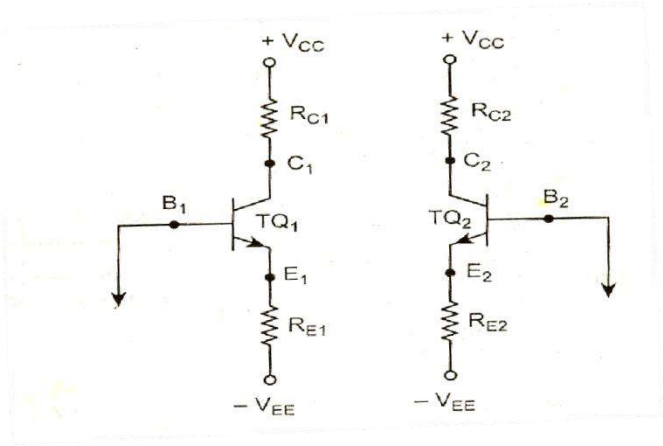
$$V_o = A_d . V_d [1 + \frac{1}{\frac{A_d}{A_c}} . \frac{V_c}{V_d}] \text{... .....(12)}$$

$$V_o = A_d . V_d [1 + \frac{1}{CMRR} . \frac{V_c}{V_d}] \text{..... (13)}$$

- Therefore, from the above equation, the CMRR is practically very large, though both V_c and V_c components are present.
- The output is proportional to the difference in signal only. Then the common mode component is greatly rejected.

❖ EMITTER COUPLED DIFFERENTIAL AMPLIFIER:

- The transistorized differential amplifier is an emitter and emitter follower circuit. So this is called as Emitter coupled differential amplifier.



Figure(1): Emitter biased circuit

- Figure(1) shows the emitter coupled biased circuit. The transistor TQ_1 and TQ_2used in the figure are identical in characteristics and also having exactly matched characteristics.
- Then the two collector resistances R_{C1} and R_{C2} are equal while the two emitter resistances R_{E1} and R_{E2} are also equal.

Therefore $R_{C1} = R_{C2}$ and $R_{E1} = R_{E2}$

- In this the magnitude of V_{CC} and $-V_{EE}$ are also same. Therefore the differential amplifier can be obtained by using such two emitter biased circuits.
- This emitter biased circuit can be obtained by connecting the E_1 of TQ_1 with E_2 of TQ_2.
- Because of this connection the R_{E1} is parallel with R_{E2}.

- The applied input V_{s1} is connected with base of TQ_1 and V_{s2} input is connected with the base of TQ_2.
- Both input voltages in Base is with respect to ground. Then its balanced output is taken in between the respective collector terminals of both transistors (TQ_1 and TQ_2).
- This amplifier is called Emitter coupled Differential Amplifier. In this circuit, the two collector resistanceR_C used are also same.
- Then the dual input differential balanced output differential amplifier is shown below. Because, none of the output terminal is grounded, the output is taken between two output terminals.
- So it is called as Balanced Differential Amplifier and it is shown in figure (2).

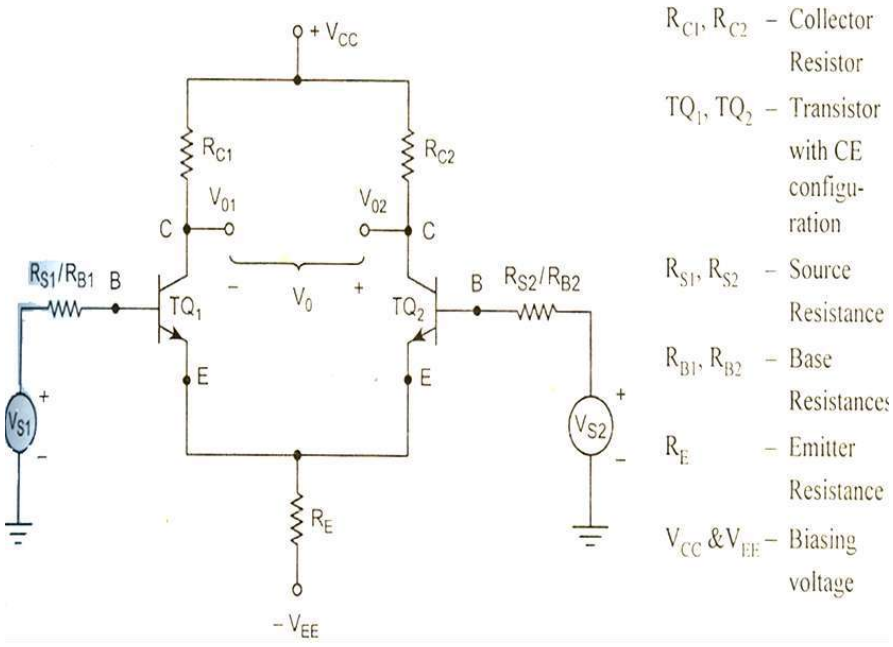


Figure (2): Balanced differential amplifier

- For studying the operation of differential amplifier, the following modes are used. (i) Differential mode, and (ii) Common mode.

i) Differential mode operation:

- In this mode, both inputs are different in either magnitude or phase like 180^o phase. This opposite phase can be obtained from the Center tap Transformer.
- That is assume that the sine wave on the base of TQ_1 is positive going while on the base of TQ_2 is negative going.
- With a positive going signal on the base of TQ_1, if amplified, a negative going signal develops and appears on the collector of TQ_1.
- Due to positive going signal, current through R_E also decrease and hence a positive going current wave is developed across R_E.

- Due to negative going signal on the base of TQ_2, an amplified positive going signal develops on the collector of TQ_2 and anegative going signal develops across R_E, because of emitter follower action of TQ_2.
- So. The signal voltage across R_E due to effect of TQ_1 and TQ_2 are equal in magnitude and 180^o out of phase due to method pair of transistors.
- Hence these two signals cancel each other and there is no signal across the emitter resistance.
- Hence there is no AC signal current flowing through the emitter resistance. Hence R_E in this case does not introduce negative feedback.

- While V_o is the output taken across collector of TQ_1 and collector ofTQ_2, the two outputs on collector C_1 and C_2 are equal in magnitude but opposite in polarity.
- And V_o is the difference between these two signals. Hence, the different output V_o is twice as large as the signal voltage from collector to ground.

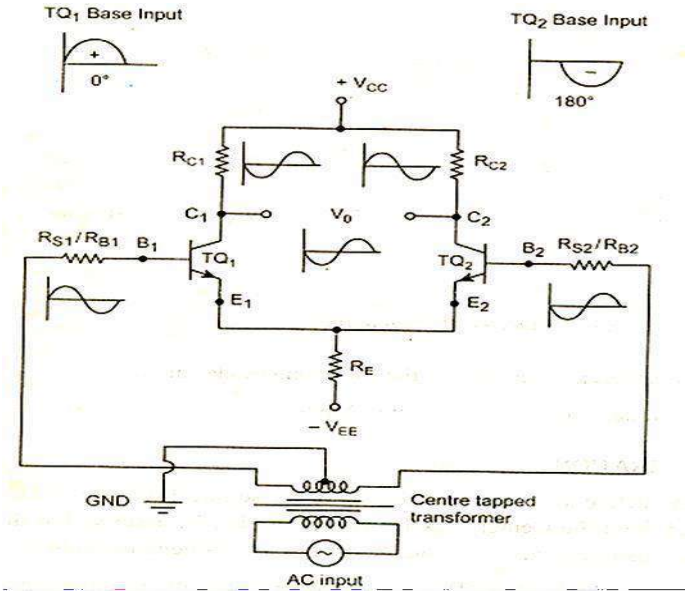


Figure (3): Differential mode

COMMON MODE OPERATION:

- In common mode the signals applied to the base of the both transistor TQ_1 and TQ_2 are in same phase, frequency and also in magnitude.

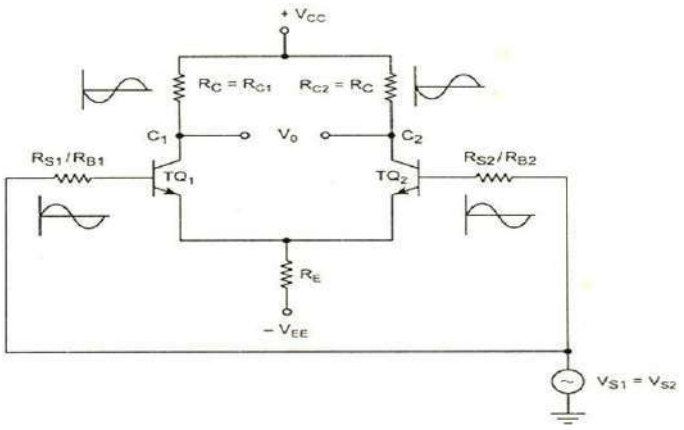


Figure (4): common mode

- In phase signal voltages at the bases of TQ_1 and TQ_2 causes in phase signal voltages to appear across R_E which add together.
- Hence R_E causes a signal current and provides negative feedback.
- This feedback reduces the common mode gain of differential amplifier.

5. **Explain the analysis of Differential amplifier. With neat sketch explain the BJT differential amplifier with active load and derive for A_d, A_c, and CMRR How CMRR improved (Nov/Dec 2015)(Nov/Dec 2016,May-2018) (OR)**
   Deduce the expression for Emitter currents in a differential amplifier under large signal operation. (April/May 2019)

- Normally, analysis in amplifier depends on both AC and DC analysis.
- In the above two, the d.c signals determines the operating values for the transistors and used as biasing.
- Similarly, a.c signals are used as input signals, which determine the output of the differential amplifier.
- The dual input, balanced output differential amplifier is also called **Symmetrical Differential Amplifier.**

❖ **DC ANALYSIS:**

- DC analysis means using D.c voltage as biasing voltage and keeping it constant (to obtain suitable operating point).
- For obtaining DC analysis, we must obtain operating point values i.e., I_{CQ} and V_{CQ} for the transistors used.
- In DC analysis, the supply voltage d.c is taken as biasing voltage and the applied input a.c signals of both V_{s1} and V_{s2} are to be zero.

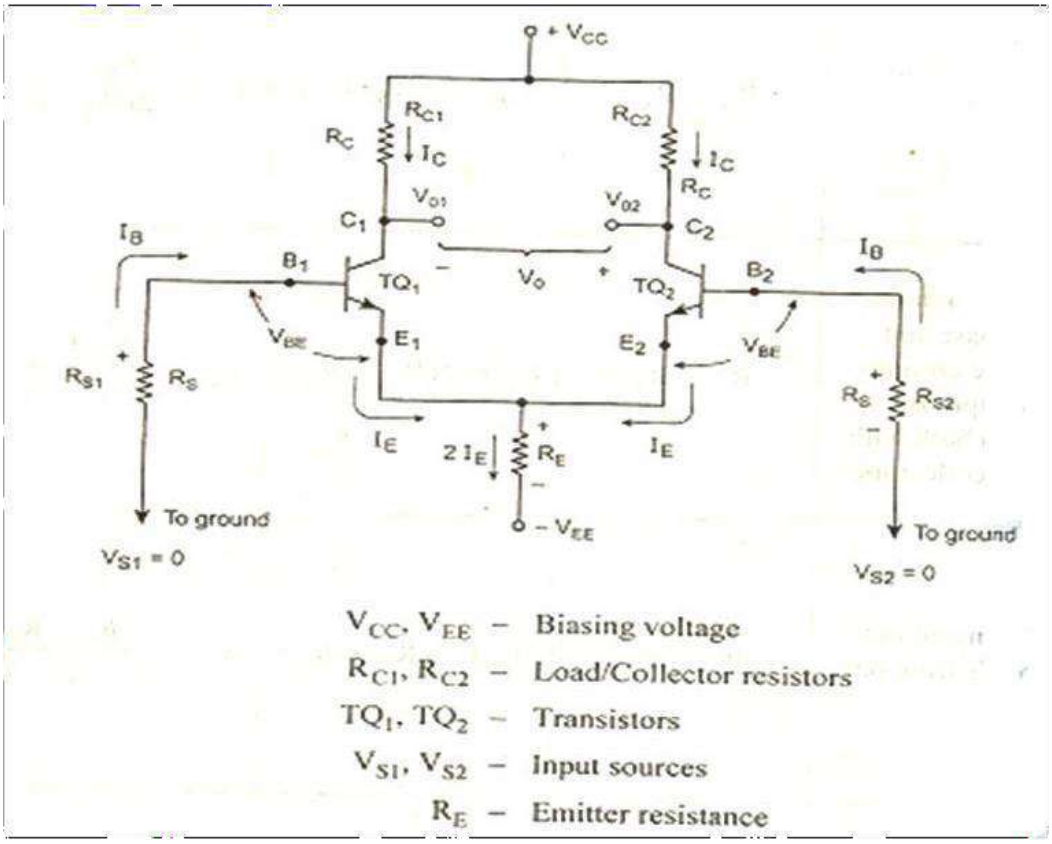


Figure (1): DC Equivalent circuit

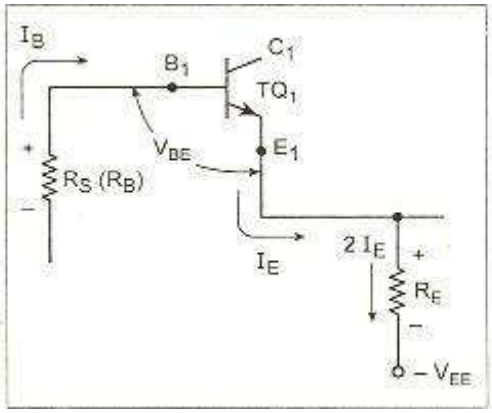
To obtain DC analysis following assumptions are to be taken:

1) Assuming $R_{S1} = R_{S2}$ (source resistances of both sides) and is simply denoted by R_S.
2) The transistor used TQ_1 and TQ_2 both are matched in their ideal identical characteristics.
3) Emitter resistances connected in both R_{E1} and R_{E2} must be the same.
   i.e., $R_{E1} = R_{E2} = R_E$

$$\text{Hence} \quad R_E = R_{E1} \| R_{E2} = \frac{R_{E1}.R_{E2}}{[R_{E1}+R_{E2}]}$$

The collector resistances of both transistors also must be in same value.
   i.e., $R_{C1} = R_{C2} = R_C$
The magnitude of $|V_{CC}| = |V_{EE}|$ are measured with respect to ground.

- Because of the above identical characteristics of both transistors, there is no necessity for finding out the operating point of each transistors.
- So, simply finding out the operating point to one is enough (I_{CQ} and V_{CEQ}).
- For finding out the I_{CQ} and $V_{CE,}$ the DC analysis diagram is needed.



Figure(2): DC analysis diagram

$$-I_BR_S - V_{BE} - 2I_ER_E = -V_{EE} \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$-I_BR_S - V_{BE} - 2I_ER_E + V_{EE} = 0 \quad \ldots\ldots\ldots\ldots\ldots (2)$$

$$\text{But,} \quad I_C = \beta I_B \quad \text{and} \quad I_C \approx I_E \ldots\ldots\ldots (3)$$

- According to equation (3), $I_B = \frac{I_C}{\beta} = \frac{I_E}{\beta}$ ……(4)

- Putting the value of equation (4) in (2),we get,

$$-\frac{I_E}{\beta}R_S - V_{BE} - 2I_ER_E + V_{EE} = 0 \ \ldots\ldots\ldots\ldots (5)$$

$$-I_E[\frac{R_S}{\beta} + 2R_E] + V_{EE} - V_{BE} = 0 \ \ldots\ldots\ldots\ldots (6)$$

$$I_E[\frac{R_S}{\beta} + 2R_E] = V_{EE} - V_{BE} \ \ldots\ldots\ldots\ldots (7)$$

$$I_E = \frac{V_{EE}-V_{BE}}{[\frac{R_S}{\beta} + 2R_E]} \cdots\cdots\cdots\cdots\cdots (8)$$

In practice, $\frac{R_S}{\beta} << 2R_E$ ……(9)

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} \quad \ldots\ldots\ldots\ldots (10)$$

- From the above equation (1), we can observe the following points.
    i. R_E(Emitter resistance) determines the emitter circuit of TQ_1 and TQ_2 for the known value of V_{EE}.
    ii. Then, the collector resistance (R_L) is independent of current that flows through Emitter terminals of TQ_1 and TQ_2.

The collector voltage, $V_C = V_{CC} - I_C R_C$ ..... (11)

- Neglecting the drop across R_S, we can obtain the emitter voltage of TQ_1 as approximately equal to $-V_{BE}$.
- Then, $V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - V_{BE}$ ..... (12)

$V_{CE} = V_{CC} + V_{BE} - I_C R_C$

- Hence, $I_E = I_C = I_{CQ}$ while $V_{CE} = V_{CEQ}$ for given values of V_{CC} and V_{EE}.
- Therefore operating point (Q) can be obtained from equation (10) and (12).

❖ **AC ANALYSIS:(Nov/Dec 2016)**

- For performing AC analysis, we must apply AC input signals as an input. So, we can calculate the following:

E. Differential mode gain (A_d).
F. Common mode gain (A_c).
G. Input resistance (R_i).
H. Output resistance (R_o).

The above can be obtained by using h-parameters.

D. Differential gain (A_d)

- To obtain the Differential mode gain, the two input signals must be different from each other.
- Here, we take the two a.c input signals as equal in magnitude but having 180^o phase shift between them.
- Then, the magnitude of each a.c input voltage V_{S1} and $V_{S2}$is $\frac{V_S}{2}$.
- For the a.c purposes, emitter terminal can be grounded which is shown in figure below with small signal analysis.

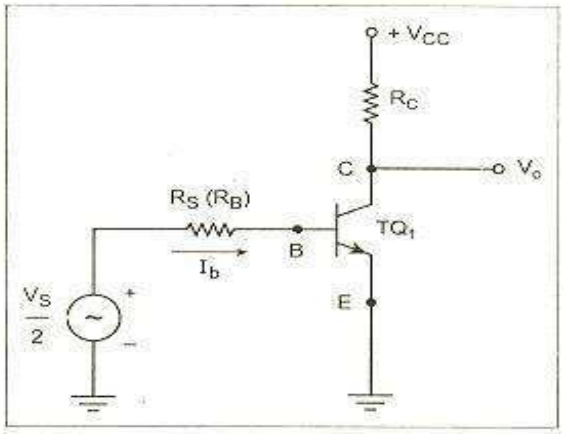
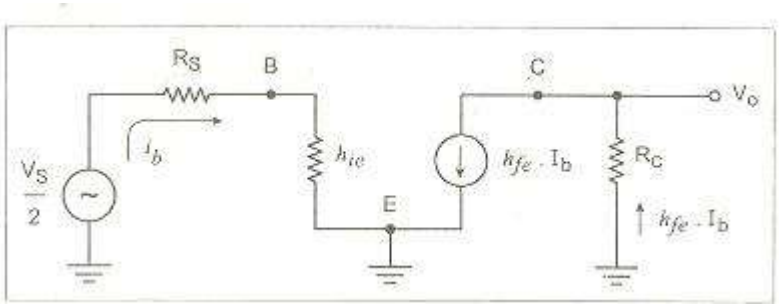


Figure (1): AC Equivalent for differential operation (half circuit concept)

- The circuit which can be analyzed by considering only one transistor is called Half circuit concept of analysis.



Figure(2): Approximate hybrid model

- For obtaining the differential mode gain (A_d) from the above hybrid model, we have to apply the Kirchhoff's voltage law in input side,

$$\frac{V_S}{2} = i_b R_S + i_b h_{ie} \quad \text{……..(1)}$$

$$\frac{V_S}{2} = i_b (R_S + h_{ie}) \quad \text{……..(2)}$$

$$i_b = \frac{V_S}{2(R_S + h_{ie})} \quad \text{……...(3)}$$

- Similarly, applying the Kirchhoff's voltage law to output loop, we get

$V_o = - I_b h_{fe} . R_C$ .....(4)

- Put the value of I_b in equation (4) from (3), we get,

$$V_o = \frac{-h_{fe} V_S R_C}{2(R_S + h_{ie})} \ldots\ldots(5)$$

- Then, $\frac{V_o}{V_S} = \frac{-h_{Fe} . R_C}{2(R_S + h_{ie})}$ …….(6)

- Negative sign indicates that 180^0 phase difference between input and output. If the input signals are equal and are out of phase by 180^0, we get

- Differential mode signal $V_d = V_1 - V_2 = (\frac{V_S}{2}) - (-\frac{V_S}{2}) = V_S$ …..(7)

Where, $V_S$is differential input voltage.

- Differential voltage gain $A_d = \frac{V_o}{V_S}$

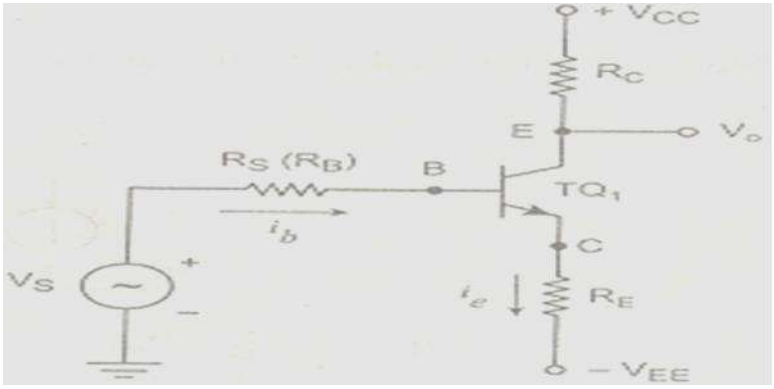
$$A_d = \frac{h_{fe}R_C}{2(R_S + h_{ie})} \ldots\ldots\ldots (8)$$

- When the output of differential amplifier is measured with reference to ground, it is called unbalanced output.
- The output across the collectors of Q_1 and Q_2 to be perfectly matched then A_d for balanced output is twice than that of A_d for unbalanced output. Therefore

$$A_d = \frac{h_{fe}R_C}{(R_S + h_{ie})} \ldots\ldots\ldots\ldots\ldots\ldots (9)$$

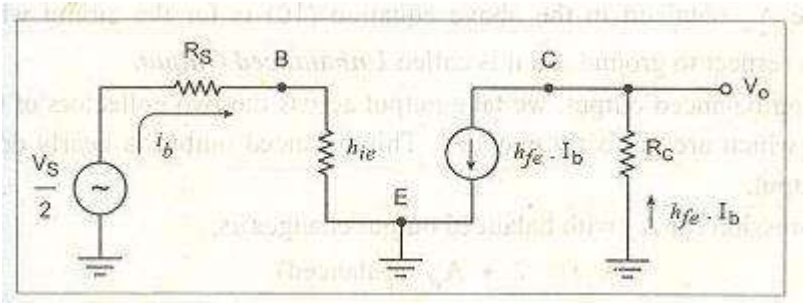
E. Common mode gain (A_C)

- In common mode, the both transistor's input magnitude and phases are also inphase with each other.
- Let us assume that input signals are having the same magnitude V_S and are in same phase.
- Common mode voltage $V_C = \frac{V_1+V_2}{2} = \frac{V_S+V_S}{2} = V_S$ ……(10)
- If suppose, the output is expressed as, $V_o = A_C . V_S$ ……(11)
- Common mode gain $A_C = \frac{V_o}{V_S}$ …….(12)
- In this mode, both the emitter current $I_{e1} = I_{e2} = I_e$ of TQ_1, TQ_2 flows through R_E in the same direction, with same magnitude.
- Hence, the total current flowing through R_E is nearly $2I_e$ …..(13)



Figure(1): A.C. Equivalent Circuit for Common Mode Configuration

- Then the approximate hybrid model for the above circuit can be obtained and is used to obtain the A_d.



Figure(2): Approximate Hybrid model

- As the current through R_E is $2I_e$, for simplicity of derivation, we have to assume the I_e and effective emitter resistance as $2R_E$.
- Current through R_C = Load current I_L
- Effective emitter = 2 R_E
- Current through emitter resistance = $I_L + I_b$
- Current through $h_{oe} = (I_L - h_{fe} \cdot I_b)$
- Now, applying Kirchhoff's voltage law to input side,

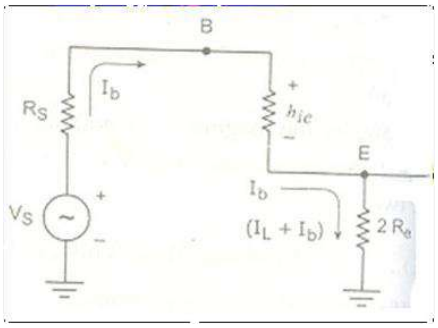


Figure (3): Input side

$$-I_b R_S + I_b h_{ie} + 2R_E(I_L + I_b) = -V_S \quad \ldots\ldots(14)$$

$$I_b R_S - I_b h_{ie} - 2R_E(I_L + I_b) = V_S \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(15)$$

$$\text{While, } V_o = -I_L \cdot R_C \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(15a)$$

- Negative sign is due to the assumed direction of current. Similarly apply KVL to output side.

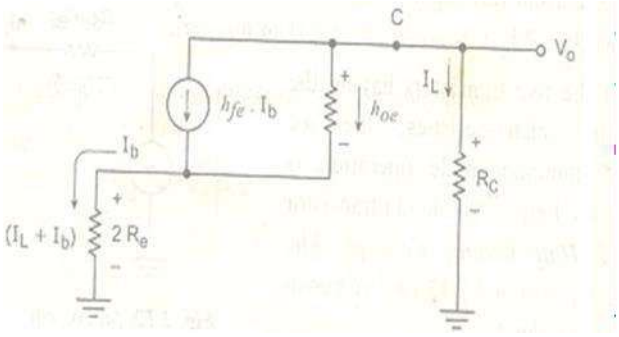


Figure (4): Output side

$$\frac{-(I_L - h_{Fe}I_b)}{h_{oe}} - 2R_E(I_L + I_b) - I_L R_C = 0 \ldots. (16)$$

$$\frac{-I_L}{h_{oe}} + \frac{h_{Fe}I_b}{h_{oe}} - 2I_L R_E - 2I_b R_E - I_L R_C = 0 \ldots (17)$$

$$I_b\left[\frac{h_{Fe}}{h_{oe}} - 2R_E\right] = I_L\left[\frac{1}{h_{oe}} + 2R_E + R_C\right] \ \ldots\ldots\ldots (18)$$

- Multiplying both sides by h_{oe}, then

$$I_b[h_{fe} - 2R_E h_{oe}] = I_L[1 + h_{oe}(2R_E + R_C)] \ldots\ldots\ldots\ldots\ldots (19)$$

$$\frac{I_L}{I_b} = \frac{[h_{fe} - 2R_E h_{oe}]}{[\,1 + h_{oe}(2R_E + R_C)]} \ldots\ldots\ldots(20)$$

$$I_b = \frac{I_L[\,1+h_{oe}(2R_E+R_C)]}{[h_{Fe}-2R_E h_{oe}]} \quad \ldots\ldots\ldots\ldots(21)$$

- Putting this I_b in equation (15),

$$V_S = \frac{I_L[1 + h_{oe}(2R_E + R_C)][R_S + h_{ie} + 2R_E] + 2R_E}{[h_{fe} - 2R_E h_{oe}]}$$

$$\frac{V_S}{I_L} = \frac{[1 + h_{oe}(2R_E + R_C)][R_S + h_{ie} + 2R_E] + 2R_E}{[h_{fe} - 2R_E h_{oe}]} \ldots(22)$$

- Then, find LCM and adjusting the terms,

$$\frac{V_S}{I_L} = \frac{2R_E(1 + h_{fe}) + R_S(1 + 2R_E h_{oe}) + h_{ie}(1 + 2R_E h_{oe}) + h_{oe}R_C(2R_E + R_S + h_{oe})}{[h_{fe} - 2R_E h_{oe}]}$$

$$\frac{V_S}{I_L} = \frac{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe}) + h_{oe}R_C(2R_E + R_S + h_{oe})}{[h_{fe} - 2R_E h_{oe}]} \ldots.(23)$$

- Actually $h_{oe}R_C \ll 1$. Neglecting the terms,

$$\frac{V_S}{I_L} = \frac{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})}{[h_{fe} - 2R_E h_{oe}]} \ldots..(24)$$

$$I_L = \frac{V_S.[h_{fe} - 2R_E h_{oe}]}{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})} \ldots..(25)$$

- Putting this I_L in equation (15a),

$$V_o = - I_L . R_C$$

$$V_o = \frac{-V_S.[h_{Fe}-2R_E h_{oe}]R_C}{2R_E(1+h_{Fe})+(R_S+ h_{ie})(1+2R_E h_{oe})} \ldots\ldots.(26)$$

- Hence the common mode gain can be written as,

$$A_C = \frac{V_o}{V_S} = \frac{[2R_E h_{oe} - h_{fe}]R_C}{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})} \ldots\ldots.(27)$$

- In practice, h_{oe} is neglected, because the expression for A_C can be further modified as,

$$A_C = \frac{-h_{fe}R_C}{R_S + h_{ie} + 2R_E(1 + h_{fe})} \ldots..(28)$$

- The above expression is same whether the output is balanced or unbalanced.

COMMON MODE REJECTION RATIO (CMRR):

- $CMRR = \left|\frac{A_d}{A_C}\right|$
- From equation (8) and (28),

$$CMRR = \left|\frac{\frac{h_{Fe}R_C}{2(R_S+h_{ie})}}{\frac{h_{Fe}R_C}{(R_S+h_{ie}+2R_E(1+h_{Fe})}}\right| \ldots\ldots(29)$$

$$\text{CMRR} = \left|\frac{(R_S + h_{ie} + 2R_E(1 + h_{fe})}{2(R_S + h_{ie})}\right| \quad \ldots(30)$$

- This is CMRR for dual input balanced output differential amplifier circuit.

- For balanced case,

$$\text{CMRR} = \left|\frac{(R_S + h_{ie} + 2R_E(1 + h_{fe})}{(R_S + h_{ie})}\right|$$

- or unbalanced case,

$$\text{CMRR} = \left|\frac{(R_S + h_{ie} + 2R_E(1 + h_{fe})}{2(R_S + h_{ie})}\right|$$

C. Input Impedance (R_i):

- R_i is defined as the equivalent resistance existing between any one of the input and the ground when other input terminal is grounded.

$$R_i = \frac{V_S}{I_b}$$

- Put the V_S and $I_b$from the above discussion, $R_i = 2(R_S + h_{ie})$.

- For one transistor and input pair, the resistance is $R_S + h_{ie}$.

- Hence for dual input circuit, the total input resistance is $2(R_S + h_{ie})$, as the 2 circuits are perfectly matched.
- This input resistance is not dependent on whether output is balanced or unbalanced.

D) OUTPUT IMPEDANCE R_O:

- It is defined as the equivalent resistance between one of the output terminals with respect to ground.
- The resistance between output terminal with respect to ground is R_C.

  $R_O = R_C$

FET input stages

6. Explain the FET input stages.

❖ **FET parameters:**

- The following are the parameters of FET as an amplifier.

1. The transcondutance 'g_m'
2. The dynamic resistance 'r_d' and
3. The amplification factor μ.

- **Transcondutance:**

✓ It is defined as the ratio of change in drain current to the change in gate source voltage at a constant drain source voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} / \Delta V_{DS} = \text{Constant}$$

✓ It is expressed in mill amperes per volt or micro mhos. It is sometimes referred to as the common source forward trans admittance.

- **Dynamic Drain Resistance or output Resistance:**

✓ The drain resistance is defined as the ratio of change in drain source voltage V_{DS} to the change in drain current I_D at a constant gate source voltage.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} / \Delta V_{GS}$$

✓ The reciprocal of drain resistance is the drain conductance, it is called sometimes as common source output conductance.

- **Amplification factor:**

✓ Amplification factor is defined as the ratio of change in drain source voltage to the change in gate source voltage at a constant drain current.

$$\mu = \frac{\Delta VDS}{\Delta V_{GS}} / \Delta I_D$$

- **Relation between FET parameters:**

✓ We know that $\mu = \frac{\Delta VDS}{\Delta V_{GS}}$

✓ Multiplying the numerator and the denominator on the R.H.S by ΔI_D, We have

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} = \frac{V_{DS}}{I_D} \times \frac{I_D}{V_{GS}} = g_m \times r_d$$

✓ Therefore $\mu = g_m \times r_d$ is the relation between the parameters of a FET.

- **FET configurations:**

✓ There are three types of configurations in the FET amplifier, they are:

- Common source configuration
- Common drain configuration
- Common gate configuration

✓ A FET can be connected in any one of the three configurations. The common drain circuit also called source follower circuit.

Single tuned amplifiers

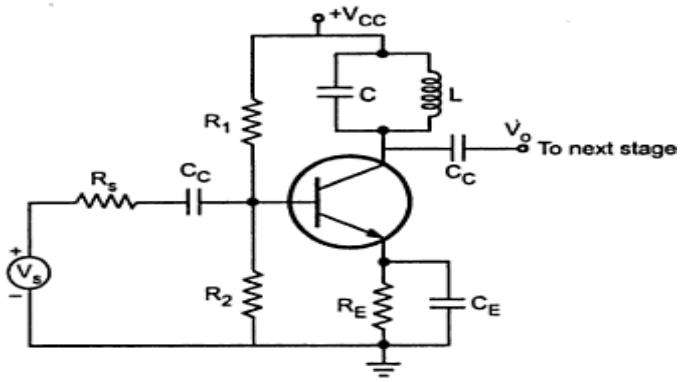
7. Draw the circuit diagram of a single tuned amplifier and obtained expression for its gain ,resonant and cut off frequency (May/June 2016), (Nov/Dec2015)

(OR)

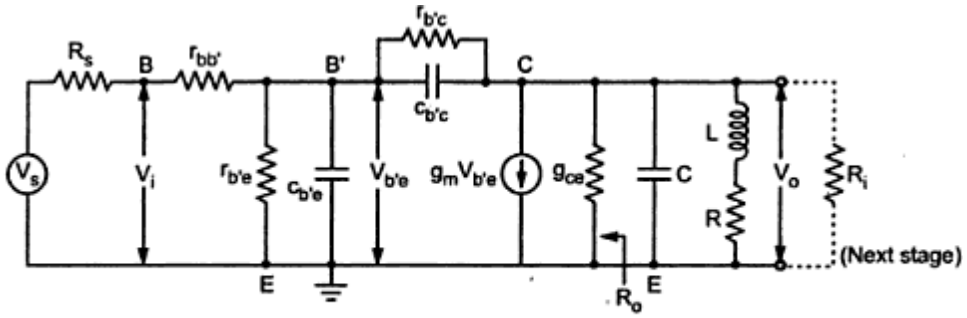
Illustrate the behavior of a MOSFET based amplifier circuit tuned load. Also deduce expression for voltage gain at Centre frequency, Q and bandwidth. (April/May 2019)

SINGLE TUNED CAPACITIVE COUPLED TUNED AMPLIFIER

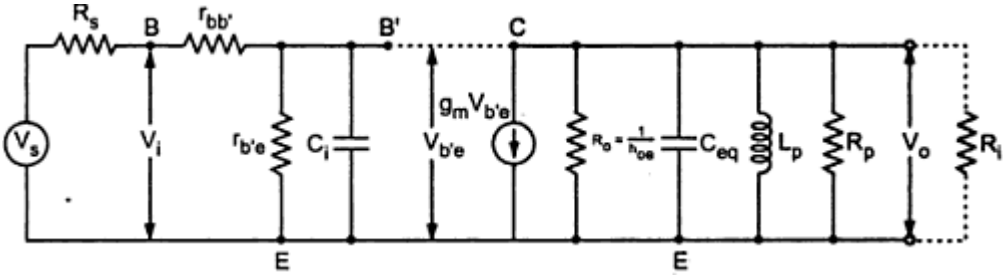
- Tuned amplifiers are amplifiers that are designed to reject a certain range of frequencies below a lower cut off frequency ω_L and above a upper cut off frequency ω_H and allows only a narrow band of frequencies.



- The output across the tuned circuit is coupled to the next stage through the coupling capacitor. The tuned circuit is formed by L and C resonates at the frequency of operation.



Equivalent circuit of single tuned amplifier



Here C_i and C_{eq} represent input and output circuits capacitance respectively. They can be given as

$C_i = C_{be} + C_{bc}(1-A)$ where A is the voltage gain of the amplifier

$C_{eq} = C_{be}(\ (A-1)\ /\ A) + C$ where C is the tuned circuit capacitance

The g_{ce} is represented as the output resistance of current of generator gmV_{be}

$g_{ce} = (1\ /\ r_{ce}) = h_{ce} - gm*h_{ce} = h_{ce} = (1/R_0)$

The admittance of the inductor along with resistor R is given by

$$Y = \frac{1}{R + j\omega L}$$

Multiplying numerator and denominator by $R + j\omega L$ we get

$$Y = \frac{R - j\omega L}{R^2 + \omega^2 L^2} = \frac{R}{R^2 + \omega^2 L^2} - \frac{j\omega L}{R^2 + \omega^2 L^2} = \frac{R}{R^2 + \omega^2 L^2} - \frac{j\omega^2 L}{\omega(R^2 + \omega^2 L^2)} = \frac{1}{R_P} + \frac{1}{j\omega L_P}$$

Where $R_P = \frac{R^2 + \omega^2 L^2}{R}$, and $L_P = \frac{R^2 + \omega^2 L^2}{\omega^2 L}$

The LP and RP are in shunt quality factor of the coil at resonance is given by

$$Qo = WoL/\ R$$

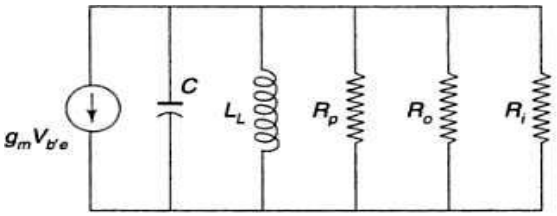
$$L_P = \frac{R^2 + \omega^2 L^2}{\omega^2 L}$$

Dividing numerator and denominator terms by $\omega^2 L$,

$$L_P = \frac{R^2/\omega^2 L + L}{1}$$

$$L_{P \approx L}$$

Hence, The output circuit of the amplifier can be modified as



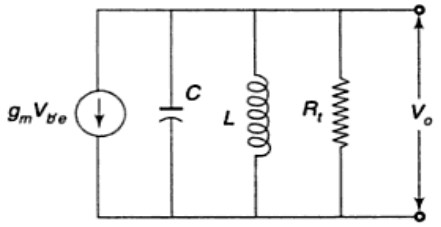
Equivalent circuit of the output part of the tuned amplifier

Taking R_1 as the parallel combination of R_0, R_P and R_i i.e.

$$\frac{1}{R_t} = \frac{1}{R_0} + \frac{1}{R_P} + \frac{1}{R_i}$$

The output circuit can be modified as shown in fig.

$$\boldsymbol{Q_e} = \frac{\text{Susceptance of inductance L C}'\text{capacitance C}}{\text{Conductance shunt resistance } R_t}$$



Simplified output circuit of the tuned amplifier

Where Z is the impedance of C, L and R_t inparallel. The admittance Y = (1/Z) is given by

$$Y = \frac{1}{Z} = \frac{1}{R} + \frac{1}{j\omega L} + j\omega C = \frac{1}{R}\left[1 + \frac{R_t}{j\omega L} + j\omega C R_t\right]$$

Multiplying numerator and denominator by ω_0

$$Y = \frac{1}{R_t}\left[1 + \frac{R_t\omega_0}{j\omega L\omega_0} + \frac{j\omega\omega_0 C R_t}{\omega_0}\right]$$

$$\frac{R_t}{L\omega_0} = \omega_0 C R_t = Q_e$$

$$Y = \frac{1 + jQ_e\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}{R_t}$$

$$Z = \frac{1}{Y} = \frac{R_t}{1 + jQ_e\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}$$

Let δ the fractional frequency variation.

$$\delta = \frac{\omega - \omega_0}{\omega_0} = \frac{\omega}{\omega_0} - 1 = \frac{\omega}{\omega_0} = 1 + \delta$$

$$Z = \frac{R_t}{1 + jQ_e\left[(1+\delta) - \left(\frac{1}{1+\delta}\right)\right]} = \frac{R_t}{1 + jQ_e\left[\frac{1 + \delta^2 + 2\delta - 1}{1+\delta}\right]}$$

$$Z = \frac{R_t}{1 + j2Q_e\delta\left[\frac{\frac{\delta}{2} + 1}{1+\delta}\right]}$$

Frequency close to resonance $\omega_0, \delta << 1$

$$Z = \frac{R_t}{1 + j2Q_e\delta}$$

At resonance $\omega = \omega_0, \delta = 0$

$$Z = R_t = R_0\, parallel\, R_P\, Parallel\, R$$

$$R_P = \frac{\omega_{0L^2}}{R} = \frac{\omega_0 L}{\omega_0 C R}$$

$$V_{b'e} = V_i \frac{r_{b'e}}{r_{bb'} + r_{b'e}}$$

$$V_0 = -g_m V_{b^F e} Z = -g_m \left(V_i \frac{r_{b^F e}}{r_{bb^F} + r_{b^F e}}\right) Z$$

Voltage gain with out considering the source resistance is given by

$$A_v = \frac{V_0}{V_i} = -g_m \left(\frac{r_{b^F e}}{r_{bbF} + r_{b^F e}}\right) Z$$

$$A_v = -g_m \left(\frac{r_{b^F e}}{r_{bbF} + r_{b^F e}}\right) * \frac{R_t}{1 + j2Q_e\delta}$$

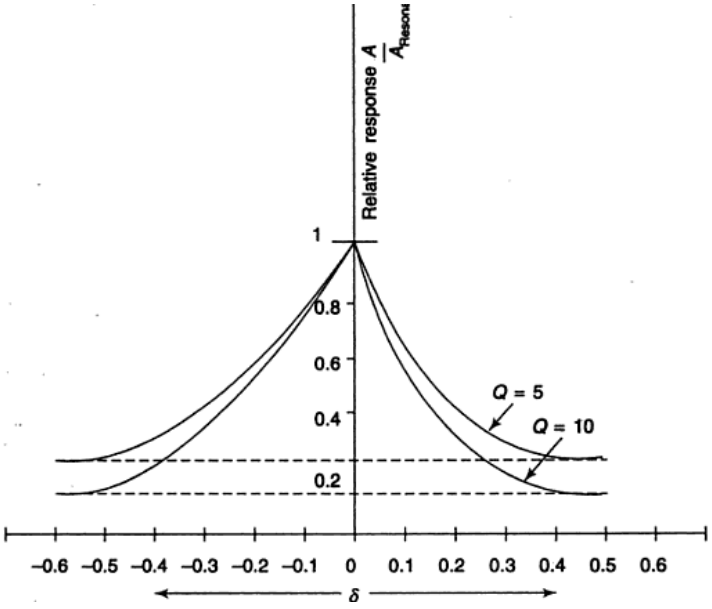
$$A_v(at\ resonance) = -g_m \left(\frac{r_{b^F e}}{r_{bbF} + r_{b^F e}}\right) * R_t$$

$$\left|\frac{A_v}{A_v(at\ resonance)}\right| = \frac{1}{\sqrt{1 + (2\delta Q_e)^2}}$$

$$2\delta = \frac{1}{Q_e}$$

$$\Delta\omega = \frac{1}{R_t C}\ rad/sec$$

Gain $\frac{Av}{A_v(at\ resonance)}$ plotted against δ



Gain and frequency response

8. Draw the frequency response of an ideal and a practical tuned amplifier and discuss their characteristics. (Nov/Dec 2018)

The amplifier that amplifies a particular frequency and rejects other frequencies are termed as tuned amplifiers.

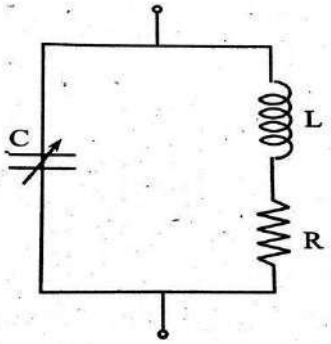


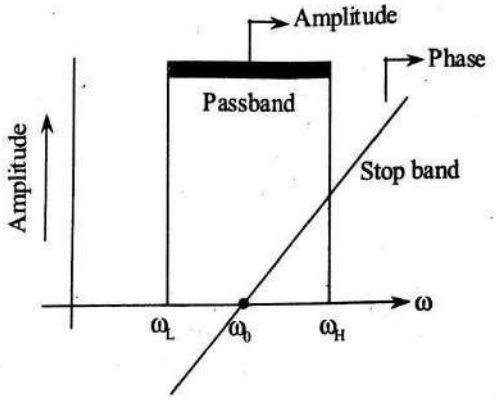
Figure (1): Ideal Tuned Circuit

Basically the tuned amplifier amplify the signal within a narrow frequency band that is centered about a frequency f_0. The signal between the lower and higher cut-off frequencies is amplified. The resonant frequency of an ideal tuned circuit is expressed as,

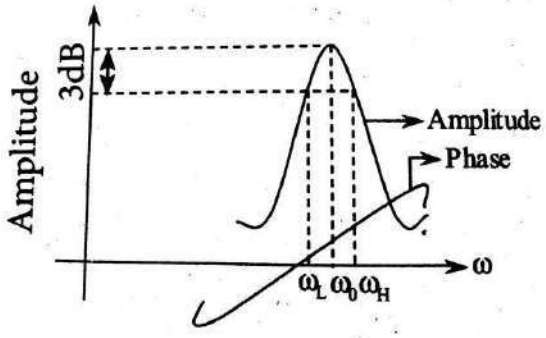
$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad \text{(or)} \quad \omega_0 = \frac{1}{\sqrt{LC}} \quad [\text{since } \omega_0 = 2\pi f_0]$$

Figures 2(a), 2(b) illustrates the ideal response and actual response curve of a tuned amplifier circuit respectively.

From the figure 2(b), it is observed that at higher and lower cut-off frequencies, the curve decreases and is maximum at resonant frequency (f_0).



(a) Ideal Response



(b) Actual Response Curve

The behavior of tuned circuit at various frequencies is,

1. At frequencies *above resonant frequency*, the circuit behaves as *capacitive load* due to which the *current leads the applied voltage*.
2. At frequencies *below resonant frequency*, the circuit behaves as *inductive load* due to which the *current lags behind the applied voltage.*
3. *At resonant frequency*, the circuit behaves as *resistive load* since the *inductive and capacitive effects are nullified.*

9. Explain briefly about gain and frequency response of single-tuned amplifier.

- The voltage gain of an amplifier depends upon current gain (β), input resistance (R_i) and effective or a.c load resistance.
- The voltage gain is given by the relation,

$$A_v = \beta \times \frac{r_L}{R_i}$$

- The a.c load resistance of a parallel resonant circuit (i.e., tuned circuit) is given by the relation,

$$R_L = Z_p = \frac{L}{CR}$$

Where, L = value of inductance,

C = value of capacitance, and

R = value of effective resistance of the inductor.

- Voltage gain of a voltage amplifier is given by the relation,

$$A_v = \beta \times \frac{\frac{L}{CR}}{R_i}$$

- We know that the value of the quantity $\frac{L}{CR}$ (changes above or below the resonant called impedance of the tuned circuit) is very high at the resonant frequency and it decreases as the frequency changes above or below the resonant frequency.
- Therefore voltage gain of a tuned amplifier is very high at the resonant frequency and it decreases as the frequency changes above or below the resonant frequency.
- The above facts are shown in the form of a voltage gain versus frequency plot shown in figure below.

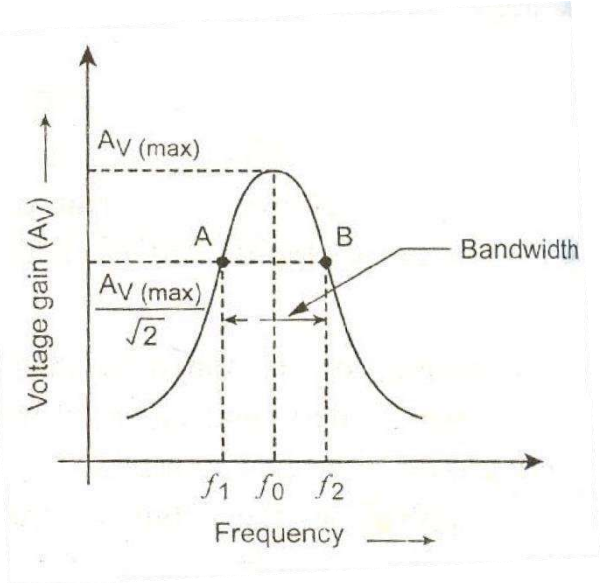


Figure: Frequency response curve

- Such a plot is called Frequency response curve of a tuned voltage amplifier.
- The bandwidth (BW) of an amplifier is equal to the frequency difference between the point A and B on either side of the resonant frequency, where the value of voltage gain drops to $1/\sqrt{2}$ of its maximum value of resonance.
- Thus bandwidth,

$$BW = \Delta f = f_2 - f_1 = \frac{f_o}{Q_o}$$

Where Q_o is the quality factor (or Q-factor) of the tuned circuit.

Neutralization methods

10. Describe any one method of neutralization used in tuned amplifier?
Briefly explain Hazel line neutralization used in tuned amplifiers for stabilization (May/June 2016)(Nov/Dec 2016,May-2018)

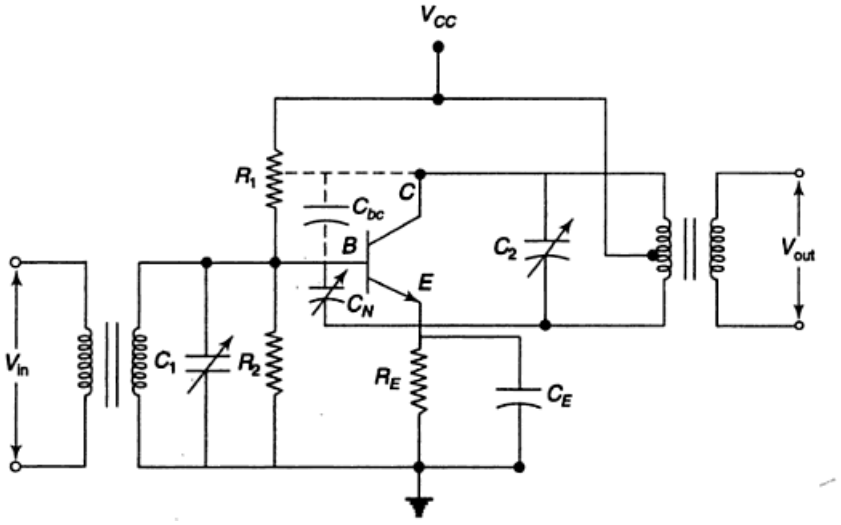
STABILITY OF TUNED AMPLIFIER

Stability of tuned amplifier is achieved by neutralization

i). Hezeltine neutralization *ii). Neutrodyne neutralization*

- In a tuned RF amplifier the transistor are used at the frequency near to their unity gain bandwidth. To amplify the narrow band of high frequencies.
- At this frequency inter-junction capacitor b/w base and collector of transistor (Cbc)of transistor becomes dominant
- As a reactance of Cbc at Rf is low and its provide feedback path from a collector to base.
- If some feedback signal reaches the input from output in a positive manner with proper phase shift then the circuit is unstable, generating its own oscillation.

Amplifier, it was necessary to reduce stage gain to a level that ensures the circuit stability



. This can be achieved in several ways

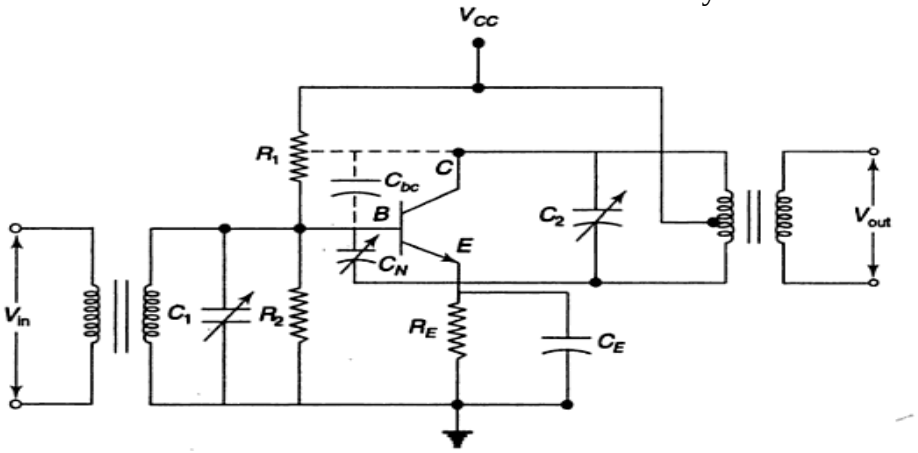
i) favoring the stability factor of the tuned circuits
ii) loose coupling b/w stages
iii) Increase looser element into the element.

- To achieve stability the professor Hazettile introduced a circuit in which the troublesome effects of the c_{bc} was neutralized by introducing a signal coupled through the C_{bc}.

HAZELTINE NEUTRALIZATION:-

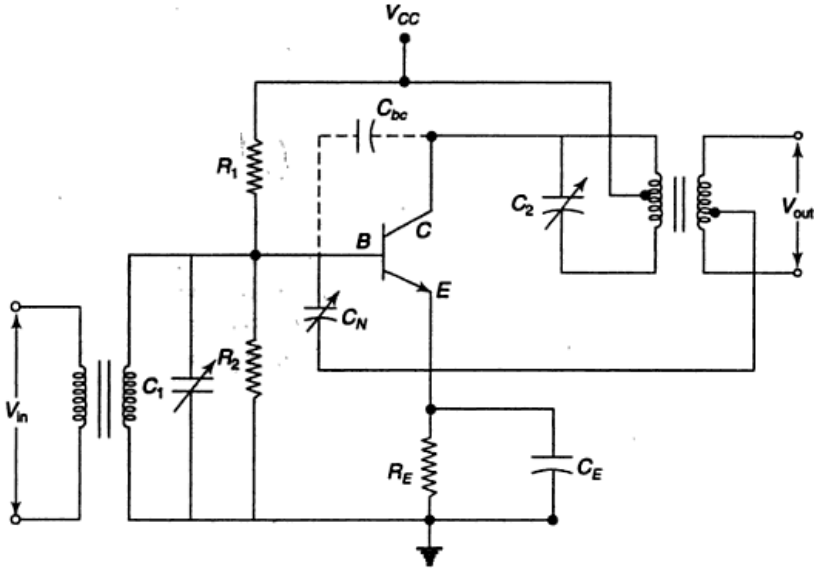
- This is the neutralization technique employed in tuned RF amplifier to maintain stability .

- The undesired effect of collector to base capacitance of the transistor is neutralized by introducing a signal which cancels the signal coupled through the collector to base capacitance
- This is achieved by a small variable capacitance (C_N)is connected from the bottom of coil to the base of the transistor .It introduce a signal to the base of the transistor such that it cancels out the signal fed to the base by Cbc
- By properly adjusted Cn exactly neutralized achived.
- Modified version of Hazeltine neutralization called neutron dyneneutralization.



NEUTRODYNE NEUTRALIZATION:-

- In a neutrodyne neutralization technique, Cn is connected to the centre trapped to the secondary coil.
- Hence it is connected with Vcc which ensures that it is insensitivity to any variation is supply voltage Vcc .Hence provided higher neutralization for the tuned amplifier.
- In principle, the circuit functions are the same manner as the hazeltine neutralizing capacitor does not have the supply voltage across it.



Power amplifiers –Types (Qualitative analysis).

11. Write a short notes on Power amplifier.(Nov/Dec 2017)

- A power amplifier is an amplifier, which is capable to providing a large amount of power to the load such as loudspeaker, or motor etc.

- It is essential in almost all electronic systems, where a large amount of power is required to be supplied to the load.
- The power amplifier, is used as a last stage in a electronic system. For example, a public address system (PAS) consists of a microphone, a multistage amplifier, a power amplifier and a loudspeaker.
- The microphone converts the sound waves into electrical signal, which is of very low voltage (usually of few millivolts).
- This signal is insufficient to drive the loudspeaker. Therefore this signal is first raised to a sufficiently high value (a few volts) by passing it through a multistage small-signal (or voltage) amplifier.
- This signal is then used to drive the power amplifier, because it is incapable of delivering a large amount of power to the loudspeakers.
- A power amplifier is more commonly known as audio amplifier. The audio amplifiers are used in public address system, tape recorders, stereo systems, television receivers, radio receivers, broadcast transmitters etc.
- It will be interesting to know that a power amplifier dies not actually amplify the power. As a matter of fact, it takes power from the d.c. power supply connected to the output circuit and converts it into useful a.c. signal power.
- The power is fed to the load. The type of a.c. power developed, at the output of a power amplifier, is controlled by the input signal.
- Thus we can say that actually a power amplifier is a d.c. to a.c. power converter, whose action is controlled by the input signal.
- The power amplifiers, are also known as large signal amplifiers.
- The term 'large signal' for the power amplifiers arises because these amplifiers use a large part of their a.c. load line for operation.
- It is in contrast to the small signal amplifiers, which use only 10% of their a.c. load line for operation. The small signal amplifiers are commonly known as voltage amplifiers.

12. Explain in detail the various types of power amplifier. *(OR)* **Explain with circuit diagram class B power amplifier and derive for its efficiency (Nov/Dec2015)(May 2017)(Nov/Dec-2017)**

i. Class-A amplifier:

- A class-A amplifier is one in which the operating point and the input signal are such that the current in the output circuit, flows at all times.
- A class-A amplifier operates essentially over a linear portion of its characteristics.
- In class-A operation, the transistor stays in the active region throughout the a.c cycle.
- The point and the input signal are such as to make the output current flows for 360°.
- **Voltage gain:** The voltage gain for a class-A amplifier may be obtained in the same way as the small-signal amplifier. It is given by the relation,

$$A_v = \frac{r_L}{r_e}$$

r_L = A.C. load resistance whose value is equal to the parallel combination of collector resistance (R_c) and load resistance (R_L).

r_e= A.C. emitter diode resistance.

- **Current gain:** the current gain of a transistor is the ratio of a.c. collector current (i_c) to the a.c. base current (i_b).

$$A_i = \frac{i_c}{i_b} = \beta$$

- **Power gain:** The a.c. input power to the base of transistor,

$$P_{in} = V_{in} \, . \, i_b$$

And the a.c. output power from the collector.

$$P_o = -V_o \, . \, i_c$$

- The negative sign in the above equation indicates that the phase of input signal is reversed at the output.

$$\text{Power gain, } A_p = \frac{P_o}{P_{in}} = \frac{-V_o . i_c}{V_{in} . i_b} = -\frac{V_o}{V_{in}} \text{ x} \frac{i_c}{i_b}$$

$$= -A_v \, . \, A = -\frac{r_L}{r_e} \text{ x } \beta$$

Where A_v = voltage gain, and

A_i = current gain.

- The overall efficiency or circuit efficiency of the amplifier circuit is defined as the ratio of a.c. power delivered to the load to the total power supplied by the d.c. source.
- Mathematically, the overall efficiency,

$$\eta_o = \frac{\text{a.c.power delivered to the load}}{\text{Total power supplied by the d.c. source}} = \frac{V_{CEQ}.I_{CQ}}{2V_{CC}.I_{CQ}}$$

- Maximum value of overall efficiency,

$$\eta_{o(max)} = \frac{V_{CEQ}.I_{CQ}}{2(V_{CEQ}.I_{CQ})} = 0.25 = 25\%$$

- The collector efficiency of the amplifier circuit is defined as the ratio of a.c. power delivered to the load, to the power supplied by thed.c. source to the transistor.
- Mathematically, collector circuit efficiency,

$$\eta_c = \frac{\text{a.c.power delivered to the load}}{\text{power supplied by the d.c.source to the transistor}}$$

- Maximum value of collector efficiency,

$$\eta_{c(max)} = \frac{V_{CEQ}.I_{CQ}}{2(V_{CEQ}.I_{CQ})} = 0.5 = 50\%$$

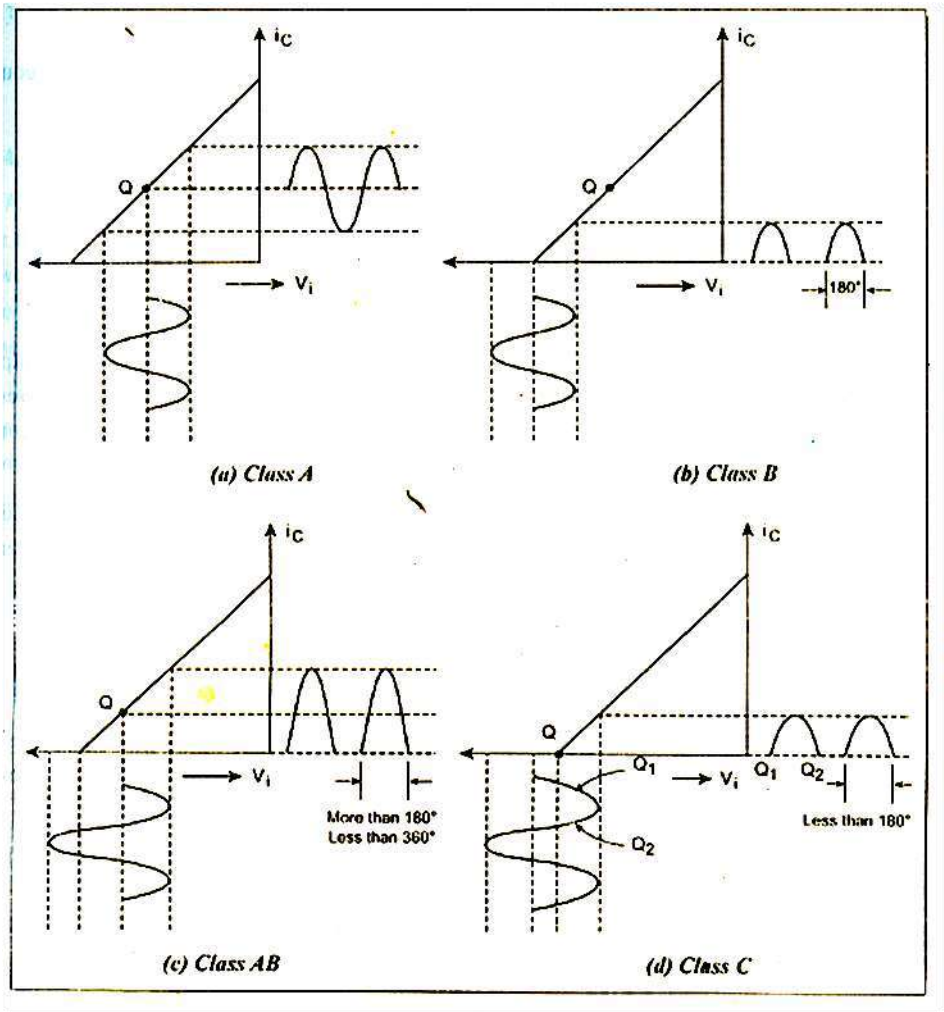


Figure: classification of amplifiers based on the biasing condition

ii. Class-B amplifier:

- A class-B amplifier is one in which the operating point is at an extreme end of its characteristics, so that the quiescent power is very small.
- Hence either the quiescent current or the quiescent voltage is approximately one half a cycle.
- In class-B operation, the transistor stays in the active region only for half the cycle. The Q-point is fixed at the cut-off point of the characteristics.
- The output current flows for 180°.
- <u>D.C. input power</u>: the input power comes from the d.c. source (i.e., the V_{CC} supply) and is given by the relation,

$$P_{in(dc)} = V_{CC} \cdot I_{dc}$$

Where I_{dc} is the average value of current drawn from the V_{CC}supply.

- <u>D.C. power loss in load resistor</u>: Its value is given by the relation,

$$P_{RL(dc)} = I^2_{dc} \cdot R_L$$

- <u>A.C. output power in load resistor</u>: Its value is given by the relation,

$P_{o(ac)} = I^2 \cdot R_L = V^2 / R_L$

Where I = the r.m.s. value of a.c. output current,

V = Ther.m.s. value of a.c. output voltage, and

V_P= The peak value of a.c. output voltage.

- Power dissipated within the resistor: Its value is given by the relation,

$$P_{c(dc)} = P_{in(dc)} - P_{RL(dc)} - P_{o(ac)}$$

- Overall efficiency: $\eta_o = \frac{P_{o(ac)}}{P_{in(dc)}} = \frac{P_o}{V_{CC} \cdot I_{dc}}$
- Maximum value of overall efficiency,

$$\eta_o = \frac{P_{o(ac)}}{P_{in(dc)}} = \frac{\frac{1}{4} V_{CP} \cdot I_{CP}}{V_{CC} \cdot I_{dc}} = 0.785 = 78.5\%$$

iii. Class-AB amplifier:

- A class-AB amplifier is one operating point between class A and class B.
- Hence the output signal is zero for part but less than one-half of an input sinusoidal signal cycle.
- The output current flows for more than 180° but less than 360°.
- a.c. power delivered to the load resistor,

$$P_{o(ac)} = V_c \cdot I_c = \left(\frac{V_P}{\sqrt{2}}\right) \cdot \left(\frac{I_P}{\sqrt{2}}\right) = \frac{V_P \cdot I_P}{2}$$

- And total power dissipation of the two transistors,

$$2P_{C(dc)} = P_{in(dc)} - P_{o(ac)} = V_c \cdot I_c - \frac{V_P \cdot I_P}{2}$$
$$= V_{CC} \cdot \frac{2I_P}{\pi} - \frac{V_P \cdot I_P}{2}$$
$$= 2I_P\left(\frac{V_{CC}}{\pi} - \frac{V_P}{4}\right)$$

- Overall efficiency,

$$\eta_o = \frac{P_{o(ac)}}{P_{in(dc)}} = \frac{\frac{V_P \cdot I_P}{2}}{V_{CC} \cdot \frac{2I_P}{\pi}} = \frac{\pi}{4} \cdot \frac{V_P}{V_{CC}} = 0.785 \frac{V_P}{V_{CC}}$$

- For the largest possible output signal, the peak value of the output voltage is equal to the V_{CC} supply (i.e., $V_P = V_{CC}$). In the case, the overall efficiency is maximum, and its value,

$$\eta_{o(max)} = 0.785 = 78.5\%$$

- The value of collector efficiency is equal to the overall efficiency, whose maximum value is also 78.5%.

iv. Class-C amplifier:

- A class-C amplifier is one in which the operating point is chosen so that the output current (or voltage) is zero for more than one-half of an input sinusoidal signal cycle.
- In class-C amplifier, the Q-point is fixed beyond the extreme end of the characteristics. The output current remains zero for more than half cycle.

- The unturned audio or video voltage amplifier with a resistive load is operated as small signal amplifier under class-A operation.
- class-B amplifiers are mostly used for power amplification in push-pull arrangement.
- class-AB and class-B operation are used with unturned power amplifiers, whereas class-C operation is used with tuned radio frequency amplifiers.

Additional Questions:

Explain briefly about push-pull amplifier

❖ **Introduction:**

- This means **one in on** and another **one is off.**
- It needs same type of transistors(i.e., NPN or PNP).
- Also it needs two transformers in both input and output sides.
- One is input transformer and other is called output transformer.
- Input is applied to input driver transformer's primary winding.
- Both transformers (input and output) is centre tapped one.
- Both are NPN means voltage V_{CC} is positive.
- Both are PNP means voltage V_{CC} is negative.

❖ **Basic principle of operation:**

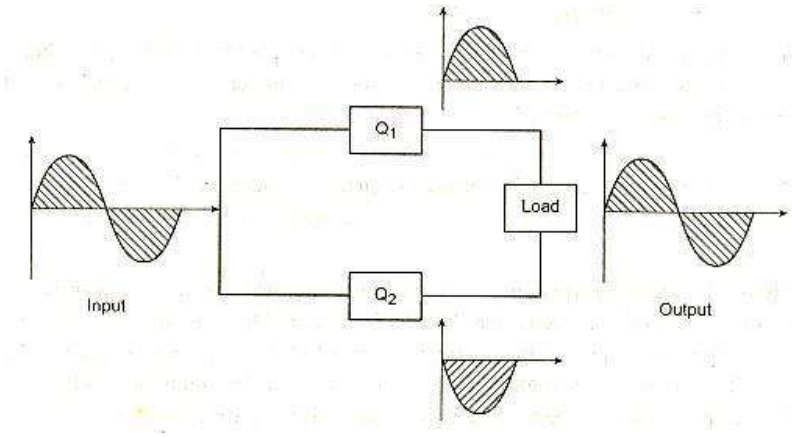


Figure: Basic operation diagram

- During the positive half cycle of the applied input Q_1 is only under ON condition. The positive half cycle is across the load.
- Similarly, During the Negative half cycle of the applied input Q_2 is only under ON condition. So the Negative half cycle is across the load.

❖ **Push-pull class-B amplifier:**

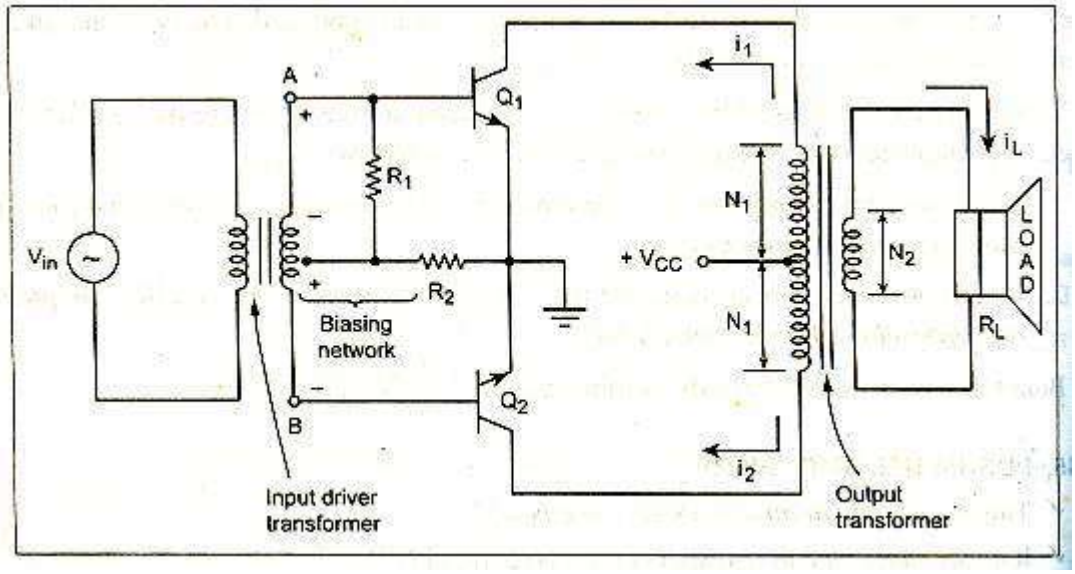


Figure: Push-pull amplifier- class-B

- In the above circuit, both transistors is of NPN type.
- If both are PNP, the supply voltage must be $-V_{CC}$. but basic diagram is same.
- Input driver transfer driver circuit drives the circuit, then the input signal is applied to the primary of the driver transformer.
- The centre tap on the secondary of the driver transformer is grounded. The centre tap on the primary of the output transformer is connected to the supply voltage $+V_{CC}$.
- Whenever the input signal is under positive half cycle, when point A is positive with respect to B, then the transistor Q_1 is in the active region. But Q_2 is under in OFF condition now.So the load gets this positive voltage drop output across it.
- Then, point B is positive with respect to A under negative half cycle. So, Q_1 is in the OFF condition.so the load gets voltage in negative across it due to negative voltage. This is shown in the waveform.
- For the output transformer, the number of turns of each half of the primary is N_1. But in the secondary, it is N_2.
- Hence, the total number of turns in primary side of output transformer is $2N_1$.
- Then turns ratio is $2N_1 : N_2$.
- **D.C operation:**
  - ✓ The Q-point is adjusted on the X-axis such that, $V_{CEQ} = V_{CC}$ and I_{CEQ} is zero. The coordinates of the Q-point are (V_{CC},0). There is no d.c base bias voltage.
- **D.C power input:**
  - ✓ Each transistor output is in the form of half rectified waveform. Hence, if I_m is the peak value of the output current of each transistor, the dc or A_V value is $\frac{I_m}{\pi}$, due to half rectified waveform.
  - ✓ Then, two currents drawn by the two transistors, form the A.C supply are in the same direction.
  - ✓ Therefore, the total D.C or average current drawn from the A.C supply is algebraic sum of the individual average current drawn by each transistor,

$$I_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi} \quad \text{.....(1)}$$

✓ The total d.c power input is given by,

$$P_{dc} = V_{CC} * I_{dc} \quad \text{.....(2)}$$

$$P_{dc} = \frac{2}{\pi} V_{CC} . I_m \quad \text{.....(3)}$$

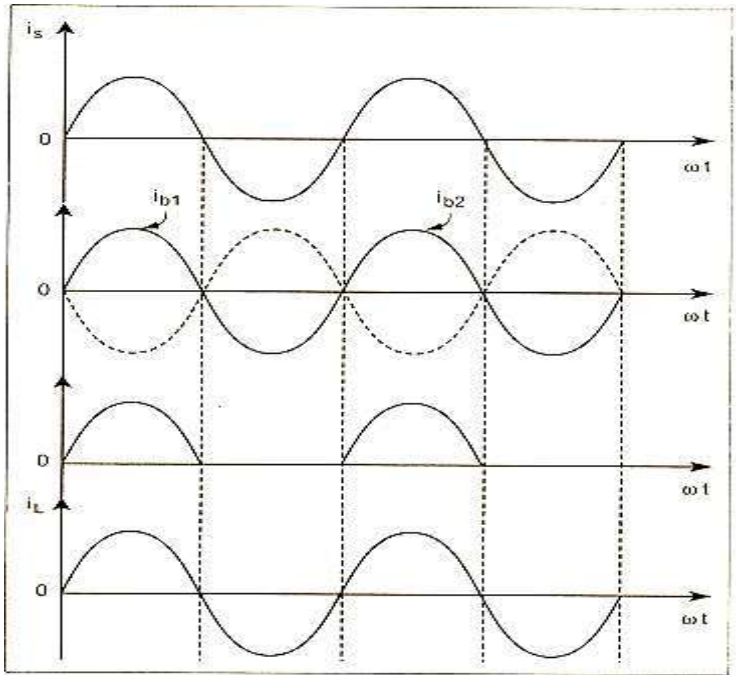


Figure: Waveform output

- **A.C operation:**
  - ✓ When A.C signal is applied to the input driver transformer, for positive half cycle Q_1 transistor is under ON condition. Then, its current flow path is shown in the following diagram.

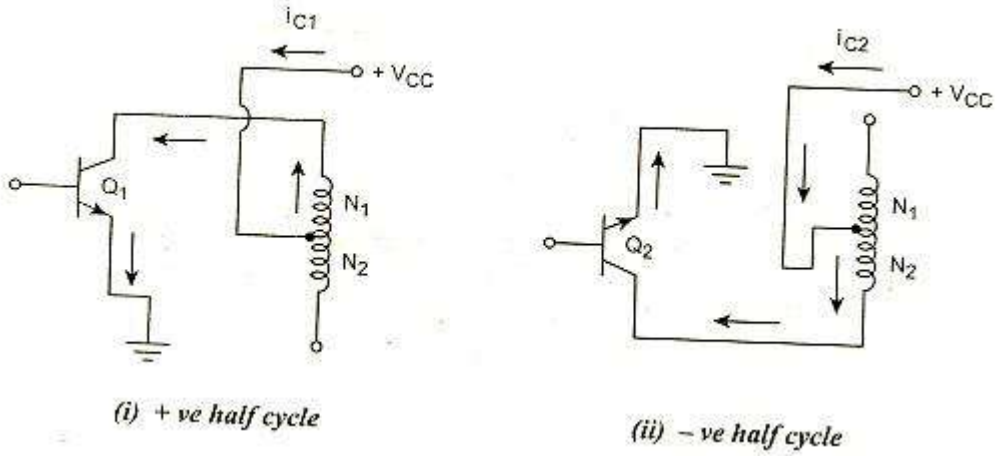


Figure: current path

  - ✓ From the above figure, when Q_1 conducts, lower half of the primary of the input transformer does not carry any current. Hence. Only N_1number of turns carry the current.
  - ✓ While, when Q_2conducts , upper half of the primary does not carry any current. Therefore again only N_1 number of turns carry the current.
  - ✓ Hence, the reflection on the primary can be written as,

$$R_L' = \frac{R_L}{n.n} \ldots\ldots..(4) \text{and} \quad n = \frac{N_2}{N_1} \quad \ldots\ldots..(5)$$

  - ✓ Note that the step down turns ratio is $2N_1 : N_2$ but while calculating the reflected load, the ratio n becomes $N_2 : N_1$.
  - ✓ So each transistor shares equal load which is the reflected load R_L'.

- ✓ The slope of the a.c load line is $\frac{-1}{RL'}$, while the d.c load line istheverticalline passing through the Q on the X-axis. The load lines are shown below.

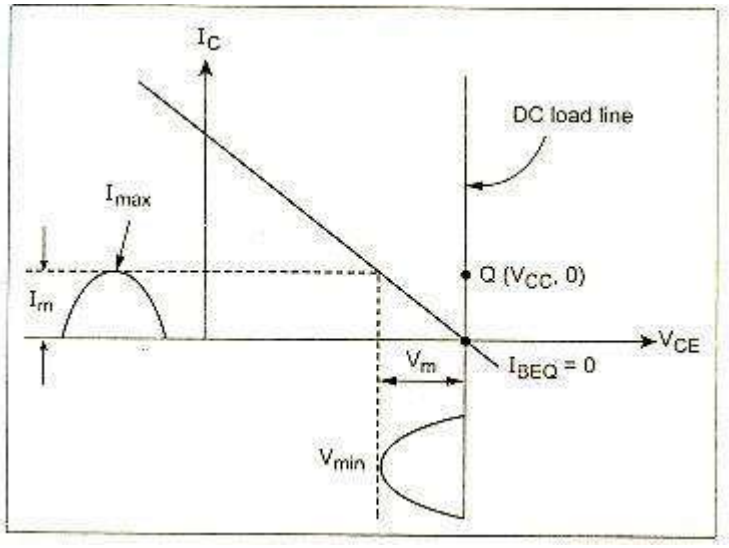


Figure: load lines for push-pull class B amplifier

- ✓ The slope of the a.c load line (magnitude of slope) can be represented in terms of V_m and I_m,

$$\frac{1}{RL'} = \frac{Im}{V_m} \text{ ……..(6)}$$

$$R_L' = \frac{V_m}{I_m} \text{ ……(7)}$$

Here, V_m = peak value of the collector circuit

- **A.C power output:**
  - ✓ As I_m and V_m are the peak values of the output current and the output voltage respectively. Then

$$V_{rms} = \frac{V_m}{\sqrt{2}} \text{ …..(8) and} I_{rms} = \frac{I_m}{\sqrt{2}} \text{ ……(9)}$$

The power output is, $P_{ac} = V_{rms} . I_{rms}$

$$= I_{rms} . R_L' . I_{rms}$$

$$= I_{rms}^2 . R_L' \text{ ..... (10)}$$

$$= V_{rms}^2 / R_L'$$

- **Efficiency:** The efficiency of class-B amplifier can be calculated as follows:

$$\%\eta = \frac{Pac}{P_{dc}} \text{ x 100 .....(11)}$$

$$= \frac{\frac{V_m I_m}{2}}{\frac{2}{\pi} V_{CC} . I_m} * 100 \text{ ……(12)}$$

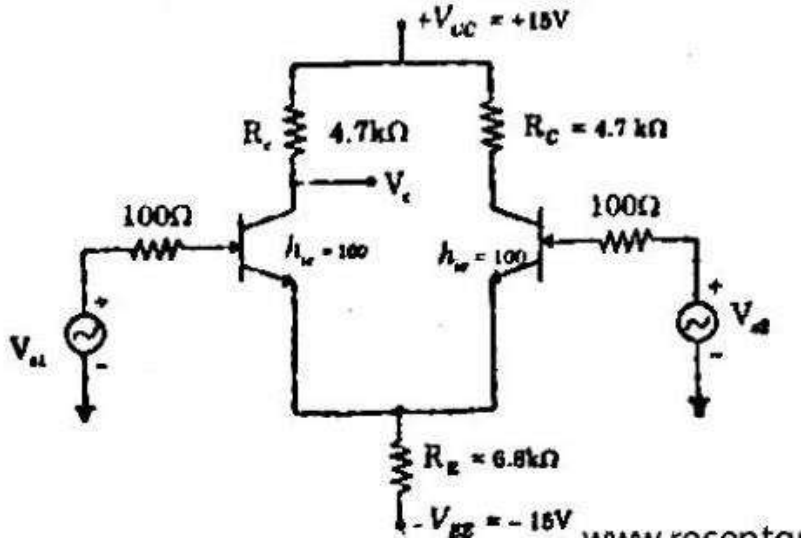
$$= \frac{\pi \ Vm}{4 \ V_{CC}} * 100 \text{ ……..(13)}$$

- **Maximum efficiency:**
  - ✓ As the peak value of the collector voltage V_m increases, the efficiency also increases.
  - ✓ Then the maximum value of V_m is possible which is equal to V_{CC}.

$$\%\eta_{max} = \frac{P_{ac}}{P_{dc}} * 100$$

$$= \frac{\pi \ Vm}{4 \ V_{CC}} * 100 = 78.5\%$$

13. Evaluate the (1) operating point (2)differential gain(3)common mode gain(4)CMRR and (5)output voltage if Vs1=70mV peak to peak at 1 Khz and Vs2=40 mV peak to peak at 1 Khz of dual input balanced output differential amplitude h_{ie}=2.8 KΩ.(Nov/Dec 2016)



1. Operating point value are I_{CQ}, V_{CEQ}. Apply KVL to input side.

$$-I_B R_S - V_{BE} - 2R_E I_E + V_{EE} = 0$$

$$\frac{-I_E}{\beta} R_S - V_{BE} - 2R_E I_E + V_{EE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_S}{\beta}}$$

$$\beta = h_{fe} = 100$$

$$I_E = \frac{15 - 0.7}{2 \times 6.8 \times 10^3 + \frac{100}{100}} = 1.051\, mA$$

$$I_C = I_E = 1.051\, mA$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C = 15 + 0.7 - 1.051 \times 10^{-3} \times 4.7 \times 10^3$$

$$\therefore V_{CEQ} = 10.758\, V$$

Differential gain, A_d

$$= \frac{h_{fe} R_C}{R_S + h_{ie}}$$

$$A_d = \frac{100 \times 4.7 \times 10^3}{100 + 2.8 \times 10^3} = 162.068$$

Common mode gain, A_C

$$= \frac{h_{fe} R_C}{2R_E(1 + h_{fe}) + R_S + h_{ie}}$$

$$A_C = \frac{100 \times 4.7 \times 10^3}{2 \times 6.8 \times 10^3 (1 + 100) + 100 + 2.8 \times 10^3}$$

$$= 0.3414$$

$$CMRR = \frac{A_d}{A_c} = \frac{162.068}{0.3414} = 474.652$$

$$\therefore CMRR = 20\log(474.652) = 53.527\ dB$$

Output voltage, $V_o = A_d V_d + A_c V_c$

$$V_d = V_{s1} - V_{s2} = 70 - 40 = 30\ mV\ (P-P)$$

$$V_c = \frac{V_{s1} + V_{s2}}{2} = \frac{70 + 40}{2} = 55\ mV\ (P-P)$$

$$V_o = 162.068 \times 30 \times 10^{-3} + 55 \times 10^{-3} \times 0.3414$$

$$= 4.86204 + 0.0187$$

$$= 4.88\ V\ (Peak - Peak)$$

14. A parallel resonant circuit has a capacitor of 250 pF in one branch and inductance of 1.2 mH and a resistance of 10Ω in parallel branch. Find (1). Resonant frequency (2). Impedance of the circuit at resonance (3). Q-factor of the circuit. (Nov/Dec 2018)

Solution:

i. Resonant frequency of the parallel tuned circuit is defined as,

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{1.25\ X\ 10^{-3}\ X\ 250\ X\ 10^{-12}} - \frac{10\ X\ 10}{(1.25\ X\ 10^{-3})^2}}$$

$f_r = \frac{1}{2\pi}\ X\ 178836.493$ = 284.7 X 10^3 Hz

f_r= 284.7 KHz

ii. Impedance of the circuit, Z_r is given by,

$$Z_r = \frac{L}{RC} = \frac{1.25\ X\ 10^{-3}}{250\ X\ 10^{-12}\ X\ 10}$$

Z_r = 500000

Z_r = 500 KΩ

iii. Q-factor of the circuit is defined as,

$$Q = \frac{2\pi f_r L}{R} = \frac{2\pi\ X\ 284.7\ X\ 10^3 X\ 1.25\ X\ 10^{-3}}{10} = \frac{2236.02}{10} = 223.6$$

Q = 223.6

15. Compare voltage and power amplifiers. (Nov/Dec 2018)

Voltage Amplifier		Power Amplifier	
1.	The amplitude of input A.C signal is small	1.	The amplitude of A.C signal is large.
2.	The collector current is low (about 1 mA)	2.	The collector current is very high (greater than 100 mA)
3.	RC coupling is used.	3.	Transformer coupling is used
4.	The A.C power output is low	4.	The A.C power output is high
5.	Heat dissipation is less	5.	Heat dissipation is high
6.	The size of power transistor is small	6.	The size of power transistor is large
7.	Current gain is low	7.	Current gain is high
8.	Output impedance is high	8.	Output impedance is low

16. Explain the self-biasing of a JFET. (Nov/Dec 2018)

- Self-bias is the most common type of JFET bias. Recall that a JFET must be operated such that the gate source junction is always reverse-biased.
- The condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for p-channel JFET. This can be achieved using the self-bias arrangement shown in Fig.1
- The gate resistor, R_G, does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V.
- R_G is necessary only to isolate an A.C. signal from ground in amplifier applications.
- The voltage drop across resistor, R_S makes gate source junction reverse biased.

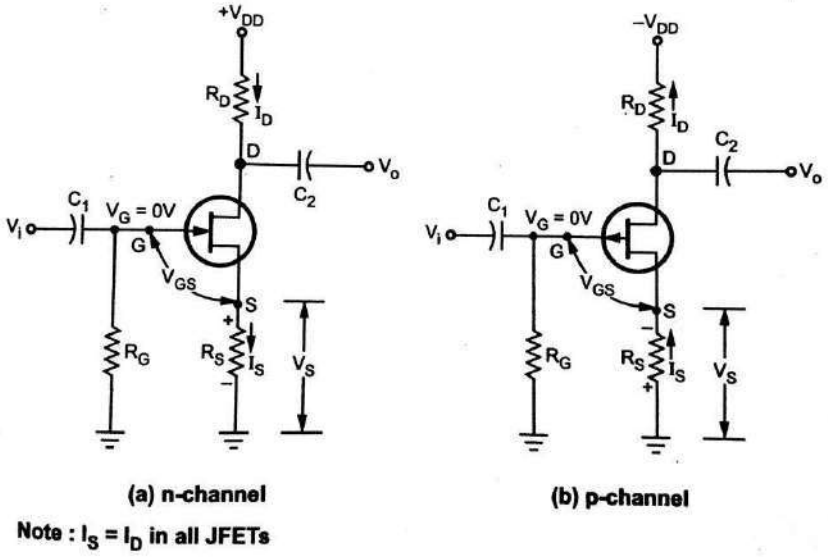


Fig 1: self-bias circuit for JFET

Step 1: Obtain expression for V_{GS}

- For the n-channel FET in Fig. 1(a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then $V_S = I_S R_S = I_D R_S$. The gate to source voltage is,
  $V_{GS} = V_G – V_S = 0 – I_D R_S = - I_D R_S$
- For the p-channel FET in Fig. 1(b), I_S produces a voltage drop across R_S and makes the source negative with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then $V_S = - I_S R_S = -I_D R_S$ the gate to source voltage is
  $V_{GS} = V_G – V_S = 0 – (-I_D R_S) = + I_D R_S$

- In the following D.C. analysis, the n-channel JFET shown in Fig. 1(a) is used to for illustration.
- For D.C. analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent, since $I_G = 0$. This is illustrated in Fig.2.

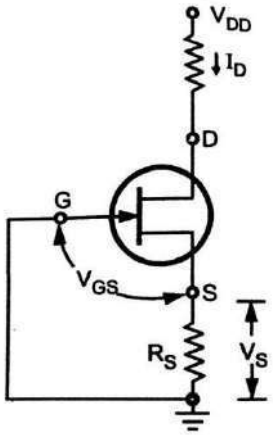


Fig 2: Simplified self-bias circuit for dc analysis

Step 2: Calculate I_{DQ}

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}^2\right]$$

Substituting value of V_{GS} in above equation we get,

$$I_D = I_{DSS}\left[1 - \frac{-I_D R_S}{V_P}^2\right] = I_{DSS}\left[1 + \frac{I_D R_S}{V_P}^2\right]$$

Step 3: Calculate V_{DS}

Applying KVL to the output circuit we get,

$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_S - I_D R_D = V_{DD} - I_D R_S - I_D R_D = V_{DD} - I_D(R_S + R_D)$$

EC8353-ELECTRON DEVICES AND CIRCUITS

UNIT-V FEEDBACK AMPLIFIERS AND OSCILLATORS

PART-A

FEEDBACK AMPLIFIERS

1. Define feedback and feedback factor. Define Positive feedback and Negative feedback.

Feedback: The process of *injecting a fraction of the output voltage of an amplifier into the input* so that it becomes a part of the input is known as feedback.

Feedback Factor: Feedback factor is defined as the ratio of feedback signal (Voltage/Current) to the amplifier output which is given as input to the feedback network. Hence, it is also called as feedback ratio and is denoted by β.
i.e., $\beta = \frac{V_f}{V_o}$; $V_f - Feedback\ Voltage$ $V_O - Amplifier\ Output\ Voltage$

Positive feedback: If the *feedback voltage is in-phase to the input from the source*, i.e., feedback signal in-phase with the original input signal. It is called positive feedback.

Negative feedback: If the *feedback voltage is opposite (out of phase) to the input from the source*, i.e., feedback signal opposes the original input signal. It is called negative or degenerative feedback.

Advantages of negative feedback

2. Mention/List the advantages of negative feedback circuits. (Nov/Dec2015), (May/June2016)
- In negative feedback amplifiers, the **voltage gain** of the amplifier remains **stable**.
- High input resistance of a voltage amplifier can be made larger
- Low output resistance of a voltage amplified can be lowered
- Frequency response improves
- Significant improvement in the linearity of operation
- The transfer gain of the amplifier with feedback can be stabilized against variation in the h parameters.

3. Write the disadvantages of negative feedback in amplifier circuits and how it can be overcome? (April/May 2015)
The main **disadvantage** of using negative or degenerative feedback in amplifier is ***Reduction*** *in* ***Gain***.
The required Gain can be attained by increasing the number of amplifier stages

4. What are the effects of a negative feedback?
a) Reduces noise
b) Reduces distortion
c) Reduces gain
d) Increases band width
e) The gain becomes stabilized with respect to changes in the amplifier active device parameters like h_{fe}.
f) The non-linear distortion is reduced there by increasing the signal handling capacity or the dynamic range of the amplifier.

5. What is the condition required for satisfactory operation of a negative feedback amplifier? (April/May 2019)
The open-loop voltage gain must be much greater than the required closed-loop gain.
Overall Voltage Gain with -ve feedback (Closed-loop Gain), $A_{vf} = \frac{A_v}{1+\beta A_v}$

$$A_{vf} = \frac{A_v}{\beta A_v} \qquad \{Since, \beta A_v \gg 1\}$$

Therefore, $A_{vf} = \frac{1}{\beta}$

{Where A_v is the voltage gain without a feedback and β is the feedback factor is due to negative feedback the gain is reduced by factor $1 + \beta A_v$}

6. With negative feedback the bandwidth of the amplifier increases- True/False?

True.

Bandwidth of amplifier with feedback is greater than bandwidth of amplifier without feedback.

Voltage / current, Series, Shunt feedback

7. Mention the four connections in Feedback.

a. Voltage series feedback.
b. Voltage shunts feedback.
c. Current series feedback.
d. Current shunt feedback.

8. Explain the voltage series feedback.

In this case, the feedback voltage is derived from the output voltage and fed in series with input signal. The input of the amplifier and the feedback network are in series is also known as series parallel in parallel, hence this configuration is also known as series parallel feedback network.

9. Explain the voltage shunt feedback.

The input of amplifier and the feedback network are in parallel and known as parallel –parallel feedback network. This type of feedback to the ideal current to voltage converter, a circulating having very low input impedance and very low output impedance.

10. Explain the current series feedback.

When the feedback voltage derived from the load current and is fed in series with the input signal, the feedback is said to be current series feedback, the inputs of the amplifier and the feedback network are in series and the output are also in series. This configuration is also called as series-series feedback configuration.

11. Explain the current shunt feedback.

When the feedback voltage is derived from the load current and a fed in parallel with the input signal, the feedback is said to be current shunt feedback. Here in the inputs of the amplifier and the feedback network are in parallel and the outputs are in series. This configuration is also known as parallel series feedback.

12. Which is the most commonly used feedback arrangement in cascaded amplifier and why? (Nov/Dec-2013-R13)

A voltage series feedback s commonly used in cascaded amplifiers. Since, it has high input impedance and low output impedance that is needed for cascaded amplifiers.

Positive feedback (Oscillators)

13. What is Oscillator?

Oscillator is an electronic device which generates electrical oscillations (i.e., repeated waveforms) of required frequency. It is used for converting DC energy into AC energy of the desired frequency.

{An oscillator is a circuit which generates an alternating voltage without any input signal. Instead of external input signal, it uses feedback path through which it provides its own input signal.
It is used for converting DC energy into AC energy of the desired frequency.}

14. What are sustained Oscillations?

Electrical oscillations in which amplitude does not change with time are called sustained oscillations. It is called as un-damped oscillations.

15. What is frequency of Oscillations?

The frequency at which circuit satisfies both the Barkhausen conditions i.e. $|A\beta| = 1$ and $\angle A\beta = 0°$ or $360°$ simultaneously is called frequency of oscillations

16. Classify the various oscillators based on the output waveforms, circuit components, operating frequencies and feedback used.

According to the *nature of waveform generated*.

1. *Sinusoidal or Harmonic Oscillators*
2. *Non-sinusoidal or Relaxation oscillators*

Based on circuit components. (Nov/Dec 2017)

According to the frequency determining networks,

1. RC oscillators (Phase-shift Oscillator and Wien Bridge Oscillator)
2. LC oscillators (Hartley Oscillator and Colpitts Oscillator)
3. Crystal oscillators

According to the frequency of the Generated Signals

1. AFO (Audio Frequency Oscillators) – upto 20 KHz
2. RFO (Radio Frequency Oscillators) – 20 KHz to 30 MHz
3. VHFO (Very High Frequency Oscillators) - 30 MHz to 300 MHz
4. UHFO (Ultra High Frequency Oscillators) - 300 MHz to 3 GHz
5. MFO (Microwave Frequency Oscillators) – above 3 GHz

17. What are the types of sinusoidal oscillator? [or] Mention the different types of sinusoidal oscillator?

a) RC phase shift Oscillator.
b) Wein bridge Oscillator.
c) Hartley Oscillator
d) Colpitts Oscillator
e) Crystal Oscillator

18. Name two low frequency oscillators?

a) RC phase shift oscillator.
b) Wein bridge oscillator.

19. Name three high frequency oscillators?

The high frequency oscillators are

a) Hartley oscillator.
b) Colpitts oscillator.
c) Crystal oscillator

Condition for oscillations

20. Write the conditions for a Oscillator. (OR)
State. Barkhausen criterion (Barkhausen condition) for sustained oscillations. (Nov/Dec-2012,2011,09), (May/June2016) (Nov/Dec-2016) (May 2017)

The Barkhausen criterion **f**or obtaining sustained oscillations,

1. The feedback voltage must be in-phase with the input, i.e., total phase-shift around the closed-loop must be 0° or 360°, and
2. Magnitude of the loop gain must be unity i.e., $|A\beta| = 1$

Where, A – Open loop Gain of the system & β – Feedback ratio.

Phase Shift and Wien bridge oscillator (RC oscillators)

21. Why an RC phase shift oscillator is called so?

An RC network products 180^o phase shift. Hence it is called RC phase shift oscillator.

22. List the advantages of phase shift oscillator. (May/June-2012)

- The phase shift oscillator does not required conductance or transformers.
- It is suitable for the low frequency range i.e., from a few hertz to several 100 kHz. The upper frequency is limited because the impedance of RC network may become so small that it loads the amplifier heavily.

23. Write the disadvantages of Phase shift oscillator.

1. It is necessary to change the C or R in all the three RC networks simultaneously for changing the frequency of oscillations. This is practically difficult.
2. It is not suitable for high frequencies.

24. Which oscillator uses both positive and negative feedback?

Wien bridge oscillator.

Hartley and Colpitts oscillators. (LC oscillators)

25. Distinguish between LC and RC oscillator.

LC Oscillator	RC Oscillator
It operates at high frequencies	It operates at low frequencies
It is suitable for RF only	It is suitable for AF only
Frequency is variable	The frequency is constant. It is known as fixed frequency oscillator.

26. Write the main drawback of LC oscillators.

1. The frequency stability is not very good.
2. They are too bulky and expensive and cannot be used to generate low frequencies.

27. What is the advantage of a colpitts oscillator compared to a phase shift oscillator? (Nov/Dec 2015)

ii) The advantage of colpitts oscillator is the frequency of oscillation is very high.

iii) We can vary the frequency of oscillation.

Crystal oscillators.

28. What is piezo electric effect? (May/June-2013)

The piezo electric crystal exhibits a property, that is, if a mechanical stress is applied across one face, an electrical potential is developed across the opposite face. The inverse is also true. This phenomenon is called piezo-electric effect.

29. Why Quartz crystal is commonly used in crystal oscillator?

Quartz crystals are generally used in crystal oscillator because of their great mechanical strength, simplicity of manufacture and abeyance to the piezo electric effect accurately.

30. What are the advantages of crystal oscillators? (NOV/DEC 2012)

The advantages of crystal oscillators are

a) Excellent frequency stability.
b) High frequency of operation
c) Automatic amplitude control.
d) It is suitable for only low power circuits
e) Large amplitude of vibrations may crack the crystal.
f) It large in frequency is only possible replacing the crystal with another one by different frequency.

31. An oscillator operating at 1 MHz has a stability of 1 in 10^4. What will be the minimum value of frequency generated? (April/May 2019)

The typical frequency stability of oscillators that do not use CRYSTAL is about 1 in 10^4.

The minimum value of frequency generated might be 100KHZ *or lower than* 1MHZ *for the oscillator operating at* 1MHZ.

{If the crystal is used, the frequency stability can be improved to better than 1 in 10^6, which gives a ±1 Hz variation in the output of a 1 MHz oscillator.}

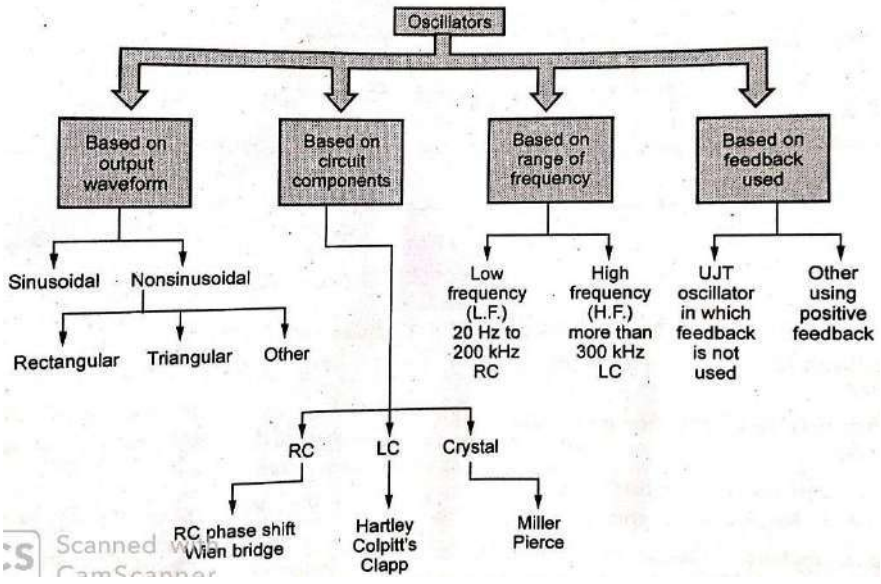
32. How does an oscillator differ from an amplifier? (or) Differentiate oscillator & amplifier. [Nov/Dec 2013] [Nov/Dec 2016]

S.No.	Oscillators	Amplifiers
1	They are self-generating circuits. They generate waveforms like sine, square and triangular waveforms of their own without having input signal.	They are not self-generating circuits. They need a signal at the input and they just increase the level of the input waveform.
2	It has infinite gain	It has finite gain
3	Oscillator uses positive feedback.	Amplifier uses negative feedback.

33. Compare RC Phase-Shift Oscillators and Wien Bridge Oscillator.

Sr. No.	RC phase shift oscillator	Wien bridge oscillator
1.	It is a phase shift oscillator used for low frequency range.	It is also a phase shift oscillator used for low frequency range.
2.	The feedback network is RC network with three RC sections.	The feedback network is lead-lag network which is called Wien bridge circuit.
3.	The feedback network introduces 180° phase shift.	The feedback network does not introduce any phase shift.
4.	Op-amp is used in an inverting mode.	Op-amp is used in non-inverting mode.
5.	Op-amp circuit introduces 180° phase shift.	Op-amp circuit does not introduce any phase shift.
6.	The frequency of oscillations is, $f = \frac{1}{2\pi RC\sqrt{6}}$	The frequency of oscillations is, $f = \frac{1}{2\pi RC}$
7.	The amplifier gain condition is. $\|A\| \geq 29$	The amplifier gain condition is, $\|A\| \geq 3$
8.	The frequency variation is difficult.	Mounting the two capacitors on common shaft and varying their values, frequency can be varied.

34. Classification of Oscillators



PART-B

Advantages of negative feedback & positive feedback

1. What is meant by feedback? What are the types of feedback and effects of negative feedback? (May/June-2012) (Nov/Dec 2017)

Negative feedback

If β is negative, the voltage feedback subtracts from the input yielding a lower output and reduced voltage gain. Hence this feedback is known as negative feedback.

Positive feedback

If the phase of the voltage feedback is such as to increase the input, then β is positive and the result is positive feedback.

Increase Stability:

The voltage gain due to a negative feedback is given by

$$A_{vf} = \frac{A_v}{1+\beta A_v} \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Where A_v is the voltage gain without a feedback and β is the feedback factor is due to negative feedback the gain is reduced by factor $1 + \beta A_v$

If $\beta A_v >> 1$ then $A_{vf} = \frac{A_v}{\beta A_v} = \frac{1}{\beta}$

Hence the gain of the amplifier with feedback has been stabilized against such problems as ageing of a transistor or a transistor being re-placed by a transistor with a different value of β.

Sensitivity of transfer gain:

The fractional change in amplification with feedback divided by the fractional change without feedback is called the sensitivity of the transfer gain

From equ 1 $\frac{dA_{vf}}{dA_v} = \frac{(1+\beta A_v)-A_v\beta}{(1+\beta A_v).^2} = \frac{1}{(1+\beta A_v).^2}$

$$\frac{dA_{vf}}{dA_v} = \frac{1}{((1+\beta A_v)^2)}$$

$$dA_{vf} = \frac{dA_v}{(1+\beta A_v)^2}$$

Dividing both side by A_{vf}

$$\frac{dA_{vf}}{A_{vf}} = \frac{dA_v}{((1+\beta A_v)^2).A_{vf}}$$

Instead of A_{vf} $sub\ \frac{A_v}{1+\beta A_v}$ in above equation

$$\frac{dA_{vf}}{A_{vf}} = \frac{dA_v}{((1+\beta A_v)^2).(\frac{A_v}{1+\beta A_v})}$$

$$= \frac{dA_v}{A_v(1+\beta A_v)}$$

Taking absolute value of the resultant equation we get

$$\frac{dA_{vf}}{A_{vf}} = \frac{1}{|1+\beta A_v|} \left|\frac{dA_v}{A_v}\right| \ldots\ldots\ldots\ldots\ldots\ldots 3$$

$$\text{Sensitivity} = \frac{\frac{|dA_{vf}|}{A_{vf}}}{\left|\frac{dA_v}{A_v}\right|} = \frac{1}{|1+\beta A_v|} \ldots\ldots\ldots\ldots\ldots\ldots\ldots 4$$

The densitivity is reciprocal of sensitivity. Hence

$$D = 1 + A_v\beta \ldots\ldots\ldots\ldots\ldots\ldots 5$$

Frequency distortion

From equ 1 we find that for a negative feedback amplifier having $A_v\beta >> 1$ the gain withfeedback is $A_{vf} = 1/\beta$. If the feedback network does not contain any reactive elements the gain is not function of frequency.

Reduction in noise

There are many sources of noise is an amplifier. If the noise present at the output is N and the amplifier gain is A. then the noise present in the amplifier with negative feedback is

$$N1 = \frac{N}{1+\beta A_v}.$$

Reduction in distortion

Let us assume that the distortion in the absence of feedback is D. Because the effect of feedback the distortion present at the input is equal to

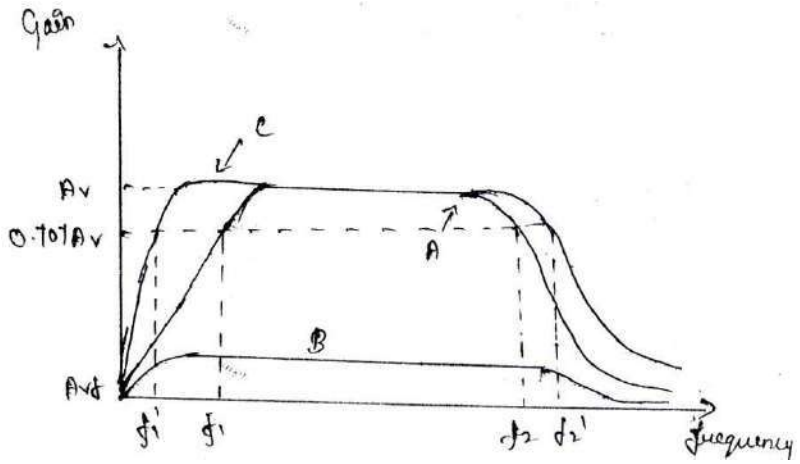
$$D_f = \frac{D}{1+\beta A_v}$$

Bandwidth

If the bandwidth of an amplifier without feedback is given by

$$Bw_f = BW(1+\beta A_v)$$

In curve a source the frequency response of an amplifier without feedback when a negative feedback is introduced the gain of the amplifier decreases.



Frequency response of an amplifier with and without feedback

Obtain curve C. from fig we can observe that there is decrease in the lower cutoff frequency and increase in upper cutoff frequency hence the bandwidth increases. Therefore β increases Bandwidth also increases ***Loop Gain***

A loop gain is used to describe the product of voltage gain A_v and feedback factor β. The amount of feedback introduced into an amplifier may be expressed in decibels according to the following definition.
F=feedback in db

$$= 20 \log \frac{A_{vf}}{A_v}$$

$$= 20 \log \frac{1}{1 + \beta A_v}$$

2. Advantages of Negative feedback in amplifiers. (Nov/Dec 2018)

The advantages of negative feedback in amplifiers are listed as follows.

1. The negative feedback amplifiers, the voltage gain of an amplifier remains stable.
2. It reduces the non-linear distortion produced in large signal amplifiers.
3. It improves the frequency response of the amplifier.
4. It increases the stability of the circuit.
5. Negative feedback increases the input impedance and decreases the output impedance of the amplifier.
6. It decreases the noise voltage in the amplifier.
7. Negative feedback amplifier is less sensitive to variations in amplifier parameters.
8. It increases the amplifier bandwidth.
9. The input and output impedances of feedback amplifier can be adjusted to desired value.
10. It has less phase, amplitude and frequency distortion.
11. Amplifier with negative feedback operates linearly.
12. Operating point of amplifier can be stabilized.

3. With proper mathematical derivation, proven that bandwidth increases in a negative feedback amplifier. (April/May 2019)

The negative feedback increases amplifier bandwidth which can be proven mathematically as below

ADDITIONAL EFFECTS OF NEGATIVE FEEDBACK

Decibels of Feedback

Negative feedback can be measured in decibels. A statement that 40 dB of feedback has been applied to an amplifier means that the amplifier gain has been reduced by 40 dB (that is, by a factor of 100). Thus,

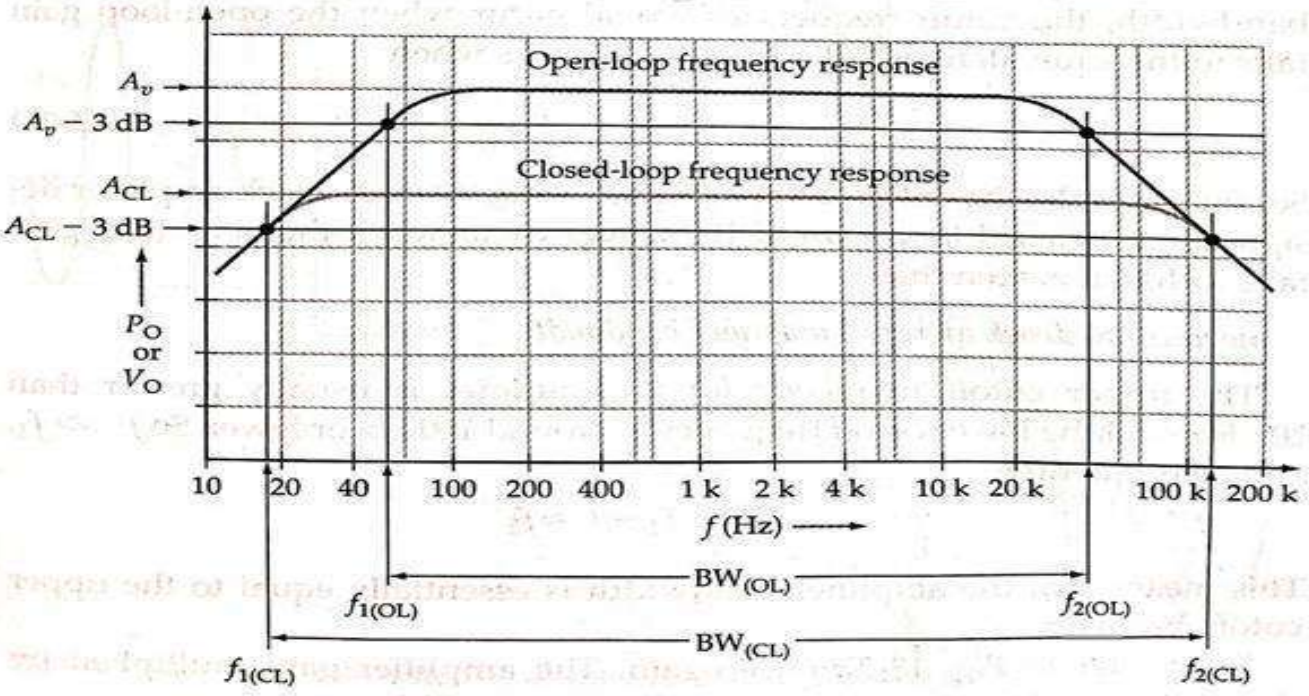
$$A_{CL} = A_v - 40 \text{ dB} = \frac{A_v}{100}$$

Bandwidth

Consider the typical gain-frequency response of an amplifier, as illustrated in Fig. . Without negative feedback, the amplifier open-loop gain (A_v) falls off to its lower 3 dB frequency ($f_{1(OL)}$), as illustrated. This is usually due to the impedance of bypass capacitors increasing as the frequency decreases. Similarly, the open-loop upper cutoff frequency ($f_{2(OL)}$) is produced by transistor cutoff, by shunting capacitance, or by a combination of both.
the circuit open-loop bandwidth is given by

$$BW_{OL} = f_{2(OL)} - f_{1(OL)}$$

Now look at the typical frequency response for the same amplifier when negative feedback is used. The closed-loop gain (A_{CL}) is much smaller than the open-loop gain, and A_{CL} does not begin to fall off (at high or low frequen-



Amplifier frequency response with and without negative feedback. Negative feedback extends the amplifier bandwidth.

cies) until A_v (open-loop gain) falls substantially. Consequently, $f_{1(CL)}$ is much lower than $f_{1(OL)}$, and $f_{2(CL)}$ is much higher than $f_{2(OL)}$. So the circuit bandwidth with negative feedback (the closed-loop bandwidth) is much greater than the bandwidth without negative feedback.

$$BW_{CL} = f_{2(CL)} - f_{1(CL)}$$

$$A_{CL} = \frac{A_v}{1 + A_v B}$$

It can be shown that there is a 90° phase shift associated with the open-loop gain at frequencies below $f_{1(OL)}$ and above $f_{2(OL)}$. Thus, above Eq. must be rewritten as

$$A_{CL} = \frac{-jA_v}{1 - jA_v B}$$

or

$$|A_{CL}| = \frac{A_v}{\sqrt{[1 + (A_v B)^2]}}$$

When $A_v = 1/B$,

$$|A_{CL}| = \frac{1/B}{\sqrt{[1 + 1]}} = \frac{A_{CL}}{\sqrt{2}}$$

$$= A_{CL} - 3 \text{ dB}$$

Thus, for a negative feedback amplifier designed to have the widest possible bandwidth, the cutoff frequencies would occur when the open-loop gain falls to the equivalent of $1/B$. Thus, $f_{2(CL)}$ occurs when

$$A_v = 1/B \approx A_{CL}$$

So, for example, the cutoff frequencies for a negative feedback amplifier designed for a closed-loop gain of 100 would occur when the open-loop gain falls to 100. It is seen that

negative feedback increases amplifier bandwidth.

The upper cutoff frequency for an amplifier is usually greater than 20 kHz, and the lower cutoff frequency is around 100 Hz or lower. So $f_2 \gg f_1$, and consequently,

$$BW = f_2 - f_1 \approx f_2$$

This means that the amplifier bandwidth is essentially equal to the upper cutoff frequency.

Now refer to Fig. once again. The amplifier gain multiplied by the upper cutoff frequency is a constant quantity. This is known as the *gain-bandwidth product*. Therefore,

$$A_{CL} \times f_{2(CL)} = A_v \times f_{2(OL)}$$

or

$$f_{2(CL)} = \frac{A_v f_{2(OL)}}{A_{CL}} \qquad (13\text{-}27)$$

Thus the closed-loop upper cutoff frequency for a negative feedback amplifier can be calculated from the open-loop upper cutoff frequency, the open-loop gain, and the closed-loop gain.

TYPES OF NEGATIVE FEEDBACK AMPLIFIER

4. Explain the various types of feedback amplifier (May 2017)

(OR)

With a neat block diagram, explain the operation of Current Shunt Feedback Amplifier.

(OR)

Determine R_{if}, R_{of}, A_v, A_{vf} for the following feedback amplifier

A. **Voltage series feedback amplifier (Series-Shunt feedback amplifier) (Nov/Dec 2016) (May 2017)**
B. **Current Series Feedback Amplifier (Shunt-Series feedback amplifier)**
C. **Current Shunt Feedback Amplifier (Series-Series feedback amplifier) (May 2017)**
D. **Voltage Shunt Feedback Amplifier (Shunt-Shunt feedback amplifier)**

(OR)

Discuss the effect of voltage series feedback and derive the expression for input resistance, output resistance and voltage gain.

(OR)

Discuss about the following feedback configurations of amplifiers and obtain the feedback factor and closed loop gain. ***(April/May 2018-R13)***

A. **Shunt-Shunt Feed Back**
B. **Series-Series Feed Back**
C. **Shunt-Series Feed Back**
D. **Series-Shunt Feed Back**

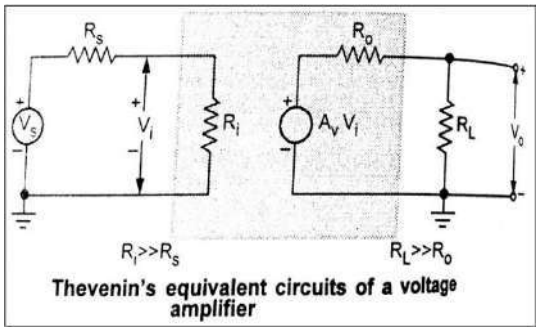
Feedback amplifier, the output signal sampled may be either voltage or current and sampled signal can be mixed either is series or in shunt with the input

The four types of amplifiers, they are

- Voltage series feedback amplifier (Series-Shunt feedback amplifier) **(Nov/Dec 2016) (May 2017)**
- Current Series Feedback Amplifier (Shunt-Series feedback amplifier)
- Current Shunt Feedback Amplifier (Series-Series feedback amplifier) **(May 2017)**
- Voltage Shunt Feedback Amplifier (Shunt-Shunt feedback amplifier)

(A) VOLTAGE SERIES AMPLIFIER:

With proper mathematical derivation, proven that output resistance reduces in a negative feedback amplifier. Assume a series shunt feedback scheme. (April/May 2019)

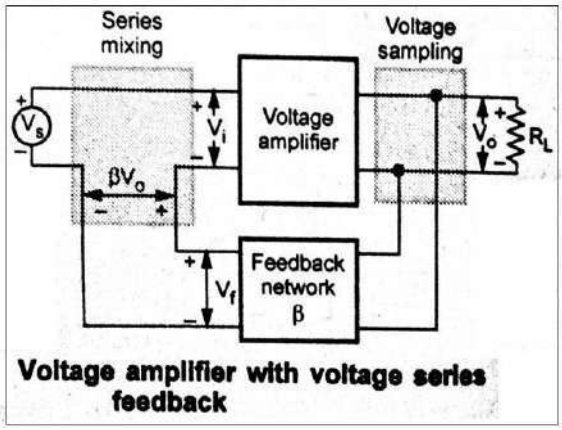


Thevenin's equivalent circuits of a voltage amplifier

- R_i – input resistance
- R_s – source resistance
- R_L – load resistance
- R_O – output resistance
- A_V – voltage gain

- $R_i >> R_S$ then $V_i = V_s$
- $R_L >> R_o$ then $V_o = A_V V_i = A_v V_s$
- Amplifier provides a voltage output proportional to the voltage input
- The proportionality factor does not depend on magnitudes of the source an load resistance
- Hence it is called voltage amplifier

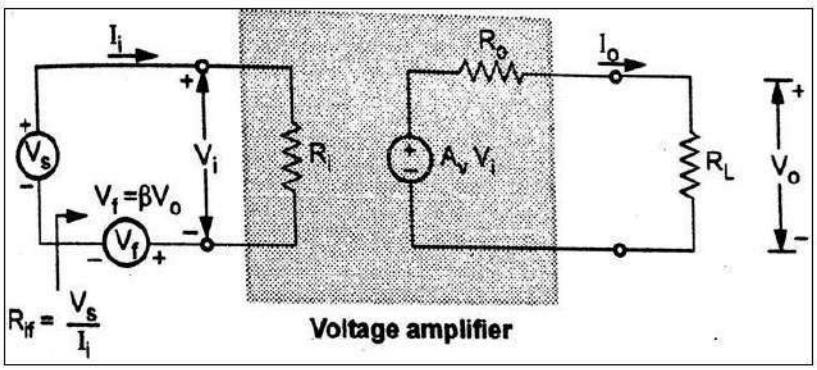
Feedback Topology



Voltage amplifier with voltage series feedback

Input resistance

Step 1: equivalent circuit



Step 2: obtain expression for V_S

Applying KVL to the input side we get,

$V_S - I_i - V_f = 0 \qquad \therefore V_s = I_i R_i + V_f = I_i R_i + \beta V_o$

$\therefore \ V_f = \beta V_o$

Step 3: obtain expression for V_o in terms of I_i

The output voltage V_o is given as

$$V_o = \frac{A_V V_i R_L}{R_O + R_L} = A_V \ V_i \quad where, \qquad A_v = \frac{A_v R_L}{R_o + R_L}$$

$V_o = A_v \ I_i \ R_i \qquad\qquad \therefore V_i = I_i \ R_i$

Step 4: obtain expression for R_{if}

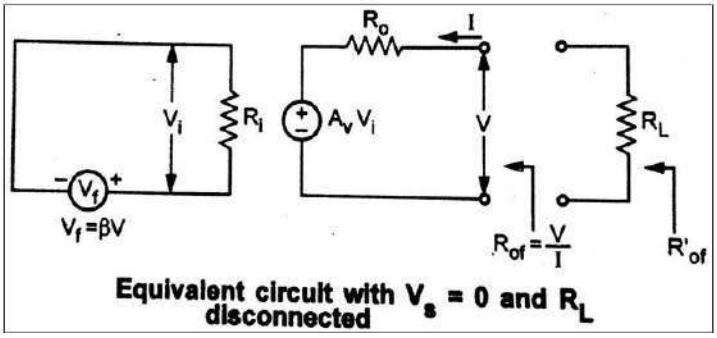
Substituting value of V_0 from above equation we get

$V_S = I_i R_i + \beta A_v I_i R_i$ $\quad\quad\quad\quad$ $\therefore R_{if} = V_s / I_i = R_i + \beta A_v R_i$

$R_{if} = R_i (1+\beta A_v)$

Output Resistance

Step 1: Equivalent circuit



Equivalent circuit with $V_s = 0$ and R_L disconnected

Step 2: obtain expression for I in terms of V

Applying KVL to the output side we get

$A_v V_i + IR_0 - V = 0$ $\quad\quad\quad\quad$ $\therefore I = \frac{V - A_V V_i}{R_0}$

The input voltage is given as

$V_i = - V_f = -\beta V$ $\quad\quad\quad\quad$ $\therefore V_s = 0$

Substituting the V_i from above equation we get

$$I = \frac{V + A_v \beta V}{R_0} = \frac{V(1 + \beta A_V)}{R_0}$$

Step 3: obtain expression for R_{of}

$$R_{of} = \frac{V}{I} \qquad R_{of} = \frac{R_o}{(1 + \beta A_v)}$$

Step 4: obtain expression for $R_{of}^{'}$

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{Of} X R_L}{R_{Of} + R_L} = \frac{\left(\frac{R_O}{1+\beta A_V}\right) X R_L}{\frac{R_O}{(1+\beta A_V)} + R_L}$$

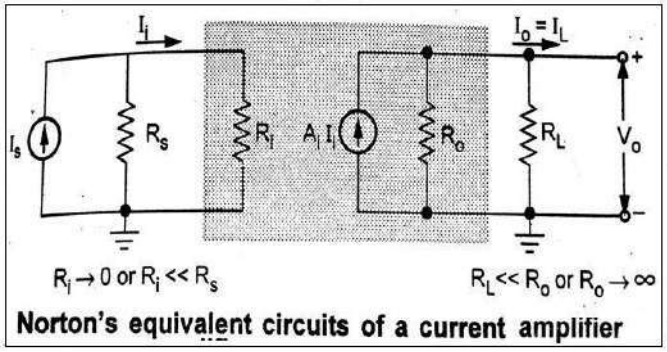
$$= \frac{R_O R_L}{R_O + R_L(1+\beta A_V)} \quad = \frac{R_O R_L}{R_O + R_L + \beta A_V R_L}$$

Dividing numerator and denominator by $(R_o + R_L)$

$$R' = \frac{\frac{R_o R_L}{R_o + R_L}}{1 + \frac{\beta A_v R_L}{R_o + R_L}} \quad \dot{R}_o' R_L = \overline{R_o + R_L} \quad and \quad A = \frac{A_v R_L}{R_o + R_L}$$

$$R_{of}' = \frac{R_o'}{1 + \beta A_v}$$

(B)<u>CURRENT SERIES AMPLIFIER:</u>

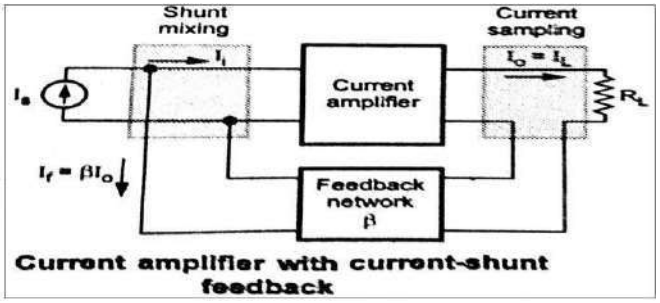


Norton's equivalent circuits of a current amplifier

- R_i – input resistance
- R_s – source resistance
- R_L – load resistance
- R_O – output resistance
- A_I – current gain

- $R_s >> R_i$ and $I_i = I_s$
- $R_o >> R_L$ $I_L = A_I I_i$
- Amplifier provides a current output proportional to the current input
- The proportionality factor does not independent on source and load resistance
- Hence it is called current amplifier

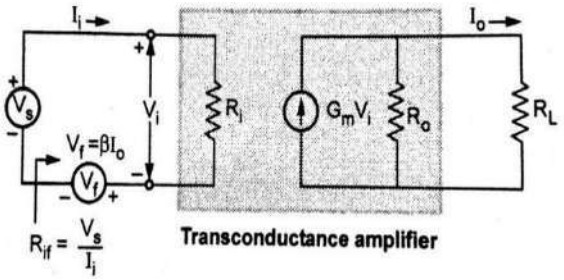
Feedback Topology



Current amplifier with current-shunt feedback

Input Resistance

Step 1: equivalent circuit



Transconductance amplifier

Step 2: obtain expression for V_S

Applying KVL to the input side we get,

$V_S - I_i R_i - V_f = 0 \qquad \therefore V_s = I_i R_i + V_f = I_i R_i + \beta I_o$

$\therefore \ V_f = \beta I_o$

Step 3: obtain expression for I_o in terms of V_i

The output current I_o is given by

$$I_o = \frac{G_m V_i R_o}{R_o + R_L} = G_M V_i \text{ where } G_M = \frac{G_m R_o}{R_o + R_L}$$

Step 4: obtain expression for R_{if}

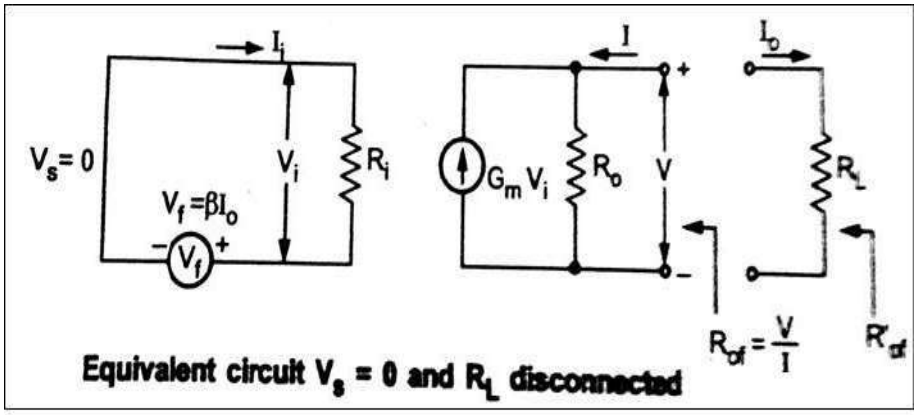
Substituting value of I_o from above equation

$V_S = I_i R_i + \beta G_M V_i = I_i R_i + \beta G_M I_i R_i \qquad \{\text{Since, } V_i = I_i R_i\}$

$R_{if} = V_s / I_i = R_i (1 + \beta G_M)$

Output Resistance

Step 1: equivalent circuit



Step 2: obtain expression for I in terms of V

Applying KVL to the output node we get

$$I = \frac{V}{R_o} - G_m V_i$$

The input voltage is given as $V_i = -V_f = -\beta I_o = \beta I \qquad \therefore I_o = -I$

Substituting value of V_i from above equation we get

$$I = \frac{V}{R_o} - G_m \beta I \qquad \frac{V}{R_o} = I + G_m \beta I = I(1 + G_m \beta)$$

Step 3: obtain expression for R_{of}

$$R_{of} = \frac{V}{I} = R_o(1 + G_m\beta)$$

$$R'_{of} = R_{of} || R_L = \frac{R_{of}\, X\, R_L}{R_{of} + R_L}$$

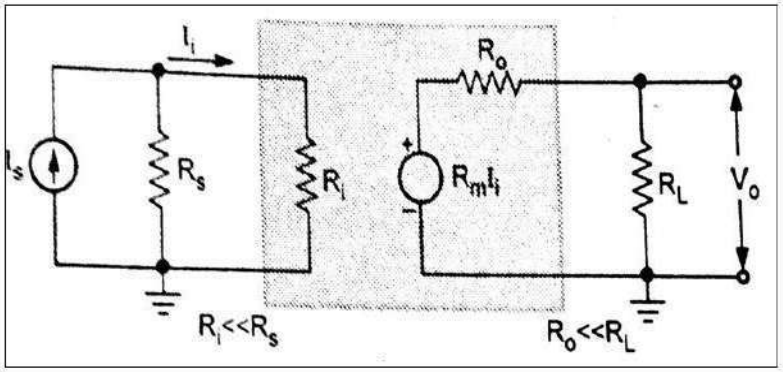
$$= \frac{R_o(1 + \beta G_m)R_L}{R_o(1 + \beta G_m) + R_L} = \frac{R_o R_L(1 + \beta G_m)}{R_o + R_L + \beta G_m R_o}$$

Dividing numerator and denominator by $R_o + R_L$ we get

$$R_{fo} = \frac{\frac{R_L R_o(1 + \beta G_m)}{R_o + R_L}}{1 + \frac{\beta G_m R_o}{R_o + R_L}}$$

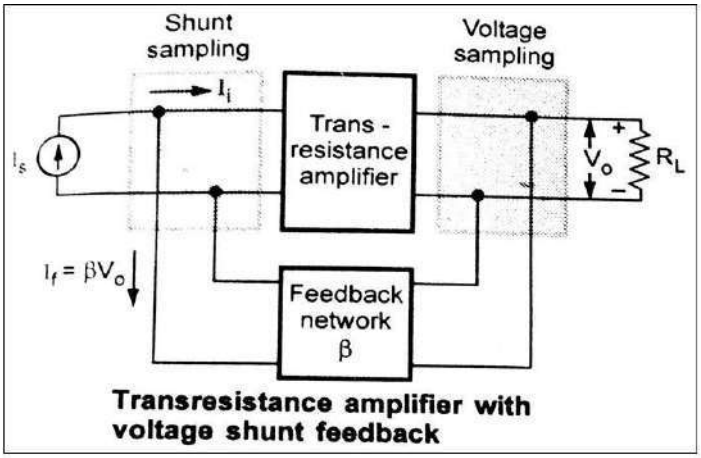
$$R'_{of} = \frac{R'_o(1 + \beta G_m)}{1 + \beta G_m} \qquad \therefore R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } G_M = \frac{G_m R_o}{R_o + R_L}$$

(C) VOLTAGE SHUNT AMPLIFIER



- $R_i << R_s$ and $R_o << R_s$'
- Since $R_i << R_s$'
- $I_i = I_s$ and $R_o << R_L$, $V_o = R_m I_s$
- Where $R_m = V_o / I_s$ is the transfer or mutual resistance

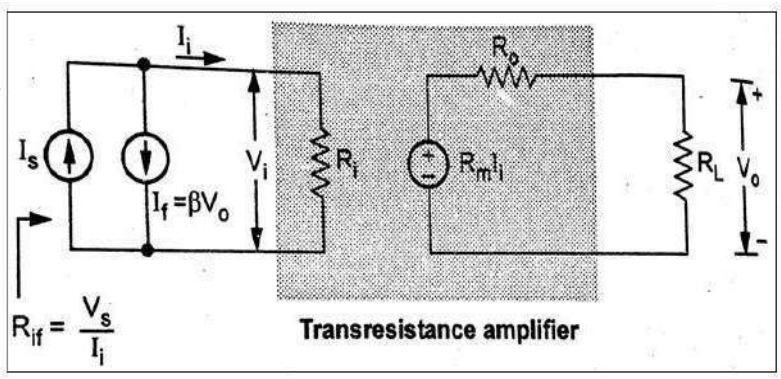
Feedback Topology



Transresistance amplifier with voltage shunt feedback

Input Resistance

Step 1: Equivalent Circuit



Step 2: obtain expression for I_s

Applying KCL at input node we get

$I_s = I_i + I_f = I_i + \beta V_o$ $\quad\quad\quad\quad$ $\therefore I_f = \beta V_o$

Step 3: obtain expression for R_{if}

The output voltage V_o is given by

$$V_o = \frac{R_m I_i R_o}{R_o + R_L} = R_M I_i \quad \text{where } R_M = \frac{R_m R_o}{R_o + R_L}$$

Step 4: obtain expression for R_{if}

Substituting value of V_o from above equation we get

$I_s = I_i + \beta R_M I_i = I_i (1 + \beta R_M)$

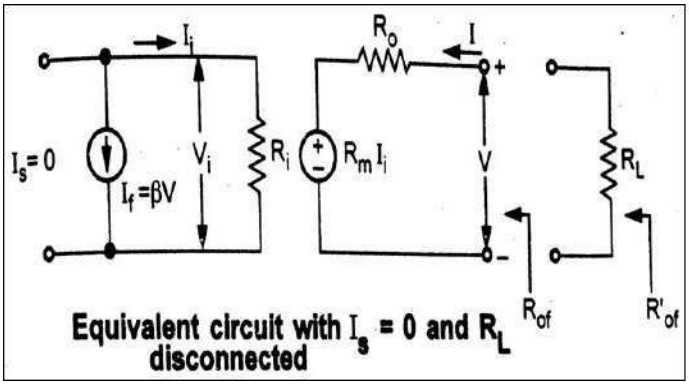
The input resistance with feedback R_{if} is given by

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i(1+\beta R_M)} \qquad \therefore R_i = \frac{V_i}{I_i}$$

$$\therefore R_{if} = \frac{R_i}{(1+\beta R_M)}$$

Output Resistance

Step 1: Equivalent Circuit



Step 2: obtain expression for I in terms of V

Applying KVL to the output side we get

$R_m I_i + I R_o - V = 0 \qquad \therefore I = \frac{V - R_m I_i}{R_o}$

The input current is given as

$I_i = - I_f = - \beta V$

Substituting I_i in above equation we get

$$I = \frac{V + R_m \beta V}{R_o} = \frac{V(1 + R_m \beta)}{R_o}$$

Step 4: obtain expression for R'_{of}

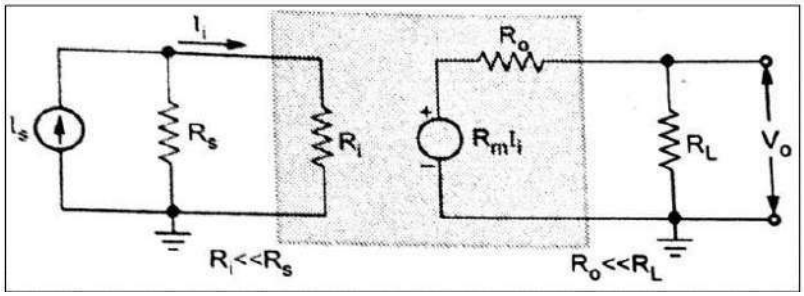
$$R'_{of} = R_{of} || R_L = \frac{R_{of} X R_L}{R_{of} + R_L} = \frac{\frac{R_o X R_L}{1 + R_m \beta}}{\frac{R_o}{1 + R_m \beta} + R_L} = \frac{R_o R_L}{R_o + R_L(1 + R_m \beta)}$$

Dividing numerator and denominator by $(R_o + R_L)$ we get

$$R'_{fo} = \frac{\frac{R_o R_L}{R_o + R_L}}{1 + \frac{\beta R_m R_L}{R_o + R_L}}$$

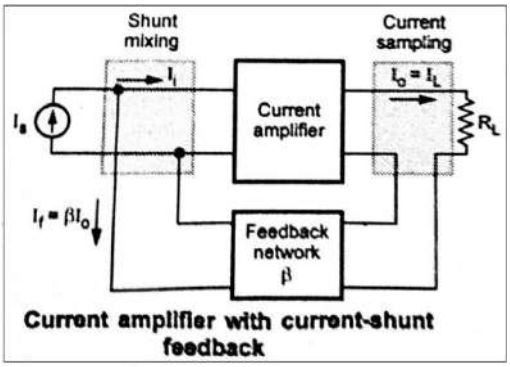
$R'_{fo} = \frac{R'_o}{1 + \beta R_M}$ where $R'_o = \frac{R_L X R_{of}}{R_L + R_{of}}$ and $R_M = \frac{R_m R_L}{(R_o + R_L)}$

(D) ***CURRENT SHUNT AMPLIFIER:***



- $R_i << R_s$ and $R_o << R_s$,
- Since $R_i << R_s$,
- $I_i = I_s$ and $R_o << R_L$, $V_o = R_m I_s$

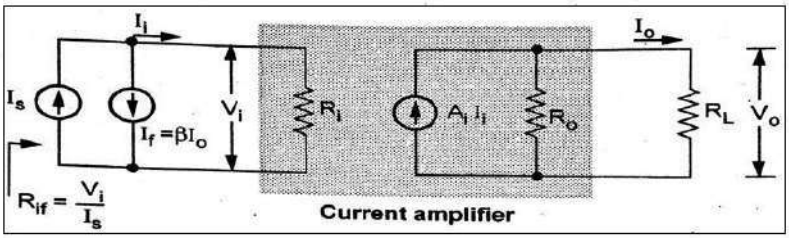
Feedback Topology



Current amplifier with current-shunt feedback

Input Resistance

Step 1: Equivalent Circuit



Step 2: obtain expression for I_s

Applying KCL to the input node we get

$$I_s = I_i + I_f = I_i + \beta I_o \quad \therefore I_f = \beta I_o$$

Step 3: obtain expression for I_o in terms of I_i

$$I_o = \frac{A_i I_i R_o}{R_o + R_L} = A_I I_i \quad \text{where } A_I = \frac{A_i R_o}{R_o + R_L}$$

Step 4: obtain expression for R_{if}

Substituting value of I_o in above equation we get

$$I_s = I_i + \beta A_I I_i = I_i (1 + \beta A_I)$$

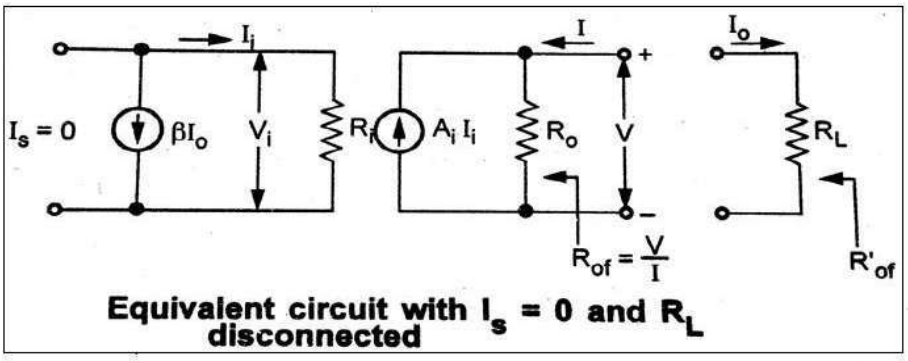
The input resistance with feedback is given as

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i(1 + \beta A_I)}$$

$$R_{if} = \frac{R_i}{(1 + \beta A_I)}$$

Output Resistance

Step 1: Equivalent Circuit



Equivalent circuit with $I_s = 0$ and R_L disconnected

Step 2: obtain expression for I in terms of V

Applying KCL to the output node we get

$$I = \frac{V}{R_o} - A_i I_i$$

The input current is given as

$I_i = - I_f = - \beta I_o \quad \therefore I_s = 0$

$I_i = \beta I \quad \therefore I = - I_o$

Substituting value of I_i in above equation we get

$$I = \frac{V}{R_o} - A_i \beta I \qquad \therefore \frac{V}{R_o} = I + A_i \beta = I (1 + \beta A_i)$$

Step 3: obtain expression for R_{of}

$$R'_{of} = R_{of} || R_L = \frac{R_{of} X R_L}{R_{of} + R_L}$$

$$= \frac{R_o(1 + \beta A_i)R_L}{R_o(1 + \beta A_i) + R_L} \qquad \therefore = \frac{R_o R_L(1 + \beta A_i)}{R_o + R_L + \beta A_i R_o}$$

Dividing numerator and denominator by $(R_o + R_L)$ we get

$$R'_{of} = \frac{\frac{R_o R_L(1 + \beta A_i)}{R_o + R_L}}{1 + \frac{\beta A_i R_o}{R_o + R_L}}$$

$$R'_{of} = \frac{R'_o(1 + \beta A_i)}{(1 + \beta A_I)}$$

$$R'_o = \frac{R_o R_L}{R_o + R_L} \quad and \quad A_I = \frac{A_i R_o}{R_o + R_L}$$

OSCILLATORS:

5. **Explain the construction and working of the following oscillators and derive the expression for frequency of oscillation. Also, write about advantages and disadvantages.**
    - **A. Phase-Shift Oscillator (RC type Oscillator)**
    - **B. Wein Bridge Oscillator (RC type Oscillator)**
    - **C. Hartley Oscillator (LC type Oscillator)**
    - **D. Colpitts Oscillator (LC type Oscillator)**
    - **E. Crystal Oscillator**

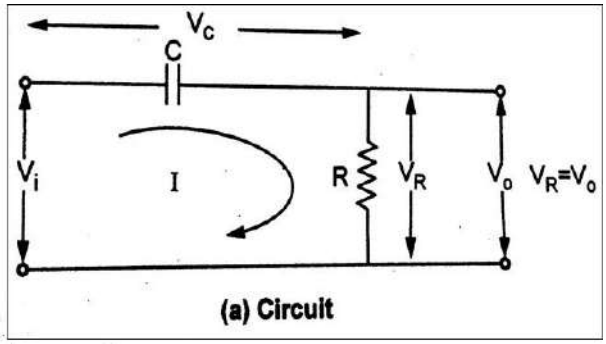
(A) RC Phase Shift Oscillator:

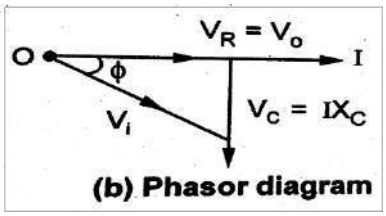
Explain the construction and working of RC Phase-Shift oscillator and derive the expression for frequency of oscillation.

- It consists of an amplifier and feedback network consisting of resistors and capacitors.
- An amplifier can be BJT, FET or operational amplifier.

Analysis of RC circuit:

- In this circuit output is taken across resistor R.





- The capacitive reactance X_C is given by $X_C = \frac{1}{2\pi fC}$ Ω where f is frequency of the input.
- The total impedance of the circuit is,

$$Z = R - jX_C = R - j\left(\frac{1}{2\pi fC}\right) \ \Omega$$

$$= |Z| < -\Phi^0 \quad \Omega$$

- The current 'I' flowing in the circuit is,

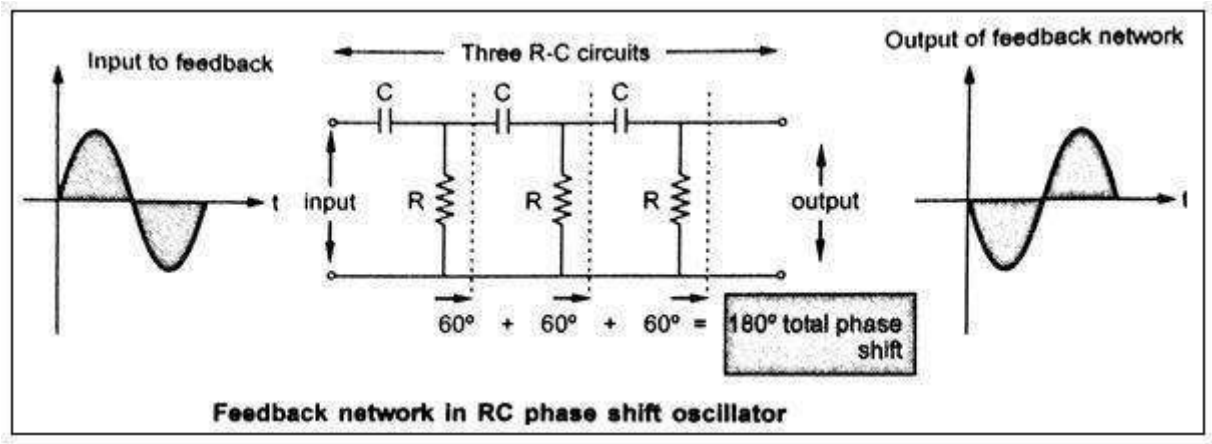
$$I = \frac{V_i < 0^0}{Z} = \frac{V_i < 0^0}{|Z| < -\Phi^0} = |\frac{V_i}{Z}| < +\Phi^0 \quad A$$

$$|Z| = \sqrt{R^2 + X_C^2} \ \ and \ \ \Phi = \tan^{-1}\frac{X_C}{R}$$

- In this equation the current 'I' leads input voltage by angle Φ
- The output voltage is drop across R hence $V_O = V_R = IR$
- The output voltage is in phase with current hence it leads input voltage by angle Φ
- Thus, RC circuit introduces a phase shift Φ between input and output which depends on R, C and frequency f.

RC Feedback Network for phase shift oscillator:

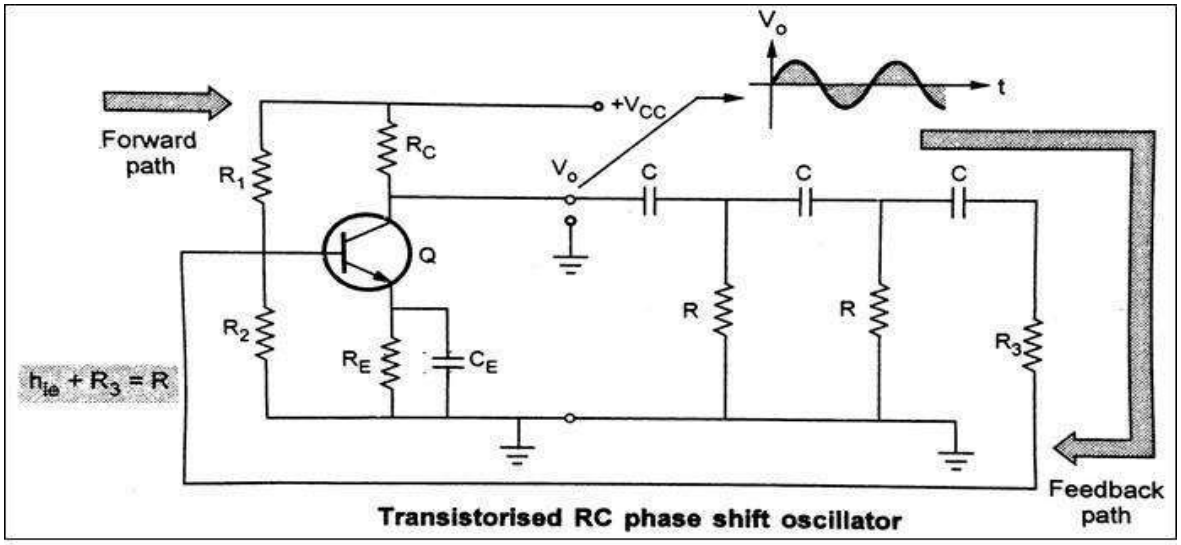
- In RC phase shift oscillator, amplifier introduces a phase shift of 180^0
- Thus, the feedback network must introduce a phase shift of 180^0 to satisfy Barkhausen condition.
- The RC feedback network consists of three RC sections, with each RC section contributing 60^0 phase-shift.
- Hence in RC phase shift oscillator, the feedback network consists of three RC sections are shown in fig.
- In all the three sections, resistance values and capacitance values are same so that at a particular frequency, each section produces precisely 60^0 phase-shift. This is the operating frequency of oscillator.



Feedback network in RC phase shift oscillator

Transistorized RC phase shift oscillator:

- The RC phase shift oscillator uses BJT amplifier stage which is single stage amplifier in common emitter configuration.
- A phase shift network has three RC sections
- The output of CE amplifier is connected as input to the RC phase shifting network
- The output of RC phase shifting network is connected as input to the amplifier
- Due to common emitter amplifier it introduces a phase shift of 180^0 between its input and output
- The RC phase shift network contributes further 180^0 phase shift so that phase shift around a loop is 360^0



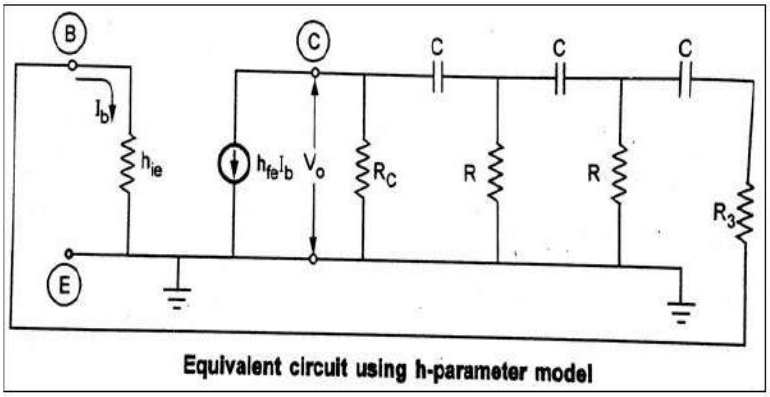
Transistorised RC phase shift oscillator

- From the fig. neglecting R1 and R2 we can write h_{ie}= input impedance of amplifier stage
- Thus, to have all three resistance values in three RC section equal, resistance in the last section is selected as R_3 so that $R_3+h_{ie}=R$

  $\boxed{R_3 + h_{ie} = R}$ i.e $\boxed{R_3 = R- h_{ie}}$ ---------- ***eq. 1***
- If R1 and R2 are not neglected then, $\boxed{R3 = R- [R_1 \parallel R_2 \parallel h_{ie}]}$ ***----- eq. 2***
- When gain A of the amplifier stage and feedback factor β are adjusted to give |Aβ| = 1, then the circuit works as an oscillator, satisfying both Barkhausen condition.

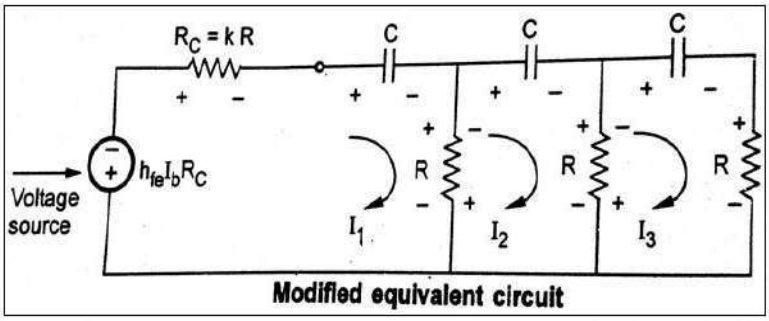
Derivation for frequency of oscillation:

- Replacing the transistor by its approximate h-parameter model, the equivalent circuit of RC phase shift oscillator is shown in fig.



Equivalent circuit using h-parameter model

- It is known that $R = h_{ie} + R_3$ and replace current source by equivalent voltage source.
- The ratio of resistance R_C to R is K. $\boxed{\frac{R_C}{R} = K}$
- The modified equivalent circuit is shown below



Modified equivalent circuit

- Applying KVL to the three loops

$$I_1R_C - \frac{1}{j\omega C}I_1 - R(I_1 - I_2) - h_{fe}I_bR_c = 0 \quad and\ use\ \ R_C = k\,R$$

$$\therefore\ I_1\left[kR + R + \frac{1}{j\omega C}\right] + I_2R = h_{fe}\ I_b\ k\ R \text{ ---------- } \textbf{\textit{eq. 3}}$$

$$-\frac{1}{j\omega C}I_2 - R(I_2 - I_1) - R(I_2 - I_3) = 0 \quad i.e \quad I_1R - I_2\left(2R + \frac{1}{j\omega C}\right) + I_3R = 0 \text{ ----- } \textbf{\textit{eq. 4}}$$

$$-\frac{1}{j\omega C}I_3 - I_3R - R(I_3 - I_2) = 0 \quad i.e\ I_2R - I_3\left(2R + \frac{1}{j\omega C}\right) = 0 \text{ ----- } \textbf{\textit{eq. 5}}$$

- Using jω = s and Cramers's rule

$$D = \begin{vmatrix} -(k+1)R - \frac{1}{sC} & +R & 0 \\ R & -2R - \frac{1}{sC} & R \\ 0 & R & -2R - \frac{1}{sC} \end{vmatrix}$$

- Solving the determinant, we get,

$$D = -\left\{\frac{s^3C^3R^3(3k+1) + s^2C^2R^2(4k+6) + sRC(5+k) + 1}{s^3C^3}\right\} \text{ ------- } \textbf{\textit{eq. 6}}$$

- To find I_3, find D_3 as,

$$D_3 = \begin{vmatrix} -(k+1)R - \frac{1}{sC} & R & h_{fe}\ I_bkR \\ R & -2R - \frac{1}{sC} & 0 \\ 0 & R & 0 \end{vmatrix} = kR^3h_{fe}I_b \text{ ---------- } \textbf{\textit{eq. 7}}$$

$$I_3 = \frac{D_3}{D} = \frac{-kR^3h_{fe}I_bs^3C^3}{s^3C^3R^3(3k+1) + s^2C^2R^2(4k+6) + sRC(5+k) + 1} \text{ ---------- } \textbf{\textit{eq. 8}}$$

I_3 = Output current of the feedback circuit
I_b = Input current of the amplifier
$I_C = h_{fe}\ I_b$ = input current of the feedback circuit

$$\beta = \frac{\text{Output of the feedback circuit}}{\text{Input to feedback circuit}} = \frac{I_3}{I_C} = \frac{I_3}{h_{fe} I_b}$$

$$A = \frac{\text{Output of the amplifier}}{\text{Input to the amplifier}} = \frac{I_3}{I_b} = h_{fe}$$

$$A\beta = h_{fe} \; X \; \frac{I_3}{h_{fe} I_b} = \frac{I_3}{I_b} \qquad \textbf{------- eq. 9}$$

From equation 8 and 9,

$$A\beta = \frac{-kR^3 h_{fe} s^3 C^3}{s^3C^3R^3(3k+1)+s^2C^2R^2(4k+6)+sRC(5+k)+1} \; - - - - - - \; \boldsymbol{eq.\ 10}$$

Using s = jω $s^2 = j^2 \omega^2 = -\omega^2$, $s^3 = j^3 \omega^3 = -j\omega^3$ and separating the real and imaginary part we get,

$$A\beta = \frac{+j\omega^3 k R^3 C^3 h_{fe}}{[1 - 4k\omega^2C^2R^2 - 6\omega^2C^2R^2] - j\omega[3k\omega^2R^3C^3 + \omega^2R^3C^3 - 5RC - kRC}$$

Dividing numerator and denominator by $j\,\omega^3 R^3 C^3$ and replacing $-1/j = +j$

$$A\beta = \frac{kh_{fe}}{-j\left\{\frac{1}{\omega^3R^3C^3} - \frac{4k}{\omega RC} - \frac{6}{\omega RC}\right\} - \left\{3k + 1 - \frac{5}{\omega R^2C^2} - \frac{k}{\omega^2R^2C^2}\right\}}$$

Replacing $1/\omega RC$ by α for simplicity

$$\boxed{A\beta = \frac{kh_{fe}}{[-3k-1+5\alpha^2+k\alpha^2]-j[\alpha^3-4k\alpha-6\alpha]}} \qquad \textbf{------- eq. 11}$$

To satisfy Barkhausen criterion, $<A\beta = 0^0$ hence imaginary part of the denominator term must be 0

$$\therefore \; \alpha^3 - 4k\alpha - 6\alpha = 0 \quad \text{i.e.} \quad \alpha\,(\,\alpha^2 - 4\,k - 6\,) = 0$$

$\therefore$ $\alpha 2 = 4\,k + 6$ $(\alpha \neq 0\,)$ i.e. $\boxed{\alpha = \sqrt{4k+6}}$ **------ eq. 12**

$\therefore$ $1/\omega RC = \sqrt{4k+6}$ i.e. $\boxed{\omega = \frac{1}{RC\sqrt{4k+6}}}$ i.e. $\boxed{f = \frac{1}{2\pi\sqrt{4k+6}}}$

This is the required frequency of oscillations.

Substituting $\alpha = \sqrt{4k+6}$ in equation 11 we get,

$$A\beta = \frac{kh_{fe}}{-3k - 1 + (4k+6)(5+k)} = \frac{kh_{fe}}{4k^2 + 23k + 29}$$

But $|A\beta| = 1 \quad i.e \quad |\frac{kh_{fe}}{4k^2+23k+29}| = 1$

$$\therefore h_{fe} = 4k + 23k + \frac{29}{k}$$

This is the required h_{fe} for the oscillations.

Minimum value of h_{fe}:

- For satisfying Aβ = 1, the expression for the value of h_{fe} of the transistor used in RC phase shift oscillator is given by,

$$h_{fe} \geq 4\ k + 23 + \frac{29}{k} \quad \text{where} \quad k = \frac{RC}{R}$$

- For minimum h_{fe}, find k for minimum h_{fe} from the expression $\frac{dh^{fe}}{dk} = 0$

$\therefore \frac{d}{dk}[4k + 23 + \frac{29}{k}] = 0$ i.e. $4 - \frac{29}{k^2} = 0$ i.e. $k^2 = \frac{29}{4}$

k = 2.6925 for minimum h_{fe}

using in the expression of h_{fe},

$$h_{fe}\ (\text{min}) = 4 \text{ X } 2.6925 + 23 + \frac{29}{2.6925} = \mathbf{44.54}$$

Thus for the circuit to oscillate, the transistor must be selected with h_{fe} greater than 44.54

Advantages:

- The circuit is simple to design
- Can produce output over audio frequency range
- Produces sinusoidal output waveform
- It is fixed frequency oscillator

Disadvantages:

- To vary the frequency, values of R and C of all three sections are to be varied simultaneously which is practically difficult. Hence frequency cannot be varied
- Frequency stability is poor due to changes in the values of various components due to effect temperature, aging etc.

(B) WEIN BRIDGE OSCILLATOR: (RC Oscillator)

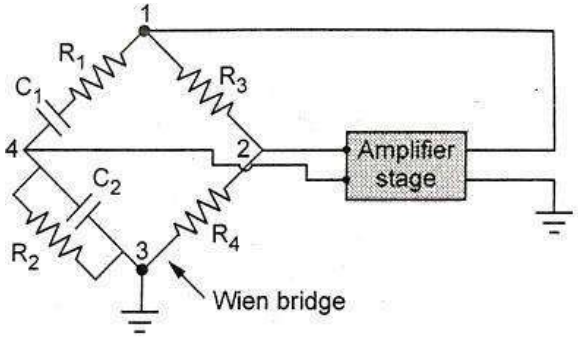
Explain the working of Wien Bridge Oscillator. Derive the expression for frequency of oscillation and condition for maintenance of oscillation.

(OR)

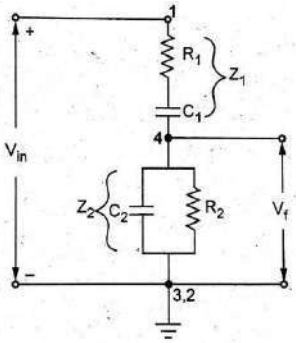
Design an oscillator to operate at a frequency of 10 KHz which gives an extremely pure sine wave output, good frequency stability and highly stabilized amplitude. Discuss the operation of this oscillator as an audio signal generator.

Construction and operation - (Wien Bridge Oscillator Circuit)

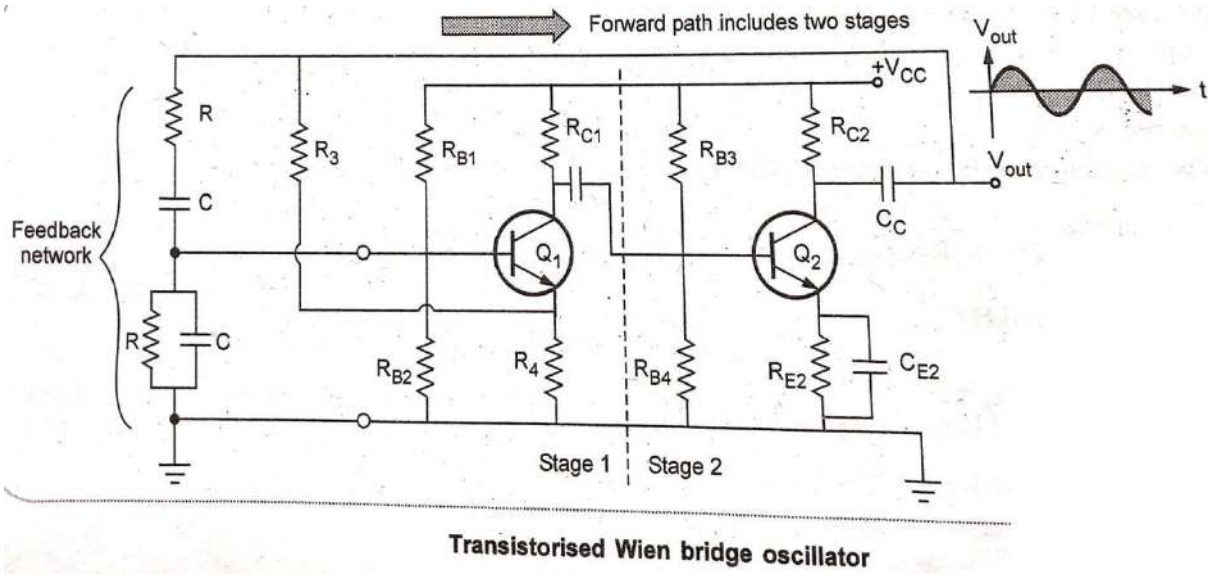
- ✓ **Two stage amplifiers (non-inverting)** and **feedback network** are used in *Wien Bridge Oscillator*.
- ✓ Both amplifier and feedback network does not introduce any phase shift i.e. 0° phase-shift around the loop in Wien Bridge Oscillator.
- ✓ R_1 & C_1 in series and R_2 & C_2 in parallel are frequency sensitive arms.
- ✓ The output of Amplifier is applied as input to Feedback Network (V_{in}) between 1 and 3.
- ✓ The output of Feedback Network (V_f) taken between 2 and 4 is given as input to amplifier.
- ✓ This Feedback Network is also known as **Lead-Lag Network**.



Basic circuit of Wien bridge oscillator



Feedback network of Wien bridge oscillator



Transistorised Wien bridge oscillator

Derive the expression for frequency of oscillation:

Analysis for frequency of oscillation:

$$Z_1 = R_1 + \frac{1}{j\omega C_1} \Rightarrow Z_1 = \frac{1 + j\omega R_1 C_1}{j\omega C_1} \quad (1)$$

$$Z_2 = R_2 \quad \frac{1}{j\omega C_2} \Rightarrow Z_2 = \frac{R_2 \times \frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}} \Rightarrow Z_2 = \frac{R_2}{1 + j\omega R_2 C_2} \quad (2)$$

$$\beta = \frac{V_f}{V_{in}} \quad (3)$$

Sub (6) in (3)

$$\Rightarrow \beta = \frac{Z_2}{Z_1 + Z_2} \quad (7)$$

$$I = \frac{V_{in}}{Z_1 + Z_2} \quad (4)$$

$$V_f = I\, Z_2 \quad (5)$$

$$Sub\ (4) in\ (5) \Rightarrow V_f = \frac{Z_2}{Z_1 + Z_2} V_{in} \quad (6)$$

$Substitute\ (1)\ \&\ (2)\ in\ (7)$

$$\beta = \frac{\frac{R_2}{1 + j\omega R_2 C_2}}{\frac{1 + j\omega R_1 C_1}{j\omega C_1} + \frac{R_2}{1 + j\omega R_2 C_2}} \quad (8)$$

Simplify the equation (8),

$$\beta = \frac{j\omega R_2 C_1}{(1 - \omega^2 R_1 R_2 C_1 C_2) + j\omega(R_1 C_1 + R_2 C_2 + R_2 C_1)} \quad (9)$$

Rationalizing and Simplifying the equation (9),

$$\beta = \frac{\omega^2 R_2 C_1 (R_1 C_1 + R_2 C_2 + R_2 C_1) + j\omega C_1 R_2 (1 - \omega^2 R_1 R_2 C_1 C_2)}{(1 - \omega^2 R_1 R_2 C_1 C_2)^2 + \omega^2 (R_1 C_1 + R_2 C_2 + R_2 C_1)^2} \quad (10)$$

To have zero phase shift, imaginary part of above equation must be zero.

$$(1 - \omega^2 R_1 R_2 C_1 C_2) = 0$$

$\omega\ (\omega^2 R_1 R_2 C_1 C_2) = 0$ but ω can not be zero. So,

$$\omega^2 R_1 R_2 C_1 C_2 = 0 \Rightarrow \omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$$

$$\Rightarrow \omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \qquad (11)$$

Frequency of Wien Bridge Oscillator, $\boldsymbol{f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}\ \text{Hz}}$ (12)

In pratice, $R_1 = R_2 = R$ and $C_1 = C_2 = C$ hence,

Frequency of Wien Bridge Oscillator, $\boldsymbol{f = \frac{1}{2\pi RC}\ Hz}$

Derive the condition for maintenance of oscillation:

Case (1): *If* $R_1 = R_2 = R$ and $C_1 = C_2 = C$ *then use* $\omega = \frac{1}{RC}\ Hz$ in (10),

we get the magnitude of the feedback network as,

$$Q = \frac{3}{0 + \frac{1}{R^2C^2}(3RC)^2} = \frac{3}{9} = \boldsymbol{\frac{1}{3}} \qquad \Rightarrow \quad Q = \boldsymbol{\frac{1}{3}}$$

As $|A\beta| \geq 1$ *hence* $|A| \geq 3$ *for Wien Bridge Oscillator.*

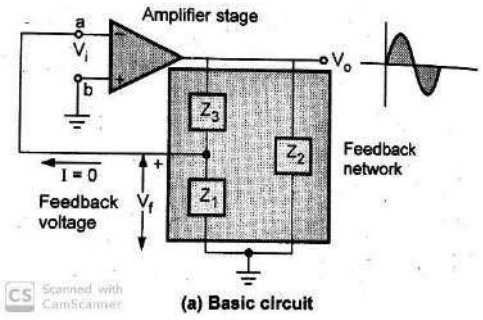
Thus, the gain of amplifier stage must be at least 3 to ensure sustained oscillations in Wien Bridge Oscillator.

Case (2): If $R_1 \neq R_2$ and $C_1 \neq C_2$ then use $\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$ *in* (10) *then*

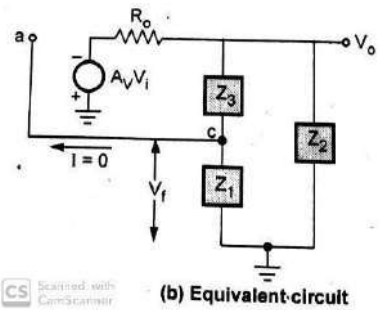
$$Q = \frac{\boldsymbol{R_2 C_1}}{\boldsymbol{R_1 C_1 + R_2 C_2 + R_2 C_1}} \qquad \Rightarrow \therefore \boldsymbol{A \geq \frac{R_1 C_1 + R_2 C_2 + R_2 C_{12}}{R_2 C_1}} \qquad \{\because\ |A\beta| \geq 1\}$$

LC OSCILLATORS:

Outline the LC tuned Oscillator and deduce expression for amplifier Gain, feedback Gain and necessary condition for LC Oscillator in general.

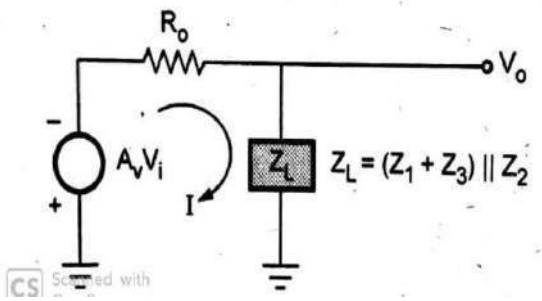


(a) Basic circuit



(b) Equivalent circuit

Analysis of Amplifier stage



R_o – Output impedance of the amplifier stage.
As, I=0 due to infinite input impedance, Z_1 and Z_3 appear in series and the combination in parallel with Z_2 as shown in figure.

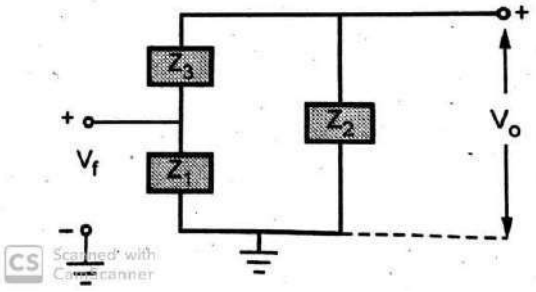
Applying KVL,

$I = -\frac{A_V V_i}{R_o + Z_L}$ and $V_O = IZ_L$

$$\boldsymbol{A = \frac{V_o}{V_i} = -\frac{A_V Z_L}{R_o + Z_L}}$$

A – Gain of amplifier stage.

Analysis of feedback stage



By voltage division in parallel circuit,

$V_f = \frac{V_o Z_1}{Z_1 + Z_3}$

i.e. $\beta = \frac{V_f}{V_o} = \frac{Z_1}{Z_1 + Z_3}$

But as feedback network introduces 180° phase-shift, use negative sign

$$Q = -\frac{\boldsymbol{Z_1}}{\boldsymbol{Z_1 + Z_3}}$$

Expression of the loop gain :

- According to Barkhausen condition loop gain $-A\beta$ is,

$$-A\beta = -\frac{A_v Z_L Z_1}{(R_o + Z_L)(Z_1 + Z_3)}$$

and $Z_L = \frac{(Z_1 + Z_3)Z_2}{Z_1 + Z_2 + Z_3}$

$$\therefore \boxed{-A\beta = -\frac{A_v Z_1 Z_2}{R_o(Z_1 + Z_2 + Z_3) + Z_2(Z_1 + Z_3)}}$$

The impedances Z_1, Z_2, Z_3 are pure reactive elements either L or C.

$$\therefore \boxed{Z_1 = jX_1,\ Z_2 = jX_2,\ Z_3 = jX_3}$$

Thus the loop gain becomes,

$$-A\beta = -\frac{A_v(jX_1)(jX_2)}{R_o j(X_1 + X_2 + X_3) + jX_2(jX_1 + jX_3)}$$

$$= \frac{A_v X_1 X_2}{-X_2(X_1 + X_3) + jR_o(X_1 + X_2 + X_3)}$$

- To have 0° phase shift for the loop gain, the imaginary part must be zero.

$$\therefore \boxed{(X_1 + X_2 + X_3) = 0}$$

$$\therefore -A\beta = \frac{-A_v X_1 X_2}{X_2(X_1 + X_3)} \text{ but } X_1 + X_3 = -X_2$$

$$\therefore \boxed{-A\beta = A_v\left(\frac{X_1}{X_2}\right)}$$

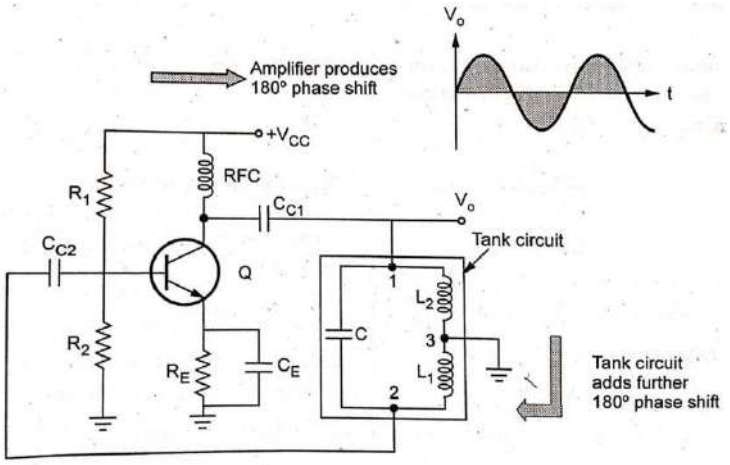
- According to Barkhausen condition $-A\beta$ must be positive and greater than equal to 1. As A_v is positive, $-A\beta$ will be positive only when X_1 and X_2 have same sign.
- Thus X_1 and X_2 must be of same type, either inductive or capacitive. And as $X_1 + X_3 = -X_2$ i.e. $X_3 = -(X_1 + X_2)$, the element X_3 must be opposite type of reactance to X_1 and X_2.

Types of LC Oscillators:

Oscillator Type	Reactance elements in the tank circuit		
	X_1	X_2	X_3
Hartley oscillator	L	L	C
Colpitts oscillator	C	C	L

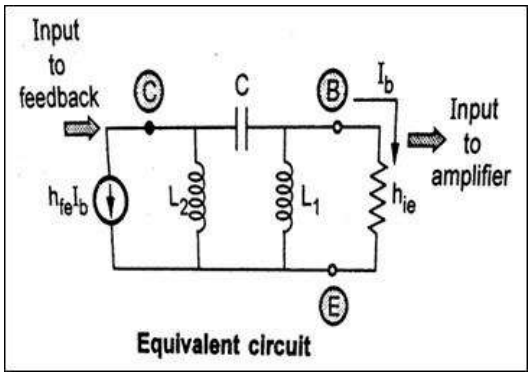
(C) Hartley Oscillator:

Explain the working of Hartley Oscillator. Derive the expression for frequency of oscillation and condition for maintenance of oscillation.

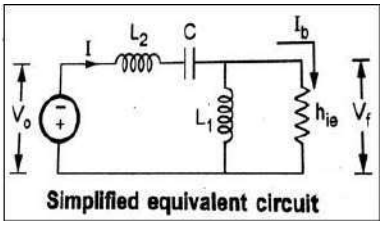


Transistorised Hartley oscillator

Circuit diagram



Equivalent circuit



Simplified equivalent circuit

Construction:

- The Hartley oscillator circuit using BJT as an active device.
- The resistances R_1, R_2 and R_E are biasing resistors
- The RFC is radio frequency chock whose reactance value is very high and high frequency and can be treated as open circuit. While for d.c operation, it is shorted hence does not cause problems for d.c operation.
- Due to RFC, the isolation between a.c and d.c operation is achieved. The C_1 and C_2 are coupling capacitors while C_E is the emitter bypass capacitor. The CE amplifier provides phase shift of 180^0.
- In the feedback circuit, as the centre of L_1 and L_2 is grounded, it provides additional phase shift of 180^0. This satisfies Barkhausen condition. In this oscillator, $X_1 = \omega L_1$, $X_2 = \omega L_2$, $X_3 = -1/\omega C$

Analysis:

- For LC oscillator, $X_1+X_2+X_3=0$

  $\therefore\ \omega L_1 + \omega L_2 - \frac{1}{\omega C} = 0$

  i.e $\omega(L_1 + L_2) = \frac{1}{\omega c}$

  $\therefore\ \omega = \frac{1}{\sqrt{(L_1+ L_2)C}}$ i.e $\boxed{f = \frac{1}{2\pi\sqrt{(L_1+ L_2)C}}}$

- The inductance L_1+L_2 is equivalent inductance denoted as L_{eq}. To satisfy $|A\beta| = 1$, then h_{fe} of the BJT used must be L_1/L_2.

  $\boxed{h_{fe} = \frac{L_1}{L_2}}$

- Practically L1 and L2 are wound on a single core and there exists a mutual inductance M between them.

  In this case, $\boxed{L_{eq} = L_1 + L_2 + 2M}$

  $\boxed{f = \frac{1}{2\pi\sqrt{L_{eq}C}}}$ and $\boxed{h_{fe} = \frac{L_1+M}{L_2+M}}$

- If capacitor C is kept variable, frequency can be varied over wide range.

Derivation of frequency of Oscillations

- The output current is collector current which is $h_{fe}\ I_b$, where I_b is base current. Assuming coupling capacitors shorted the capacitor C gets connected between collector and base.
- As emitter is grounded for a.c analysis, L_1 is between emitter and base while L_2 is between emitter and collector.
- h_{ie} is the input impedance of the transistor. The output current is I_b while input current is $h_{fe}\ I_b$. Convert current source to voltage source.

  $\boxed{V_O = h_{fe}I_b jX_{L2} = h_{fe}I_b j\omega L_2}$

- Total current I is,

$$I = \frac{-V_o}{[X_{L2} + X_C] + [X_{L1}||h_{ie}]}$$

- Negative sign is because direction of I is opposite to the polarities of V_o

$$X_{L2} + X_C = j\omega L_2 + \frac{1}{j\omega C} = \frac{-\omega^2 L_2 C + 1}{j\omega C}$$

$$X_{L1}||h_{ie} = \frac{j\omega L_1 h_{ie}}{j\omega L_1 + h_{ie}}$$

$$\therefore I = \frac{-h_{fe} I_b j\omega L_2}{\frac{-\omega^2 L_1 C + 1}{j\omega C} + \frac{j\omega L_1 h_{ie}}{j\omega L_1 + h_{ie}}}$$

- Using current division rule for parallel elements,

$$I_b = I \; X \; \frac{j\omega L_1}{j\omega L_1 + h_{ie}}$$

$$I_b = \frac{-h_{fe} I_b j\omega L_2}{\frac{-\omega^2 L_2 C + 1}{j\omega C} + \frac{j\omega L_1 h_{ie}}{j\omega L_1 + h_{ie}}} \; X \; \frac{j\omega L_1}{j\omega L_1 + h_{ie}}$$

$$\therefore 1 = \frac{j\omega^3 h_{fe} C L_1 L_2}{-j\omega^3 L_1 L_2 C h_{ie}(L_1 + L_2) + j\omega L_1 + h_{ie}}$$

$$\therefore 1 = \frac{j\omega^3 h_{fe} C L_1 L_2}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)] + j\omega L_1 (1 - \omega^2 L_2 C)}$$

- Rationalizing R.H.S of the above equation,

$$1 = \frac{\omega^4 h_{fe} L_1^2 L_2 C(1 - \omega^2 L_2 C) + j\omega^3 h_{fe} L_1 L_2 C[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)]}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)]^2 + \omega^2 L_1^2 (1 - \omega^2 L_2 C)^2}$$

- Imaginary part of R.H.S of above equation must be Zero

$$\therefore \; 1 - \omega^3 C(L_1 + L_2) = 0 \quad i.e \; \omega = \frac{1}{\sqrt{C(L_1 + L_2)}} \qquad (\omega^3 h_{fe} h_{ie} L_1 L_2 C \neq 0)$$

$$\boxed{f = \frac{1}{2\pi\sqrt{C(L_1 + L_2)}} = \frac{1}{2\pi\sqrt{C} L_{eq}}}$$

- Equating magnitude of both sides of the equation and using $\omega = \frac{1}{\sqrt{C(L_1 + L_2)}}$ *we get* $h_{fe} = \frac{L_1}{L_2}$ h_{fe} *required for oscillation*
- In practice, L_1 and L_2 may be wound on a single core so that there exists a mutual inductance between them denoted as M.
- In such a case, the mutual inductance is considered while determining the equivalent inductance L_{eq}, $\boxed{L_{eq} = L_1 + L_2 + 2M}$
- If L_1 and L_2 are assisting each other, then sign of 2M is positive while if L1 and L2 are in series opposition then sign of 2M is negative.

Advantage:

- The frequency can be easily varied by variable capacitor
- The output amplitude remains constant over the frequency range
- The feedback ratio of L1 and L2 remains constant
- It can be operated over wide range of frequency

Disadvantage:

- The output is rich in harmonics hence not suitable for pure sine wave requirement
- Poor frequency stability

Applications:

- Used as local oscillators in TV and radio receivers
- In function generators
- In radio frequency sources

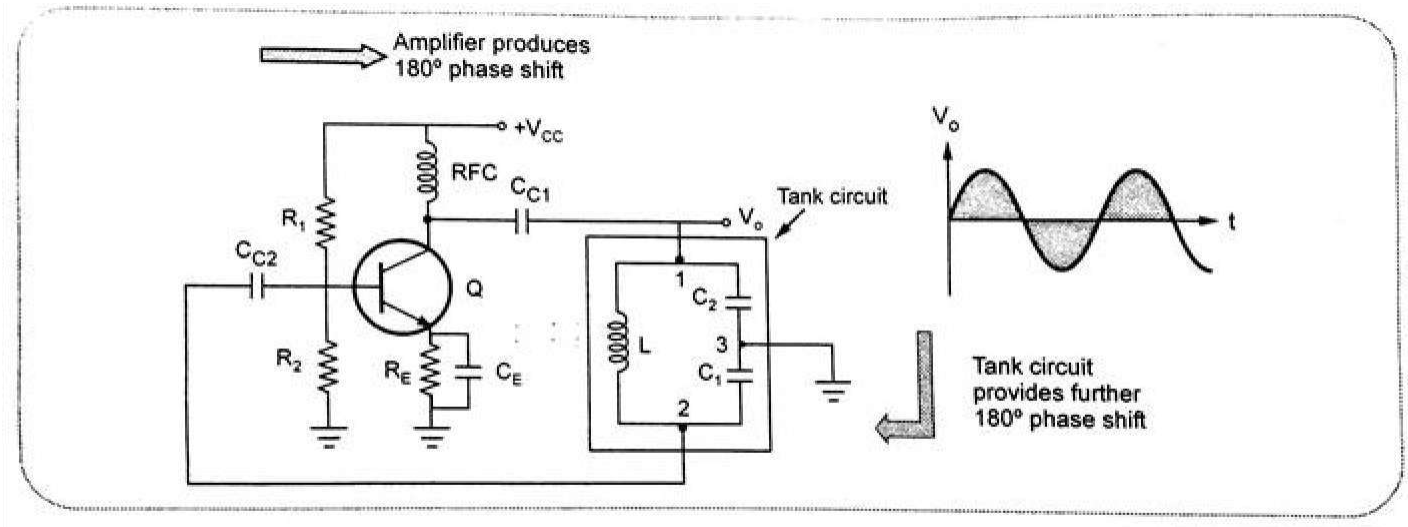
(D) COLPITTS OSCILLATOR:

Explain the working of Colpitts Oscillator. Derive the expression for frequency of oscillation and condition for maintenance of oscillation.

(OR)

With a neat circuit diagram deduce the necessary condition for oscillations and expression for oscillation frequency in the case of Colpitts Oscillator.

Construction:



Transistorised Colpitts oscillator

- It uses ***two capacitive resistances and one inductive reactance in its feedback network***.
- The amplifier stage uses BJT in common emitter configuration providing 180^o phase shift. The resistance R_1, R_2 and R_E are the biasing resistors.
- The RFC is radio frequency choke providing insulation between AC and DC operations. The C_{C1} and C_{C2} are coupling capacitors. In the feedback circuit, as the center C_1 and C_2 are grounded, it provides additional phase shift of 180^0, satisfying Barkhausen angle condition.

- In this oscillator $X_1 = \frac{-1}{\omega C_1}$ $X_2 = \frac{-1}{\omega C_2}$ $X_3 = \omega L$
- For LC oscillator, $X_1+X_2+X_3=0$

  $\therefore -\frac{1}{\omega C_1} - \frac{1}{\omega C_2} + \omega L = 0$ i.e $\omega L = \frac{1}{\omega}[\frac{1}{C_1} + \frac{1}{C_2}]$

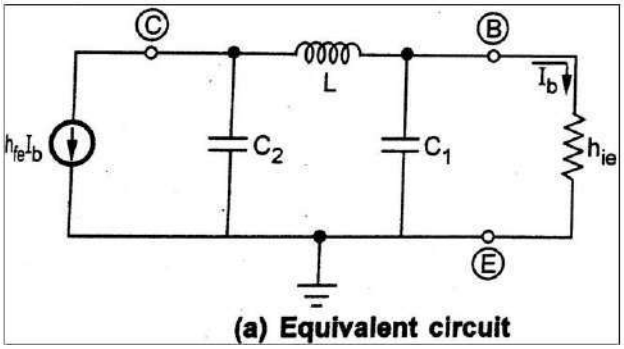
  $\therefore \omega^2 = \frac{1}{L[\frac{C_1C_2}{C_1+C_2}]}$ where $\frac{C1C2}{C_1+C_2} = C_{eq}$

  $\therefore \omega = \frac{1}{\sqrt{LC_{eq}}}$ i.e $\boxed{f = \frac{1}{2\pi\sqrt{LC_{eq}}} \text{ and } C_{eq} = \frac{C_1C_2}{C_1+C_2}}$
- To satisfy magnitude condition of Barkhausen criterion, the h_{fe} of BJT used is given by

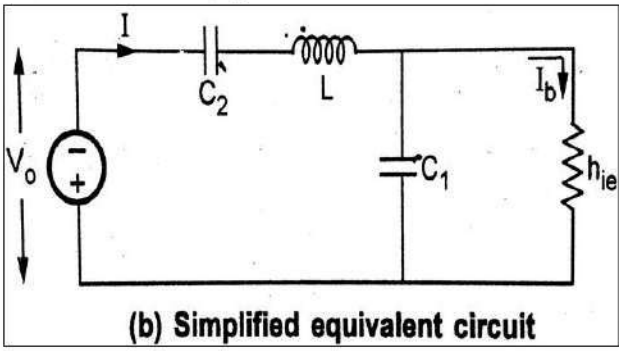
$$h_{fe} = \frac{C_2}{C_1}$$

Derivation of Frequency of oscillations

- The equivalent circuit and simplified equivalent circuit.



(a) Equivalent circuit



(b) Simplified equivalent circuit

$\boxed{V_0 = h_{fe}I_bX_{C2} = \frac{-jh_{fe}I_b}{\omega C_2}}$ ….. $X_{C2} = \frac{1}{j\omega C_2} = -\frac{j}{\omega C_2}$

- The total current drawn I is,

$$I = \frac{-V_0}{[XC_2 + X_L] + [XC_1||h_{ie}]}$$

$$XC_2 + X_L = \frac{-j}{\omega C_2} + j\omega L = \frac{-j(1-\omega^2 LC_2)}{\omega C_2}$$

$$X_{C1}||h_{ie} = \frac{-\frac{j}{\omega C_1} X\, h_{ie}}{-\frac{j}{\omega C_1} + h_{ie}} = \frac{-jh_{ie}}{-j + \omega C_1 h_{ie}}$$

$$I = \frac{-[-\frac{jh_{fe}I_b}{\omega C_2}]}{\frac{-j(1-\omega^2 LC_2)}{\omega C_2} - \frac{-jh_{ie}}{-j+\omega C_1 h_{ie}}}$$

- Using current division rule for parallel elements

$$I_b = I\ X\ \frac{\frac{-j}{\omega C_1}}{\frac{-j}{\omega C_1} + h_{ie}} = \frac{-jI}{-j + \omega C_1 h_{ie}}$$

$$I_b = -j\left[\frac{\frac{jh_{fe}I_b}{\omega C_2}}{\frac{-j(1-\omega^2 LC_2)}{\omega C_2}\ \frac{-jh_{ie}}{-j + \omega C_1 h_{ie}}}\right]\left[\frac{1}{-j + \omega C_1 h_{ie}}\right]$$

$$1 = \frac{-h_{fe}}{(1-\omega^2 LC_2) + j\omega h_{ie}[C_1 + C_2 - \omega^2 LC_1C_2]} \quad \text{----------} \ (1)$$

- To have imaginary part of above equation zero
  $C1+C2-\omega^2 LC_1C_2 = 0$ i.e $\omega^2 = \frac{C_1+C_2}{LC_1C_2} = \frac{1}{L\left[\frac{C_1C_2}{C_1+C_2}\right]}$

$$\omega = \frac{1}{\sqrt{LC_{eq}}} \quad and \quad f = \frac{1}{2\pi\sqrt{LC_{eq}}} \quad where\ C_{eq} = \frac{C_1C_2}{C_1+C_2}$$

- Substituting ω in equation 1 and equating magnitudes of both sides

$$h_{fe} = \frac{C_2}{C_1}$$

Advantages:

- Pure output waveform
- Good stability at high frequency
- Improved performance at high frequency
- Wide range of frequency
- Simple construction
-

Disadvantages:

- Difficult to adjust the feedback
- Poor isolation

Applications:

- Its main application is high frequency function generators.

(E) CRYSTAL OSCILLATOR:

Describe and explain the operation of the crystal oscillator.

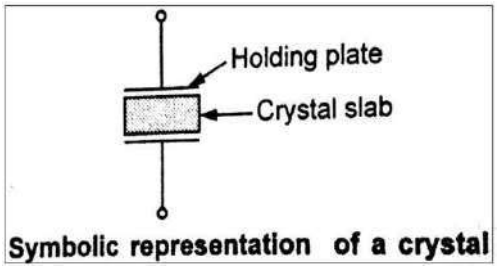
(OR)

Can you use Piezo-Electric effect for electric oscillators? If so, explain a component with such characteristics. Also draw a circuit for the same.

- The crystals are either naturally occurring or synthetically manufactured, exhibiting the piezoelectric effect
- The piezoelectric effect means under the influence of mechanical pressure, the voltage gets generated across the opposite faces of the crystal
- If the mechanical force is applied in such a way to force the crystal to vibrate the a.c voltage gets generated across it.
- Every crystal has its own resonating frequency depending on its cut. So under the influence of the mechanical vibrations, the crystal generates an electrical signal of very constant frequency
- The crystal has a greater stability in holding the constant frequency. The crystal oscillators are preferred when greater frequency stability is stability
- Quartz is a compromise between the piezoelectric activity of Rochelle salt and the strength of the tourmaline.
- Quartz is inexpensive and easily available in nature hence very commonly used in the crystal oscillators.

Constructional Details:

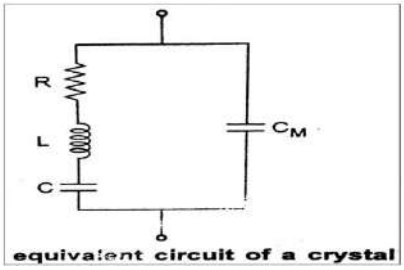
- The natural shape of quartz is a hexagonal prism. But for its practical use, it is cut to the rectangular slab. This slab is then mounted between the two metal plates.



Symbolic representation of a crystal

- The metal plates are called holding plates, as they hold the crystal slab in between them.

A.C. Equivalent circuit:



equivalent circuit of a crystal

C_M – Mounting Capacitance (due to two metal plates separated by dielectric like crystal slab).
R – Resistance (internal friction loss during vibration)
L – Inductance (indication of inertia of mass of crystal)
C – Capacitor (stiffness during vibrating)

- RLC forms a resonating circuit. The expression for the resonating frequency f_r is,

$$f_r = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{Q^2}{1+Q^2}}$$ where Q = Quality factor of crystal

$$Q = \frac{\omega L}{R}$$

- The Q factor of the crystal is very high, typically 20,000. Value of Q up to 10^6 also can be achieved. Hence $\sqrt{\frac{Q^2}{1+Q^2}}$ factor approaches to unity and we get the resonating frequency as $f_r = \frac{1}{2\pi\sqrt{LC}}$
- The crystal frequency is in fact inversely proportional to the thickness of the crystal.
  - $f \alpha \frac{1}{t}$ where t = Thickness
- So to have very frequencies, thickness of the crystal should be very small
- The crystal has two resonating frequencies, series resonant frequency and parallel resonant frequency.

Applications

- Watches
- Communication transmitters and receivers

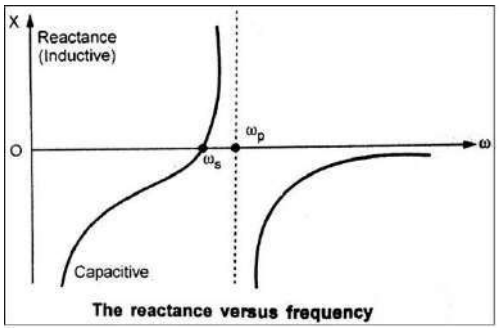
Series and Parallel resonance:

- **Series Resonance frequency**

$$f_s = \frac{1}{2\pi\sqrt{LC}}$$

- **Parallel Resonance frequency**

$$f_P = \frac{1}{2\pi\sqrt{LC_{eq}}}$$



The reactance versus frequency

- If we neglect the resistance R, the impedance of the crystal is a reactance jX which depends on the frequency as,

$$jX = -\frac{j \quad \omega^2 - \omega_s^2}{\omega C_M \, \omega^2 - \omega_p^2}$$

Where, ω_s = Series resonant frequency

- Reactance against frequency is shown in fig.

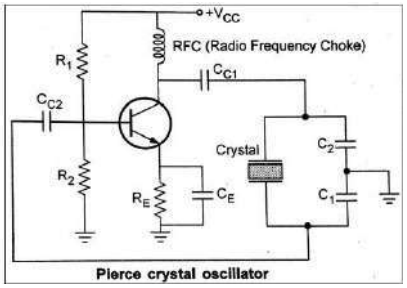
Crystal Stability:

i. Temperature stability
ii. Long term stability
iii. Short term stability

Types of Crystal Oscillator:

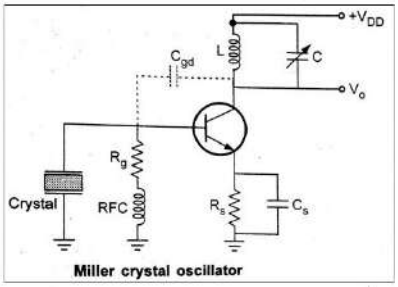
1. Pierce Crystal Oscillator:
2. Miller Crystal Oscillator:

Pierce Crystal Oscillator:



Pierce crystal oscillator

Miller Crystal Oscillator:



Miller crystal oscillator

Comparison between Crystal and LC Oscillator:

Sr. No.	LC oscillators	Crystal oscillators
1.	The separate L and C components are necessary in the tuned circuit.	The single crystal serves the purpose of tuned circuit.
2.	The Q value of LC tuned circuit is less as compared to the crystal.	The Q value is much higher than LC tuned circuit.
3.	The frequency stability is less.	Very high frequency stability.
4.	The bandwidth is more.	The bandwidth is very small.
5.	The effect of temperature on the frequency is more severe.	The effect of temperature on frequency is negligible.
6.	The frequency range which can be generated is more.	There is limit to the frequency generated due to thickness of the crystal.
7.	Used in general purpose applications like signal generators.	Used in specific applications which need high frequency stability like watches, computers, counters.

Solved Problems

1. **In a Hartley oscillator, if L_1=0.2mH, L_2=0.3mH and C=0.003μF. Calculate the frequency of oscillations. [MAY 2012]**

   Given: L_1=0.2mH, L_2=0.3mH, C=0.003μF

   To find frequency of oscillations **$f=1/(2\pi\sqrt{[(L1+L2)\ C)]}$** by substituting **f=129.949KHz**

2. **In a RC phase shift oscillator if $R_1=R_2=R_3$=200KΩ and $C_1=C_2=C_3$=100PF. Find the frequency of oscillation? (Apr/May 2018)**

   Solution:

   The frequency of an RC phase shift oscillator is given by

   $F_o = \frac{1}{2\pi RC\sqrt{6}}$ $F_o = \frac{1}{2\pi\times200\times10^3\times100\times10^{-12}\times\sqrt{6}}$ **F_o = 3.248KHZ**

3. **In a phase shift oscillator, R1=R2=R3=1 MΩ and C1=C2=C3=68 pF. At what frequency does the circuit oscillate. (Nov/Dec 2018)**

   Given that,

   For a phase shift oscillator, Resistance, $R_1 = R_2 = R_3$ = 1 MΩ; Capacitor, $C_1 = C_2 = C_3$ = 68 pF

   Frequency, f = ?

   Frequency of phase shift oscillator is given by, $f = \frac{1}{2\pi RC\sqrt{6}}$

   Substituting corresponding values in above equation, $f = \frac{1}{2\pi\ X\ 1X10^6\ X\ 68\ X\ \sqrt{6}} = 955.9\ Hz$ frequency, f = 955.9 Hz

4. **A wien bridge oscillator is used for operation at 10KHz. If the value of the resistor R is 100Kohms, what is the value of C required?**

Solution:

Given: F = 10KHZ, R = 100KΩ, C= ?

The frequency of oscillation is

$F = \frac{1}{2\pi RC}$ $C = \frac{1}{2\pi RF}$ $C = \frac{1}{2\pi \times 100 \times 10^3 \times 10 \times 10^3}$

$C = 1.591 \times 10^{-10}$ F

5. **An amplifier has a c urrent gain of 240 and input impedance of 15 k Ω without feedback. If negative current feedback (mi = 0.015) is applied, what will be the input impedance of the amplifier? (Nov/Dec 2017)**

Solution. $Z'_{in} = \frac{Z_{in}}{1 + m_i A_i}$

Here $Z_{in} = 15\,\text{k}\Omega$; $A_i = 240$; $m_i = 0.015$

$\therefore$ $Z'_{in} = \frac{15}{1 + (0.015)(240)} = 3.26\,\text{k}\Omega$

6. **Design a Wien bridge oscillator circuit to oscillate at a frequency of 20KHz. (Nov/Dec2015)**

Solution:

$f = \frac{1}{2\pi Rc}$ f = 20 kHz, Let C = 0.01μF

$f = \frac{1}{2\pi Rc}$, $R = \frac{1}{2\pi fC} = \frac{1}{2 \times \pi \times 20000 \times 0.01 \times 10^{-6}} = 80$ohms.

7. **A 1 mH inductor is available. Find the capacitor values of a colpitt's oscillator so that f=1 MHz and feedback fraction=0.25 (Nov/Dec 2018)**

Solution:

Given that,

For a Colpitts oscillator,

Inductance, L = 1 mH

Resonant frequency, f_0 = 1 MHz

Feedback factor, β = 0.25

The resonant frequency of Colpitts oscillator is given by,

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}} \quad ----(1)$$

Where, $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$

From equation (1),

$$C_{eq} = \frac{1}{4\pi^2 f_0^2 L} \quad ----(2)$$

Given feedback factor, $\beta = \frac{C_1}{C_2} = 0.25$

$C_2 = 4C_1$

Substituting the given specifications in equation (2)

$$C_{eq} = \frac{1}{4\pi^2(10^6)^2 X\ 10^{-3}}$$

$$\frac{C_1 C_2}{C_1 + C_2} = 2.533\ X\ 10^{-11}$$

$$\frac{4\ C_1^2}{5C_1} = 2.53\ X\ 10^{-11}$$

C_1 = 3.166 X 10^{-11} = 31.66 pF

From $C_2 = 4C_1$,

$C_2 = 4$ X (3.166 X 10^{-11})

C_2 = 126.65 pF

8. The overall gain of a multistage amplifier is 140. When negative voltage feedback is applied the gain is reduced to 17.5 find the fraction of the output that is feedback to the input. (Nov/Dec 2018)

Given that,

For a multistage feedback amplifier,

Overall gain, A_V = 140

Feedback gain, A_{vf} = 17.5

Feedback fraction, β = ?

Voltage gain of negative feedback amplifier is defined as,

$$A_{vf} = \frac{A_v}{1 + A_v\beta} \quad 17.5 = \frac{40}{1 + 140\beta}$$

17.5 + 2450 β = 140

$$\beta = \frac{1}{20} = 0.05$$

β = 0.05

9. **In colpitts oscillator C1 = 1nF and C2 = 100nF. If the frequency of oscillation is 1 kHz find the value of inductor. Also find the minimum gain required for obtaining sustained oscillations. (May / Jun 2016)**

Given data:

C1 = 1nF, C2 = 100nF, Frequency of oscillation f = 100 kHz.

Formulae used:

$f = \frac{1}{2n}\sqrt{\frac{C1+C2}{L1C1C2}},\ A_V = \frac{C1}{C2}$

Frequency of oscillations $L = \frac{C1+C2}{4n^2 f_r^2 C1C2} = \frac{101\times10^{-6}}{4n^2\times(10\times1000)^2\times100\times10^{-12}}$

$= \frac{101\times10^6}{4n^2\times(100000)^2} = \frac{101}{3.99}\times10^{-5} = 25.634\times10^{-5}H = 256.34\mu F$

$$A_V > \frac{C1}{C2} = \frac{1}{100} = 0.01nF$$

10. Design a RC phase Shift Oscillator to generate 5KHz sine wave with 20 V peak to Peak amplitude. Assume h_{fe}=Q = 150, $C = 1.5nF$, hre=1.2KΩ(Nov.Dec 2016)

$$f = \frac{1}{2\pi Rc\sqrt{6}}; \qquad 5 \times 10^3 = \frac{1}{2\pi \times 1.5 \times 10^{-9}\sqrt{6} \times R} \qquad R = \frac{1}{2\pi \times 1.5 \times 10^{-9} \times \sqrt{6} \times 5 \times 10^3}$$

$$R = 8.67\ k\ \Omega$$

11. In Colpitts Oscillator, the desired frequency is 500 KHz. Find the value of L. Assume C= 1000pF. (Apr/May 2018)

$$\therefore \quad C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = 500 \text{ pF}$$

The frequency is given by,

$$f = \frac{1}{2\pi\sqrt{L\, C_{eq}}}$$

$$\therefore \quad 500 \times 10^3 = \frac{1}{2\pi\sqrt{L \times 500 \times 10^{-12}}}$$

$$\therefore \quad (500 \times 10^3)^2 = \frac{1}{4\pi^2 [L \times 500 \times 10^{-12}]}$$

$$\therefore \quad L = 202.642\ \mu H$$

12. When negative voltage feedback is applied to an amplifier of gain 100, the overall gain falls to 50. Calculate the fraction of the output voltage fedback. If this fraction is maintained, calculate the value of the amplifier gain required if the overall stage gain is to be 75. (Nov/Dec 2017)

(*i*) Gain without feedback, $A_v = 100$

Gain with feedback, $A_{vf} = 50$

Let m_v be the fraction of the output voltage fedback.

Now $$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

or $$50 = \frac{100}{1 + 100\, m_v}$$

or $$50 + 5000\, m_v = 100$$

or $$m_v = \frac{100 - 50}{5000} = 0.01$$

(*ii*) $A_{vf} = 75; \quad m_v = 0.01; \quad A_v = ?$

$$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

or $$75 = \frac{A_v}{1 + 0.01\, A_v}$$

or $$75 + 0.75\, A_v = A_v$$

$\therefore$ $$A_v = \frac{75}{1 - 0.75} = 300$$

13. In Colpitts oscillator, C1 = C2 =C and L=100 X 10-6 H. The frequency of oscillation is 500 KHz. Determine the value of C. (Apr/May 2018)

Solution : The given values are,

$$L = 100\ \mu H,\ C_1 = C_2 = C \text{ and } f = 500\ kHz$$

Now $$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$\therefore \quad 500\times10^3 = \frac{1}{2\pi\sqrt{100\times10^{-6}\times C_{eq}}}$$

$$\therefore \quad (500\times10^3)^2 = \frac{1}{4\pi^2\times100\times10^{-6}\times C_{eq}}$$

$$\therefore \quad C_{eq} = 1.0132\times10^{-9}\ F$$

but $$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \quad \text{and} \quad C_1 = C_2 = C$$

$$\therefore \quad C_{eq} = \frac{C\times C}{C + C} = \frac{C}{2}$$

$$\therefore \quad 1.0132\times10^{-9} = \frac{C}{2}$$

$$\therefore \quad C = 2.026\times10^{-9}\ F = \mathbf{2.026\ nF}$$

14. An amplifier in required with a voltage gain of 100 which does not vary by more that 1%. If it is to use negative feedback with a basic amplifier the voltage gain of which vary by 20%, find the minimum voltage gain required and the feedback factor. (Nov/Dec 2018)

Solution:

Closed loop voltage gain of amplifier, A_f is defined as,

$$A_f = \frac{A_m}{1 + A_m\,\beta} \qquad -----(1)$$

$$100 = \frac{A_m}{1 + A_m\,\beta}$$

$$A_m = 100 + 100\,A_m\,\beta \qquad -----(2)$$

Since, feedback voltage gain, A_f does not vary more than 1% and amplifier gain varies by 20% equation (1) can be written as,

$$99 = \frac{0.8\,A_m}{1 + 0.8\,A_m\,\beta}$$

$$0.8\,A_m = 99 + 79.2\,A_m\,\beta \qquad -----(3)$$

Multiplying equation (1) with 0.792 or both sides,

$$0.792\,A_M = 79.2 + 79.2\,A_m\,\beta \qquad -----(4)$$

Subtracting equation (3) and (4),

$0.008\ A_m = 19.8;$ $\quad = \frac{19.8}{0.008}$ $\quad$ **$A_m = 2475$**

A_n

Substituting A_m in equation (2),

$$2475 = 100 + 100\ X\ 2475\ X\ \beta$$

$$\beta = \frac{2475 - 100}{2475\ X\ 100}$$

$\beta = 0.0096$

∴ Feedback factor, $\beta = 0.0096$ and minimum voltage gain $A_m = 2475$ V.

Additional Important Questions:

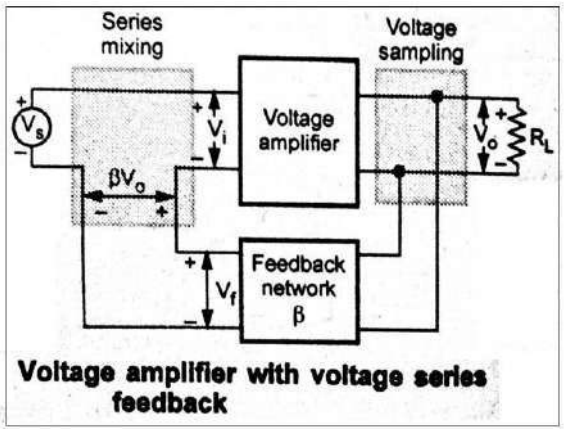
6. Discuss the effect for the following negative feedback amplifiers and derive the expression for input resistance, output resistance and voltage gain for common emitter amplifier.

A. **VOLTAGE SERIES FEEDBACK**
B. **VOLTAGE SHUNTFEEDBACK**
C. **CURRENT SERIES FEEDBACK**
D. **CURRENT SHUNT FEEDBACK**

(A) VOLTAGE SERIES FEEDBACK

Draw circuit of CE amplifier with Voltage Series feedback and obtain the expression for feedback ratio, voltage gain, input and output resistances.

Input is the feedback network is parallel with output of amplifier shunt connection to reduce output resistance R_o series connection at the input increase the input resistance.



Voltage amplifier with voltage series feedback

$$Voltage\ feedback\ factor\ \beta = \frac{V_f}{V_o}$$

Gain

Amplifier Gain $A_v = \frac{V_o}{V_i}$

$$V_o = A_v V_i \quad ---(1)$$

Feedback is connected $V_s = V_i + V_f$; $V_i = V_s - V_f$

Now $V_s = V_i + \beta V_o = V_i + \beta A_v V_i$

$$V_s = V_i(1 + A\beta) \quad ---(2)$$

$$V_i = V_s - V_f \quad \& \quad V_i = I_i R_i$$

$$\therefore V_s = V_i + V_f = I_i R_i + A\beta V_i$$

$$= I_i R_i + A\beta R_i I_i$$

$$V_s = R_i I_i(1 + A\beta)$$

Now, Input Impedance $Z_{if} = \frac{V_i}{I_i} = \frac{I_i R_i(1+A\beta)}{I_i}$

$$= \frac{V_i}{I_i}(1 + A\beta)$$

$$Z_{if} = Z_i(1 + A\beta)$$

Output impedance, $V_o = R_o I_o + AV_i$, $V_i = V_s - V_P$

$$V_s = 0$$

$$V_i = -V_P = \beta V_o$$

$$\therefore V_o = I_o R_o - A\beta V_o$$

$$V_o + A\beta V_o = I_o R_o$$

$$V_o(1 + A\beta) = I_o R_o$$

$$\frac{V_o}{I_o} = \frac{R_o}{1 + A\beta}$$

$$Z_o = \frac{R_o}{1 + A\beta}$$

$R_o \rightarrow$ *output resistance of amplifier without feedback.*

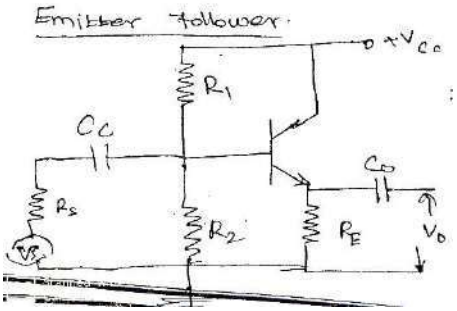
$$A_i = \frac{I_e}{I_b} = \frac{I_b + I_c}{I_b} = 1 + h_{fe}$$

$$R_i = h_{ie} + (1 + h_{fe})R_E$$

$$A_V = \frac{A_C R_L}{R_i} = \frac{(1+h_{fe})R_L}{h_{ie}+(1+h_{fe})R_L} = 1 - \frac{h_{ie}}{R_i}$$

$$R_o = \frac{h_{ie} + R_s}{1 + h_{fe}}$$

$$R_{of} = R_o \parallel R_c$$

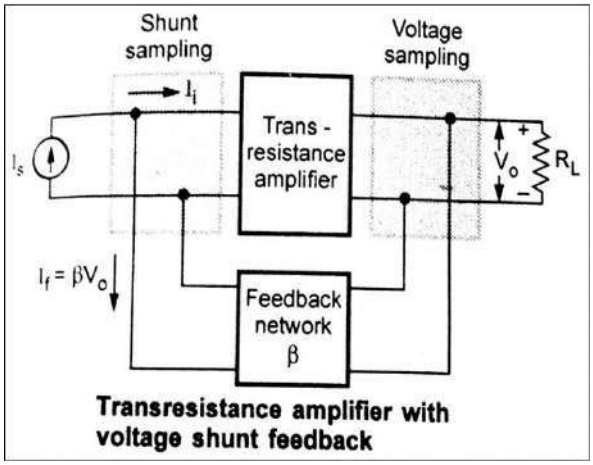


(B) VOLTAGE SHUNT FEEDBACK AMPLIFIER

Draw circuit of CE amplifier with Voltage Shunt feedback and obtain the expression for feedback ratio, voltage gain, input and output resistances. (April / May 2015 -R13)

Trans resistance Amplifier

Connection Diagram:



Transresistance amplifier with voltage shunt feedback

$Gain:\quad A_F = \frac{V_o}{I_s} = \frac{V_o}{I_i}$

$$I_s = I_i + I_f$$

$$= I_i + \beta V_o$$

$$I_s = I_i + A\beta I_i = I_i(1 + A\beta)$$

$$A_F = \frac{V_o}{I_s} = \frac{AI_i}{I_i(1+A\beta)} = \frac{A}{1+A\beta} \quad without\ feedback.$$

$\therefore$ The gain of the amplifier without feedback is reduced by a factor of $(1 + A\beta)$

Input Impedance:

$$Z_i = \frac{V_i}{I_s}; \quad Z_i = \frac{V_i}{I_i + I_f}; \qquad Z_i = \frac{V_i}{I_i + \beta V_o}; \qquad Z_i = \frac{V_i}{I_i + A\beta I_i}; \qquad Z_i = \frac{V_i}{I_i(1+A\beta)};$$

$$Z_i = \frac{Z_i}{(1+A\beta)}$$

Input impedance is reduced by the factor $(1 + A\beta)$ for both series, shunt feedback connection.

Output Impedance

$V_o = R_o I_o - A I_i$ $\qquad I_i = I_S - I_F$, I_f I_s *transferred to output side* $I_s = 0$

$= R_o I_o - A I_F$ $\qquad \therefore \quad I_i = -I_F$

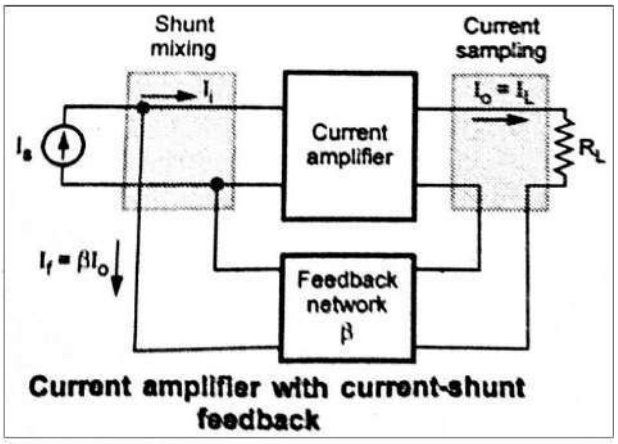
$V_o + A\beta V_o = R_o I_o \qquad V_o(1 + A\beta) = R_o I_o$

$\frac{V_o}{I_o} = \frac{R_o}{1+A\beta} \quad Z_o = \frac{V_o}{I_o} = \frac{R_o}{1+A\beta}$

(C) CURRENT SHUNT FEEDBACK AMPLIFIER

Draw circuit of CE amplifier with Current Shunt feedback and obtain the expression for feedback ratio, voltage gain, input and output resistances. (April / May 2015 -R13)

Connection Diagram



Current amplifier with current-shunt feedback

Amplifier Gain, $A = \frac{V_o}{I_i}$ $\qquad I_S = I_i + I_F$

Feedback factor $\beta = \frac{I_F}{I_o}$ $\qquad I_F = \beta I_o$

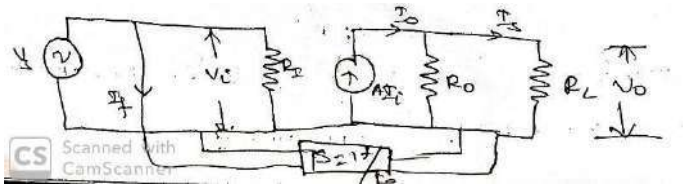
$I_o = A I_i$

Gain of the Amplifier

$$A_F = \frac{I_o}{I_s} = \frac{AI_i}{I_i + I_F} = \frac{AI_i}{I_i + \beta I_o} = \frac{AI_i}{I_i + \beta\, AI_i}$$

$$A_F = \frac{A}{1 + \beta A}$$

Input Impedance:



$I_s = I_i + I_F$

$I_s = \frac{V_i}{R_i} + \beta I_o$; $I_s = \frac{V_i}{R_i} + A\beta I_i$; $I_s = \frac{V_i}{R_i} + \frac{A\beta V_i}{R_i}$; $I_s = \frac{V_i}{R_i}(1 + A\beta)$

Input resistance of amplifier with feedback R_{if}

$R_{if} = \frac{V_i}{I_s} = \frac{R_i}{1+A\beta}$

Output Impedance:

$I_s = I_i + I_F$ $I_i = I_s - I_F$

$I_s = 0$, Source transferred to output side to calculate the output impedance.

$$I_o = A I_i + \frac{V_o}{R_o}$$

$$\frac{V_o}{R_o} = (1 + A\beta)$$

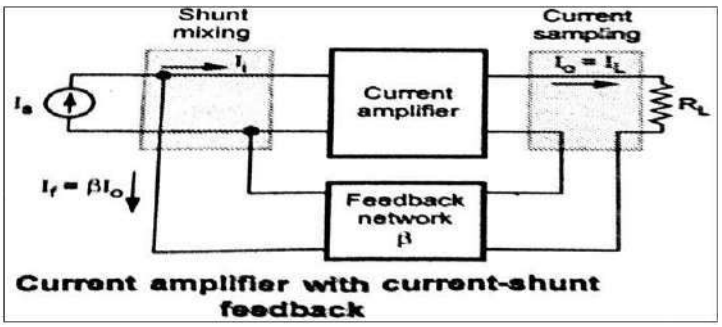
$$R_F = \frac{V_o}{R_o} = R_o(1 + A\beta)$$

Thus, output impedance increased by $(1 + A\beta)$

(D) CURRENT SERIES FEEDBACK AMPLIFIER

Draw circuit of CE amplifier with Current Series feedback and obtain the expression for feedback ratio, voltage gain, input and output resistances. (April / May 2015 -R13)

Transconductance Amplifier:

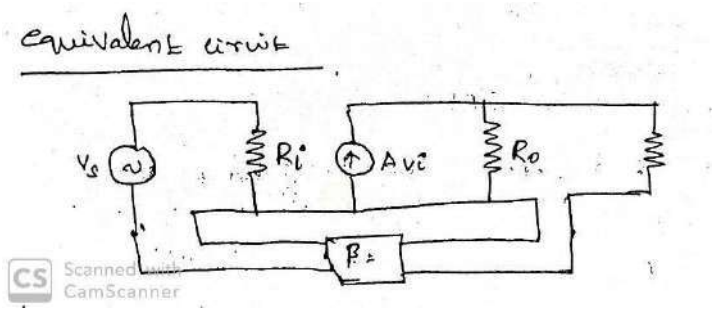


$Gain = \frac{I_o}{V_o} = \frac{I_o}{V_i + V_F}$

$$= \frac{A V_i}{V_i + \beta I_o} \Rightarrow \frac{A V_i}{V_i + A\beta V_i}$$

$$A_F = \frac{A V_i}{V_i(1 + A\beta)} = \frac{A}{1 + A\beta}$$

Equivalent Circuit



Input Impedance:

$V_s = I_i R_i + V_F$

$= I_i R_i + \beta I_o$

$= I_i R_i + A\beta V_i$

$= I_i R_i + A\beta I_i R_i$

$= I_i R_i(1 + A\beta)$

$$Z_i = \frac{V_s}{I_i} = R_i(1 + A\beta)$$

$\therefore$ *Input impedance increased by* $factor(1 + A\beta)$

Output Impedance:

$V_s = 0$

$V_s = V_i + V_F$

$V_i + V_F = 0; \qquad V_i = -V_F$

$$I_o = AV_i + \frac{V_o}{Z_o} = -AV_i + \frac{V_o}{Z_o}$$

$$= -A\beta I_o + \frac{V_o}{Z_o}$$

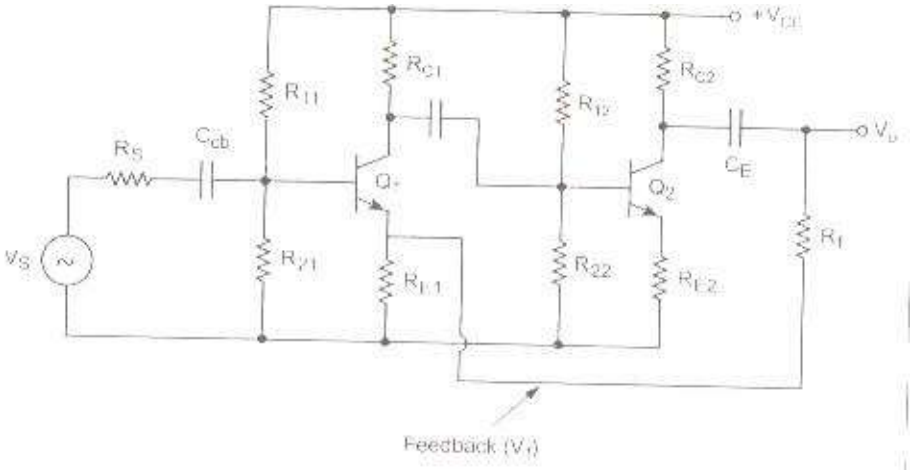
$$I_o + A\beta_o = \frac{V_o}{Z_o}; \qquad I_o(1 + A\beta) = \frac{V_o}{Z_o}$$

$$Z_{OF} = \frac{V_o}{I_o} = Z_o(1 + A\beta)$$

The output impedance is increased by factor $(1 + A\beta)$

7. Sketch the circuit diagram of a two-stage capacitor coupled BJT amplifier that uses series voltage negative feedback. Briefly explain h_{oe} the feedback operates (Nov/Dec 2015)

It is a shunt or nodal sampling and series mixing. Also cascading means two or more amplifier are connected in series using coupling capacitor or coupling elements. This is shown in fig.



Above fig shows cascaded voltage series amplifier. This analysis of cascaded amplifiers is as follows.

Step 1:

RF and RE1 acts as feedback. The,

i) ß network is directly taken from V_0. Therefore, it is called voltage sampled.
ii) Also βnetwork is not directly connected to base hence it is not shunt mixing and therefore it is series feedback.

Therefore, the voltage series feedback X_0, X_S, X_i, X_f are voltages. Then its analysis is as followings.

Step 2 :

$$\beta = \frac{V_f}{V_0}$$

$$Where V_f = \left(\frac{V_0}{R_f + R_{E1}}\right) R_{E1}$$

$$Also, \beta = \frac{\left(\frac{V_0}{R_f + R_{E1}}\right) R_{E1}}{V_0}$$

$$\therefore \beta = \frac{R_{E1}}{R_f + R_{E1}}$$

Step 3 : $Drawing basic amplifier.=$

$$(i) For the input circuit go to output and put X_0 = 0; i.e., V_0 = 0$$

$$(ii) For output circuit go to input and put I_i = 0$$

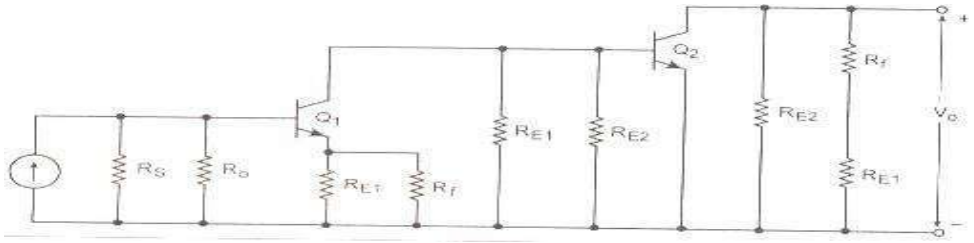
$$Anyhow, \quad R_E = R_{E1} \parallel R_f \quad (or)$$

$$R_E = \frac{R_{E1} R_f}{R_{E1} + R_f}$$

$$Also, \quad R_{L2} = R_{C2} \parallel (R_f + R_{E1})$$

$$R_{L2} = \frac{R_{C2} \times (R_f + R_{E1})}{R_{C2} + R_f + R_{E1}}$$

This is the basic amplifier equivalent circuit is as in figure 3.40



Here, the first stage is common emitter connection with feedback resistor $R_f and R_{E1}$ is also called***globalfeedback.***

$Step\ 4:\ Analysisgivesthefollowingresultsinshort,$

$i.e.,$ $\quad D = 1 + A_V\beta$

$$A_{Vf} = \frac{A_V}{D} \text{ or } \frac{A_V}{(1 + A_V\beta)}$$

$$R_{if} = R_i \times D \text{ or } R_i(1 + A_V\beta)$$

$$R_{0f} = \frac{R_0}{D} \text{ or } \frac{R_0}{(1 + A_V\beta)}$$

From the above analysis voltage gain with feedback A_{VF} and output resistance R_{0f} is reduced by $(1 + A\beta)$ times, and input resistance (R_{if}) with feedback is increased by $(1 + A\beta)$ times.

MADHA
Expertise | Empathy | Excellence
ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

EC 3452 ELECTROMAGENTIC FIELDS

Semester - 04

Notes

MADHA
Expertise | Empathy | Excellence
ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Vision

To excel in providing value based education in the field of Electronics and Communication Engineering, keeping in pace with the latest technical developments through commendable research, to raise the intellectual competence to match global standards and to make significant contributions to the society upholding the ethical standards.

Mission

- ✓ To deliver Quality Technical Education, with an equal emphasis on theoretical and practical aspects.
- ✓ To provide state of the art infrastructure for the students and faculty to upgrade their skills and knowledge.
- ✓ To create an open and conducive environment for faculty and students to carry out research and excel in their field of specialization.
- ✓ To focus especially on innovation and development of technologies that is sustainable and inclusive, and thus benefits all sections of the society.
- ✓ To establish a strong Industry Academic Collaboration for teaching and research, that could foster entrepreneurship and innovation in knowledge exchange.
- ✓ To produce quality Engineers who uphold and advance the integrity, honour and dignity of the engineering.

PROGRAMEDUCATIONALOBJECTIVES(PEOs)

1. To provide the students with a strong foundation in the required sciences in order to pursue studies in Electronics and Communication Engineering.
2. To gain adequate knowledge to become good professional in electronic and communication engineering associated industries, higher education and research.
3. To develop attitude in lifelong learning, applying and adapting new ideas and technologies as their field evolves.
4. To prepare students to critically analyze existing literature in an area of specialization and ethically develop innovative and research oriented methodologies to solve the problems identified.
5. To inculcate in the students a professional and ethical attitude and anability to visualize the engineering issues in a broader social context.

PROGRAMSPECIFICOUTCOMES(PSOs)

PSO1: Design, develop and analyze electronic systems through application of relevant electronics, mathematics and engineering principles.

PSO2: Design, develop and analyze communication systems through application of fundamentals from communication principles, signal processing, and RF System Design &Electromagnetics.

PSO3: Adapt to emerging electronics and communication technologies and develop innovative solutions for existing and newer problems.

EC3452 ELECTROMAGNETIC FIELDS L T P C
3 0 0 3

COURSE OBJECTIVES :

- To impart knowledge on the basics of static electric field and the associated laws
- To impart knowledge on the basics of static magnetic field and the associated laws
- To give insight into coupling between electric and magnetic fields through Faraday's law, displacement current and Maxwell's equations
- To gain the behaviour of the propagation of EM waves
- To study the significance of Time varying fields.

UNIT I INTRODUCTION 9

Electromagnetic model, Units and constants, Review of vector algebra, Rectangular, cylindrical and spherical coordinate systems, Line, surface and volume integrals, Gradient of a scalar field, Divergence of a vector field, Divergence theorem, Curl of a vector field, Stoke's theorem, Null identities, Helmholtz's theorem, Verify theorems for different path, surface and volume.

UNIT II ELECTROSTATICS 9

Electric field, Coulomb's law, Gauss's law and applications, Electric potential, Conductors in static electric field, Dielectrics in static electric field, Electric flux density and dielectric constant, Boundary conditions, Electrostatics boundary value problems, Capacitance, Parallel, cylindrical and spherical capacitors, Electrostatic energy, Poisson's and Laplace's equations, Uniqueness of electrostatic solutions, Current density and Ohm's law, Electromotive force and Kirchhoff's voltage law, Equation of continuity and Kirchhoff's current law

UNIT III MAGNETOSTATICS 9

Lorentz force equation, Ampere's law, Vector magnetic potential, Biot-Savart law and applications, Magnetic field intensity and idea of relative permeability, Calculation of magnetic field intensity for various current distributions Magnetic circuits, Behaviour of magnetic materials, Boundary conditions, Inductance and inductors, Magnetic energy, Magnetic forces and torques

UNIT IV TIME-VARYING FIELDS AND MAXWELL's EQUATIONS 9

Faraday's law, Displacement current and Maxwell-Ampere law, Maxwell's equations, Potential functions, Electromagnetic boundary conditions, Wave equations and solutions, Time-harmonic fields, Observing the Phenomenon of wave propagation with the aid of Maxwell's equations

UNIT V PLANE ELECTROMAGNETIC WAVES 9

Plane waves in lossless media, Plane waves in lossy media (low-loss dielectrics and good conductors), Group velocity, Electromagnetic power flow and Poynting vector, Normal incidence at a plane conducting boundary, Normal incidence at a plane dielectric boundary 32

COURSE OUTCOMES :

At the end of the course the students will be able to

CO1: Relate the fundamentals of vector, coordinate system to electromagnetic concepts
CO2: Analyze the characteristics of Electrostatic field
CO3: Interpret the concepts of Electric field in material space and solve the boundary conditions
CO4: Explain the concepts and characteristics of Magneto Static field in material space and solve boundary conditions.
CO5: Determine the significance of time varying fields

TOTAL:45 PERIODS

TEXT BOOKS

1. D.K. Cheng, Field and wave electromagnetics, 2nd ed., Pearson (India), 2002
2. M.N.O.Sadiku and S.V. Kulkarni, Principles of electromagnetics, 6th ed., Oxford(Asian Edition), 2015

REFERENCES

1. Edward C. Jordan & Keith G. Balmain,Electromagnetic waves and Radiating Systems, Second Edition, Prentice-Hall Electrical Engineering Series, 2012.
2. W.H. Hayt and J.A. Buck, Engineering electromagnetics, 7th ed., McGraw-Hill (India), 2006
3. B.M. Notaros, Electromagnetics, Pearson: New Jersey, 2011

UNIT-1

VECTOR ANALYSIS

INTRODUCTION:

Electromagnetics is a branch of Physics (or) electrical engineering which is used to study the electric and magnetic phenomena.

What is a field?

Consider a magnet. It has its own effect in a region surrounding it. The effect can be placed by placing another magnet near the first magnet. such an effect can be desined by a particular physical function.

In the region surrounding the magnet, there exists a particular value for that physical function, at every point, describing the effect of magnet.

So field can be desined as the region in which, at each point there exists a corresponding value of some physical function.

If the field is produced is due to magnetic effects, it is called MAGNETIC FIELD.

There are two types of electric charges, positive and negative. such an electric charge produces a field around it which is called an ELECTRIC FIELD

Moving charges produces current and current carrying conductor produces a magnetic field. In such case electric and magnetic fields are related to each other. such a field is called ELECTROMAGNETIC FIELD. Such fields may be time varying or time independent.

It is seen that distribution of a quantity in a space is defined by a field. Hence to quantify the field, three dimensional representation plays an important role. Such three dimensional representation can be made easy by the use of vector analysis.

SCALARS & VECTORS:

The various quantities involved in the study of engineering electromagnetics can be classified as

1. scalars &
2. vectors.

SCALAR:

The scalar is a quantity whose value may be represented by a single real number, which may be +ve (or) -ve. The direction is not at all required in describing a scalar. Thus

A scalar is a quantity which is wholly characterized by its magnitude.

eg: temperature, mass, volume, density, speed electric charge etc.

VECTOR:

A quantity which has both, a magnitude and a specific direction in space is called a vector.

In electromagnetics vectors defined in two and three dimensional spaces are required but vectors may be defined in n-dimensional space.

A vector is a quantity which is characterized by both, a magnitude and a direction.

eg: force, velocity, displacement, electric field intensity, magnetic field intensity, acceleration etc.

VECTOR FIELD

SCALAR FIELD :

The distribution of a scalar quantity with a definite position in a space is called SCALAR FIELD.

eg :- 1. Temperature of atmosphere.
(It has a desinite value in the atmosphere but no need of direction to specisy).

2. Height of surface of earth above sea level
3. Sound intensity in an auditorium.
4. Light intensity in a room.
5. Atmospheric pressure in a given region etc.

VECTOR FIELD :

Is a quantity which is specisied in a region to define a field is a vector then the corresponding field is called a vector field.

eg :- 1. Gravitational force on a mass in a space is a vector field. [This force has a value at various points in a space and always has a specisic direction].

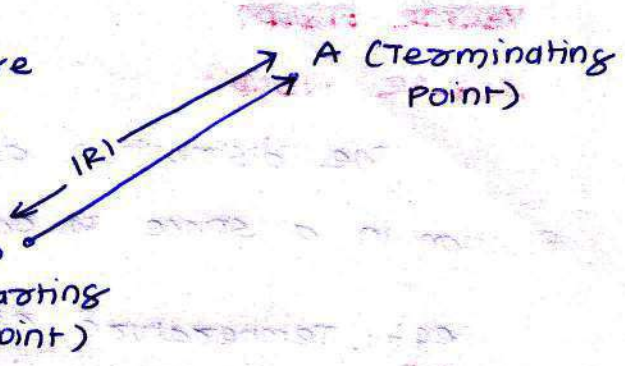
2. Velocity of particles in a moving fluid
3. Wind velocity of atmosphere
4. Voltage gradient in a cable
5. Displacement of a flying bird in a space.
6. Magnetic field existing from north to south poles.

REPRESENTATION OF A VECTOR :

In two dimensional, a vector can be represented by a straight line with an arrow in a plane. The length of the segment is the magnitude of a vector while the

arrow indicates the direction of the vector.

The vector shown in figure is symbolically denoted as $\vec{OA}$. It's length is called as magnitude, which is R for the vector OA.

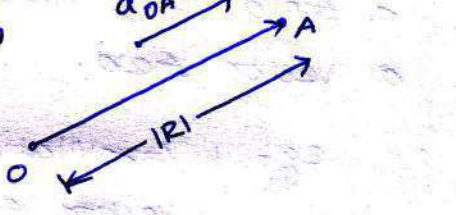


It is represented as $|\vec{OA}| = R$

UNIT VECTOR:

A unit vector has a function to indicate the direction. It's magnitude is always unity, irrespective of its direction. Thus for any vector, to indicate its direction a unit vector can be used.

consider a unit vector $\vec{a}_{OA}$ in the direction of $\vec{OA}$ as shown in fig. This indicates the direction of $\vec{OA}$ but its magnitude is unity.



So vector $\vec{OA}$ can be represented completely as its magnitude R and the direction as indicated by the unit vector along its direction.

$$\vec{OA} = |\vec{OA}|\,\vec{a}_{OA} = R\vec{a}_{OA}$$

↳ unit vector along the direction OA and $|\vec{a}_{OA}| = 1$

letter $\vec{a}$ is used to indicate the unit vector

2 Mark Question:

1. Mention the purpose of unit vector in vector algebra.

In case is a vector is known then the unit vector along that vector can be obtained by dividing the vector by its magnitude. Thus unit vector can be expressed as,

$$\text{Unit vector } \vec{a}_{OA} = \frac{\vec{OA}}{|OA|}$$

2mark question.

1. **Express unit vector in terms of a vector and its magnitude.**

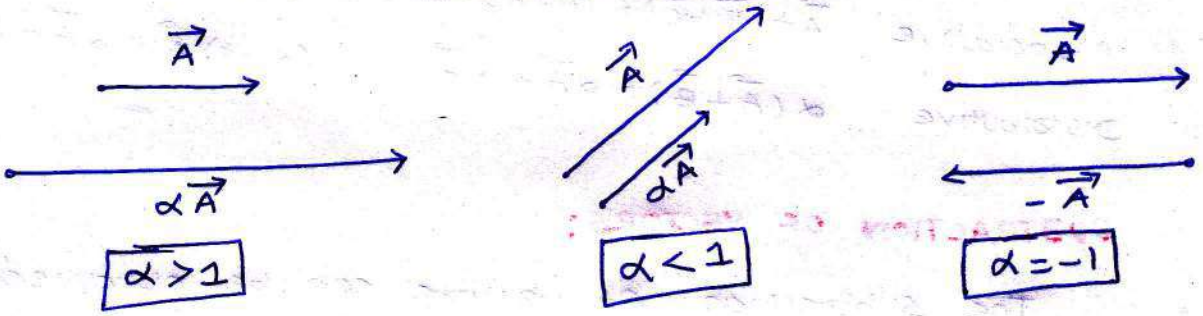
VECTOR ALGEBRA: [Scaling, Addition, subtraction].

SCALING OF VECTOR

→ This is multiplication by a scalar to a vector

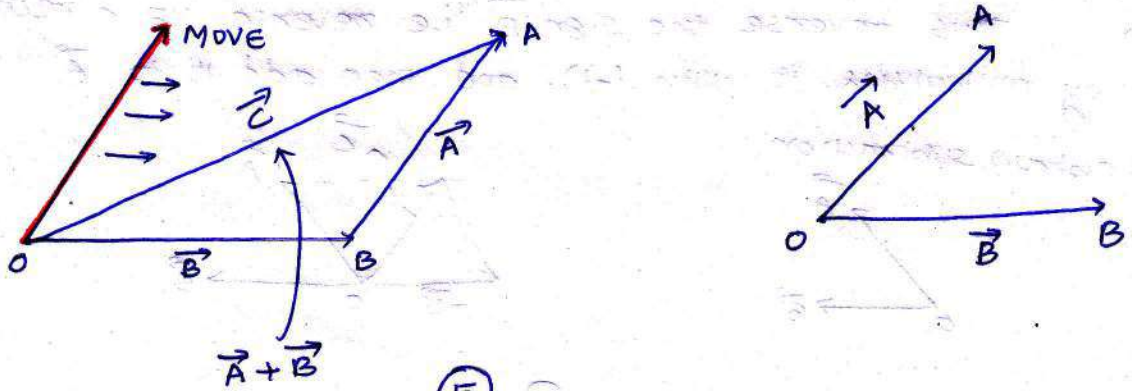
→ This changes the magnitude (length) of a vector but not its direction, when scalar is POSITIVE

→ when scalar = -1, the magnitude remains same but direction of the vector reverses.



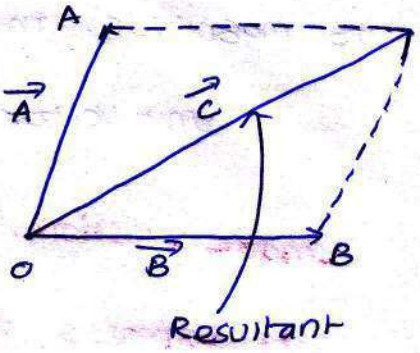
ADDITION OF VECTORS:

→ The vectors which lie on the same plane are called coplanar vectors.

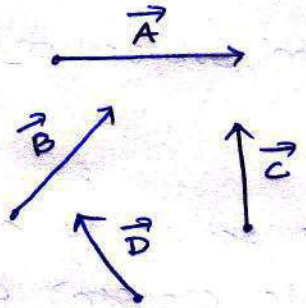


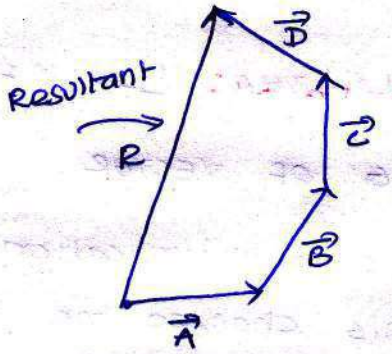
PARALLELOGRAM RULE:-

Complete the parallelogram as shown in fig. Then the diagonal of the parallelogram represents the addition of the two vectors.



HEAD TO TRIAL RULE:-





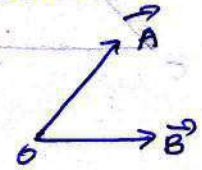
Law	Addition	Multiplication by scalar
commutative	$\vec{A}+\vec{B}=\vec{B}+\vec{A}$	$\alpha\vec{A}=\vec{A}\alpha$
Associative	$\vec{A}+(\vec{B}+\vec{C})=(\vec{A}+\vec{B})+\vec{C}$	$\beta(\alpha\vec{A})=(\beta\alpha)\vec{A}$
Distributive	$\alpha(\vec{A}+\vec{B})=\alpha\vec{A}+\alpha\vec{B}$	$(\alpha+\beta)\vec{A}=\alpha\vec{A}+\beta\vec{A}$

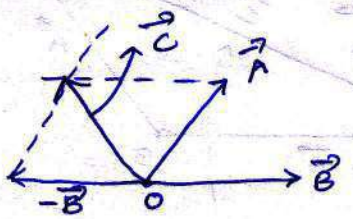
SUBTRACTION OF VECTORS:

The subtraction of vectors can be obtained from the rules of addition. If $\vec{B}$ is to be subtracted from $\vec{A}$ then based on addition it can be represented as

$$\vec{C}=\vec{A}+(-\vec{B}).$$

Thus reverse the sign $\vec{B}$ i.e reverse its direction by multiplying it with (-1). and then add it to $\vec{A}$ to obtain subtraction.





Identical Vectors:

Two vectors are said to be identical if their difference is zero.

eg: $\vec{A} - \vec{B} = 0$ $\vec{A}$ & $\vec{B}$ are identical.

$\Rightarrow \vec{A} = \vec{B}$

VECTOR MULTIPLICATION:

Consider two vectors $\vec{A}$ and $\vec{B}$. There are two types of Products existing depending upon the result of the multiplication. These two types of products are

1. Scalar (or) DOT Product
2. Vector (or) Cross Product

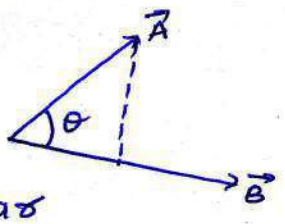
SCALAR (OR) DOT PRODUCT OF VECTORS:

→ It is denoted by $\vec{A} \cdot \vec{B}$

→ It is desined as the Product of the magnitve of $\vec{A}$, the magnitude of $\vec{B}$ and the cosine of smaller angle b/w them.

→ It also can be desined as the Product of magnitude of $\vec{B}$ and the projection of $\vec{A}$ onto $\vec{B}$ or vice versa

$$\boxed{\vec{A} \cdot \vec{B} = |\vec{A}|\,|\vec{B}| \cos\theta_{AB}}$$



The result of such a dot Product is scalar hence it is also called as scalar Product.

PROPERTIES OF DOT PRODUCT

1. If the two vectors are $\parallel^{el}$ to each other i.e $\theta = 0$ then

$\cos\theta_{AB} = 1$ Thus

$\vec{A} \cdot \vec{B} = |\vec{A}|\,|\vec{B}|$ for $\parallel^{el}$ vectors.

2. If two vectors are $\perp^{r}$ to each other i.e $\theta = 90^{\circ}$ then

$\cos\theta_{AB} = 0^{\circ}$ Thus

$\vec{A} \cdot \vec{B} = 0$ for $\perp^{r}$ vectors.

3. If the dot product of vector with itself is performed, the result is square of the magnitude of that vector.

$$\vec{A} \cdot \vec{A} = |\vec{A}|\,|\vec{A}| \cos\theta = |\vec{A}|^2$$

4. Any unit vector dotted with itself is unity.

$$\vec{a}_x \cdot \vec{a}_x = 1 = \vec{a}_y \cdot \vec{a}_y = \vec{a}_z \cdot \vec{a}_z$$

5. The dot product obeys commutative, & distributive law

(ie) $\vec{A} \cdot \vec{B} = \vec{B} \cdot \vec{A}$

$$\vec{A} \cdot (\vec{B} + \vec{C}) = \vec{A} \cdot \vec{B} + \vec{A} \cdot \vec{C}$$

2 mark question.

1. Given two vectors, How to identify whether they are $\perp^{re}$ or $\parallel^{el}$ to each other.

APPLICATION OF DOT PRODUCT:

1. To determine the angle b/w the two vectors.

$$\theta = \cos^{-1}\left\{\frac{\vec{A} \cdot \vec{B}}{|\vec{A}|\,|\vec{B}|}\right\}.$$

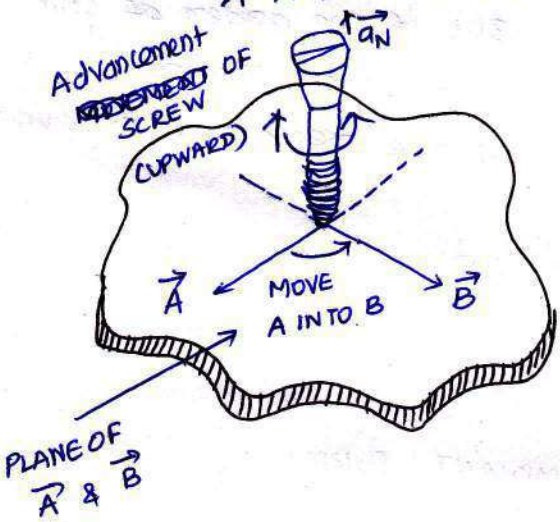
VECTOR (OR) CROSS PRODUCT OF VECTORS:

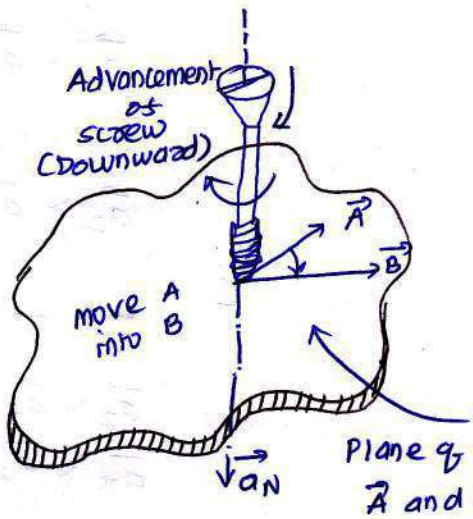
consider two vectors $\vec{A}$ & $\vec{B}$ then the cross product is denoted as $\vec{A} \times \vec{B}$ and defined as the product of the magnitudes of $\vec{A}$ & $\vec{B}$ and the sine of the smaller angle between $\vec{A}$ and $\vec{B}$.

CROSS PRODUCT is a vector quantity and has a direction $\perp^r$ to the plane, containing the two vectors $\vec{A}$ and $\vec{B}$.

Mathematically cross product is expressed as

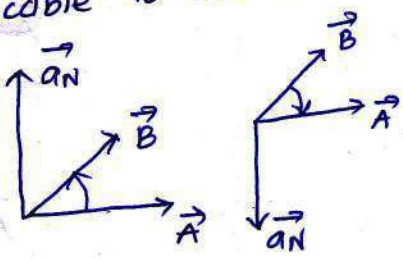
$$\vec{A} \times \vec{B} = |\vec{A}|\,|\vec{B}| \sin\theta_{AB}\, \vec{a}_N$$





PROPERTIES OF CROSS PRODUCT:

1. The commutative law is not applicable to the cross product thus $\boxed{\vec{A} \times \vec{B} \neq \vec{B} \times \vec{A}}$



2. Reversing the order of the vectors $\vec{A}$ and $\vec{B}$, a unit vector $\vec{a}_N$ reverses its direction hence we can write

$$\vec{A} \times \vec{B} = -[\vec{B} \times \vec{B}]$$ anticommutative

3. The cross product is not associative, thus

$$\vec{A} \times (\vec{B} \times \vec{C}) \neq (\vec{A} \times \vec{B}) \times \vec{C}$$

4. With respect to addition cross product is distributive, thus

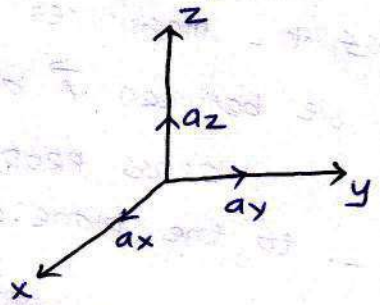
$$\vec{A} \times (\vec{B} + \vec{C}) = \vec{A} \times \vec{B} + \vec{A} \times \vec{C}.$$

5. If two vectors are $\parallel^{el}$ to each other, (ie) They are in same direction then $\theta = 0^\circ$ & hence cross product of such two vectors is zero.

6. $\vec{A} \times \vec{A} = 0$ [cross product to itself].

7. cross product of unit vectors.

consider the unit vectors $\vec{a}_x$, $\vec{a}_y$ and $\vec{a}_z$ which are mutually $\perp^r$ to each other as shown in fig.



Then

$$\vec{a}_x \times \vec{a}_y = |\vec{a}_x||\vec{a}_y| \sin(90^\circ)\, \vec{a}_N$$

In this case $\vec{a}_N = \vec{a}_z$

and $|\vec{a}_x| = |\vec{a}_y| = \sin(90^\circ) = 1$

$$\therefore \quad \vec{a}_x \times \vec{a}_y = \vec{a}_z$$
$$\vec{a}_y \times \vec{a}_z = \vec{a}_x$$
$$\vec{a}_z \times \vec{a}_x = \vec{a}_y$$

But if the order of unit vectors is reversed, the result is -ve of the remaining third unit vector

Thus

$$\vec{a}_y \times \vec{a}_x = -\vec{a}_z$$
$$\vec{a}_z \times \vec{a}_y = -\vec{a}_x$$
$$\vec{a}_x \times \vec{a}_z = -\vec{a}_y$$

CROSS PRODUCT IN DETERMINANT FORM:

consider two vectors

$$\vec{A} = A_x \vec{a}_x + A_y \vec{a}_y + A_z \vec{a}_z$$
$$\vec{B} = B_x \vec{a}_x + B_y \vec{a}_y + B_z \vec{a}_y$$

$$\vec{A} \times \vec{B} = \begin{vmatrix} \vec{a}_x & \vec{a}_y & \vec{a}_z \\ A_x & A_y & A_z \\ B_x & B_y & B_z \end{vmatrix}$$

$$\vec{A} \times \vec{B} = [A_y B_z - B_y A_z]\vec{a}_x + [A_z B_x - A_x B_z]\vec{a}_y + [A_x B_y - A_y B_x]\vec{a}_z$$

PRODUCTS OF THREE VECTORS :-

Let $\vec{A}$, $\vec{B}$ and $\vec{C}$ are the three given vectors. Then the product of these three vectors is classified into two ways called,

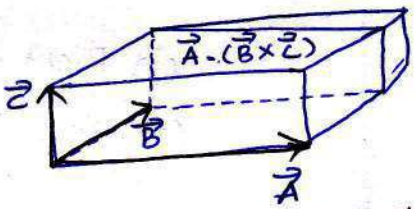
1. Scalar triple Product
2. Vector triple Product.

SCALAR TRIPLE PRODUCT: (scalar triple product of 3 vectors $\vec{A}, \vec{B}$ & $\vec{C}$).

$$\vec{A}.(\vec{B}\times\vec{C}) = \vec{B}.(\vec{C}\times\vec{A}) = \vec{C}.(\vec{A}\times\vec{B}).$$

$$\vec{A}.(\vec{B}\times\vec{C}) = \begin{vmatrix} A_x & A_y & A_z \\ B_x & B_y & B_z \\ C_x & C_y & C_z \end{vmatrix}$$

1. It represents the volume of Parallelepiped.



2. If two (or) three vectors are equal then the result of the scalar triple product is zero.

3. cyclic order a, b, c is to be followed. If the order is changed, the sign is reversed.

$$\vec{A}.(\vec{B}\times\vec{C}) = -\vec{B}.(\vec{A}\times\vec{C}).$$

VECTOR TRIPLE PRODUCT :-

The vector triple product of the three vectors $\vec{A}$, $\vec{B}$ and $\vec{C}$ is mathematically defined as

$$\vec{A}\times(\vec{B}\times\vec{C}) = \vec{B}(\vec{A}.\vec{C}) - \vec{C}(\vec{A}.\vec{B})$$

"bac-cab" RULE

Problem

1. Three fields are given by $\vec{A} = 2\vec{a}_x - \vec{a}_z$, $\vec{B} = 2\vec{a}_x - \vec{a}_y + 2\vec{a}_z$, $\vec{C} = 2\vec{a}_x - 3\vec{a}_y + \vec{a}_z$.

Find the scalar and vector triple product.

Scalar triple product. (ii)

$$\vec{A}.(\vec{B}\times\vec{C}) = \begin{vmatrix} 2 & 0 & 1 \\ 2 & -1 & 2 \\ 2 & -3 & 1 \end{vmatrix}$$

$$= 14.$$

Vector triple product.

$$\vec{A}\times(\vec{B}\times\vec{C}) = \vec{B}(\vec{A}.\vec{C}) - \vec{C}(\vec{A}.\vec{B})$$

$$\vec{A}.\vec{C} = (2)(2) + (0)(-3) + (-1)(1) = 3$$

$$\vec{A}.\vec{B} = (2)(2) + (0)(-1) + (-1)(2) = 2$$

$$\vec{A}\times(\vec{B}\times\vec{C}) = 3\vec{B} - 2\vec{C}$$

$$= 3[2\vec{a}_x - \vec{a}_y + 2\vec{a}_z] - 2[2\vec{a}_x - 3\vec{a}_y + \vec{a}_z]$$

$$= 2\vec{a}_x + 3\vec{a}_y + 4\vec{a}_z.$$

CO-ORDINATE SYSTEM:

Three types of co-ordinate systems are

(i) Cartesian (or) Rectangular co-ordinate system
(ii) cylindrical co-ordinate system
(iii) spherical co-ordinate system.

CARTESIAN CO-ORDINATE SYSTEM:

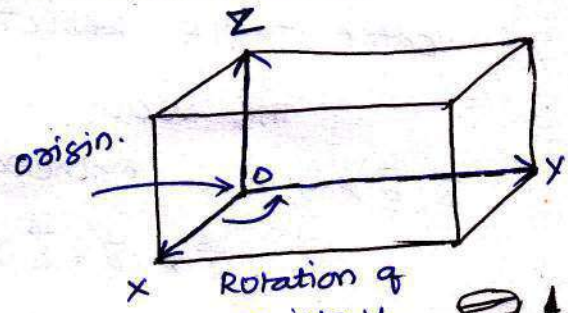
- Also called Rectangular co-ordinate system
- Three co-ordinates x, y, z mutually $\perp^r$ to each other.
- Intersection of x, y, z is called origin.

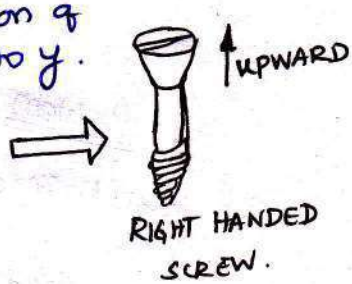
There are two types of such systems, they are

(i) Right handed system
(ii) Left handed system.

RIGHT HANDED SYSTEM:

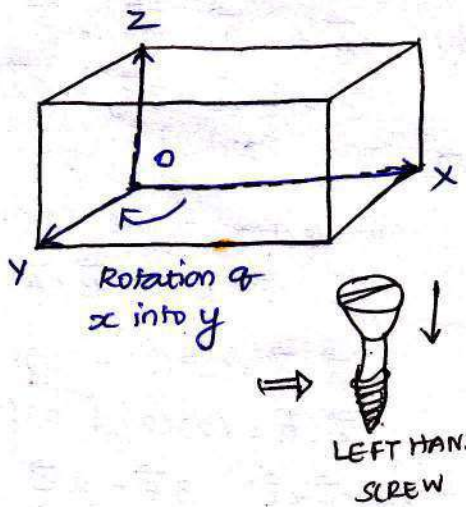
If x axis is rotated towards y axis through a smaller angle, thus this rotation causes the upward movement of right handed screw in the 'z' axis direction.





LEFT HANDED SYSTEM:

Downward movement of screw.



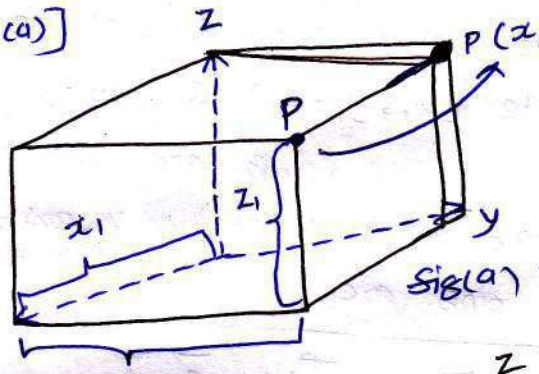
Note: RIGHT HANDED SYSTEM IS COMMONLY USED

REPRESENTING A POINT IN RECTANGULAR CO-ORDINATE SYSTEMS

→ A point in rectangular co-ordinate system is located by three coordinates namely x, y and z co-ordinates.

→ The point can be reached by moving from origin, the distance x in x direction, then the distance y in y direction and finally distance z in z direction.

→ Consider a point P having co-ordinates x_1, y_1 and z_1. It is represented as $P(x_1, y_1, z_1)$. The co-ordinates x_1, y_1, z_1 may be +ve or -ve [fig (a)]



fig(a)

→ The point Q(3, -1, 2) can be shown in this system as shown in fig (b)

FOLLOW (13A) & (13B) sheets & come here

POSITION & DISTANCE VECTORS:

Consider a point $P[x_1, y_1, z_1]$ in cartesian co-ordinate system as shown in fig (c). Then the **position vector** of point 'P' is represented by the distance of point P from the origin directed from origin to point P. This is also called **RADIUS VECTOR**.

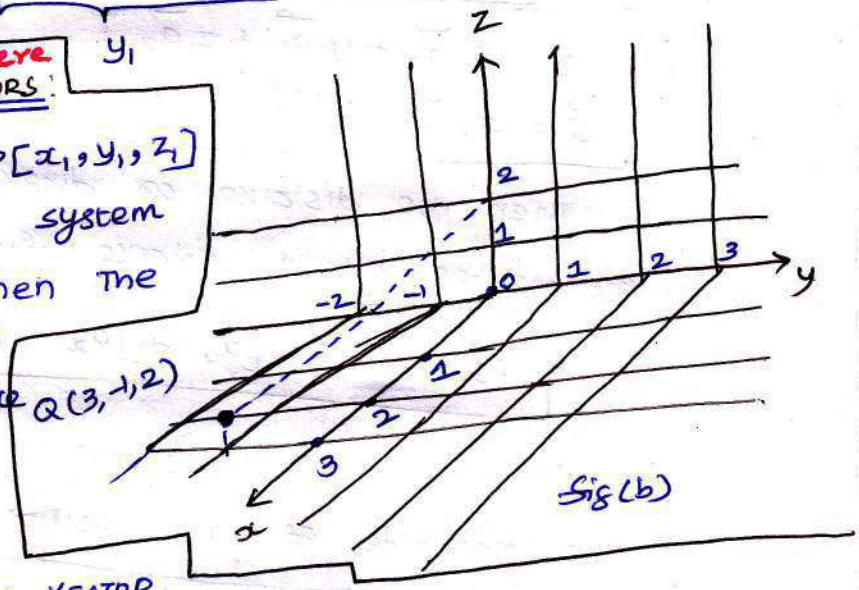
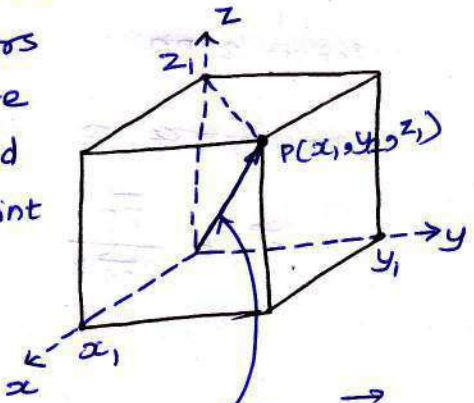


fig (b)

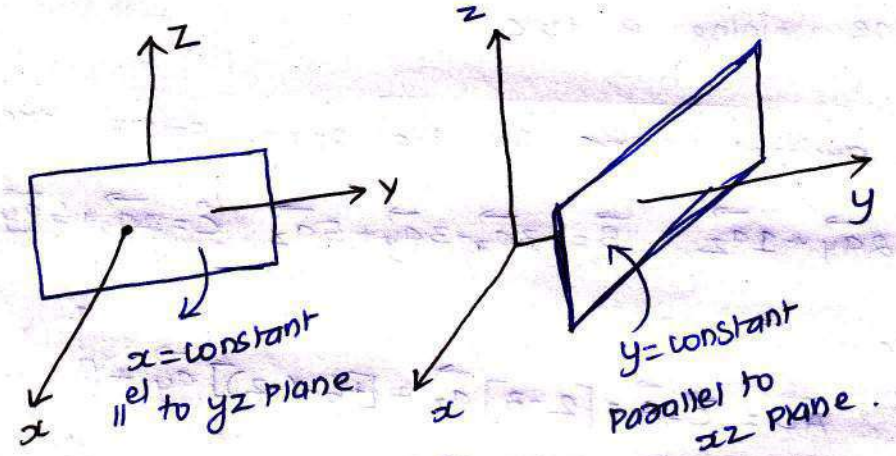
- The three components of the position vector $\vec{r}_{op}$ are three vectors oriented along the three co-ordinate axes with the magnitudes x_1, y_1 and z_1. Thus the position vector of point P can be represented as

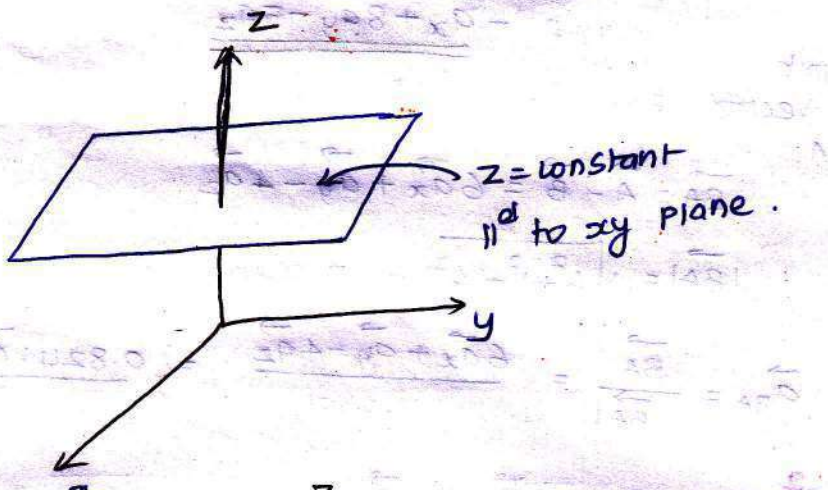
$$\vec{r}_{op} = x_1 \vec{a}_x + y_1 \vec{a}_y + z_1 \vec{a}_z$$

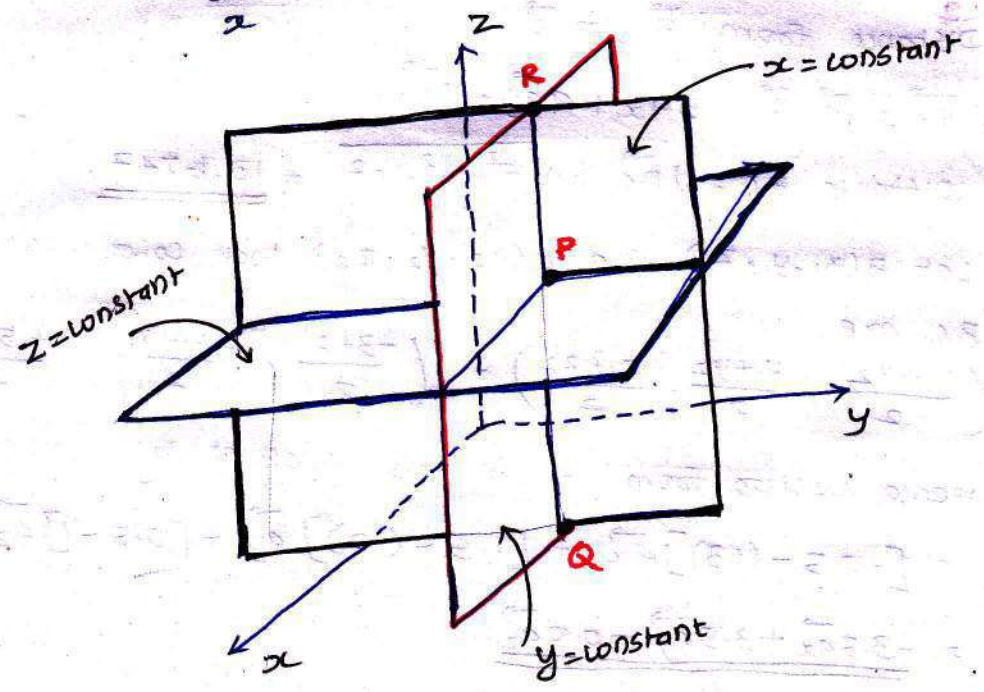


ALTERNATE METHOD TO DEFINE A POINT IN CARTESIAN SYSTEM:

Alternate method to consider three surfaces namely x = constant, y = constant and z = constant. The common intersection of all these three surfaces is the point to be defined and the constants indicate the co-ordinates of that point. as shown in figures given below.







Problem

Given three Points in cartesian co-ordinate system as A(3,-2,1), B(-3,-3,5) and C(2,6,-4)

Find (i) The vector from A to C

(ii) The unit vector from B to A

(iii) The distance from B to C.

(iv) The vector from A to the midpoint of the straight line joining B to C.

Solution:

The position vectors for the given points are

$\vec{A} = 3\vec{a}_x - 2\vec{a}_y + 1\vec{a}_z \quad \vec{B} = -3\vec{a}_x - 3\vec{a}_y + 5\vec{a}_z \quad \vec{C} = 2\vec{a}_x + 6\vec{a}_y - 4\vec{a}_z$

(i) from vector $\vec{A}$ to $\vec{C}$

$$\vec{AC} = \vec{C} - \vec{A} = [2-3]\vec{a}_x + [+6-(-2)]\vec{a}_y + [-4-(+1)]\vec{a}_z$$

$$= -\vec{a}_x + 8\vec{a}_y - 5\vec{a}_z$$

(ii) unit vector from from $\vec{B}$ to $\vec{A}$

$$\vec{BA} = \vec{A} - \vec{B} = 6\vec{a}_x + \vec{a}_y - 4\vec{a}_z$$

$$|\vec{BA}| = \sqrt{6^2+1^2+4^2} = 7.2801.$$

$$\vec{a}_{BA} = \frac{\vec{BA}}{|\vec{BA}|} = \frac{6\vec{a}_x + \vec{a}_y - 4\vec{a}_z}{7.2801} = 0.8241\vec{a}_x + 0.1373\vec{a}_y - 0.5494\vec{a}_z$$

(iii) Distance from $\vec{B}$ to $\vec{C}$

$$\vec{BC} = \vec{C} - \vec{B} = 5\vec{a}_x + 9\vec{a}_y - 9\vec{a}_z$$

Distance $BC = |\vec{BC}| = \sqrt{5^2+9^2+9^2} = 13.6747.$

(iv) Let $B(x_1,y_1,z_1)$ and $C(x_2,y_2,z_2)$ then co-ordinates of midpoint of BC are

$$\left(\frac{x_1+x_2}{2}, \frac{y_1+y_2}{2}, \frac{z_1+z_2}{2}\right) = \left(\frac{-3+2}{2}, \frac{-3+6}{2}, \frac{+5-4}{2}\right) = (-0.5, 1.5, 0.5)$$

Hence vector from A to this midpoint is

$$= [-0.5-(+3)]\vec{a}_x + [1.5-(-2)]\vec{a}_y + [0.5-1]\vec{a}_z$$

$$= -3.5\vec{a}_x + 3.5\vec{a}_y - 0.5\vec{a}_z$$

The magnitude of vectors interms of three mutually ⊥r components are given by

$$|\vec{r}_{OP}| = \sqrt{(x_1)^2 + (y_1)^2 + (z_1)^2}$$

if Point P has co-ordinates (1, 2, 3) then its position vector is

$$\vec{r}_{OP} = 1\vec{a}_x + 2\vec{a}_y + 3\vec{a}_z \qquad |\vec{r}_{OP}| = \sqrt{1^2+2^2+3^2} = \sqrt{14} = 3.7416.$$

Now consider two points in a cartesian coordinate system, P and Q with the co-ordinate (x_1, y_1, z_1) & (x_2, y_2, z_2) respectively. The points are shown in fig 1. The individual position vectors of the points are

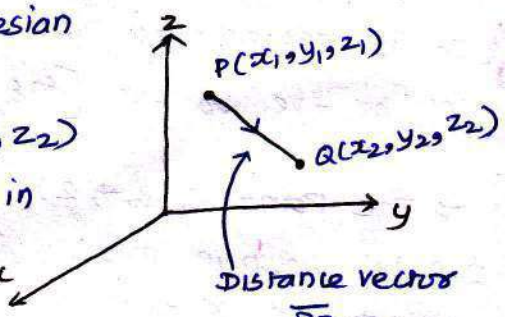


Fig 1

$$\vec{P} = x_1\vec{a}_x + y_1\vec{a}_y + z_1\vec{a}_z$$
$$\vec{Q} = x_2\vec{a}_x + y_2\vec{a}_y + z_2\vec{a}_z$$

Then the distance or displacement from P to Q is represented by a distance vector $\vec{PQ}$ and is given by

$$\vec{PQ} = \vec{Q} - \vec{P} = [x_2 - x_1]\vec{a}_x + [y_2 - y_1]\vec{a}_y + [z_2 - z_1]\vec{a}_z$$

This is also called seperation vectors.

The magnitude of this vector is given by

$$|\vec{PQ}| = \sqrt{(x_2-x_1)^2 + (y_2-y_1)^2 + (z_2-z_1)^2}$$

distance formula → $|\vec{PQ}|$ ← length of PQ

~~Direction of~~ unit vector along direction of PQ is

$$\vec{a}_{PQ} = \frac{\vec{PQ}}{|\vec{PQ}|}.$$

PROBLEM:

1. Obtain the unit vector in the direction from the origin towards the point P(3, -3, 2)

Solution:

The origin O(0,0,0) while P(3,-3,2) hence the distance vector $\vec{OP}$ is

$$\vec{OP} = (3-0)\vec{a}_x + (-3-0)\vec{a}_y + (-2-0)\vec{a}_z$$

$$= 3\vec{a}_x - 3\vec{a}_y - 2\vec{a}_z$$

$$|\vec{OP}| = \sqrt{3^2 + (-3)^2 + (-2)^2} = 4.6904.$$

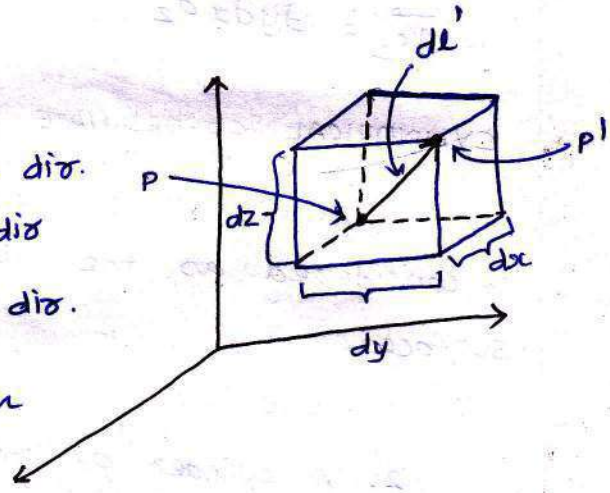
Hence the unit vector along the direction OP is

$$\vec{a}_{OP} = \frac{\vec{OP}}{|\vec{OP}|} = \frac{3\vec{a}_x - 3\vec{a}_y - 2\vec{a}_z}{4.6904}$$

$$= 0.6396\vec{a}_x - 0.6396\vec{a}_y - 0.4264\vec{a}_z$$

DIFFERENTIAL ELEMENTS IN CARTESIAN CO-ORDINATOR SYSTEM:

Consider a point P(x,y,z) in the rectangular coordinate system. Let us increase each co-ordinate by differential amount. A new point P' will be obtained. having co-ordinates (x+dx, y+dy, z+dz)



dx = Differential length in x dir.

dy = Differential length in y dir

dz = Differential length in z dir.

Hence differential vector length also called elementary vector length can be represented as

$$\vec{dl} = dx\vec{a}_x + dy\vec{a}_y + dz\vec{a}_z$$

↳ This is the vector joining P to new point P'.

The distance of P' from P is given by magnitude of the differential vector length.

$$|\vec{dl}| = \sqrt{(dx)^2 + (dy)^2 + (dz)^2}$$

Hence the differential volume of the rectangular Parallelepiped is given by,

$$\boxed{dV = dx\, dy\, dz}$$

Note: $\vec{dl}$ is a vector but dV is a scalar.

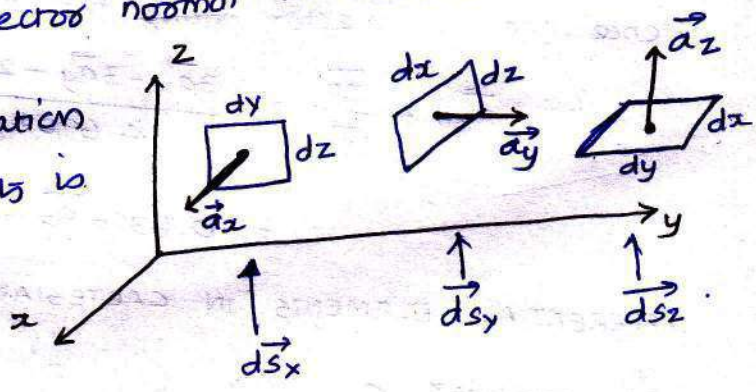
Let us define differential surface areas, the differential surface element $\vec{ds}$ is represented as

$$\vec{ds} = ds\, \vec{a}_n$$

where ds = Differential surface area of the element.

$\vec{a}_n$ = unit vector normal to surface ds.

The vector representation of these three elements is given as,



$$\vec{ds}_x = dy\,dz\,\vec{a}_x$$

$$\vec{ds}_y = dx\,dz\,\vec{a}_y$$

$$\vec{ds}_z = dy\,dx\,\vec{a}_z$$

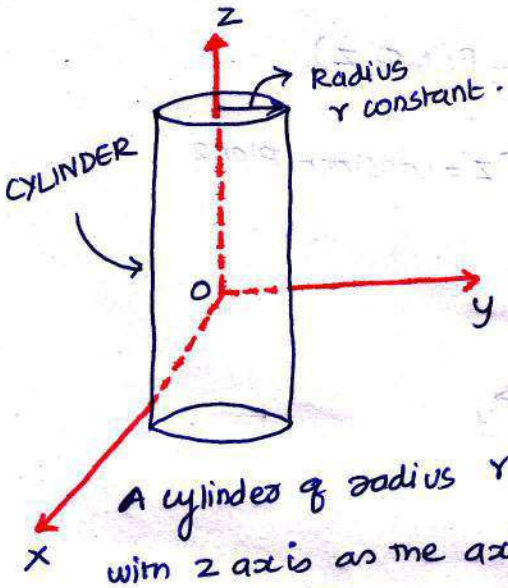
CYLINDRICAL CO-ORDINATE SYSTEM :-

In this system of co-ordinates, any point in a space is considered as the point of intersection of the following surfaces.

1. Plane of constant z which is $\parallel^{el}$ to xy plane
2. A cylinder of radius r with z axis as the axis of the cylinder
3. A half plane $\perp^{r}$ to xy plane and at an angle ϕ w.r.to xz plane. The angle ϕ is called azimuthal angle

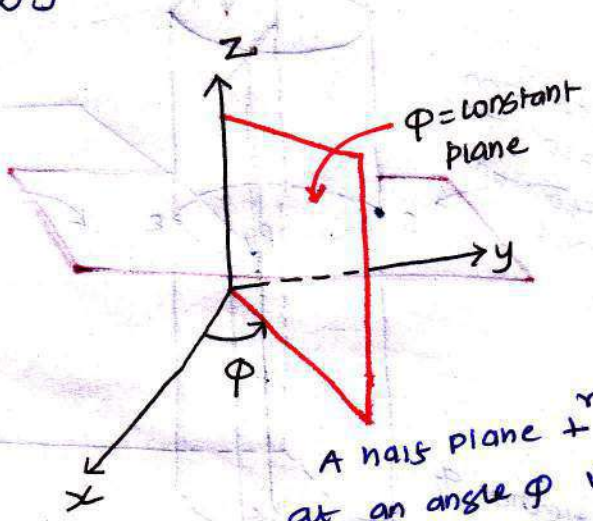
The range of variables are

$$\left.\begin{aligned} 0 \le r \le \infty \\ 0 \le \varphi \le 2\pi \\ -\infty \le z \le \infty \end{aligned}\right\} \quad -(1)$$



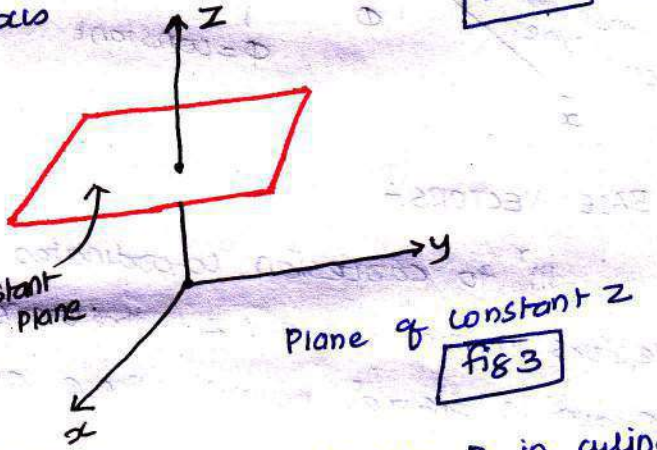
A cylinder of radius r with z axis as the axis of the cylinder

Fig 1



A half plane + r to xy plane at an angle φ w.r.to xz plane

Fig 2



Plane of constant z

Fig 3

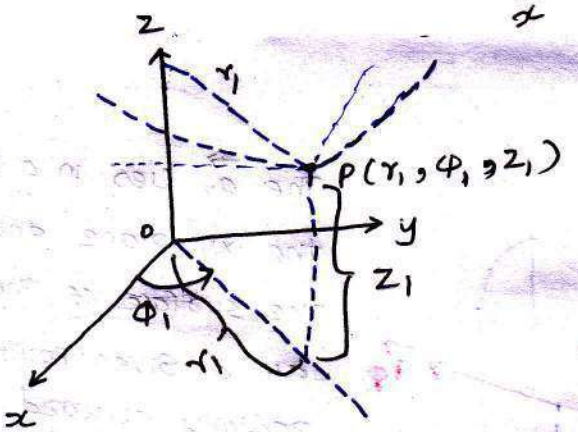
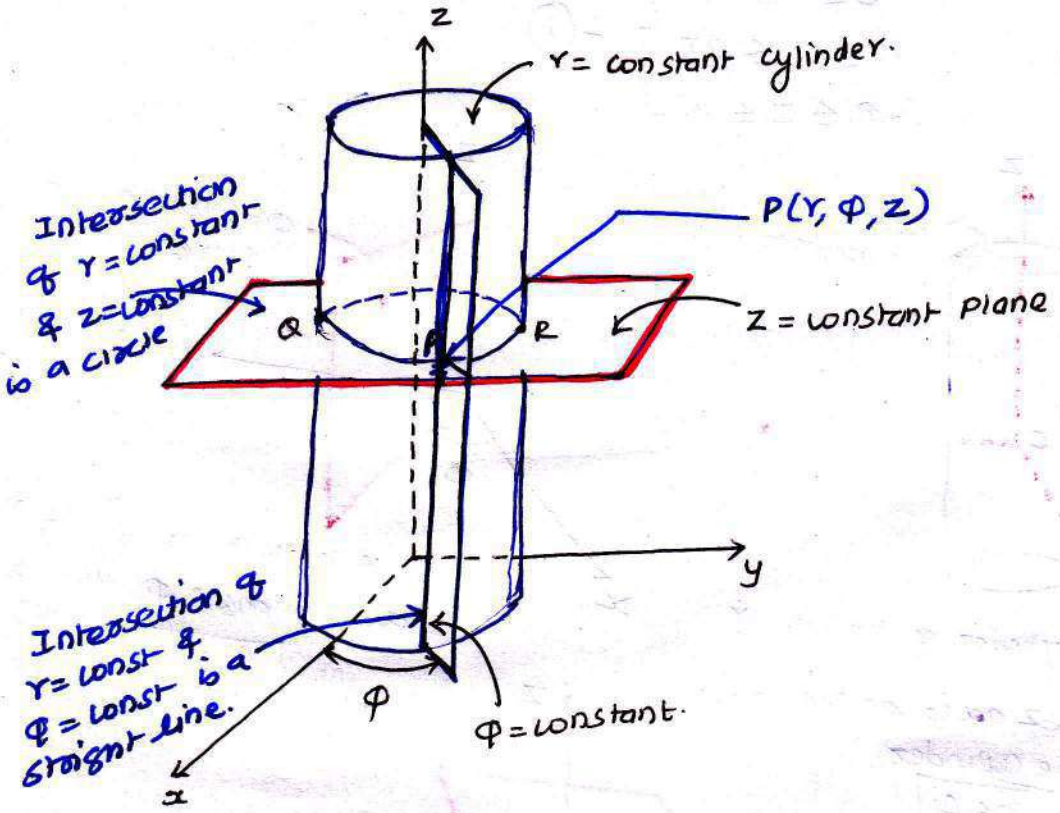


Fig 4

The point P in cylindrical co-ordinate system has three co-ordinates r, φ and z whose values lie in the respective ranges as given in (1).

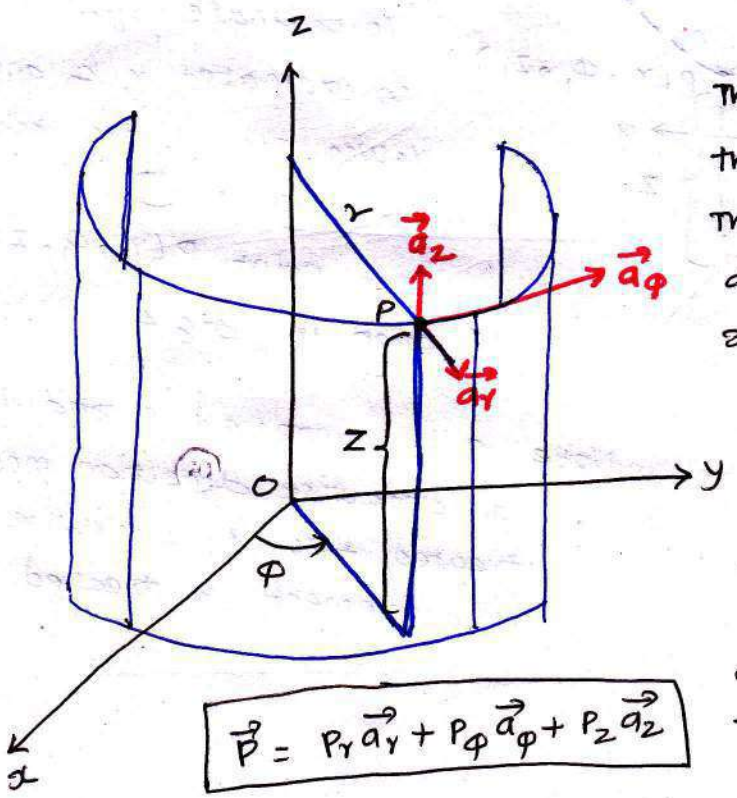
The point $P(r_1, \varphi_1, z_1)$ can be seen in fig 4

Note: φ is expressed in radians and for φ, anticlockwise direction measurement is treated +ve & clockwise direction measurement is treated -ve.



BASE VECTORS:-

III^{r} to cartesian co-ordinates system, there are three unit vectors in the r, φ and z directions denoted as $\vec{a}_r$, $\vec{a}_\varphi$ and $\vec{a}_z$ as shown in figure below. These are mutually $\perp^{r}$ to each other.



$$\vec{P} = P_r \vec{a}_r + P_\varphi \vec{a}_\varphi + P_z \vec{a}_z$$

The $\vec{a}_r$ lies in a plane $\parallel^{el}$ to the xy plane and is $\perp^{r}$ to the surface of the cylinder at a given point coming radially outward.

The unit vector $\vec{a}_\varphi$ also lies in a plane $\parallel^{el}$ to xy plane but it is tangent to the cylinder, pointing in the direction of increasing φ, at the given point.

The unit vector $\vec{a}_z$ is $\parallel^{el}$ to z axis and directed towards increasing 'z'.

$$\vec{P} = P_r \vec{a}_r + P_\phi \vec{a}_\phi + P_z \vec{a}_z$$

where P_r is radius r

P_ϕ is angle ϕ

P_z is co-ordinate of Point P.

Key note:

In the cartesian co-ordinate system, the unit vectors are not dependent on the co-ordinates. But in cylindrical co-ordinate system $\vec{a}_r$ and $\vec{a}_\phi$ are functions of ϕ co-ordinate as their direction changes as ϕ changes. Hence the differentiation or integration w.r.to ϕ components in $\vec{a}_r$ and $\vec{a}_\phi$ should not be treated as constants.

DIFFERENTIAL ELEMENTS IN CYLINDRICAL CO-ORDINATE SYSTEM:

Consider a point $P(r, \phi, z)$ in a cylindrical co-ordinate system. Let each co-ordinate is increased by the differential amount. The differential increments in r, ϕ, z are dr, $d\phi$ and dz respectively.

→ Now there are two cylinders of radius r and $r+dr$

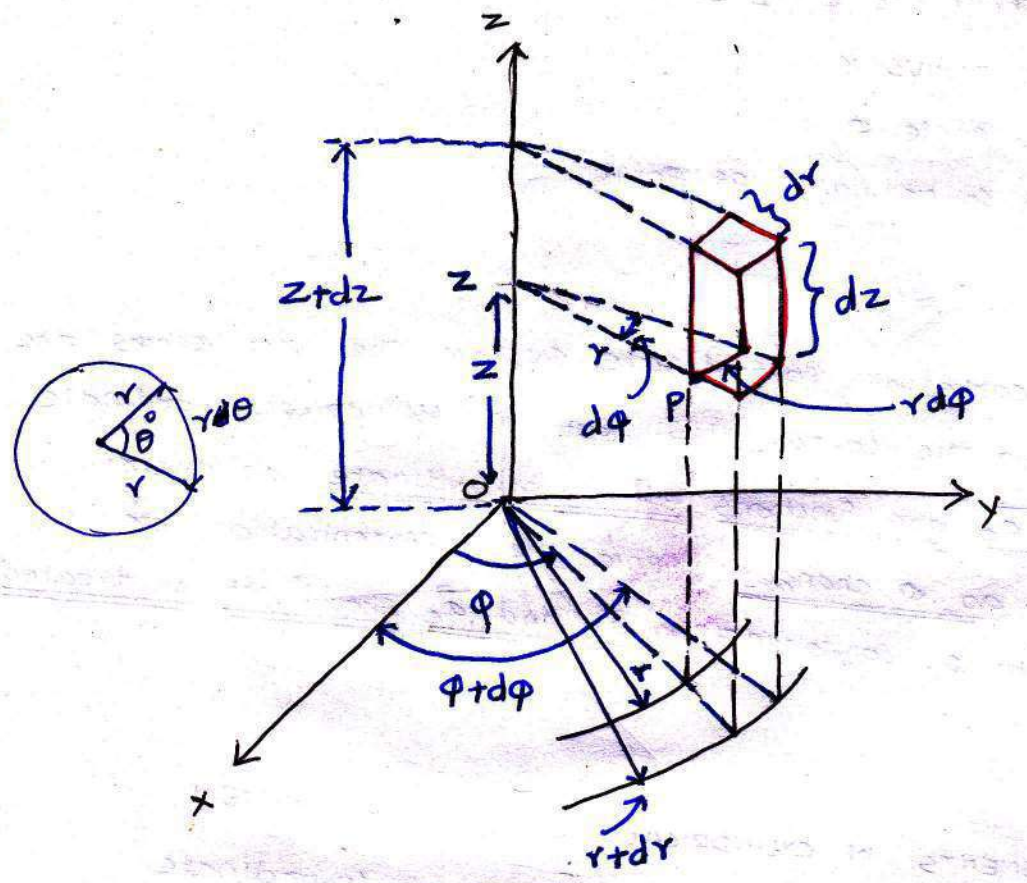
→ There are two radial planes at the angles ϕ and $\phi+d\phi$

→ Two Horizontal planes at the heights z and $z+dz$.

→ Differential lengths in r and z directions are dr and dz respectively.

→ In ϕ direction, $d\phi$ is the change in angle ϕ and is not the differential length.

→ Due to this change $d\phi$, there exists a differential arc length in ϕ direction. This differential length, due to $d\phi$, in ϕ direction is $r\,d\phi$ as shown in fig.



Hence the differential vector length in cylindrical co-ordinate system is given by,

$$\vec{dl} = dr\,\vec{a}_r + r\,d\phi\,\vec{a}_\phi + dz\,\vec{a}_z$$

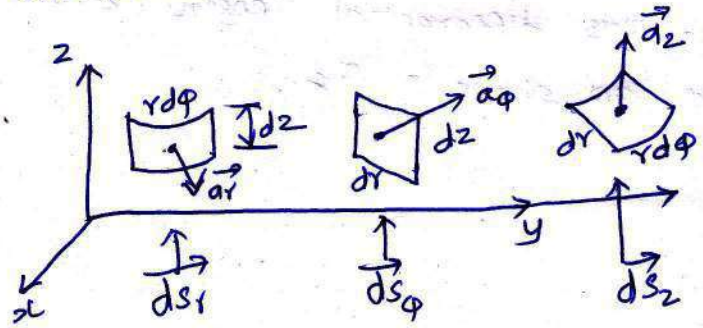
The magnitude of the differential length vector is given by,

$$|\vec{dl}| = \sqrt{(dr)^2 + (r\,d\phi)^2 + (dz)^2}$$

The volume of the differential element formed is given by,

$$dV = dr \times r\,d\phi \times dz$$

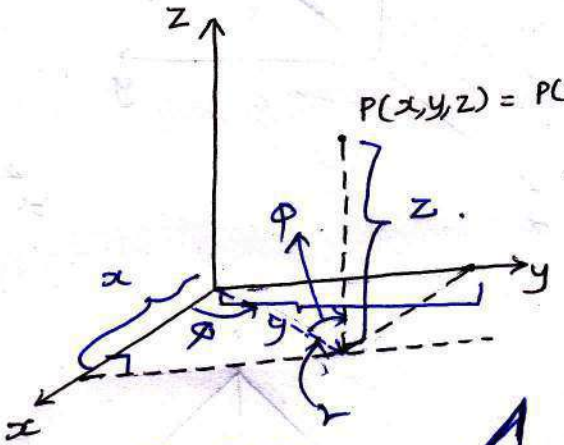
The differential surface areas in the three directions are shown in fig below.



$$\vec{ds_1} = r\,d\phi\,dz\,\vec{a}_r$$
$$\vec{ds_\phi} = dr\,dz\,\vec{a}_\phi$$
$$\vec{ds_2} = r\,d\phi\,dr\,\vec{a}_z$$

RELATIONSHIP B/W CARTESIAN & CYLINDRICAL SYSTEMS:

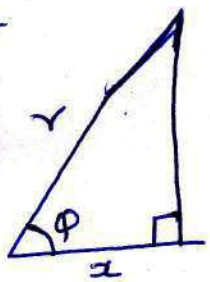
Consider a point 'P' whose cartesian co-ordinates are x, y and z while the cylindrical co-ordinates are r, ϕ and z as shown in fig below.



$$x = r\cos\phi$$
$$y = r\sin\phi$$
$$z = z$$

It can be seen that, r can be expressed interms of x and y as.

From the planes

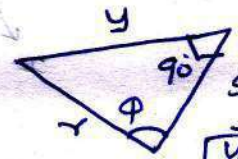


$\cos\phi = \frac{x}{r}$

$x = r\cos\phi$

$$r = \sqrt{x^2 + y^2}$$

While $\tan\phi = \frac{y}{x}$



$\sin\phi = \frac{y}{r}$

$y = r\sin\phi$

Thus the transformation from cartesian to cylindrical can be obtained from the equations.

$$r = \sqrt{x^2 + y^2}, \quad \phi = \tan^{-1}\frac{y}{x} \quad \text{and} \quad z = z$$

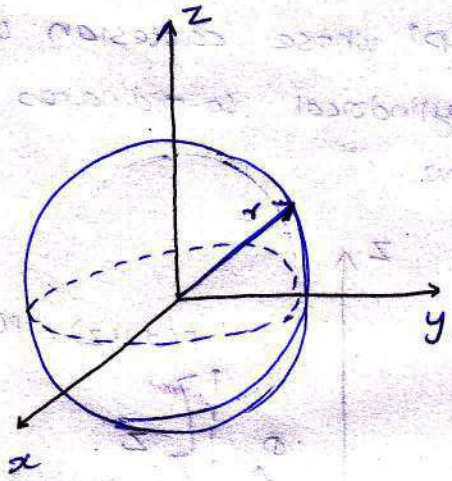
SPHERICAL CO-ORDINATE SYSTEM:

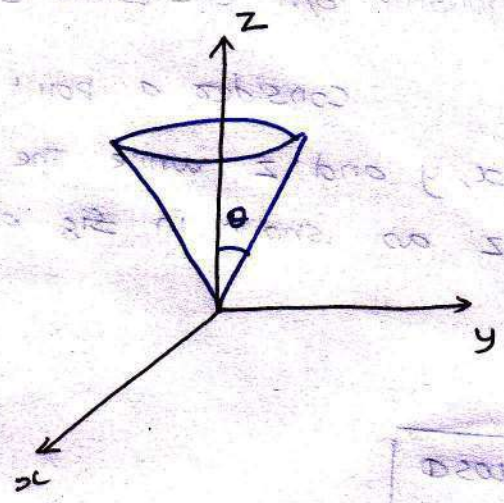
The surfaces which are used to define the spherical co-ordinate system on the three cartesian axes are

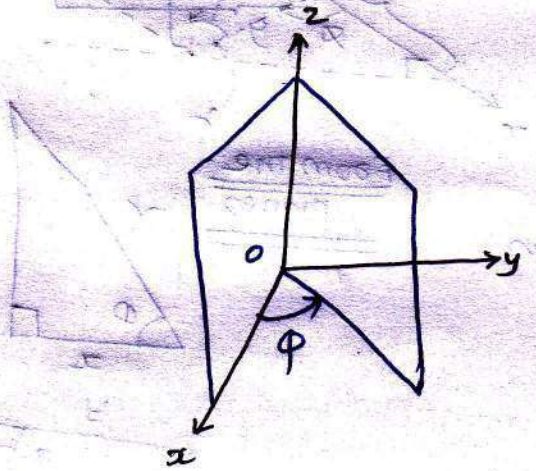
(i) Sphere of radius r, origin as the centre of the sphere

(ii) A right circular cone with its apex at the origin and its axis as z axis. Its half angle is θ. It rotates about z axis and θ varies from 0° to 180°

(iii) A half plane $\perp r$ to xy plane containing z axis, making an angle ϕ with the xz plane.





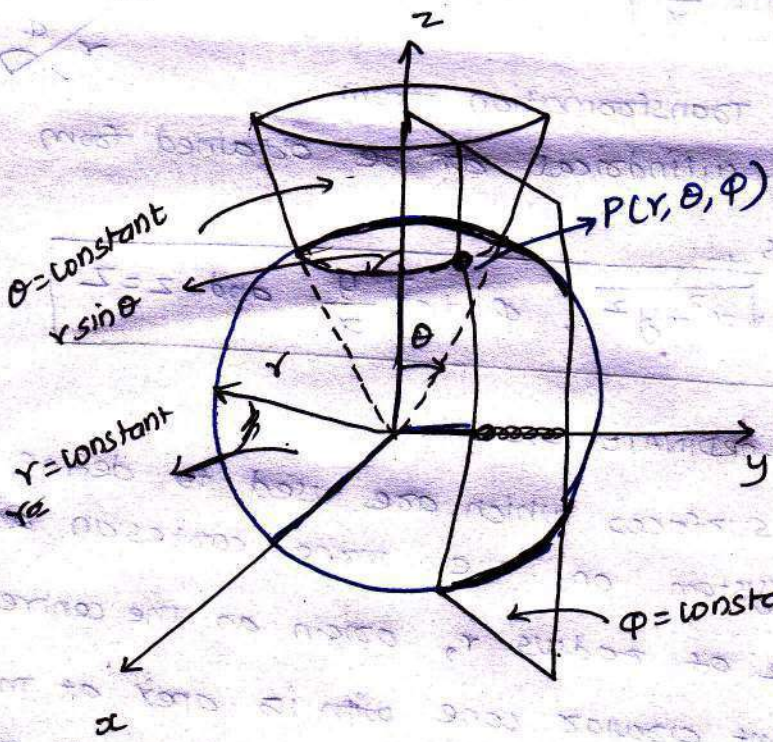


The range of the variables are

$0 \leq r \leq \infty$

$0 \leq \phi \leq 2\pi$

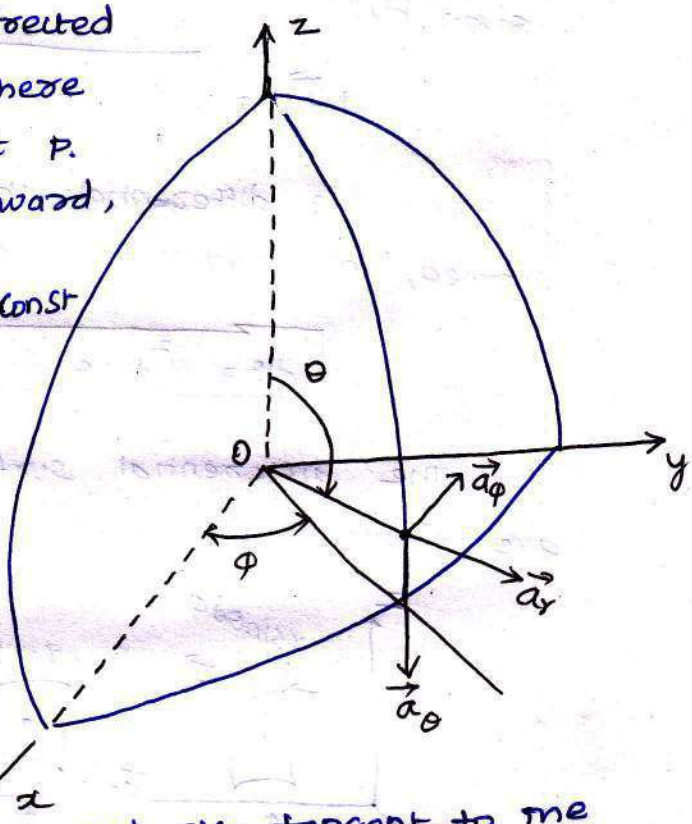
$0 \leq \theta \leq \pi$ as $\frac{1}{2}$ angle.



BASE VECTORS:

→ The unit vector $\vec{a}_r$ is directed from the centre of the sphere i.e. origin to the given point P. It is directed radially outward, normal to the sphere.

It lies in the cone θ = Const and plane φ = constant.



→ The unit vector $\vec{a}_\theta$ is tangent to the sphere and oriented in the direction of increasing θ. It is normal to the conical surface

→ The 3rd unit vector $\vec{a}_\phi$ is tangent to the sphere and also tangent to the conical surface. It is oriented in the direction of increasing φ. It is same as defined in the cylindrical co-ordinate system.

Here the vector of point 'P' can be represented as

$$\vec{P} = P_r \vec{a}_r + P_\theta \vec{a}_\theta + P_\phi \vec{a}_\phi$$

DIFFERENTIAL ELEMENTS IN SPHERICAL CO-ORDINATE SYSTEMS:

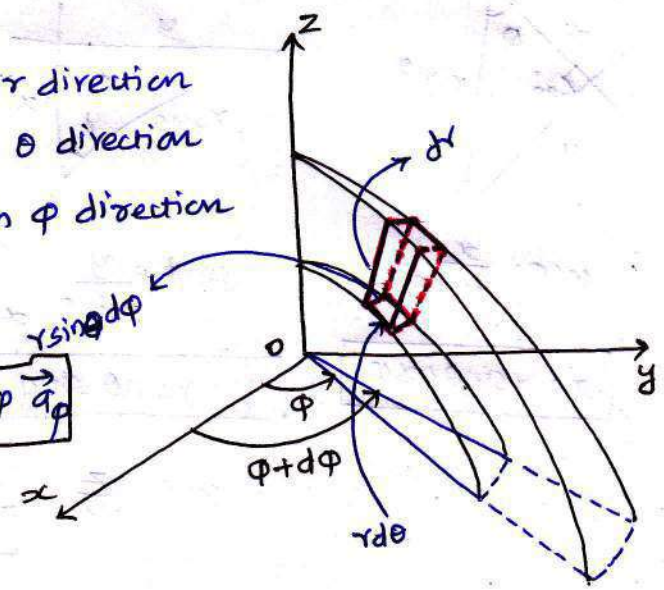
dr = Differential length in r direction

rdθ = Differential length in θ direction

rsinθdφ = Differential length in φ direction

∴ differential vector length

$$\vec{dl} = dr\vec{a}_r + rd\theta \vec{a}_\theta + r\sin\theta d\phi \vec{a}_\phi$$



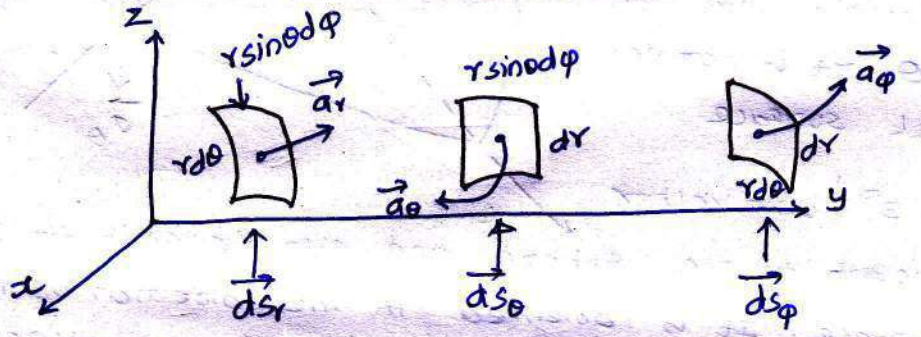
Hence the magnitude of the differential length vector is given by,

$$|\vec{dl}| = \sqrt{(dr)^2 + (r d\theta)^2 + (r \sin\theta\, d\phi)^2}$$

Hence the differential volume of the differential element formed, in spherical co-ordinate system is given by,

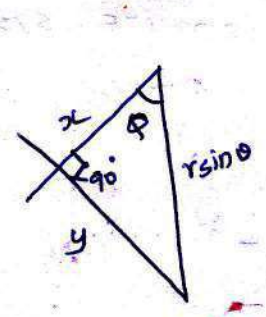
$$\boxed{dv = r^2 \sin\theta\, dr\, d\theta\, d\phi}$$

The differential surface areas in the three directions are shown in fig below.



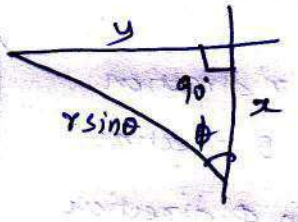
$$\vec{ds}_r = r^2 \sin\theta\, d\theta\, d\phi \qquad \vec{ds}_\theta = r \sin\theta\, dr\, d\phi \qquad \vec{ds}_\phi = r\, dr\, d\theta .$$

RELATIONSHIP B/W CARTESIAN & SPHERICAL SYSTEMS :-



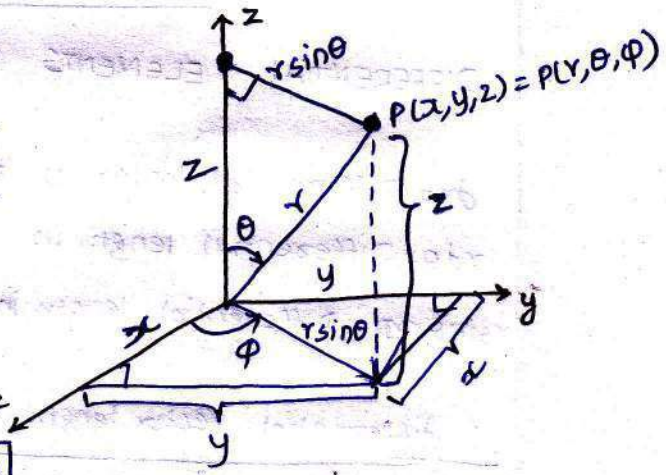
$$\cos\phi = \frac{x}{r\sin\theta}$$

$$\boxed{x = r\sin\theta\cos\phi}$$



$$\sin\phi = \frac{y}{r\sin\theta}$$

$$\boxed{y = r\sin\theta\sin\phi}$$



$$\cos\theta = \frac{z}{r}$$

$$\boxed{z = r\cos\theta}$$

Hence the transformation from spherical to cartesian can be obtained from equations,

$$x = r\sin\theta\cos\phi$$
$$y = r\sin\theta\sin\phi$$
$$z = r\cos\theta.$$

Now r can be expressed as,

$$x^2+y^2+z^2 = r^2\sin^2\theta\cos^2\phi + r^2\sin^2\theta\sin^2\phi + r^2\cos^2\phi$$
$$= r^2\sin^2\theta[\cos^2\phi+\sin^2\phi] + r^2\cos^2\theta$$
$$= r^2[\sin^2\theta+\cos^2\theta]$$
$$= r^2$$

$$\boxed{r = \sqrt{x^2+y^2+z^2}}$$

While $\tan\phi = \frac{y}{z}$ and $\cos\theta = \frac{z}{r}$.

As r is known, θ can be obtained.

Thus the Transformation from cartesian to spherical co-ordinates system can be obtained from the following equations.

$$r = \sqrt{x^2+y^2+z^2}, \quad \theta = \cos^{-1}\left[\frac{z}{\sqrt{x^2+y^2+z^2}}\right] \text{ and } \phi = \tan^{-1}\left(\frac{y}{x}\right)$$

TRANSFORMATION OF VECTORS:

TRANSFORMATION OF VECTORS FROM CARTESIAN TO CYLINDRICAL

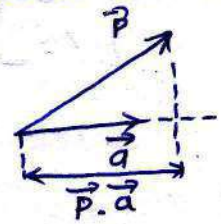
Consider a vector $\vec{A}$ in cartesian co-ordinate system as,

$$\vec{A} = A_x\vec{a_x} + A_y\vec{a_y} + A_z\vec{a_z}$$

While the same vector in cylindrical co-ordinate system can be represented as

$$\vec{A} = A_r\vec{a_r} + A_\phi\vec{a_\phi} + A_z\vec{a_z}.$$

From the dot product it is known that the component of vector in the direction of unit vector is it dot product with that unit vector.

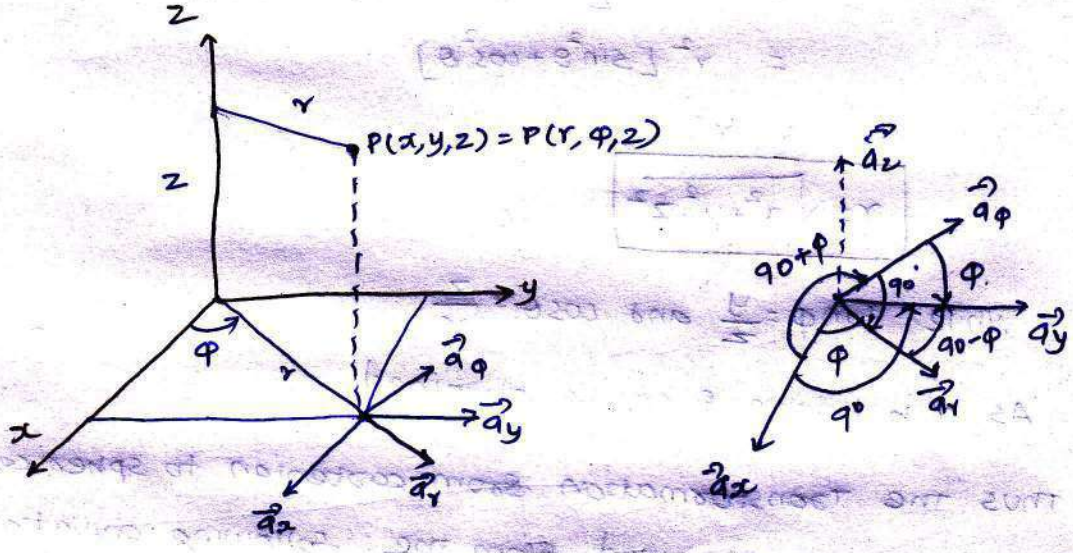


Hence the component of $\vec{A}$ in the direction of $\vec{a}_r$ is the dot product of $\vec{A}$ with $\vec{a}_r$. This component is nothing but A_r.

$$\therefore A_r = \vec{A} \cdot \vec{a}_r$$

$$= [A_x \vec{a}_x + A_y \vec{a}_y + A_z \vec{a}_z] \cdot \vec{a}_r$$

$$= A_x \vec{a}_x \cdot \vec{a}_r + A_y \vec{a}_y \cdot \vec{a}_r + A_z \vec{a}_z \cdot \vec{a}_r$$



$$\vec{a}_x \cdot \vec{a}_r = (1)(1)\cos\phi_{xr} = (1)(1)\cos\phi = \cos\phi.$$

$$\vec{a}_x \cdot \vec{a}_\phi = (1)(1)\cos(90+\phi) = -\sin\phi$$

$$\vec{a}_y \cdot \vec{a}_r = (1)(1)\cos(90-\phi) = \sin\phi$$

$$\vec{a}_y \cdot \vec{a}_\phi = (1)(1)\cos\phi = \cos\phi.$$

$$\vec{a}_z \cdot \vec{a}_r = \vec{a}_z \cdot \vec{a}_\phi = 0$$

$$\vec{a}_z \cdot \vec{a}_z = 1 \Rightarrow A_r = A_x \cos\phi + A_y \sin\phi.$$

In my

$$A_\phi = \vec{A} \cdot \vec{a}_\phi \Rightarrow \vec{A}_\phi = -A_x \sin\phi + A_y \cos\phi$$

$$\vec{A}_z = \vec{A} \cdot \vec{a}_z = A_z \Rightarrow A_z = A_z$$

$$\therefore \begin{bmatrix} A_r \\ A_\phi \\ A_z \end{bmatrix} = \begin{bmatrix} \cos\phi & \sin\phi & 0 \\ -\sin\phi & \cos\phi & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} A_x \\ A_y \\ A_z \end{bmatrix}.$$

TRANSFORMATION OF VECTORS FROM CYLINDRICAL TO CARTESIAN

Now it is necessary to find the transformation from cylindrical to cartesian. Hence we assume $\vec{A}$ is known in cylindrical system.

Thus component of $\vec{A}$ in a_x direction is given by

$$\vec{A}_x = \vec{A} \cdot \vec{a}_x = [A_r \vec{a}_r + A_\phi \vec{a}_\phi + A_z \vec{a}_z] \cdot \vec{a}_x$$

$$= A_r \vec{a}_r \cdot \vec{a}_x + A_\phi \vec{a}_\phi \cdot \vec{a}_x + A_z \vec{a}_z \cdot \vec{a}_x$$

As dot product is commutative

$$\vec{a}_r \cdot \vec{a}_x = \vec{a}_x \cdot \vec{a}_r = \cos\phi$$

Hence

$$\vec{A}_x = A_r \cos\phi + (-\sin\phi) A_\phi$$

$$\vec{A}_x = A_r \cos\phi - A_\phi \sin\phi$$

III^ly

$$\vec{A}_y = \vec{A} \cdot \vec{a}_y = \sin\phi A_r + \cos\phi A_\phi$$

$$A_z = A_z$$

$$\therefore \begin{bmatrix} A_x \\ A_y \\ A_z \end{bmatrix} = \begin{bmatrix} \cos\phi & -\sin\phi & 0 \\ \sin\phi & \cos\phi & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} A_r \\ A_\phi \\ A_z \end{bmatrix}$$

TRANSFORMATION OF VECTORS FROM CARTESIAN TO SPHERICAL

Let

$$\vec{A} = A_x \vec{a}_x + A_y \vec{a}_y + A_z \vec{a}_z$$

$$A_r = \vec{A} \cdot \vec{a}_r = [A_x \vec{a}_x + A_y \vec{a}_y + A_z \vec{a}_z] \cdot \vec{a}_r$$

$$A_r = A_x \vec{a}_x \cdot \vec{a}_r + A_y \vec{a}_y \cdot \vec{a}_r + A_z \vec{a}_z \cdot \vec{a}_r$$

$$A_\theta = \vec{A} \cdot \vec{a}_\theta = [A_x \vec{a}_x + A_y \vec{a}_y + A_z \vec{a}_z] \cdot \vec{a}_\theta$$

$$A_\theta = A_x \vec{a}_x \cdot \vec{a}_\theta + A_y \vec{a}_y \cdot \vec{a}_\theta + A_z \vec{a}_z \cdot \vec{a}_\theta$$

$$A_\phi = \vec{A} \cdot \vec{a}_\phi = [A_x \vec{a}_x + A_y \vec{a}_y + A_z \vec{a}_z] \cdot \vec{a}_\phi$$

$$= A_x \vec{a}_x \cdot \vec{a}_\phi + A_y \vec{a}_y \cdot \vec{a}_\phi + A_z \vec{a}_z \cdot \vec{a}_\phi$$

The dot product of spherical unit vectors are given below.

·	$\vec{a}_r$	$\vec{a}_\theta$	$\vec{a}_\phi$
$\vec{a}_x$	$\sin\theta\cos\phi$	$\cos\theta\cos\phi$	$-\sin\phi$
$\vec{a}_y$	$\sin\theta\sin\phi$	$\cos\theta\sin\phi$	$\cos\phi$
$\vec{a}_z$	$\cos\theta$	$-\sin\theta$	0

$$\therefore \begin{bmatrix} A_r \\ A_\theta \\ A_\phi \end{bmatrix} = \begin{bmatrix} \sin\theta\cos\phi & \sin\theta\sin\phi & \cos\theta \\ \cos\theta\cos\phi & \cos\theta\sin\phi & -\sin\theta \\ -\sin\phi & \cos\phi & 0 \end{bmatrix} \begin{bmatrix} A_x \\ A_y \\ A_z \end{bmatrix}$$

TRANSFORMATION OF VECTORS FROM SPHERICAL TO CARTESIAN

$$\vec{A} = A_r \vec{a}_r + A_\theta \vec{a}_\theta + A_\phi \vec{a}_\phi$$

$$A_x = \vec{A} \cdot \vec{a}_x = A_r \vec{a}_r \cdot \vec{a}_x + A_\theta \vec{a}_\theta \cdot \vec{a}_x + A_\phi \vec{a}_\phi \cdot \vec{a}_x$$

$$A_y = \vec{A} \cdot \vec{a}_y = A_r \vec{a}_r \cdot \vec{a}_y + A_\theta \vec{a}_\theta \cdot \vec{a}_y + A_\phi \vec{a}_\phi \cdot \vec{a}_y$$

$$A_z = \vec{A} \cdot \vec{a}_z = A_r \vec{a}_r \cdot \vec{a}_z + A_\theta \vec{a}_\theta \cdot \vec{a}_z + A_\phi \vec{a}_\phi \cdot \vec{a}_z$$

$$\begin{bmatrix} A_x \\ A_y \\ A_z \end{bmatrix} = \begin{bmatrix} \sin\theta\cos\phi & \cos\theta\cos\phi & -\sin\phi \\ \sin\theta\sin\phi & \cos\theta\sin\phi & \cos\phi \\ \cos\theta & -\sin\phi & 0 \end{bmatrix} \begin{bmatrix} A_r \\ A_\theta \\ A_\phi \end{bmatrix}$$

DISTANCE OF ALL CO-ORDINATE SYSTEMS

$$d = \sqrt{(x_2-x_1)^2 + (y_2-y_1)^2 + (z_2-z_1)^2} \quad - \text{ cartesian}$$

$$d = \sqrt{r_2^2 + r_1^2 - 2r_1r_2\cos(\phi_2-\phi_1) + (z_2-z_1)^2} \quad - \text{ cylindrical}$$

$$d = \sqrt{r_2^2 + r_1^2 - 2r_1r_2\cos\theta_2\cos\theta_1 - 2r_1r_2\sin\theta_2\sin\theta_1\cos(\phi_2-\phi_1)}$$

- spherical.

TRANSFORMATION OF VECTORS FROM SPHERICAL TO CYLINDRICAL

Let

$$\vec{A} = A_r \vec{a}_r + A_\theta \vec{a}_\theta + A_\phi \vec{a}_\phi$$

$$A_\rho = A_r \vec{a}_r \cdot \vec{a}_\rho + A_\theta \vec{a}_\theta \cdot \vec{a}_\rho + A_\phi \vec{a}_\phi \cdot \vec{a}_\rho$$

$$A_\phi = A_r \vec{a}_r \cdot \vec{a}_\phi + A_\theta \vec{a}_\theta \cdot \vec{a}_\phi + A_\phi \vec{a}_\phi \cdot \vec{a}_\phi$$

$$A_z = A_r \vec{a}_r \cdot \vec{a}_z + A_\theta \vec{a}_\theta \cdot \vec{a}_z + A_\phi \vec{a}_\phi \cdot \vec{a}_z$$

$\vec{a}_r \cdot \vec{a}_\rho = \sin\theta$ $\quad \vec{a}_\theta \cdot \vec{a}_\rho = \cos\theta$ $\quad \vec{a}_\phi \cdot \vec{a}_\rho = 0$

$\vec{a}_r \cdot \vec{a}_\phi = 0$ $\quad \vec{a}_\theta \cdot \vec{a}_\phi = 0$ $\quad \vec{a}_\phi \cdot \vec{a}_\phi = 1$

$\vec{a}_r \cdot \vec{a}_z = \cos\theta$ $\quad \vec{a}_\theta \cdot \vec{a}_z = -\sin\theta$ $\quad \vec{a}_\phi \cdot \vec{a}_z = 0$.

$$\begin{bmatrix} A_\rho \\ A_\phi \\ A_z \end{bmatrix} = \begin{bmatrix} \sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \\ \cos\theta & -\sin\theta & 0 \end{bmatrix} \begin{bmatrix} A_r \\ A_\theta \\ A_\phi \end{bmatrix}$$

TRANSFORMATION OF VECTORS FRON CYLINDRICAL TO SPHERICAL

Let

$$\vec{A} = A_\rho \vec{a}_\rho + A_\phi \vec{a}_\phi + A_z \vec{a}_z$$

$$A_r = A_\rho \vec{a}_\rho \cdot \vec{a}_r + A_\phi \vec{a}_\phi \cdot \vec{a}_r + A_z \vec{a}_z \cdot \vec{a}_r$$

$$A_\theta = A_\rho \vec{a}_\rho \cdot \vec{a}_\theta + A_\phi \vec{a}_\phi \cdot \vec{a}_\theta + A_z \vec{a}_z \cdot \vec{a}_\theta$$

$$A_\phi = A_\rho \vec{a}_\rho \cdot \vec{a}_\phi + A_\phi \vec{a}_\phi \cdot \vec{a}_\phi + A_z \vec{a}_z \cdot \vec{a}_\phi$$

$$\begin{bmatrix} A_r \\ A_\theta \\ A_\phi \end{bmatrix} = \begin{bmatrix} \sin\theta & 0 & \cos\theta \\ \cos\theta & 0 & -\sin\theta \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} A_\rho \\ A_\phi \\ A_z \end{bmatrix}$$

TYPES OF INTEGRAL RELATED TO ELECTROMAGNETIC THEORY

In electromagnetic theory a charge can exist in Point form, line form, surface form or volume form.

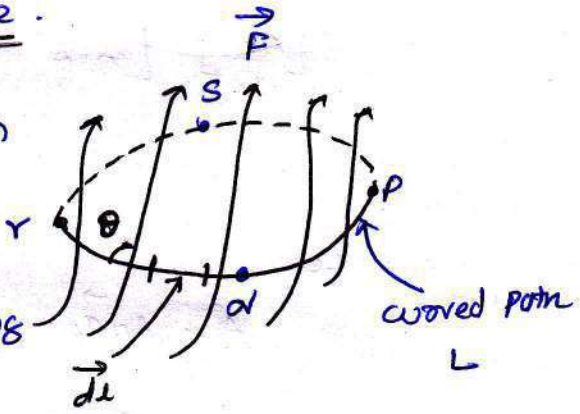
Hence for charge distribution analysis, the following types of integrals are required.

1. Line integral
2. surface integral
3. Volume integral.

LINE INTEGRAL

- A line can exist as a straight line or it can be distance travelled along a curve
- From mathematical Point of view, a line is a curved path in a space.

Consider a vector field $\vec{F}$ shown in fig. The curved path shown in the field is P-Y. This is called Path of integration and corresponding integral can be defined as



$$\int_L \vec{F}.\vec{dl} = \int_P^Y |F|\, dl \cos\theta \cdot \text{[using dot product definition]}.$$

where

$dl \rightarrow$ Elementary length.

This is called line integral of $\vec{F}$ around the curved path L.

The curved path can be of two types.

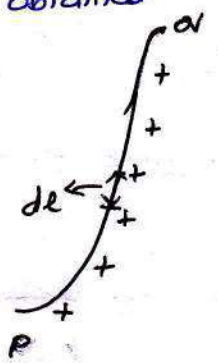
(i) open path as P-Y shown in fig

(ii) closed path as P-Q-Y-S-P.

The closed path is also called contour. The corresponding integral is called contour integral, closed integral (or) circular integral, and mathematicalled defined as.

$$\oint_L \vec{F}.\vec{dl} = \text{circular integral.}$$

If there exists a charge along a ~~straight~~ line as shown in figure, then the total charge is obtained by calculating a line integral.

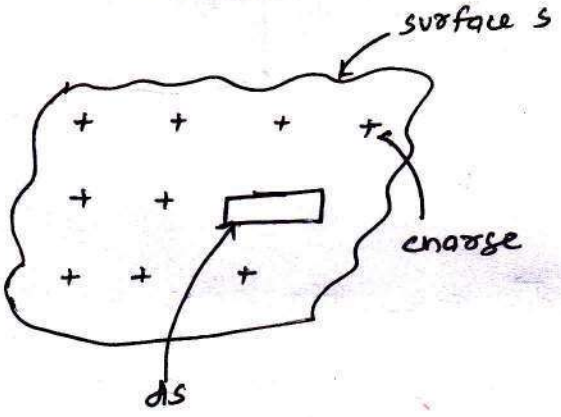


$$Q = \int_L \rho_L \cdot dl$$

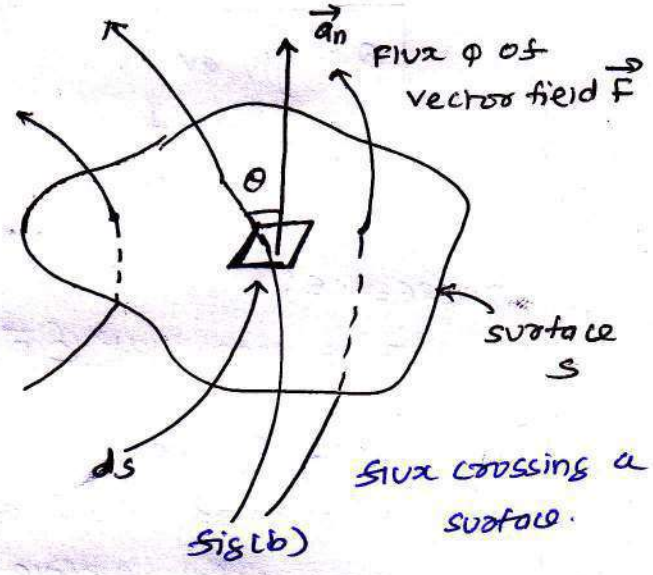
ρ_L = Line charge density (or)
charge per unit length (C/m).

SURFACE INTEGRAL:

In electromagnetic theory a charge may exist in a distributed form. It may be spreaded over a surface as shown in figure(a) below.



fig(a)



fig(b)

flux crossing a surface.

similarly a flux φ may pass through a surface as shown in fig(b). while doing analysis of such cases an integral is required called SURFACE INTEGRAL, to be carried out over a surface related to a vector field.

For a charge distribution shown in fig(a), we can write total charge existing on the surface as

$$Q = \int_S \rho_s \, ds \cdot \quad \rho_s \rightarrow \text{surface charge density in } C/m^2$$

$ds \rightarrow$ Elementary surface area.

Similarly from fig(b), the total flux crossing the surface S can be expressed as

$$\varphi = \int_S \vec{F} \cdot \vec{ds} = \int_S |\vec{F}| \, ds \cos\theta$$

If the surface is closed, then it defines a volume and corresponding surface integral is given by,

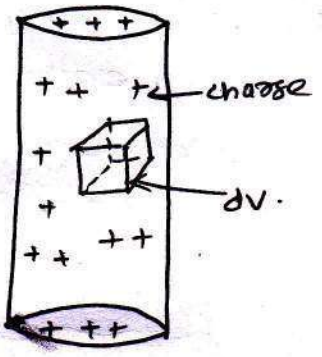
$$\Phi = \oint_S \vec{F} \cdot \vec{ds} .$$

VOLUME INTEGRAL

If the charge distribution exists in a three dimensional volume form as shown in figure below, then a volume integral is required to calculate the total charge.

Thus if ρ_v is the volume charge density over volume V. then the volume integral is defined as

$$Q = \int_V \rho_v \, dv .$$



dv = Elementary volume.

DIVERGENCE:

It is seen that $\oint_S \vec{F} \cdot \vec{ds}$ gives the flux flowing across the surface S. Then mathematically divergence is defined as the net outward flow of the flux per unit volume over a closed incremental surface. It is denoted as div $\vec{F}$ and given by

$$\text{div } \vec{F} = \lim_{\Delta v \to 0} \frac{\oint \vec{F} \cdot \vec{ds}}{\Delta v} = \text{Divergence of } \vec{F}.$$

symbolically it is denoted as

$$\nabla \cdot \vec{F} = \text{Divergence of } \vec{F}$$

Where ∇ = Vector operator $= \frac{\partial}{\partial x}\vec{a}_x + \frac{\partial}{\partial y}\vec{a}_y + \frac{\partial}{\partial z}\vec{a}_z$

But $\vec{F} = F_x \vec{a}_x + F_y \vec{a}_y + F_z \vec{a}_z$

$$\therefore \boxed{\nabla \cdot \vec{F} = \frac{\partial F_x}{\partial x} + \frac{\partial F_y}{\partial y} + \frac{\partial F_z}{\partial z}} \rightarrow \text{In cartesian form}$$

III^ry Divergence in other co-ordinates.

$$\nabla.\vec{F} = \frac{1}{r}\frac{\partial}{\partial r}(rF_r) + \frac{1}{r}\frac{\partial F_\phi}{\partial \phi} + \frac{\partial F_z}{\partial z} \quad \text{cylindrical}$$

$$\nabla.\vec{F} = \frac{1}{r^2}\cdot\frac{\partial}{\partial r}(r^2F_r) + \frac{1}{r\sin\theta}\frac{\partial}{\partial \theta}(\sin\theta F_\theta) + \frac{1}{r\sin\theta}\frac{\partial F_\phi}{\partial \phi} \quad \text{spherical.}$$

The vector field having its divergence zero is called solenoidal field

$$\boxed{\nabla.\vec{A} = 0 \text{ for } \vec{A} \text{ to be solenoidal}}$$

GRADIENT OF A SCALAR:-

Consider that in space let W be the uniave function of x, y and z co-ordinates. in the cartesian system. This is the scalar function and denoted as $W(x,y,z)$. Consider a vector operator in cartesian system denoted as ∇ (called del). It is defined as.

$$\nabla(\text{del}) = \frac{\partial}{\partial x}\vec{a_x} + \frac{\partial}{\partial y}\vec{a_y} + \frac{\partial}{\partial z}\vec{a_z}$$

The operation of the vector operator del(∇) on a scalar function is called gradient of a scalar.

$$\text{Grad } W = \nabla W = \left(\frac{\partial}{\partial x}\vec{a_x} + \frac{\partial}{\partial y}\vec{a_y} + \frac{\partial}{\partial z}\vec{a_z}\right)W$$

$$\boxed{\nabla W = \frac{\partial W}{\partial x}\vec{a_x} + \frac{\partial W}{\partial y}\vec{a_y} + \frac{\partial W}{\partial z}\vec{a_z}} \quad \text{cartesian.}$$

In cylindrical co-ordinates.

$$\nabla W = \frac{\partial W}{\partial r}\vec{a_r} + \frac{1}{r}\frac{\partial W}{\partial \phi}\vec{a_\phi} + \frac{\partial W}{\partial z}\vec{a_z}$$

spherical co-ordinates

$$\nabla W = \frac{\partial W}{\partial r}\vec{a_r} + \frac{1}{r}\frac{\partial W}{\partial \theta}\vec{a_\theta} + \frac{1}{r\sin\theta}\frac{\partial W}{\partial \phi}\vec{a_\phi}$$

CURL OF A VECTOR:

$$\nabla \times \vec{F} = \text{curl of } \vec{F}$$

curl indicates the rotational property of vector field. If curl of vector is zero, the vector field is irrotational.

$$\nabla \times \vec{F} = \left[\frac{\partial F_z}{\partial y} - \frac{\partial F_y}{\partial z}\right]\vec{a}_x + \left[\frac{\partial F_x}{\partial z} - \frac{\partial F_z}{\partial x}\right]\vec{a}_y + \left[\frac{\partial F_y}{\partial x} - \frac{\partial F_x}{\partial y}\right]\vec{a}_z$$

$$\nabla \times \vec{F} = \begin{bmatrix} \vec{a}_x & \vec{a}_y & \vec{a}_z \\ \frac{\partial}{\partial x} & \frac{\partial}{\partial y} & \frac{\partial}{\partial z} \\ F_x & F_y & F_z \end{bmatrix}$$ CARTESIAN

$$\nabla \times \vec{F} = \begin{bmatrix} \vec{a}_r & r\vec{a}_\phi & \vec{a}_z \\ \frac{\partial}{\partial r} & \frac{\partial}{\partial \phi} & \frac{\partial}{\partial z} \\ F_r & F_\phi & F_z \end{bmatrix}$$ CYLINDRICAL

$$\nabla \times \vec{F} = \begin{bmatrix} \vec{a}_r & r\vec{a}_\theta & r\sin\theta\,\vec{a}_\phi \\ \frac{\partial}{\partial r} & \frac{\partial}{\partial \theta} & \frac{\partial}{\partial \phi} \\ F_r & rF_\theta & r\sin\theta F_\phi \end{bmatrix}$$ SPHERICAL

ELECTROSTATICS:

→ Electrostatics is a science related to the electric charges which are static i.e are at rest.

→ An Electric charge has an effect in a region or a space around it. This region is called an electric field of that charge.

→ such an Electric field Produced due to stationary electric charge doesnot vary with time. It is time invarient and called static electric field.

COULOMB'S LAW:

→ Study of electrostatics started from foench army engineer, colonel charles Coulomb.

→ The experiments are related to the force exerted b/w the two point charges, which are placed near each other.

→ The force exerted is due to the electric fields Produced by the point charges.

POINT CHARGE:

- A Point charge means that the electric charge which is spreaded on a surface or space whose geometrical dimensions are very very small compared to the other dimensions, in which the effect of its electric field is to be studied. Thus a point charge has a location but not the dimensions.

- A charge can be +ve or -ve
- A charge is actually the defficiency or excess of electrons in the atoms of a particle.
- An electron Possesses a -ve charge. so the deficiency of an electron produces +ve charge while excess of an electron Produces -ve charge.

- The charge is measured in COULOMBS (C).

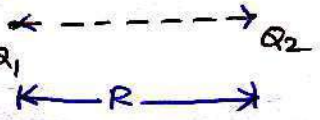
~~Some scientists measure charge~~

STATEMENT OF COULOMB'S LAW:

The coulomb's law states that force b/w the two point charges Q_1 and Q_2

1. Acts along the line joining the two point charges.
2. Is directly proportional to the product (Q_1, Q_2) of the two charges
3. Is inversely proportional to the square of distance b/w them.

- Consider two point charges Q_1 & Q_2 seperated by distance R.



→ The charge Q_1 exerts a force on Q_2 while Q_2 exerts a force on Q_1.

→ The force acts along the line joining Q_1 and Q_2

→ The force exerted b/w them is repulsive if the charges are of same polarity, while it is attractive if charges are of different polarity.

Force F b/w two charges is expressed as

$$F \propto \frac{Q_1 Q_2}{R^2}$$

The coulomb's law also states that this force depends on the medium in which the point charge are located. This effect is included as constant of proportionality

$$\therefore F = K \frac{Q_1 Q_2}{R^2}$$

$K = \frac{1}{4\pi\epsilon}$ $\epsilon \rightarrow$ Permittivity of the medium in which charges are located.

Units of ϵ Farads/metres (F/m).

In general ϵ is expressed as

$$\epsilon = \epsilon_0 \epsilon_r$$

$\epsilon_0 \rightarrow$ Permittivity of free space or vaccum.

$\epsilon_r \rightarrow$ Relative Permittivity (or) dielectric constant of the medium w.r.to free space.

$\epsilon \rightarrow$ Absolute permittivity

For the free space or vaccum, $\epsilon_r = 1$

$\therefore \epsilon = \epsilon_0$

$$\therefore F = \frac{1}{4\pi\epsilon_0} \frac{Q_1 Q_2}{R^2}$$

$$\epsilon_0 = \frac{1}{36\pi} \times 10^{-9} = 8.854 \times 10^{-12} \text{ F/m.}$$

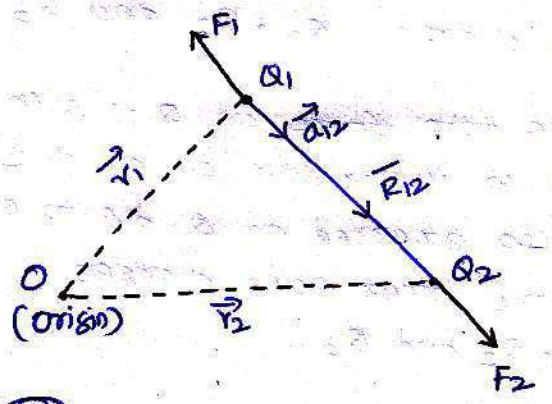
$$k = \frac{1}{4\pi\epsilon_0} = \frac{1}{4\pi \times 8.854 \times 10^{-12}} = 8.98 \times 10^{9} \simeq 9 \times 10^{9} \text{ m/F.}$$

$$\boxed{F = \frac{Q_1 Q_2}{4\pi\epsilon_0 R^2}}$$ ← This is the force b/w two point charges located in free space or vaccum.

VECTOR FORM OF COULOMB'S LAW:

The force exerted b/w the two point charges has a fixed direction which is a straight line joining the two charges. Hence the force exerted b/w the two charges can be expressed in a vector form.

Consider two point charges Q_1 and Q_2 located at the points having position vectors $\vec{r}_1$ and $\vec{r}_2$ as shown in fig below



Then the force exerted by Q_1 on Q_2 acts along the direction $\vec{R}_{12}$ where $\vec{a}_{12}$ is unit vector along $\vec{R}_{12}$. Hence the force in the vector form can be expressed as.

$$\vec{F}_2 = \frac{Q_1 Q_2}{4\pi\epsilon_0 R_{12}^2} \vec{a}_{12}$$

$\vec{a}_{12}$ = unit vector along $\vec{R}_{12}$ = $\frac{\text{Vector}}{\text{Magnitude of vector}}$

$$\vec{a}_{12} = \frac{\vec{R}_{12}}{|\vec{R}_{12}|} = \frac{\vec{r}_2 - \vec{r}_1}{|\vec{R}_{12}|} = \frac{\vec{r}_2 - \vec{r}_1}{|\vec{r}_2 - \vec{r}_1|}.$$

where $|\vec{R}_{12}|$ is the distance b/w the two charges.

Illly the force f_1 is exerted on Q_1 due to Q_2. It can be expressed as

$$\vec{F}_1 = \frac{Q_1 Q_2}{4\pi\epsilon_0^2 R_{21}^2} \vec{a}_{21}$$

$$\vec{a}_{21} = \frac{\vec{r}_1 - \vec{r}_2}{|\vec{r}_1 - \vec{r}_2|} \quad \text{But} \quad \vec{r}_1 - \vec{r}_2 = -[\vec{r}_2 - \vec{r}_1]$$

$$\vec{a}_{21} = -\vec{a}_{12}$$

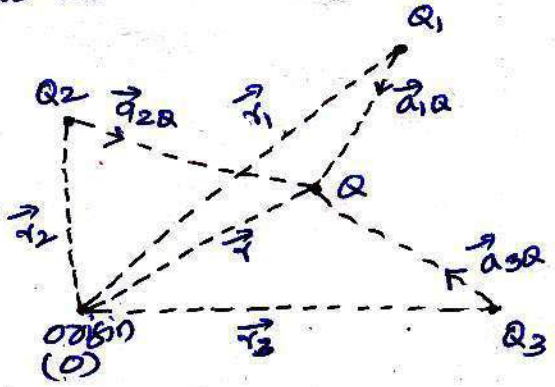
$$\therefore \vec{F}_1 = -\vec{F}_2$$

PRINCIPLE OF SUPERPOSITION:

If there are more than two point charges, then each will exert on the other, then the net force on any charge can be obtained by the principle of super position.

Consider a point charge Q surrounded by three other point charges Q_1, Q_2 and Q_3 as shown in figure below.

The total force on Q in such a case is vector sum of all the forces exerted on Q due to each of the other point charges Q_1, Q_2 and Q_3.



consider force exerted on Q due to Q_1. At this time, according to principle of superposition effects of Q_2 & Q_3 are to be suppressed.

$$\vec{F}_{Q1Q} = \frac{Q_1 Q}{4\pi\epsilon_0 R_{1Q}^2} \vec{a}_{1Q} \quad \text{where} \quad \vec{a}_{1Q} = \frac{\vec{r} - \vec{r}_1}{|\vec{r} - \vec{r}_1|}$$

Any force exerted due to Q_2 on Q is

$$\vec{F}_{Q2Q} = \frac{Q_2 Q}{4\pi\epsilon_0 R_{2Q}^2} \vec{a}_{2Q} \quad \text{where} \quad \vec{a}_{2Q} = \frac{\vec{r} - \vec{r}_2}{|\vec{r} - \vec{r}_2|}$$

and force exerted due to Q_3 on Q is

$$\vec{F}_{Q3Q} = \frac{Q_3 Q}{4\pi\epsilon_0 R_{3Q}^2} \vec{a}_{3Q} \quad \text{where} \quad \vec{a}_{3Q} = \frac{\vec{r} - \vec{r}_3}{|\vec{r} - \vec{r}_3|}.$$

Hence the total force on Q is

$$\vec{F}_Q = \vec{F}_{Q1Q} + \vec{F}_{Q2Q} + \vec{F}_{Q3Q}$$

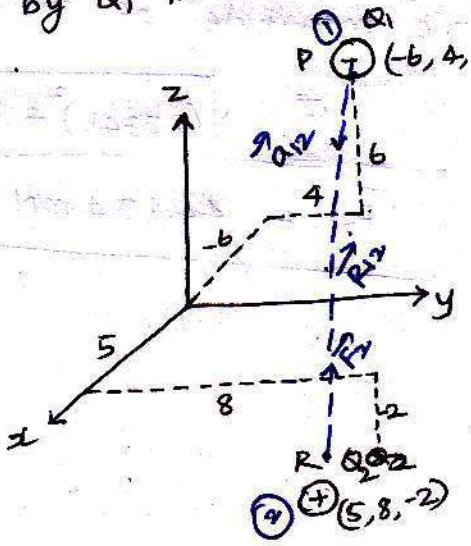
In general if there are n other charges then force exerted on Q due to all other charges is,

$$\vec{F}_Q = \vec{F}_{Q1Q} + \vec{F}_{Q2Q} + \cdots + \vec{F}_{QnQ}$$

$$\boxed{\vec{F}_Q = \frac{Q}{4\pi\epsilon_0} \sum_{i=1}^{n} \frac{Q_i}{R_{iQ}^2} \frac{\vec{r} - \vec{r}_i}{|\vec{r} - \vec{r}_i|}}$$

Problems:

A charge $Q_1 = -20\mu C$ is located at P(-6, 4, 6) and a charge $Q_2 = 50\mu C$ is located at R(5, 8, -2) in a free space. Find the force exerted on Q_2 by Q_1 in vector form. The distance given are in meters.



From the co-ordinates of P and R, the respective position vectors are

$$\vec{P} = -6\vec{a}_x + 4\vec{a}_y + 6\vec{a}_z \quad (Q_1)$$

and $$\vec{R} = 5\vec{a}_x + 8\vec{a}_y - 2\vec{a}_z \quad (Q_2)$$

The force on Q_2 is given by,

$$\vec{F}_{Q_2} = \frac{Q_1 Q_2}{4\pi\epsilon_0 R_{12}^2}\vec{a}_{12}$$

$$\vec{R}_{12} = \vec{R}_{PR} = \vec{R} - \vec{P} = 11\vec{a}_x + 4\vec{a}_y - 8\vec{a}_z$$

$$|\vec{R}_{12}| = \sqrt{11^2 + 4^2 + 8^2} = 14.1774$$

$$\therefore \vec{a}_{12} = \frac{\vec{R}_{12}}{|\vec{R}_{12}|} = \frac{11\vec{a}_x + 4\vec{a}_y - 8\vec{a}_z}{14.1774}$$

$$\boxed{\vec{a}_{12} = 0.7758\vec{a}_x + 0.2821\vec{a}_y - 0.5642\vec{a}_z}$$

$$\therefore \vec{F}_2 = \frac{-20\times10^{-6}\times50\times10^{-6}}{4\pi\times8.854\times10^{-12}(14.1774)^2}[\vec{a}_{12}]$$

$$= -0.0447[0.7758\vec{a}_x + 0.2821\vec{a}_y - 0.5642\vec{a}_z]$$

$$\boxed{\vec{F}_2 = -0.0346\vec{a}_x - 0.01261\vec{a}_y + 0.02522\vec{a}_z \text{ N}}$$

This is the required force exerted on Q_2 by Q_1.

The magnitude of the force is,

$$|\vec{F}_2| = \sqrt{(0.0346)^2 + (0.01261)^2 + (-0.02522)^2}$$

$$\boxed{|\vec{F}_2| = 44.634\text{ mN}}$$

Problem 2:

Four point charges each of 10nC are placed in free space at the points (1,0,0), (-1,0,0), (0,1,0) and (0,-1,0)m respectively. Determine the force on a point charge of 30nC located at a point (0,0,1)m.

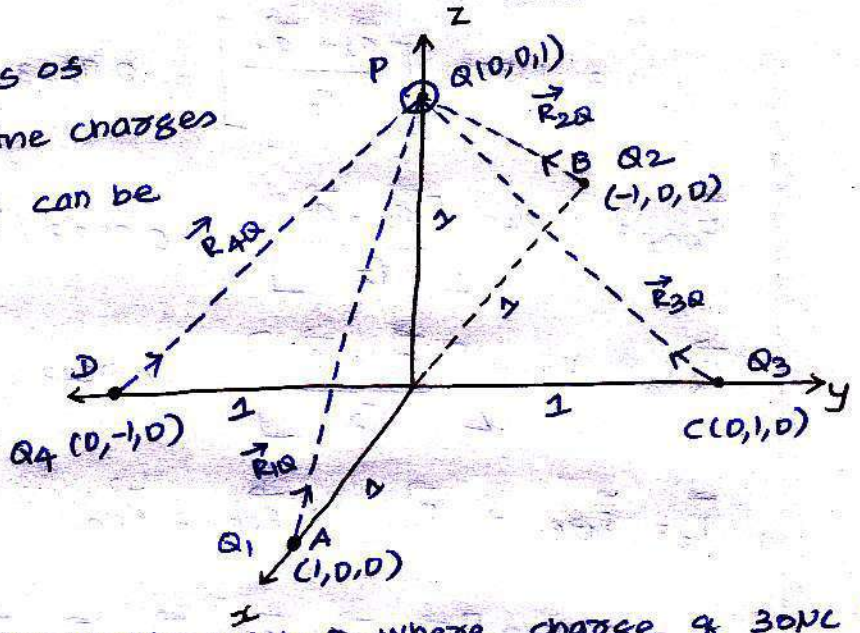
The position vectors of 4 points at which the charges Q_1 to Q_4 are located can be obtained as,

$\vec{A} = \vec{a}_x$

$B = -\vec{a}_x$

$C = \vec{a}_y$

$D = -\vec{a}_y$



While the position vector of point P where charge of 30nC is situated is

$$\vec{P} = \vec{a}_z$$

Consider force on Q due to Q_1 is

$$\vec{F}_{QQ_1} = \frac{Q Q_1}{4\pi\epsilon_0 R_{1Q}^2} \vec{a}_{1Q}$$

$$\vec{R}_{1Q} = \vec{R}_{AP} = \vec{P} - \vec{A} = \vec{a}_z - (\vec{a}_x) = \vec{a}_z - \vec{a}_x$$

$$|\vec{R}_{1Q}| = \sqrt{1^2+1^2} = \sqrt{2}$$

$$\therefore \vec{F}_{QQ_1} = \frac{10\times10^{-6} \times 30\times10^{-6}}{4\pi 8.854\times10^{-12}\times(\sqrt{2})^2} \left[\frac{\vec{a}_z - \vec{a}_x}{\sqrt{2}}\right]$$

$$\boxed{\vec{F}_{QQ_1} = 0.9533(\vec{a}_z - \vec{a}_x)}$$

Due to symmentry from the figure

$$|\vec{R}_{2Q}| = |\vec{R}_{3Q}| = |\vec{R}_{4Q}| = |\vec{R}_{1Q}| = \sqrt{2}.$$

$$\vec{R}_{2Q} = \vec{P} - \vec{B} = \vec{a}_z + \vec{a}_x \quad \therefore \vec{a}_{2Q} = \frac{\vec{a}_z + \vec{a}_x}{\sqrt{2}}$$

$$\vec{R}_{3Q} = \vec{P} - \vec{C} = \vec{a}_z - \vec{a}_y \qquad \vec{a}_{3Q} = \frac{\vec{a}_z - \vec{a}_y}{\sqrt{2}}$$

$$\vec{R}_{4Q} = \vec{P} - \vec{D} = \vec{a}_z + \vec{a}_y \qquad \vec{a}_{4Q} = \frac{\vec{a}_z + \vec{a}_y}{\sqrt{2}}$$

$$\vec{F}_{QQ_2} = \frac{Q Q_2}{4\pi\epsilon_0 R_{2Q}^2} \vec{a}_{2Q}$$

$$= 1.3481 \left[\frac{\vec{a}_z + \vec{a}_x}{\sqrt{2}} \right] = 0.9533 (\vec{a}_z + \vec{a}_x)$$

$$\vec{F}_{QQ_3} = 1.3481 \left[\frac{\vec{a}_z - \vec{a}_y}{\sqrt{2}} \right] = 0.9533 (\vec{a}_z - \vec{a}_y)$$

$$\vec{F}_{QQ_4} = 1.3481 \left[\frac{\vec{a}_z + \vec{a}_y}{\sqrt{2}} \right] = 0.9533 (\vec{a}_z + \vec{a}_y)$$

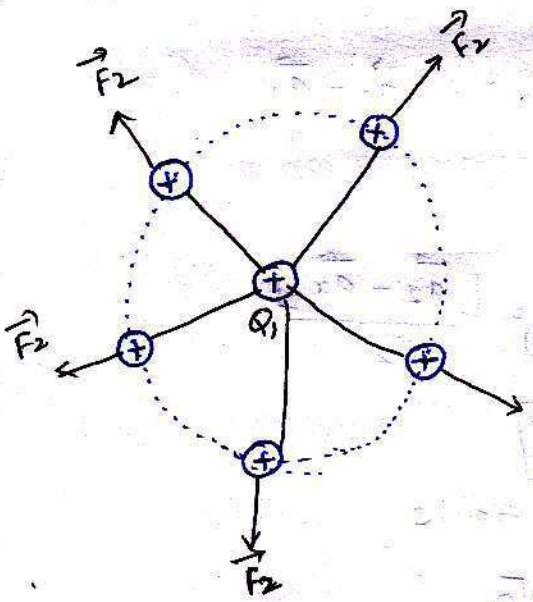
$$\vec{F}_t = \vec{F}_{QQ_1} + \vec{F}_{QQ_2} + \vec{F}_{QQ_3} + \vec{F}_{QQ_4}$$

$$= 0.9533 [\vec{a}_z - \vec{a}_x + \vec{a}_z + \vec{a}_x + \vec{a}_z - \vec{a}_y + \vec{a}_z + \vec{a}_y]$$

$$\boxed{\vec{F}_t = 3.813 \vec{a}_z \text{ N}}$$

ELECTRIC FIELD INTENSITY:

Consider a point charge Q_1 as shown in fig.

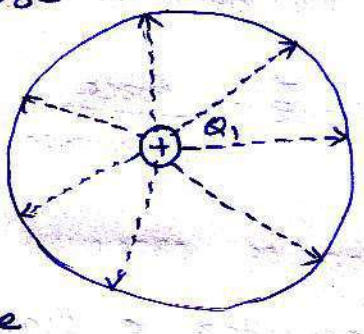


If any other similar charge Q_2 is brought near it, Q_2 experiences a force. Infact if Q_2 is moved around Q_1, still Q_2 experiences a force as shown in fig.

Thus there exists a region around a charge in which it exerts a force on any other charge. This region when a particular charge exerts a force on any other charge located in that region is called ELECTRIC FIELD of that charge.

The electric field of Q_1 is shown in fig below.

The force experienced by the charge Q_2 due to Q_1 is given by Coulomb's law as



$$\vec{F}_2 = \frac{Q_1 Q_2}{4\pi\epsilon_0 R_{12}^2} \vec{a}_{12}$$

Thus force per unit charge can be written as

$$\frac{\vec{F}_2}{Q_2} = \frac{Q_1}{4\pi\epsilon_0 R_{12}^2} \vec{a}_{12}$$

2 marks

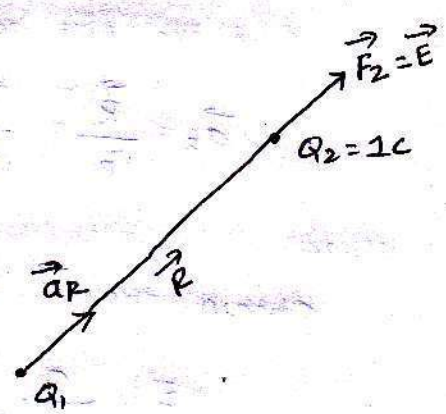
(This force exerted by unit charge is called ELECTRIC FIELD INTENSITY (or) ELECTRIC STRENGTH. It is a vector quantity and is directed along a segment from the charge Q_1 to the position of any other charge. It is denoted by E.

$$\vec{E} = \frac{Q_1}{4\pi\epsilon_0 R_{1P}^2} \vec{a}_{1P}$$

where P = Position of any other charge around Q_1)

Consider a charge Q_1 as shown in figure below. The unit positive charge $Q_2 = 1C$ is placed at a distance of R from Q_1. Then the force acting on Q_2 due to Q_1 is along the unit vector $\vec{a}_R$. As the charge Q_2 is unit charge, the force exerted on Q_2 is nothing but electric field intensity $\vec{E}$ of Q_1 at the point where unit charge is placed.

$$\vec{E} = \frac{Q_1}{4\pi\epsilon_0 R^2} \vec{a}_R$$



$$E = \frac{Q_1}{4\pi\epsilon_0 r^2} \vec{a}_r$$ – spherical system.

$r \rightarrow$ radius of sphere 'r'.

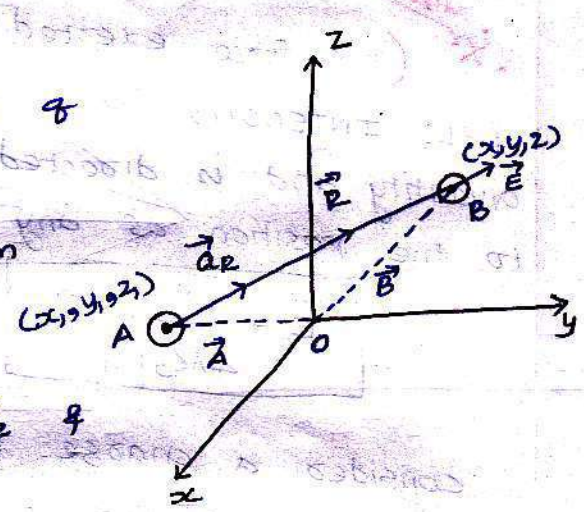
UNITS OF $\vec{E}$:

The definition of Electric field intensity is,

$$\vec{E} = \frac{\text{force}}{\text{unit charge}} = \frac{N \text{ (Newtons)}}{C \text{ (Coulomb)}}.$$

METHOD OF OBTAINING $\vec{E}$ in CARTESIAN SYSTEM:

Consider a charge Q_1 located at point $A(x_1, y_1, z_1)$ as shown in figure. It is required to obtain $\vec{E}$ at any point $B(x, y, z)$ in the cartesian system. then $\vec{E}$ at point B can be obtained using following steps:



STEP 1:

Obtain the position vectors of Points A & B

$\therefore \vec{r}_A = \vec{A}$ while $\vec{r}_B = \vec{B}$ from their co-ordinates.

$$\therefore \vec{A} = x_1 \vec{a}_x + y_1 \vec{a}_y + z_1 \vec{a}_z \text{ \&}$$

$$\vec{B} = x\vec{a}_x + y\vec{a}_y + z\vec{a}_z$$

STEP 2: Find the distance vector $\vec{R}$ directed from A to B.

$$\vec{R} = \vec{B} - \vec{A} = (x - x_1)\vec{a}_x + (y - y_1)\vec{a}_y + (z - z_1)\vec{a}_z$$

STEP 3:

Find the unit vector $\vec{a}_R$ along the direction from A to B.

$$\vec{a}_R = \frac{\vec{R}}{|\vec{R}|} = \frac{\vec{B} - \vec{A}}{|\vec{B} - \vec{A}|}.$$

Step4:

Obtain the $\vec{E}$ at the point B as,

$$E = \frac{Q}{4\pi\epsilon_0 R^2} \vec{a}_R = \frac{Q}{4\pi\epsilon_0 R^2} \frac{\vec{R}}{|\vec{R}|} \text{ V/m}.$$

where $R^2 = |\vec{R}|^2$ = Distance b/w the points A & B.

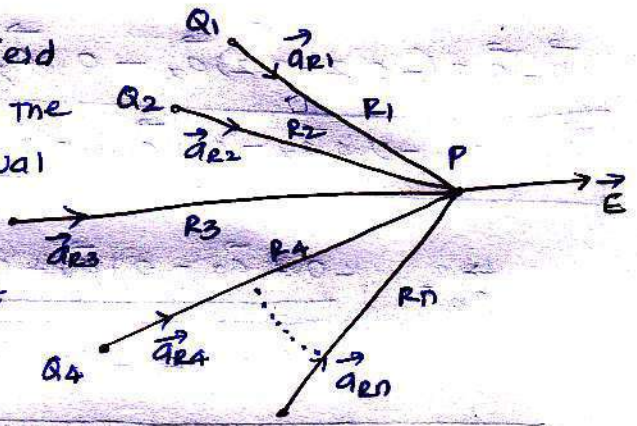
Step 5:

Magnitude of $\vec{E}$ is given by,

$$|\vec{E}| = \frac{Q}{4\pi\epsilon_0 R^2} \text{ V/m}.$$

ELECTRIC FIELD INTENSITY DUE TO DISCRETE CHARGES:

Consider 'n' charges $Q_1, Q_2, \ldots, Q_n$ as shown in figure given below. The combined electric field intensity is to be obtained at Point P. The distances of point P from $Q_1, Q_2, \ldots, Q_n$ are $R_1, R_2, \ldots, R_n$ respectively. The unit vectors along these directions are $\vec{a}_{R1}, \vec{a}_{R2}, \ldots, \vec{a}_{Rn}$ respectively.



Then the total electric field intensity at point P is the vector sum of the individual field intensities produced by the various charges at the point P.

$$\vec{E} = \vec{E}_1 + \vec{E}_2 + \ldots + \vec{E}_n$$

$$= \frac{Q_1}{4\pi\epsilon_0 R_1^2}\vec{a}_{R1} + \frac{Q_2}{4\pi\epsilon_0 R_2^2}\vec{a}_{R2} + \ldots + \frac{Q_n}{4\pi\epsilon_0 R_n^2}\vec{a}_{Rn}$$

$$\therefore \vec{E} = \frac{1}{4\pi\epsilon_0}\sum_{i=1}^{n}\frac{Q_i}{R_i^2}\vec{a}_{Ri}$$

Each unit vector can be obtained by using the method discussed earlier

$$\vec{a}_{Ri} = \frac{\vec{r}_p - \vec{r}_i}{|\vec{r}_p - \vec{r}_i|}$$

$\vec{r}_p \rightarrow$ Position vector of point P

$\vec{r}_i \rightarrow$ Position vector of point where charge Q_i is placed.

Problems :

1. Determine the electric field intensity at P(-0.2, 0, -2.3) m due to a point charge of +5nC at Q(0.2, 0.1, -2.5) m in air.

$$\vec{E} = \frac{Q}{4\pi\epsilon_0 R^2}\vec{a}_R$$

$$\vec{a}_R = \frac{\vec{R}_{QP}}{|\vec{R}_{QP}|} = \frac{\vec{P}-\vec{Q}}{|\vec{P}-\vec{Q}|}$$

$$\vec{P} = -0.2\vec{a}_x + 0\vec{a}_y - 2.3\vec{a}_z$$

$$\vec{Q} = 0.2\vec{a}_x + 0.1\vec{a}_y - 2.5\vec{a}_z$$

$$\vec{P}-\vec{Q} = (-0.2-0.2)\vec{a}_x - 0.1\vec{a}_y + (-2.3+2.5)\vec{a}_z$$

$$\boxed{\vec{R}_{QP} = -0.4\vec{a}_x - 0.1\vec{a}_y + 0.2\vec{a}_z}$$

$$\vec{a}_R = \frac{-0.4\vec{a}_x - 0.1\vec{a}_y + 0.2\vec{a}_z}{\sqrt{(-0.4)^2 + (0.1)^2 + (0.2)^2}} = \frac{-0.4\vec{a}_x - 0.1\vec{a}_y + 0.2\vec{a}_z}{0.45825}$$

$$\boxed{\vec{a}_R = -0.8728\vec{a}_x - 0.2182\vec{a}_y + 0.4364\vec{a}_z}$$

$$\therefore E = \frac{5\times10^{-9}}{4\pi\times8.854\times10^{-12}\times(0.45825)^2}\left[-0.8728\vec{a}_x - 0.2182\vec{a}_y + 0.4364\vec{a}_z\right]$$

$$\boxed{\vec{E} = -186.779\vec{a}_x - 46.694\vec{a}_y + 93.389\vec{a}_z \ V/m}$$

2. A charge of 1C is at (2, 0, 0). What charge must be placed at (-2, 0, 0) which will make y component of total $\vec{E}$ zero at the point (1, 2, 2) ?

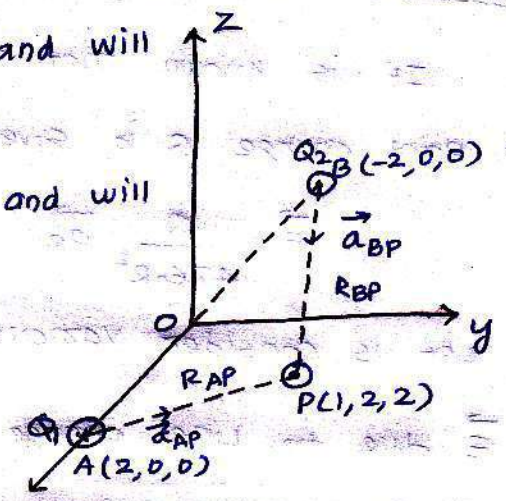
The position vectors of points A, B and P are

$$\vec{A} = 2\vec{a}_x \qquad \vec{P} = \vec{a}_x + 2\vec{a}_y + 2\vec{a}_z$$

$$\vec{B} = -2\vec{a}_y$$

$\vec{E}_A$ is field at P due to Q_1, and will act along $\vec{a}_{AP}$.

$\vec{E}_B$ is field at P due to Q_2 and will act along $\vec{a}_{BP}$



$$\therefore \vec{E}_A = \frac{Q_1}{4\pi\epsilon_0 R_{AP}^2}\vec{a}_{AP}$$

$$= \frac{Q_1}{4\pi\epsilon_0 R_{AP}^2}\left|\frac{\vec{P}-\vec{A}}{|\vec{P}-\vec{A}|}\right.$$

$$\vec{E}_B = \frac{Q_2}{4\pi\epsilon_0 R_{BP}^2}\vec{a}_{BP} = \frac{Q_2}{4\pi\epsilon_0 R_{BP}^2}\frac{\vec{P}-\vec{B}}{|\vec{P}-\vec{A}|}$$

$$\vec{E} \text{ at } P = \vec{E}_A + \vec{E}_B$$

$$= \frac{1}{4\pi\epsilon_0}\left[\frac{Q_1}{R_{AP}^2}\frac{\vec{P}-\vec{A}}{|\vec{P}-\vec{A}|} + \frac{Q_2}{R_{BP}^2}\frac{\vec{P}-\vec{B}}{|\vec{P}-\vec{B}|}\right]$$

$$= \frac{1}{4\pi\epsilon_0}\left[\frac{1[-\vec{a}_x + 2\vec{a}_y + 2\vec{a}_z]}{(\sqrt{9})^2\sqrt{9}} + \frac{Q_2(3\vec{a}_x + 2\vec{a}_y + 2\vec{a}_z)}{(\sqrt{17})^2(\sqrt{17})}\right]$$

$$= \frac{1}{4\pi\epsilon_0}\left[\frac{-\vec{a}_x + 2\vec{a}_y + 2\vec{a}_z}{27} + \frac{Q_2[3\vec{a}_x + 2\vec{a}_y + 2\vec{a}_z]}{70.0927}\right]$$

The y component of $\vec{E}$ must be zero

$$\therefore \frac{2}{27} + \frac{2Q_2}{70.0927} = 0$$

$$Q_2 = -\frac{2}{27} \times \frac{70.0927}{2} = -2.596\,C$$

This is required charge Q_2 to be placed at (-2, 0, 0) which will make y component of $\vec{E}$ zero at point P.

ELECTRIC FIELD INTENSITY DUE TO VARIOUS CHARGE DISTRIBUTION

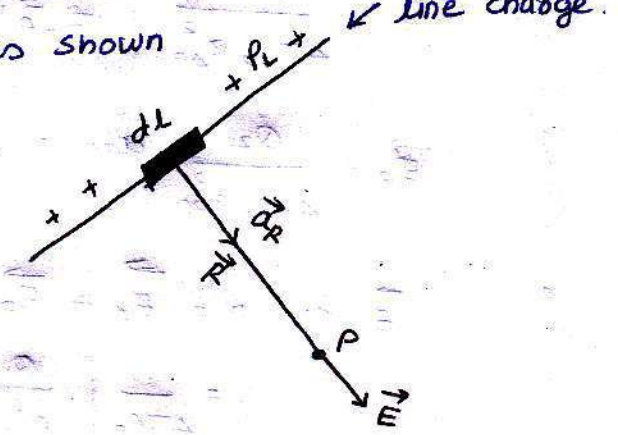
It is known that the electric field intensity due to a point charge Q is given by

$$\vec{E} = \frac{Q}{4\pi\epsilon_0 R^2}\vec{a}_R$$

Let us consider various charge distributions.

$\vec{E}$ due to line charge:

Consider a line charge distribution having a charge density ρ_L as shown in figure.



The charge dQ on the differential length dl is

$$dQ = \rho_L\, dl$$

Hence the differential electric field $\vec{dE}$ at point P due to dQ is given by.

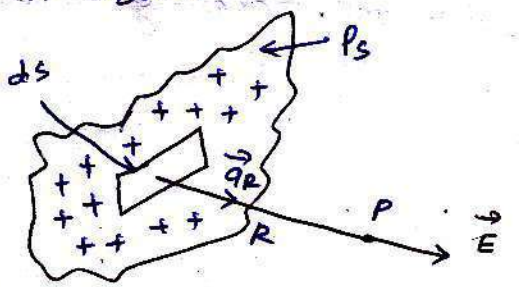
$$\vec{dE} = \frac{dQ}{4\pi\epsilon_0 R^2}\vec{a}_R = \frac{\rho_L\, dl}{4\pi\epsilon_0 R^2}\vec{a}_R$$

Hence the total $\vec{E}$ at a point P due to line charge can be obtained by integrating $\vec{dE}$ over the length of the charge

$$\vec{E} = \int_L \frac{\rho_L\, dl}{4\pi\epsilon_0 R^2}\vec{a}_R$$

$\vec{E}$ due to SURFACE CHARGE:

Consider a surface charge distribution having a charge density ρ_s as shown in figure.



The charge dQ on the differential surface area ds is

$$dQ = \rho_s\, ds$$

Hence the differential electric field $d\vec{E}$ at point P due to dQ is given by

$$\vec{dE} = \frac{dQ}{4\pi\epsilon_0 R^2}\vec{a}_R = \frac{\rho_s ds}{4\pi\epsilon_0 R^2}\vec{a}_R$$

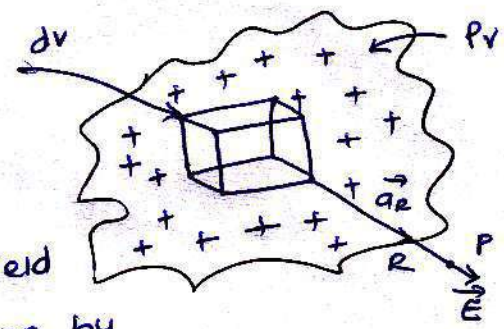
Hence the total $\vec{E}$ at a point P is to be obtained by integrating $d\vec{E}$ over the surface area on which charge is distributed. Note that this will be a double integration.

$$\therefore \vec{E} = \int_S \frac{\rho_s ds}{4\pi\epsilon_0 R^2}\vec{a}_R$$

The $\vec{a}_R$ and ds to be obtained according to the position of the sheet of charge and the co-ordinate system used.

$\vec{E}$ due to VOLUME CHARGE:

Consider a volume charge distribution having a charge density ρ_v as shown in figure.



The charge dQ on differential volume dv is

$$dQ = \rho_v dv$$

Hence the differential electric field $\vec{dE}$ at a point P due to dQ is given by

$$\vec{dE} = \frac{dQ}{4\pi\epsilon_0 R^2}\vec{a}_R = \frac{\rho_v dv}{4\pi\epsilon_0 R^2}\vec{a}_R$$

Hence the total $\vec{E}$ at a point P is to be obtained by integrating $\vec{dE}$ over the volume in which charge is accumulated. Note that this integration will be a triple integration.

$$\vec{E} = \int_{Vol} \frac{\rho_v dv}{4\pi\epsilon_0 R^2}\vec{a}_R$$

$\vec{a}_R$ & dv must be obtained according to the co-ordinate system used.

UNIT-II

ELECTRIC FLUX:

1837 - Michael Faraday - Experimented on Electric Field.

- Electric field around a charge can be imagined as lines of force around it.
- He suggested that the electric field should be assumed to be composed of very small bunches containing a fixed number of electric lines of force. Such a bunch or closed area is called a **tube of flux**. The total number of tubes of flux in any particular electric field is called as the **Electric flux**.

The total number of lines of force in any particular electric field is called the electric flux. It is represented by the symbol ψ. similar to the charge, unit of electric flux is also coulomb C.

PROPERTIES OF FLUX LINES:

Electric flux - The lines of force, around a charge.

1. The flux lines start from +ve charge and terminate on the negative charge.
2. If -ve charge is absent, then the flux lines will terminate at infinity as shown in fig (a). While in absence of +ve charge, the electric flux terminates on the negative charge from infinity. This is shown in fig (b).

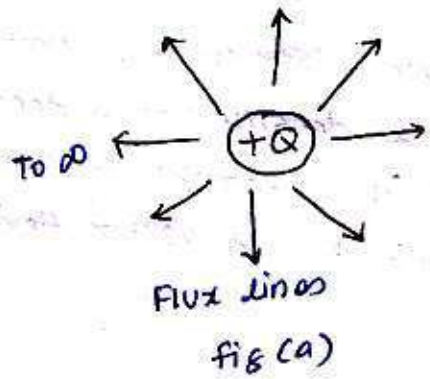


fig (a)

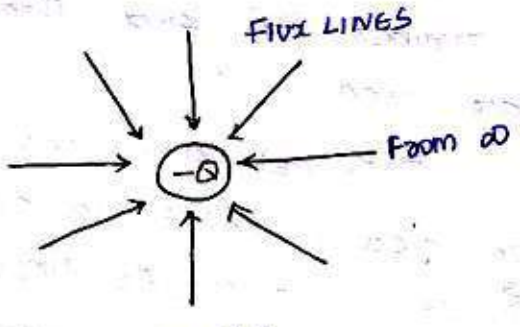


Fig (b).

3. There are more number of lines. i.e. crowding of lines if electric field is stronger.

4. The flux lines are independent of the medium in which charges are placed.

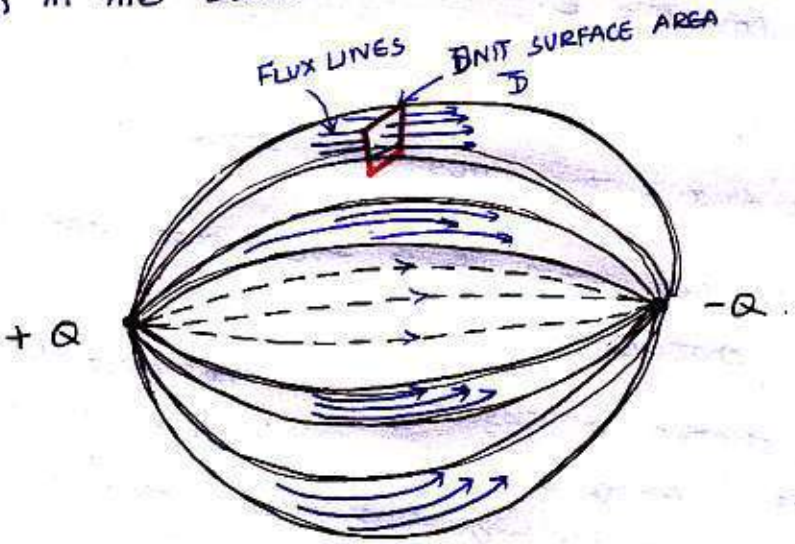
5. If the charge on a body is $\pm Q$ coulombs, then the total number of lines originating or terminating on it is also Q.

$\therefore$ **Electric flux $\psi = Q$ coulombs**

The electric flux is also called DISPLACEMENT FLUX.

ELECTRIC FLUX DENSITY ($\bar{D}$).

Consider the two point charges as shown in the figure below. The flux lines originating from Positive charge and terminating at negative charge as shown in the form of tubes.



Consider a unit surface area as shown in figure. The number of flux lines are passing thro' this surface area.

The net flux passing normal through the unit surface area is called the electric flux density. It is denoted as $\vec{D}$. It has a specific direction which is normal to the surface area under consideration hence it is a vector field.

Consider a sphere with a charge Q placed at its centre. There are no other charges present around. The Total flux distributes radially around the charge is $\psi = Q$. This flux distributes uniformly over the surface of the sphere.

ψ = Total flux

S = Total surface area of sphere

Then Electric flux density is defined as

$$D = \frac{\psi}{S} \text{ in magnitude}$$

ψ is measured in coulombs

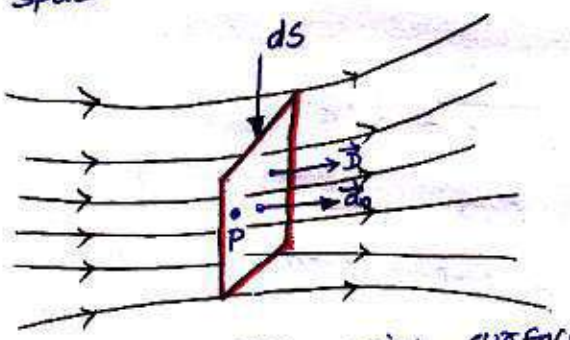
S is measured in sq.meters

$\therefore$ D unit is C/m^2.

'D' is also called as displacement flux density (or) displacement density.

VECTOR FORM OF ELECTRIC FLUX DENSITY:

Consider the flux distribution, due to a certain charge in the free space as shown in figure below.



Consider the differential surface area ds at point P. The flux crossing through this differential area is $d\psi$. The direction of $\vec{D}$ is same as that of direction of flux lines at that point.

The differential area and flux lines are at right angles to each other at point P. Hence the direction of $\vec{D}$ is also normal to the surface area ds. Near point P, all the lines of flux $d\psi$ are having same direction as that of $\vec{a_n}$.

Hence the flux density $\vec{D}$ at the point P can be represented in the vector form as

$$\vec{D} = \frac{d\psi}{ds}\vec{a}_n \quad C/m^2$$

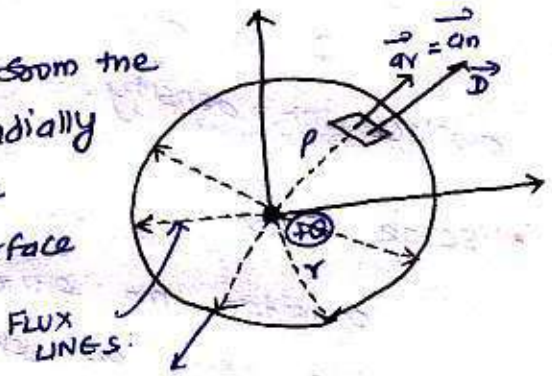
$d\psi \rightarrow$ Total flux lines crossing normal thro' the differential area ds.

$ds \rightarrow$ Differential surface area

$\vec{a}_n \rightarrow$ unit vector in the direction normal to the differential surface area.

$\vec{D}$ due to a point charge Q

Consider a point charge +Q placed at the centre of the imaginary sphere of radius r. This is shown in the figure.



The flux lines originating from the point charge +Q are directed radially outwards. The magnitude of flux density at any point on the surface is.

$$|\vec{D}| = \frac{\text{Total flux } \psi}{\text{Total surface area 'S'}}$$

$\psi = Q =$ total flux

$S = 4\pi r^2 =$ Total surface area

$$\boxed{|\vec{D}| = \frac{Q}{4\pi r^2}}$$

The unit vector directed radially outwards and normal to the surface at any point on the on the sphere is $\vec{a}_n = \vec{a}_r$. Thus in vector form, Electric flux density at a point which is at a distance of r, from the point charge +Q is given by

$$\boxed{\vec{D} = \frac{Q}{4\pi r^2}\vec{a}_r \quad C/m^2}$$

RELATIONSHIP BETWEEN $\vec{D}$ & $\vec{E}$

We know that, the Electric field Intensity $\vec{E}$ at a distance of r, from a Point charge +Q is given by

$$\boxed{\vec{E} = \frac{Q}{4\pi\epsilon_0 r^2}\vec{a}_r} \quad ---- (1)$$

& Electric flux density ($\vec{D}$) is given by

$$\boxed{\vec{D} = \frac{Q}{4\pi r^2}\vec{a}_r} \quad ---- (2)$$

(2) ÷ (1) we get

$$\frac{\vec{D}}{\vec{E}} = \frac{[Q/4\pi r^2]\vec{a}_r}{[Q/4\pi\epsilon_0 r^2]\vec{a}_r} = \epsilon_0$$

$$\boxed{\vec{D} = \epsilon_0\vec{E}} \quad --- \text{for free space}$$

Thus $\vec{D}$ & $\vec{E}$ are related thro' the Permittivity. If the medium in which charge is located ~~in free space~~ is other than free space having relative Permittivity ϵ_r, then

$$\boxed{\vec{D} = \epsilon_0\epsilon_r\vec{E}} = \epsilon\vec{E}$$

ELECTRIC FLUX DENSITY FOR VARIOUS CHARGE DISTRIBUTIONS:

LINE CHARGE:

Consider a line charge having uniform charge density of ρ_L c/m. Then the total charge along the line is given by,

$$Q = \int_L \rho_L \, dl$$

$$\& \quad \vec{D} = \frac{Q}{4\pi r^2}\vec{a}_r = \boxed{\frac{\int_L \rho_L \, dl}{4\pi r^2}\vec{a}_r}$$

If the line charge is infinite then $\vec{E}$ is derived as,

$$\vec{E} = \frac{\rho_L}{2\pi\epsilon_0 r}\vec{a}_r \quad \& \quad \boxed{\vec{D} = \epsilon_0 E = \frac{\rho_L}{2\pi r}\vec{a}_r}$$

SURFACE CHARGE:-

Consider a sheet of charge having uniform charge density of ρ_s C/m^2. Then the total charge on the surface is given by,

$$Q = \int_S \rho_s \, ds$$

$$\therefore \quad \vec{D} = \frac{Q}{4\pi r^2} \vec{a}_r$$

$$\vec{D} = \frac{\int_S \rho_s \, ds}{4\pi r^2} \vec{a}_r$$

The integration is over the surface S and is double integral.

If the sheet of charge is infinite then $\vec{E}$ is derived as

$$\vec{E} = \frac{\rho_s}{2\epsilon_0} \vec{a}_n$$

$$\therefore \quad \vec{D} = \epsilon_0 \vec{E}$$

$$\vec{D} = \frac{\rho_s}{2} \vec{a}_n$$

VOLUME CHARGE

Consider a charge enclosed by a volume, with a uniform charge density ρ_v C/m^3. Then the total charge enclosed by the volume is given by,

$$Q = \int_{Vol} \rho_v \, dv. \qquad E = \frac{\int_{Vol} \rho_v . dv}{4\pi\epsilon_0 r^2} \vec{a}_r$$

$$\vec{D} = \epsilon_0 E = \frac{\int_{Vol} \rho_v . dv}{4\pi r^2} \vec{a}_r$$

PROBLEM:

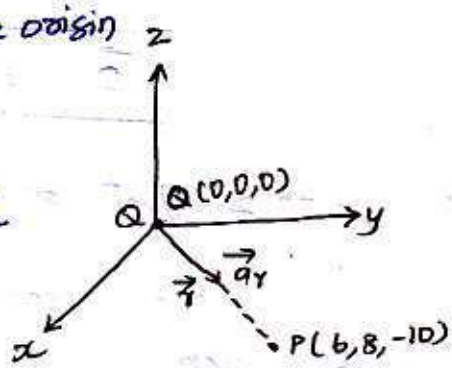
Find $\vec{D}$ in Cartesian co-ordinate at Point (6, 8, -10) due to

a) a Point charge of 40mC at the origin.

b) a uniform line charge of $\rho_L = 40 \mu C/m$ on the z-axis

& c) a uniform surface charge density $\rho_s = 57.2 \, nC/m^2$ on the Plane $x = 12m$

a) A Point charge of 40mC at the origin



P(6, 8, -10) & O(0, 0, 0)

$\therefore \vec{r} = (6-0)\vec{a}_x + (8-0)\vec{a}_y + (-10-0)\vec{a}_z$

$\vec{r} = 6\vec{a}_x + 8\vec{a}_y - 10\vec{a}_z$

$\therefore |\vec{r}| = \sqrt{6^2 + 8^2 + 10^2} = \sqrt{200}$

$\therefore \vec{a}_r = \frac{\vec{r}}{|\vec{r}|} = \frac{6\vec{a}_x + 8\vec{a}_y - 10\vec{a}_z}{\sqrt{200}}$

$\therefore \vec{D} = \frac{Q}{4\pi r^2} \vec{a}_r = \frac{40 \times 10^{-3}}{4\pi \times (\sqrt{200})^2} \left\{ \frac{6\vec{a}_x + 8\vec{a}_y - 10\vec{a}_z}{\sqrt{200}} \right\}.$

$$\vec{D} = 6.752 \times 10^{-6} \vec{a}_x + 9.003 \times 10^{-6} \vec{a}_y - 11.254 \times 10^{-6} a_z \; C/m^2$$

(b) $\rho_L = 40 \mu C/m$ along z-axis.

The charge is infinite hence,

$$\vec{E} = \frac{\rho_L}{2\pi\epsilon_0 r} \vec{a}_r$$

As the charge is along z-axis there cannot be any component of $\vec{E}$ along z-direction.

Consider a point on the line charge (0, 0, z) and P(6, 8, -10). But while obtaining $\vec{r}$ do not consider z co-ordinate as $\vec{E}$ and $\vec{D}$ have no $\vec{a}_z$ component.

$$\therefore \vec{r} = (6-0)\vec{a}_x + (8-0)\vec{a}_y = 6\vec{a}_x + 8\vec{a}_y$$

$$|\vec{Y}| = \sqrt{6^2+8^2} = 10$$

$$\vec{a}_Y = \frac{6\vec{a}_x + 8\vec{a}_y}{10}$$

$$\vec{E} = \frac{\rho_L}{2\pi\epsilon_0(10)}\left[\frac{6\vec{a}_x + 8\vec{a}_y}{10}\right]$$

$$\vec{D} = \epsilon_0\vec{E} = \frac{\rho_L}{2\pi\times 10}\left[\frac{6\vec{a}_x + 8\vec{a}_y}{10}\right]$$

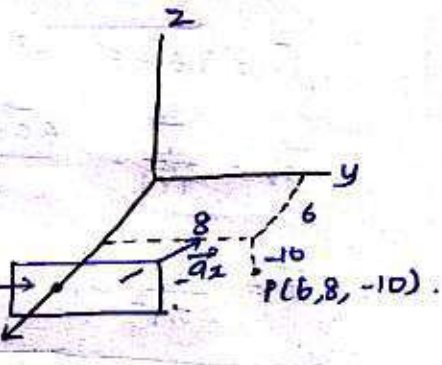
$$\boxed{\vec{D} = 3.819\times10^{-7}\vec{a}_x + 5.092\times10^{-7}\vec{a}_y \ C/m^2}$$

c) $\rho_S = 57.2\,nC/m^2$ on the plane $x=12$

The sheet of charge is infinite over the plane $x=12$ which is $\parallel^{el}$ to yz plane. The unit vector normal to this plane is $\vec{a}_n = \vec{a}_x$

$$\therefore E = \frac{\rho_S}{2\epsilon_0}\vec{a}_n$$

$$= \frac{\rho_S}{2\epsilon_0}(-\vec{a}_x)$$



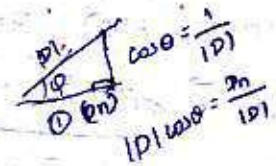
↳ The point P is back side of the plane hence $\vec{a}_n = -\vec{a}_x$ as shown in figure.

$$\therefore \vec{E} = -\frac{\rho_S}{2\epsilon_0}\vec{a}_x$$

$$\boxed{\vec{D} = \epsilon_0\vec{E} = -\frac{\rho_S}{2}\vec{a}_x = 28.6\times10^{-6}\vec{a}_x \ C/m^2}$$

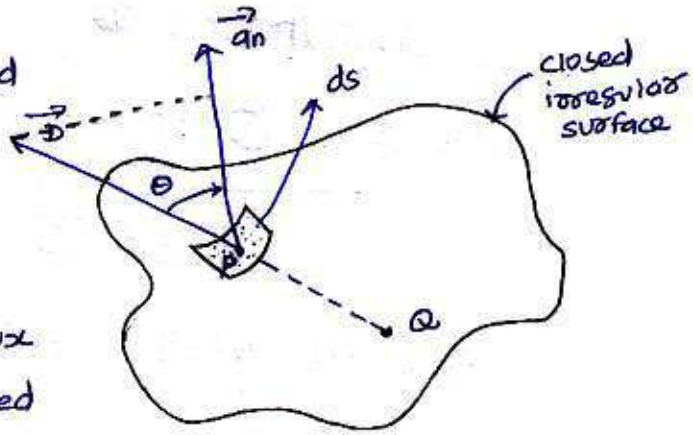
GAUSS'S LAW:

The electric flux passing thro' any closed surface is equal to the total charge enclosed by that surface.



MATHEMATICAL REPRESENTATION OF GAUSS'S LAW:

Consider any object of irregular shape as shown in the figure.



The total charge enclosed by the irregular closed surface is Q coulombs. It may be in any form of distribution. Hence the total flux that has to pass thro' the closed surface is Q.

Consider a small differential surface ds at point P. As the surface is irregular, the direction of $\vec{D}$ as well as its magnitude is going to change from point to point on the surface.

The surface ds under consideration can be represented in the vector form interms of its area and direction normal to the surface at the point. $\vec{V} = V\vec{a}$

$\therefore \vec{ds} = ds\vec{a}_n$

where $\vec{a}_n$ is unit vector normal to the surface ds at point P.

The flux density at point 'P' is $\vec{D}$ and its direction is such that it makes an angle θ with the normal direction at point P.

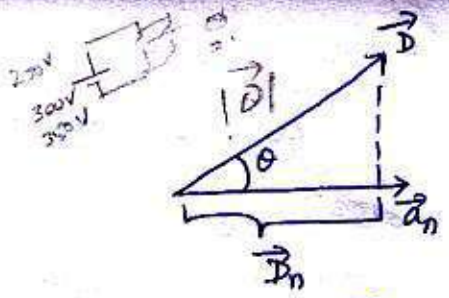
The flux $d\psi$ passing through the surface ds is the product of the component of $\vec{D}$ in the direction normal to the ds and ds.

i.e. $\boxed{d\psi = \vec{D}_n ds}$ --① $[\because \psi = Ds ; \therefore d\psi = D\,ds]$.

Where D_n is the component of $\vec{D}$ in the direction of normal to the surface ds.

From the figure

$$D_n = |D| \cos\theta \quad \text{--- (2)}$$



$$\cos\theta = \frac{D_n}{|D|}$$

Sub (2) in (1) we get

$$d\psi = |\vec{D}| \cos\theta \, ds \quad \text{--- (3)}$$

from the definition of dot product

$$\vec{A} \cdot \vec{B} = |A||B| \cos\theta_{AB}$$

∴ we can write

$$|\vec{D}| ds \cos\theta = \vec{D} \cdot \vec{ds}$$

$$\therefore d\psi = \vec{D} \cdot \vec{ds} \quad \text{--- (4)}$$

[Density is mass per unit area]

This is the flux passing through the incremental surface area ds.

Hence the total flux passing through the entire closed surface is to be obtained by finding the surface integration of the equation (4)

$$\therefore \psi = \int d\psi = \oint_S \vec{D} \cdot \vec{ds} \quad \text{--- (5)}$$

$\oint$ → Indicates integration over the closed surface and is called closed surface integral. It's a double integration. closed surface over which the integration is carried out is called GAUSSIAN SURFACE.

Now irrespective of the shape of the surface and the charge distribution, the total flux passing through the surface is the total charge enclosed by the surface.

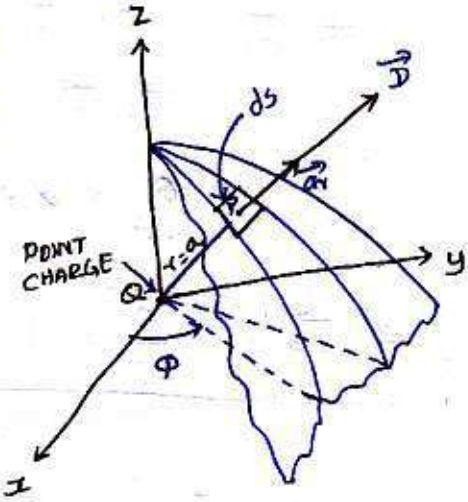
$$\psi = \oint_S \vec{D} \cdot \vec{ds} = Q = \text{charge enclosed}$$

↳ Mathematic representation of Gauss' law.

PROOF FOR GAUSS'S LAW:

Let a point charge Q is located at the origin. To determine $\vec{D}$ and to apply Gauss's law, consider a spherical surface around Q, with centre as origin. This spherical surface is gaussian surface. The $\vec{D}$ is always directed radially outwards along $\vec{a}_r$ which is normal to the spherical surface at any point P on the surface. This is shown in figure below.

Consider a differential surface area ds as shown. The direction normal to the surface ds is $\vec{a}_r$, considering spherical co-ordinate system. The radius of the sphere is r=a.



The direction of $\vec{D}$ is along $\vec{a}_r$ which is normal to ds at any point P.

In spherical co-ordinate systems, the ds normal to radial direction $\vec{a}_r$ is given by [Refer Unit 1 Page No: 24].

$$\boxed{ds = r^2 \sin\theta \, d\theta \, d\varphi} \quad ---(1)$$

W.K.T. $\therefore$ $\boxed{r = a}$ ----(2)

Sub (2) in (1) we get

$$ds = a^2 \sin\theta \, d\theta \, d\varphi \quad ---(3)$$

$$\therefore \vec{ds} = ds \, \vec{a}_n \quad ---(4)$$

& $\vec{a}_n = \vec{a}_r$

$$\therefore \boxed{\vec{ds} = a^2 \sin\theta \, d\theta \, d\varphi \, \vec{a}_r} \quad ---(5)$$

Now $\vec{D}$ due to point charge is given by,

$$\vec{D} = \frac{Q}{4\pi r^2} \vec{a}_r = \frac{Q}{4\pi a^2} \vec{a}_r \quad [\text{as } r = a].$$

$\therefore \vec{D} \cdot \vec{ds} = |\vec{D}||\vec{ds}| \cos\theta'$

where θ' is the angle b/w $\vec{D}$ and $\vec{ds}$

Where $|\vec{D}| = \frac{Q}{4\pi a^2}$ ----⑥

$|\vec{ds}| = a^2 \sin\theta \, d\theta \, d\phi$ ---⑦

The normal to $\vec{ds}$ is $\vec{a_r}$ while $\vec{D}$ also acts along $\vec{a_r}$ hence angle between $\vec{ds}$ and $\vec{D}$ is zero (i.e) $\theta' = 0$

$\therefore \vec{D} \cdot \vec{ds} = |\vec{D}| \, |\vec{ds}| \cos 0^\circ$

$= |\vec{D}||\vec{ds}|$

$= \frac{Q}{4\pi a^2} \times a^2 \sin\theta \, d\theta \, d\phi$

$$\boxed{\vec{D} \cdot \vec{ds} = \frac{Q}{4\pi} \sin\theta \, d\theta \, d\phi} \quad ----⑧$$

$\therefore \psi = \oint_S \vec{D} \cdot \vec{ds}$

$$= \int_{\phi=0}^{2\pi} \int_{\theta=0}^{\pi} \frac{Q}{4\pi} \sin\theta \, d\theta \, d\phi$$

$$= \frac{Q}{4\pi} \left[\int_{\phi=0}^{2\pi} d\phi \int_{\theta=0}^{\pi} \sin\theta \, d\theta \right]$$

$$= \frac{Q}{4\pi} [\phi]_0^{2\pi} [-\cos\theta]_0^{\pi}$$

$$= \frac{Q}{4\pi} [2\pi - 0][-\cos\pi + \cos 0]$$

$$= \frac{Q}{4\pi} \times 2\pi [-(-1) + 1] \Rightarrow \frac{Q}{4\pi} \times 2\pi \times 2$$

$$\Rightarrow \boxed{\psi = Q}$$

This Proves Gauss's law that Q coulombs of flux crosses the surface is Q coulombs of charge is enclosed by that surface.

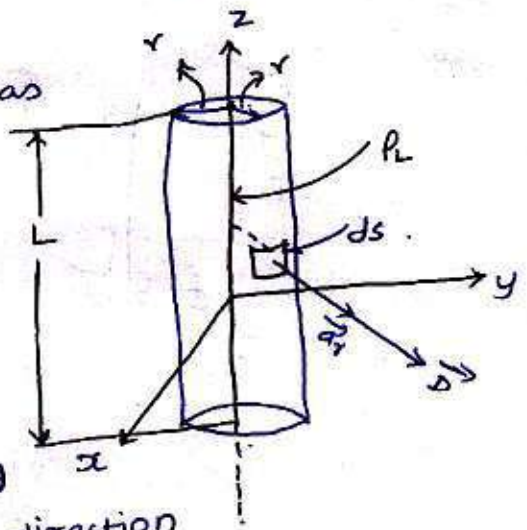
APPLICATIONS OF GAUSS'S LAW:

Gauss's law is used to find $\vec{D}$ or $\vec{E}$ due to some symmetric charge distributions like.

(i) Point charge
(ii) Line charge
(iii) Surface charge
(iv) Volume charge
(v) Co-axial cable & so on.

GAUSS'S LAW APPLIED TO INFINITE LINE CHARGE:

Consider an infinite line charge of density ρ_L C/m lying along z-axis from $-\infty$ to $+\infty$. This is shown in figure below.



Consider the Gaussian surface as the right circular cylinder with z axis as its axis and radius r as shown in the figure. The length of the cylinder is L.

The flux density at any point on the surface is directed radially outwards i.e in the $\vec{a}_r$ direction according to cylindrical-co-ordinate system.

Consider a differential surface area ds as shown which is at a radial distance r from the line charge. The direction normal to ds is $\vec{a}_r$

As the line charge is along z-axis, there cannot be any component of $\vec{D}$ in the z direction. So $\vec{D}$ has only radial component

Now $Q = \oint \vec{D} \cdot \vec{ds}$

This integration is to be evalvated for side surface, top surface and bottom surface.

$$\therefore Q = \oint_{side} \vec{D}\cdot\vec{ds} + \oint_{top} \vec{D}\cdot ds + \oint_{bottom} \vec{D}\cdot\vec{ds}$$

Now $\vec{D} = D_r \vec{a}_r$ has only radial component.

and $\vec{ds} = r\,d\phi\,dz\,\vec{a}_r$ normal to $\vec{a}_r$ direction [From Page No:2D & unit-I]

$$\vec{D}\cdot\vec{ds} = D_r \cdot r\,d\phi\,dz\,[\vec{a}_r\cdot\vec{a}_r]$$

$$\vec{D}\cdot\vec{ds} = D_r\, r\,d\phi\,dz \qquad [\because \vec{a}_r\cdot\vec{a}_r = 1]$$

Note D_r is constant over the side surface

As $\vec{D}$ has only radial component and no component along $\vec{a}_z$ and $-\vec{a}_z$ hence integrations over top and bottom surfaces is zero.

$$\therefore \oint_{top} \vec{D}\cdot ds = \oint_{bottom} \vec{D}\cdot\vec{ds} = 0.$$

$$\therefore Q = \oint_{side} \vec{D}\cdot\vec{ds} = \oint_{side} D_r\, r\,d\phi\,dz$$

$$= D_r r \int d\phi\,dz$$

$$= r D_r \left[\int_{\phi=0}^{2\pi} d\phi \int_{z=0}^{L} dz\right]$$

$$= r D_r \left[[\phi]_0^{2\pi}\ [z]_0^{L}\right]$$

$$Q = 2\pi r D_r L$$

$$D_r = \frac{Q}{2\pi r L} \qquad \therefore \vec{D} = D_r \vec{a}_r = \frac{Q}{2\pi r L}\vec{a}_r$$

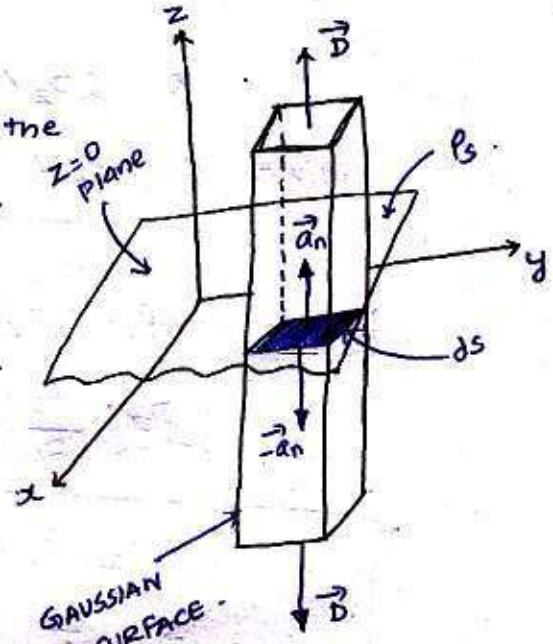
But $\frac{Q}{L} = \rho_L$ C/m.

$$\therefore \boxed{\vec{D} = \frac{\rho_L}{2\pi r}\vec{a}_r \ C/m^2} \ \& \ \boxed{E = \frac{\vec{D}}{\epsilon_a} = \frac{\rho_L}{2\pi\epsilon_0 r}\vec{a}_r \ V/m}$$

GAUSS'S LAW APPLIED TO INFINITE SHEET OF CHARGE:

Consider the infinite sheet of charge of uniform charge density ρ_s C/m^2, lying in the $z=0$ plane. i.e. xy plane as shown in fig.

consider a rectangular box as a Gaussian surface which is cut by the sheet of charge to give $ds = dx\,dy$.



$\vec{D}$ acts normal to the plane i.e $\vec{a}_n = \vec{a}_z$ and $-\vec{a}_n = -\vec{a}_z$ direction.

Hence $\vec{D} = 0$ in x and y directions.

Hence the charge enclosed can be written as

$$Q = \oint_S \vec{D}\cdot d\vec{s} = \oint_{\text{sides}} \vec{D}\cdot d\vec{s} + \oint_{\text{top}} \vec{D}\cdot d\vec{s} + \oint_{\text{bottom}} \vec{D}\cdot d\vec{s}$$

But $\oint_{\text{sides}} \vec{D}\cdot d\vec{s} = 0$ as $\vec{D}$ has no component in x and y direction.

Now $\vec{D} = D_z \vec{a}_z$ <u>for top surface</u>

and $\vec{ds} = dx\,dy\,\vec{a}_z$ [From Page No: 16 of unit-I].

$$\therefore \vec{D}\cdot\vec{ds} = D_z\,dx\,dy\,(\vec{a}_z\cdot\vec{a}_z)$$

$$\vec{D}\cdot\vec{ds} = D_z\,dx\,dy$$

<u>For bottom surface</u>

$$\vec{D} = D_z(-\vec{a}_z)$$

$$\vec{ds} = dx\,dy(-\vec{a}_z)$$

$$\therefore \vec{D}\cdot\vec{ds} = D_z\,dx\,dy\,(-\vec{a}_z\cdot-\vec{a}_z)$$

$$\vec{D}\cdot\vec{ds} = D_z\,dx\,dy.$$

$$\therefore Q = \oint_{top} D_z \, dx\, dy + \oint_{bottom} D_z \, dx\, dy$$

Let $\oint_{top} dx\, dy = \oint_{bottom} dx\, dy = A$ = Area of surface

$$\rho_s = \frac{Q}{A}$$

$$\therefore Q = 2 D_z A$$

W.K.T $Q = \rho_s A$ → surface charge density

$$\therefore \rho_s = 2 D_z$$

$$D_z = \frac{\rho_s}{2}$$

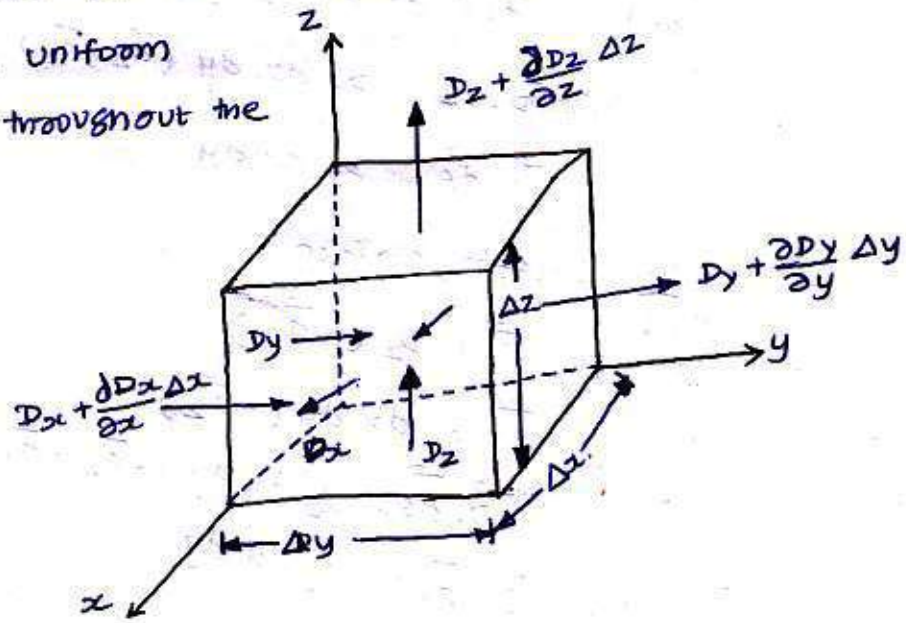
$$\therefore \vec{D} = D_z \cdot \vec{a}_z = \frac{\rho_s}{2} \vec{a}_z \ c/m^2$$

$$\therefore \vec{E} = \frac{\vec{D}}{\epsilon_0} = \frac{\rho_s}{2\epsilon_0} \vec{a}_z \ V/m.$$

GAUSS'S LAW APPLIED OF DIFFERENTIAL VOLUME ELEMENT.

[POINT FORM OF GAUSS'S LAW] (or) GAUSS'S LAW IN DIFFERENTIAL FORM

Consider a small volume $\Delta V = \Delta x\, \Delta y\, \Delta z$ in cartesian system. Here Δx, Δy and Δz are the edges of this small volume in the direction of x, y, z axes respectively. Assume uniform charge density ρ_v throughout the volume.



Now consider this volume is placed in an electric field with the flux density $\vec{D}$ given by

$$\vec{D} = D_x \vec{a}_x + D_y \vec{a}_y + D_z \vec{a}_z \ (C/m^2)$$

Here D_x, D_y and D_z are the flux densities at $x=0$, $y=0$ and $z=0$ planes respectively as shown in fig. In order to derive point form of gauss law, we use integral form of Gauss's law.

$$\oint \vec{D} \cdot d\vec{s} = Q_{enclosed} = \int_V \rho_v \, dv.$$

To obtain RHS.

$$Q_{enclosed} = \oint_V \rho_v dv = \int_0^{\Delta z} \int_0^{\Delta y} \int_0^{\Delta x} \rho_v \, dx \, dy \, dz$$

$$= \rho_v \Delta x \Delta y \Delta z$$

TO OBTAIN LHS:

The closed surface integral consists of six components as

$$\oint_S \vec{D} \cdot d\vec{s} = \int_{back} \vec{D} \cdot d\vec{s} + \int_{front} + \int_{left} + \int_{right} + \int_{bottom} + \int_{top}.$$

This requires knowledge of flux density $\vec{D}$ at each surface, which is obtained as follows:

The flux density D_x is in the direction of x-axis, then the normal outward component of $\vec{D}$ at the back face is $-D_x$.

If the field changes b/w the back and front faces, the rate of change of D in the x direction is $\frac{\partial D_x}{\partial x}$.

The Total change in D b/w back and front face is $\frac{\partial D_x}{\partial x} \cdot \Delta x$.

But the flux density at the back face is D_x

then the normal component of $\vec{D}$ at the front face is

D_x + change in $\vec{D}$ from back to front = $D_x + \frac{\partial D_x}{\partial x}\Delta x$.

Similarly, the normal component of $\vec{D}$ at the

left side face = $-D_y$

Right side face = $D_y + \frac{\partial D_y}{\partial y}\Delta y$

bottom face = $-D_z$

top face = $D_z + \frac{\partial D_z}{\partial z}\Delta z$.

Knowing $\vec{D}$ at each surface now the integrals can be solved.

$$\int_{back} \vec{D}\cdot\vec{ds} = \int_0^{\Delta z}\int_0^{\Delta y} D_x \vec{a}_x \cdot dz\,dy\,\vec{a}_x = -D_x \Delta z \Delta y \quad \text{---(1)}$$

$$\int_{front} \vec{D}\cdot\vec{ds} = \int_0^{\Delta z}\int_0^{\Delta y} \left(D_x + \frac{\partial D_x}{\partial x}\Delta x\right)\vec{a}_x \cdot dz\,dy\,\vec{a}_x$$

$$= \left[D_x + \frac{\partial D_x}{\partial x}\Delta x\right]\Delta y\,\Delta z \quad \text{--(2)}$$

(111) only

$$\int_{left} \vec{D}\cdot\vec{ds} = -D_y \Delta x \Delta z \quad \text{---(3)}$$

$$\int_{top} \vec{D}\cdot\vec{ds} = \left(D_z + \frac{\partial D_z}{\partial z}\Delta z\right)\Delta x \Delta y \quad \text{---(5)}$$

$$\int_{Right} \vec{D}\cdot\vec{ds} = \left(D_y + \frac{\partial D_y}{\partial y}\Delta y\right)\Delta x \Delta z \quad \text{---(4)}$$

$$\int_{bottom} \vec{D}\cdot\vec{ds} = -D_z \Delta x \Delta y \quad \text{---(6)}$$

(1)+(2)+(3)+(4)+(5)+(6) we get

$$LHS = \left[\frac{\partial D_x}{\partial x} + \frac{\partial D_y}{\partial y} + \frac{\partial D_z}{\partial z}\right]\Delta x\,\Delta y\,\Delta z = RHS = \rho_v\,\Delta x\,\Delta y\,\Delta z$$

$$\therefore \rho_v = \frac{\partial D_x}{\partial x} + \frac{\partial D_y}{\partial y} + \frac{\partial D_z}{\partial z} = \left(\frac{\partial}{\partial x}\vec{a}_x + \frac{\partial}{\partial y}\vec{a}_y + \frac{\partial}{\partial z}\vec{a}_z\right)\cdot(D_x\vec{a}_x + D_y\vec{a}_y + D_z\vec{a}_z)$$

Maxwell's First Equation (or) Gauss's law in differential form (18)

$$\rho_v = \nabla\cdot\vec{D} = \text{div}\,\vec{D}$$

→ vector operator.

MATHEMATICAL DEFINITION OF DIVERGENCE:

$\nabla \cdot \vec{D} = 0$ Solenoidal

consider Gauss's law for the electric field in differential form.

$$\nabla \cdot \vec{D} = \rho_v \quad \text{----} (1)$$

We wish to express $\nabla \cdot \vec{D}$ at a point in the charge region interms of $\vec{D}$ at that point.

(1) x ΔV on both sides

$$(\nabla \cdot \vec{D})\,\Delta V = \rho_v \Delta V \quad \text{---} (2)$$

where ΔV is infinitesimal volume ΔV at that point.

But W.K.T ρ_v volume charge density is (C/m^3)

and ΔV is volume in m^3.

$\therefore$ $\rho_v \Delta V$ = charge contained in that volume.

$\therefore$ equation (2) gives the charge enclosed

$$Q_{enclosed} = \rho_v \Delta V \quad \text{----} (3)$$

According to Gauss's law for the electric field in integral form

$$Q_{enclosed} = \oint_S \vec{D} \cdot \vec{ds} \quad \text{----} (4)$$

(3)

$\therefore$ (3) = (4)

$$\Rightarrow \oint_S \vec{D} \cdot \vec{ds} = \rho_v \Delta V \quad \text{---} (5)$$

sub (2) in (5) we get

$$(\nabla \cdot \vec{D})\,\Delta V = \oint \vec{D} \cdot \vec{ds}$$

$$\Rightarrow \nabla \cdot \vec{D} = \frac{\oint \vec{D} \cdot \vec{ds}}{\Delta V}$$

To express $\nabla . \vec{D}$ at a point, let us limit that ΔV tends to zero, at that point

$$\nabla . \vec{D} = \lim_{\Delta V \to 0} \frac{\oint \vec{D} . \vec{ds}}{\Delta V}$$

Thus for any vector $\vec{A}$, divergence is defined as follows.

$$\nabla . \vec{A} = \lim_{\Delta V \to 0} \frac{\oint_S \vec{A} . \vec{ds}}{\Delta V}$$ = divergence of $\vec{A}$ (or) div $\vec{A}$.

PHYSICAL SIGNIFICANCE OF DIVERGENCE:

Definition: It is defined as the out flow of vector over the surface per unit volume as volume approaches zero.

PROPERTIES OF DIVERGENCE OF VECTOR FIELD:

1. The divergence produces a scalar field as the dot product is involved in the operation. The result does not have direction associated with it.

2. $\nabla . (\vec{A} + \vec{B}) = \nabla . \vec{A} + \nabla . \vec{B}$. Distributive

MAXWELL'S FIRST EQUATION:

$$\text{div } \vec{D} = \nabla . \vec{D} = \rho_v$$

This above equation is called Maxwell's first equation applied to electrostatics. This is also called the point form of Gauss's law (or) Gauss's law in differential form.

Problems

(1) Given, $\vec{A} = 2xy\,\vec{a}_x + z\,\vec{a}_y + yz^2\,\vec{a}_z$

Find $\nabla \cdot \vec{A}$ at $P(2,-1,3)$.

$$\nabla \cdot \vec{A} = \text{div}\vec{A} = \frac{\partial A_x}{\partial x} + \frac{\partial A_y}{\partial y} + \frac{\partial A_z}{\partial z}$$

$$= \frac{\partial}{\partial x}[2xy] + \frac{\partial}{\partial y}(z) + \frac{\partial}{\partial z}(yz^2)$$

$$= 2y + 0 + 2zy$$

At $P(2,-1,3) \Rightarrow x = 2, y = -1, z = 3$.

$$\nabla \cdot \vec{A} = 2(-1) + 0 + 2(3)(-1)$$

$$= -2 - 6 = -8$$

$$\Rightarrow \boxed{\nabla \cdot \vec{A} = -8}$$

(2) Find the divergence of $\vec{A}$ at $P(5, \pi/2, 1)$ where $\vec{A} = r^2 z \sin\phi\,\vec{a}_r + 3rz^2\cos\phi\,\vec{a}_\phi$ [in cylindrical system]

$$\text{div}\vec{A} = \frac{1}{r}\frac{\partial}{\partial r}(rA_r) + \frac{1}{r}\frac{\partial}{\partial \phi}A_\phi + \frac{\partial A_z}{\partial z}$$

$A_r = r^2 z \sin\phi \quad A_\phi = 3rz^2\cos\phi \quad A_z = 0$

$$\text{div}\vec{A} = \frac{1}{r}\frac{\partial}{\partial r}[r^2 z\sin\phi] + \frac{1}{r}\frac{\partial}{\partial \phi}[3rz^2\cos\phi]$$

$$= \frac{1}{r}\frac{\partial}{\partial r}[r^2 z\sin\phi] + \frac{1}{r}\cdot 3rz^2\frac{\partial}{\partial\phi}[\cos\phi]$$

$$= \frac{1}{r}\frac{\partial}{\partial r}[r^2 z\sin\phi] + 3z^2[-\sin\phi]$$

$$= \frac{1}{r}\cdot 2rz\sin\phi + 3z^2[-\sin\phi]$$

$$= 2z\sin\phi - 3z^2\sin\phi$$

$$\text{div}\vec{A} = 2z\sin\phi - 3z^2\sin\phi$$

at point $P(5, \pi/2, 1)$ $\quad r = 5, \ \phi = \pi/2, \ z = 1$

$$\text{div}\vec{A} = 2\times1\times\sin\frac{\pi}{2} - 3\times1\times\sin\pi/2$$

$$= 2-3$$

$$\boxed{\text{div}\vec{A}\big|_p = -1}$$

DIVERGENCE THEOREM:

Gauss's law in integral form.

$$Q = \oint_S \vec{D}.\vec{ds} \quad ---①$$

while charge enclosed in a volume is given by

$$Q = \int_V \rho_v \, dV \quad ---②$$

Gauss's law in Point form

$$\nabla.\vec{D} = \rho_v \quad ---③$$

Sub ③ in ② we get

$$Q = \int_V (\nabla.\vec{D})\, dV \quad ---④$$

Equating ① & ④ we get

$$\boxed{\oint_S \vec{D}.\vec{ds} = \int_V (\nabla.\vec{D})dV.} \quad ---⑤$$

Equation ⑤ is called DIVERGENCE THEOREM. It is also called as GAUSS-OSTRDGRADSKY THEOREM.

The integral of the normal component of any vector field over a closed surface is equal to the integral of the divergence of this vector field throughout the volume enclosed by that closed surface

The theorem can be applied to any vector but Partial derivatives of that vector field must exist.

With the help of the divergence theorem, the surface integral can be converted into a volume integral, provided that the closed surface encloses certain volume.

PROOF OF DIVERGENCE THEOREM:

According to divergence theorem, the surface integral is converted into a volume integral, provided that closed surface encloses certain volume.

Let the closed surface encloses certain volume V. subdivide this volume V into a large number of subsections called cells.

Let the vector field associated with surface S is $\vec{D}$. Then i^{th} cell has the volume ΔV_i and is bounded by the surface S_i then we can write,

$$\oint_S \vec{D}.\vec{ds} = \sum_i \oint_{S_i} \vec{D}.\vec{ds} = \sum_i \frac{\oint_{S_i} \vec{D}.\vec{ds}}{\Delta V_i} . \Delta V_i \quad \text{---} (1)$$

The cells are adjacent to each other hence the outward flux to one cell is inward to its neighbouring cells. Thus on every interior surface b/w the cells, there is cancellation of surface integrals and hence the sum of the surface integrals over surfaces S_i's is equal to the total surface integrals over the entire surface S.

$$\therefore \oint_S \vec{D}.\vec{ds} = \frac{\oint_S \vec{D}.\vec{ds}}{\Delta V} . \Delta V \text{---} (2)$$

Taking Lim ΔV tends to zero of RHS of (2) i.e. the volume shrinks about a point, the RHS of (2) gives divergence of $\vec{D}$,

According to the definition of divergence,

$$\lim_{\Delta V \to 0} \frac{\oint_S \vec{D} \cdot d\vec{s}}{\Delta V} = \text{div}\vec{D} = \nabla \cdot \vec{D} \quad \text{--- (3)}$$

sub (3) in (2) we get

$$\oint_S \vec{D} \cdot d\vec{s} = [\nabla \cdot \vec{D}] \Delta V. \quad \text{--- (4)}$$

For considering entire volume, integrate RHS over the entire volume V, enclosed by the surface

$$\therefore \oint_S \vec{D} \cdot d\vec{s} = \int_V [\nabla \cdot \vec{D}] dv. \quad \text{--- (5)}$$

Eqvation (5) is the statement of the divergence theorem and hence divergence theorem is proved.

Problems

(i) Given that $\vec{A} = 30e^{r}\vec{a}_r - 2z\vec{a}_z$ in the cylindrical co-ordinates. Evaluate both sides of the divergence theorem for the volume enclosed by $r = 2$, $z = 0$ and $z = 5$.

SOLUTION:-

The divergence theorem states that

$$\oint_S \vec{A} \cdot d\vec{s} = \oint_V (\nabla \cdot \vec{A}) dv.$$

Now $$\oint_S \vec{A} \cdot d\vec{s} = \left[\oint_{\text{side}} + \oint_{\text{top}} + \oint_{\text{bottom}} \right] \vec{A} \cdot d\vec{s}$$

consider $d\vec{s}$ normal to $\vec{a}_r$ direction which is for the side surface.

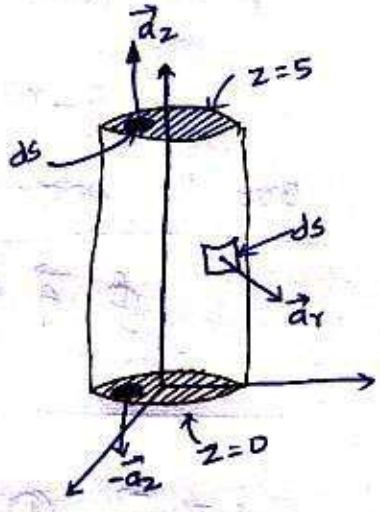
$$d\vec{s} = r\, d\varphi\, dz\, \vec{a}_r$$

$$\vec{A}.\vec{ds} = [30e^{-r}\vec{a}_r - 2z\,\vec{a}_z].\, r\,d\phi\,dz\,\vec{a}_r$$

$$= 30e^{-r} r\,d\phi\,dz\,(\vec{a}_r.\vec{a}_r) - 2zr\,d\phi\,dz\,[\vec{a}_z.\vec{a}_r]$$ (0)

$$\vec{A}.\vec{ds} = 30e^{-r} r\,d\phi\,dz$$

$$\oint_{side} \vec{A}.\vec{ds} = \int_{\phi=0}^{2\pi}\int_{z=0}^{5} 30e^{-r} r\,d\phi\,dz$$



$$\Rightarrow 30e^{-r}\,[\phi]_0^{2\pi}\,[z]_0^5$$

$$\Rightarrow 30e^{-r}(2\pi)(5)$$

$$\Rightarrow 300\pi e^{-r}$$

Given that $r = 2$

$$\therefore \oint_{side} \vec{A}.\vec{ds} = 300\pi\, e^{-2}\cdot 2 = 600\pi e^{-2} = 255.1 \quad \text{---(1)}$$

The $\vec{ds}$ on top has direction $\vec{a}_z$, hence for top surface

$$\vec{ds} = r\,dr\,d\phi\,\vec{a}_z$$

$$\vec{A}.\vec{ds} = [30e^{-r}\vec{a}_r - 2z\vec{a}_z].\, r\,dr\,d\phi\,\vec{a}_z$$

$$= 30e^{-r} r\,dr\,d\phi\,[\vec{a}_r.\vec{a}_z] - 2zr\,dr\,d\phi\,[\vec{a}_z.\vec{a}_z]$$ (0)

$$= -2zr\,dr\,d\phi$$

$$\oint_{top} \vec{A}.\vec{ds} = \oint_{top} -2zr\,dr\,d\phi \Rightarrow -2z\int_{\phi=0}^{2\pi}\int_{r=0}^{2} r\,dr\,d\phi$$

$$\Rightarrow -2z\,[\phi]_0^{2\pi}\left[\frac{r^2}{2}\right]_0^2$$

$$= -2z(2\pi)\left(\frac{4}{2}\right)$$

$$\oint_{top} \vec{A}.\vec{ds} = -8\pi z$$

W.K.T $z = 5$

$$\therefore \oint_{top} \vec{A}.\vec{ds} = -40\pi \quad \text{---(2)}$$

While $\vec{ds}$ for bottom has direction $(-\vec{a}_z)$ hence for bottom surface,

$$\vec{ds} = r\,dr\,d\phi\,(-\vec{a}_z)$$

$$\vec{A}.\vec{ds} = (30e^{-r}\vec{a}_r - 22\vec{a}_z).(r\,dr\,d\phi\,(-\vec{a}_z))$$

$$= 22r\,dr\,d\phi$$

But for bottom surface $z = 0$

$$\therefore \oint_{\text{bottom}} \vec{A}.\vec{ds} = 0 \quad \text{--- (3)}$$

$$\therefore \oint \vec{A}.\vec{ds} = (1) + (2) + (3)$$

$$= 255.1 - 40\pi$$

$$\oint \vec{A}.\vec{ds} = 129.4363 = \text{LHS of divergence theorem.}$$

RHS of divergence theorem is $\int_V (\nabla.\vec{A})\,dv$

$$\nabla.\vec{A} = \frac{1}{r}\frac{\partial}{\partial r}(rA_r) + \frac{1}{r}\frac{\partial A_\phi}{\partial \phi} + \frac{\partial A_z}{\partial z}$$

$$A_r = 30e^{-r} \qquad A_\phi = 0 \qquad A_z = -2z$$

$$\therefore \nabla.\vec{A} = \frac{1}{r}\frac{\partial}{\partial r}(r30e^{-r}) + 0 + \frac{\partial}{\partial z}(-2z)$$

$$= \frac{1}{r}\left[30r\{-e^{-r}\} + 30e^{-r}(1)\right] - 2$$

$$= -30e^{-r} + \frac{30}{r}e^{-r} - 2$$

In cylindrical system $dv = r\,d\phi\,dr\,dz$

$$\therefore \int_V (\nabla \cdot \vec{A})\, dv = \int_{z=0}^{5} \int_{\phi=0}^{2\pi} \int_{r=0}^{2} \left(-30e^{-r} + \frac{30}{r} e^{-r} - 2\right) r\, dr\, d\phi\, dz$$

$$= \int_{r=0}^{2} \int_{\phi=0}^{2\pi} \int_{z=0}^{5} \left(-30e^{-r} \cdot r + 30e^{-r} - 2r\right) dr\, d\phi\, dz$$

$$= \int_{r=0}^{2} \left[-30e^{-r} \cdot r + 30e^{-r} - 2r\right] dr * \int_{\phi=0}^{2\pi} d\phi * \int_{z=0}^{5} dz \cdot$$

$$= -30 \int_{r=0}^{2} re^{-r} dr + 30 \int_{r=0}^{2} e^{-r} dr - 2 \int_{r=0}^{2} r\, dr * [\phi]_0^{2\pi} * [z]_0^{5}$$

$u = r \quad dv = e^{-r}$

$$= \left\{-30\left[r\left[\frac{e^{-r}}{-1}\right]_0^2 - \int_0^2 e^{-r} dr\right\} + 30\left[\frac{e^{-r}}{-1}\right]_0^2 - 2\left[\frac{r^2}{2}\right]_0^2 \right\} \times 2\pi \times 5$$

$\left[\int u\,dv = uv - \int v\,du\right]$

$$= \left\{\left\{-30\frac{re^{-r}}{-1} - 30\frac{e^{-r}}{-1}\right\}_0^2 - 30\left[e^{-r}\right]_0^2 - \left[r^2\right]_0^2\right\} 10\pi$$

$$= \left[30re^{-r} + 30e^{-r} - 30e^{-r} - r^2\right]_0^2 10\pi$$

$$= \left[60e^{-2} - 2^2\right] \times 10\pi = 129.437$$

$\therefore \oint_V (\nabla \cdot \vec{A})\, dv = 129.437$ = RHS of divergence theorem.

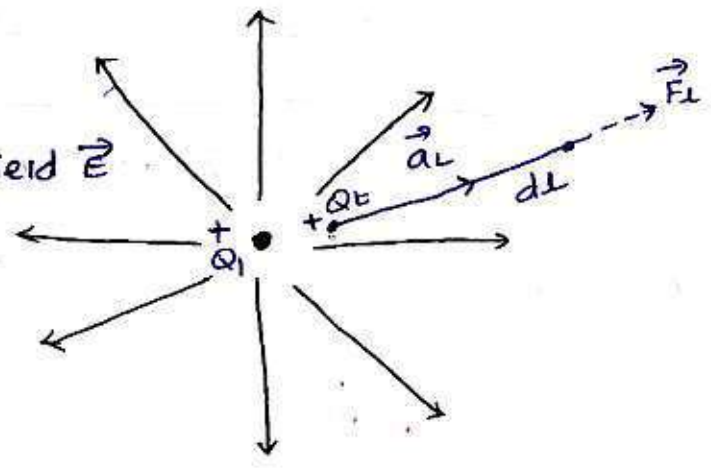
ELECTRIC POTENTIAL:

Consider an Electric field due to a Positive charge Q. If a unit test Positive charge Q_t is Placed at any Point in this field, it experiences a repulsive force and tends to move in the direction of force.

But if a Positive test charge Q_t is to be moved towards the Positive base charge Q then it is required to be moved against the electric field of charge Q i.e. against the repulsive force exerted by charge Q on the test charge Q_t.

While doing so, an external source has to do work to move the test charge Q_t against the electric field. This work done becomes the potential energy of the test charge Q_t, at the Point at which it is moved.

Consider a Positive charge Q_1 and its electric field $\vec{E}$. If a Positive test charge Q_t is Placed in this field, it will move due to force of repulsion. Let the movement of the charge Q_t is dl. The direction in which the movement has taken place is denoted by unit vector $\vec{a}_L$, in the direction of dl. This is shown in figure



According to coulomb's law the force exerted by the field $\vec{E}$ is given by,

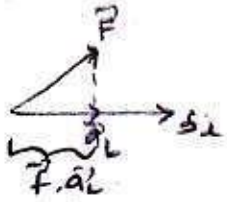
$$\vec{F} = Q_t \vec{E} \quad N.$$

But the component of this force exerted by the field in the direction of dl, is responsible to move the charge Q_t, thro' the distance dl.

W.K.T the component of a vector in the direction of the unit vector is the dot product of the vector with that unit vector. Thus the component of $\vec{F}$ in the direction of unit vector $\vec{a}_L$ is given by,

$$\vec{F}_L = \vec{F} \cdot \vec{a}_L \quad \text{sub (1) in (2)}$$

$$\vec{F}_L = Q_t \vec{E} \cdot \vec{a}_L \ \text{N} \quad \text{---- (2)}$$



This is the force responsible to move the charge Q_t thro' the distance dl, in the direction of the field.

To keep the charge in Equilibrium, it is necessary to apply the force which is equal and opposite to the force exerted by the field in the direction dl.

$$\therefore \quad F_{applied} = -\vec{F}_L = -Q_t \vec{E} \cdot \vec{a}_L \ \text{N} \quad \text{--- (3)}$$

In this case, work is said to be done.

Mathematically the differential work done by an external source in moving the charge Q_t, through a distance dl, against the direction of field $\vec{E}$ is given by,

$$dW = \vec{F}_{applied} \times dl \qquad [\text{work done} = \text{force} \times \text{distance}]$$

$$= -Q_t \vec{E} \cdot \vec{a}_L \, dl$$

But $dl\,\vec{a}_L = \vec{dL}$ = distance vector

$$dW = -Q_t \vec{E} \cdot \vec{dL} \ \text{J}$$

Scalar quantity.

Thus if a charge Q is moved from initial position to final position, against the direction of electric field $\vec{E}$ then the total work done is obtained by integrating the differential work done over the distance from initial position to the final position.

$$\therefore W = \int_{\text{Initial}}^{\text{final}} dW = \int_{\text{initial}}^{\text{final}} -Q\vec{E}\cdot\vec{dL}$$

$$\boxed{W = -Q\int_{\text{initial}}^{\text{final}} \vec{E}\cdot\vec{dL}\ \text{J}}$$

This work done is measured in Joules.

† THE LINE INTEGRAL:

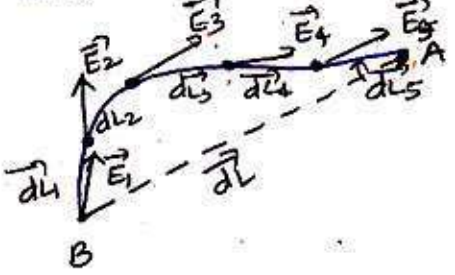
Consider that the charge is moved from initial position B to the final position A, against the electric field $\vec{E}$ then the work done is given by,

$$W = -Q\int_{B}^{A} \vec{E}\cdot\vec{dL}$$

This is called the line integral, where $\vec{E}\cdot\vec{dL}$ is the component of $\vec{E}$ along the direction $\vec{dL}$.

The line integral is basically a summation and accurate result is obtained when the number of segments becomes infinite.

Consider an uniform electric field $\vec{E}$. The charge is moved from B to A along the path shown in figure.

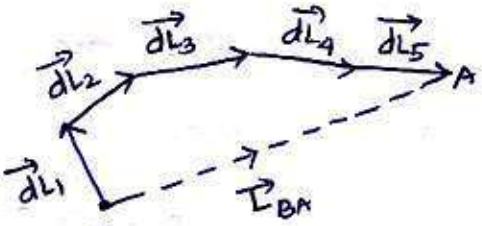


The path B to A is divided into number of small segments.

The various distance vectors along the segments choosen are $\vec{dL_1}$, $\vec{dL_2}$, $\vec{dL_3}$, $\vec{dL_4}$ and $\vec{dL_5}$ while Electric field in these directions is $\vec{E_1}$, $\vec{E_2}$, $\vec{E_3}$, $\vec{E_4}$ & $\vec{E_5}$. Hence the line integral from B to A can be expressed as summation of dot Products.

$$W = -Q\left[\vec{E_1}\cdot\vec{dL_1} + \vec{E_2}\cdot\vec{dL_2} + \cdots + \vec{E_5}\cdot\vec{dL_5}\right] \quad \text{---①}$$

But the electric field is uniform and equal in all the directions.



$$\therefore \vec{E_1} = \vec{E_2} = \vec{E_3} = \vec{E_4} = \vec{E_5} = \vec{E} \quad \text{---②}$$

sub ② in ① leads to

$$\therefore W = -Q\vec{E}\cdot\left[\vec{dL_1} + \vec{dL_2} + \vec{dL_3} + \cdots + \vec{dL_5}\right] \quad \text{---③}$$

Now $\vec{dL_1} + \vec{dL_2} + \cdots + \vec{dL_5}$ is vector addition.

Is $\vec{dL_1} + \vec{dL_2} + \cdots + \vec{dL_5} = \vec{L}_{BA}$ Then

$$\boxed{W = -Q\vec{E}\cdot\vec{L}_{BA}}$$

Thus it can be seen that vector sum of small segments choosen along any path, a curve or a straight line remains same as $\vec{L}_{BA}$ and it depends on initial and final point only.

Thus, the work done in moving a charge from one location B to another A, in a static, uniform or nonuniform electric field $\vec{E}$ is independent of the path selected.

$$\begin{cases} \vec{dL} = dx\,\vec{a_x} + dy\,\vec{a_y} + dz\,\vec{a_z} & \text{[cartesian system]} \\ \vec{dL} = dr\,\vec{a_r} + r\,d\phi\,\vec{a_\phi} + dz\,\vec{a_z} & \text{[cylindrical]} \\ \vec{dL} = dr\,\vec{a_r} + r\,d\theta\,\vec{a_\theta} + r\sin\theta\,d\phi\,\vec{a_\phi} & \text{[Spherical]} \end{cases}$$

POTENTIAL DIFFERENCE:

The work done in moving a point charge Q from point B to A in the electric field $\vec{E}$ is given by,

$$W = -Q \int_B^A \vec{E} \cdot \vec{dL} \quad ---(1)$$

If the charge Q is selected as unit test charge then from the above equation we get the work done in moving unit charge from B to A in the field $\vec{E}$.

This work done in moving unit charge from point B to A in the field $\vec{E}$ is called Potential difference, b/w the points B to A. It is denoted as V

$$\therefore V = -\int_B^A \vec{E} \cdot \vec{dL} \quad ---(2)$$

Thus work done per unit charge in moving unit charge from B to A in the field $\vec{E}$ is called potential difference b/w the points B and A.

$$V_{AB} = -\int_B^A \vec{E} \cdot \vec{dL}$$

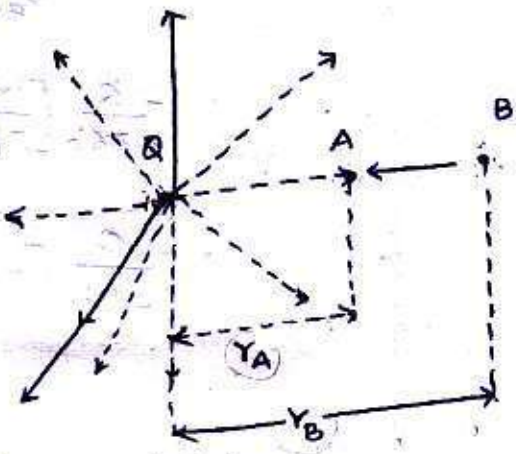
Potential difference is work done per unit charge unit is (J/c)

one volt Potential difference is one Jouie of work done in moving unit charge from one point to other in the field $\vec{E}$

$$\therefore 1 \text{ Volt} = \frac{1 \text{ Joule}}{1 \text{ coulomb}}.$$

POTENTIAL DUE TO POINT CHARGE:

consider a point charge, located at the origin of a spherical co-ordinate system, producing $\vec{E}$ radially in all the directions as shown in figure.



Assuming free space, the field $\vec{E}$ due to a point charge Q at a point having radial distance r from the origin is given by

$$\vec{E} = \frac{Q}{4\pi\epsilon_0 r^2}\,\vec{a}_r \quad \text{---- (1)}$$

consider a unit charge which is placed at a point B which is at a radial distance of r_B from the origin. It is moved against the direction of $\vec{E}$ from point B to point A. The point A is at a radial distance of r_A from the origin.

The differential length in spherical system is

$$\vec{dL} = dr\,\vec{a}_r + r\,d\theta\,\vec{a}_\theta + r\sin\theta\,d\phi\,\vec{a}_\phi$$

Hence potential difference V_{AB} between points A and B is given by

$$V_{AB} = -\int_B^A \vec{E}\cdot\vec{dL} \qquad \text{Here } B = r_B,\ A = r_A$$

$$\therefore V_{AB} = -\int_{r_B}^{r_A} \vec{E}\cdot\vec{dL}$$

$$= -\int_{r_B}^{r_A} \left(\frac{Q}{4\pi\epsilon_0 r^2}\,\vec{a}_r\right)\cdot\left(dr\,\vec{a}_r + r\,d\theta\,\vec{a}_\theta + r\sin\theta\,d\phi\,\vec{a}_\phi\right)$$

$$V_{AB} = -\int_{r_B}^{r_A} \frac{Q}{4\pi\epsilon_0 r^2}\, dr$$

$$= \frac{-Q}{4\pi\epsilon_0} \int_{r_B}^{r_A} r^{-2}\, dr$$

$$= \frac{-Q}{4\pi\epsilon_0} \left[\frac{r^{-1}}{-1}\right]_{r_B}^{r_A}$$

$$= -\frac{Q}{4\pi\epsilon_0}\left[-\frac{1}{r}\right]_{r_B}^{r_A} \Rightarrow -\frac{Q}{4\pi\epsilon_0}\left[-\frac{1}{r_A} - \left(-\frac{1}{r_B}\right)\right]$$

$$\Rightarrow -\frac{Q}{4\pi\epsilon_0}\left[-\frac{1}{r_A} + \frac{1}{r_B}\right]$$

$$\boxed{V_{AB} = +\frac{Q}{4\pi\epsilon_0}\left[\frac{1}{r_A} - \frac{1}{r_B}\right] V}$$

When $r_B > r_A$, $\frac{1}{r_B} < \frac{1}{r_A}$ and V_{AB} is +ve. This indicates work is done by external source in moving unit charge from B to A.

CONCEPT OF ABSOLUTE POTENTIAL:

Instead of potential difference, it is more convenient to express absolute potentials ~~at~~ of various points in the field. such absolute potentials are measured w.r.to a specified reference position. such reference position is assumed to be at zero potential.

For Practical circuits, zero reference point is selected as ground.

Consider potential ~~dif~~ difference V_{AB} due to movement of unit charge from B to A. in to a field of a point charge Q. It is given by

$$V_{AB} = \frac{Q}{4\pi\epsilon_0}\left[\frac{1}{r_A} - \frac{1}{r_B}\right] \text{---} (A)$$

Now let the charge is moved from infinity to the Point A i.e, $r_B = \infty$. Hence $\frac{1}{r_B} = \frac{1}{\infty} = 0$.

$$\therefore V_{AB} = \frac{Q}{4\pi\epsilon_0}\left[\frac{1}{r_A} - \frac{1}{\infty}\right] = \frac{Q}{4\pi\epsilon_0 r_A} \quad \text{--- (B)}$$

The quantity represented in eqn (B) is called potential of Point A denoted as V_A.

$$\therefore \boxed{V_A = \frac{Q}{4\pi\epsilon_0 r_A} \text{ V}}$$ → This is also called absolute potential of Point A.

Similarly absolute potential of Point B can be defined as

$$\boxed{V_B = \frac{Q}{4\pi\epsilon_0 r_B} \text{ V}}$$

This is work done in moving unit charge from ∞ at Point B.

Hence the potential difference can be expressed as the difference b/w the absolute potentials of the two points.

$$\therefore \boxed{V_{AB} = V_A - V_B \text{ V}}$$

POTENTIAL DUE TO POINT CHARGE NOT AT ORIGIN:

If the point charge Q is not located at the origin of a spherical system then obtain the position vector r' of the point where Q is located.

Then absolute potential at a point A located at a distance r from the origin is given by,

$$V(r) = V_A = \frac{Q}{4\pi\epsilon_0 |r - r'|}$$

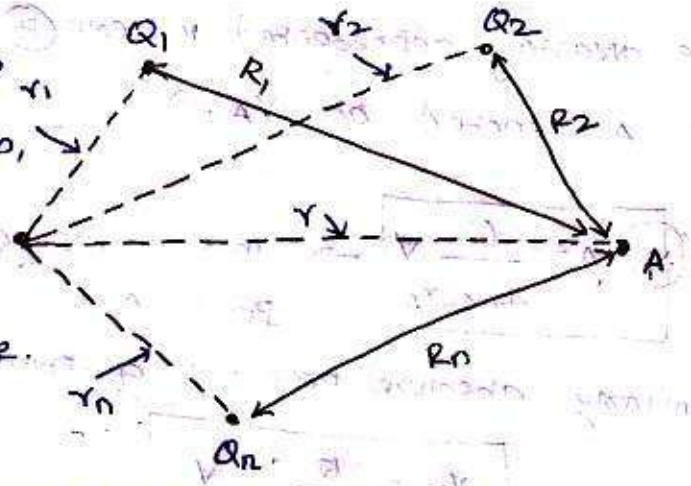
$$= \frac{Q}{4\pi\epsilon_0 R_A}$$

where R_A is the distance b/w Point at which potential is to be calculated and the location of the charge.

POTENTIAL DUE TO SEVERAL POINT CHARGES:

Consider the various point charges $Q_1, Q_2, \ldots, Q_n$ located at the distance of $r_1, r_2, \ldots, r_n$ from the origin as shown in the figure.

The Potential due to all these point charges, at point A is to be determined. Use superposition principle.



Consider the point charge Q_1

The Potential V_{A1} due to Q_1 is given by

$$V_{A1} = \frac{Q_1}{4\pi\epsilon_0 |r - r_1|} = \frac{Q_1}{4\pi\epsilon_0 R_1} V$$

where $R_1 = |r - r_1|$ = Distance b/w point A and Position of Q_1.

The Potential V_{A2} due to Q_2 is given by

$$V_{A2} = \frac{Q_2}{4\pi\epsilon_0 |r - r_2|} = \frac{Q_2}{4\pi\epsilon_0 R_2} V$$

Thus Potential V_{An} due to Q_n is given by

$$V_{An} = \frac{Q_n}{4\pi\epsilon_0 |r - r_n|} = \frac{Q_n}{4\pi\epsilon_0 R_n} V.$$

The net Potential at Point A is the algebraic sum of the Potentials at A due to individual Point charges is

$$V_A = V_{A1} + V_{A2} + \cdots + V_{An} = \frac{Q_1}{4\pi\epsilon_0 R_1} + \frac{Q_2}{4\pi\epsilon_0 R_2} + \cdots + \frac{Q_n}{4\pi\epsilon_0 R_n}$$

$$= \sum_{m=1}^{n} \frac{Q_m}{4\pi\epsilon_0 |r - r_m|} = \sum_{m=1}^{n} \frac{Q_m}{4\pi\epsilon_0 R_m} V.$$

Problems:

1. A point charge $Q = 0.4nC$ is located at the origin. obtain the absolute potential of $A(2,2,3)$.

SOLUTION:

The potential of A due to point charge Q at the origin is given by

$$V_A = \frac{Q}{4\pi\epsilon_0 R_A} \quad \text{and} \quad A(2,2,3),\ Q \text{ at } (0,0,0)$$

$$\therefore R_A = \sqrt{(2-0)^2 + (2-0)^2 + (3-0)^2} = \sqrt{17}$$

$$V_A = \frac{0.4 \times 10^{-9}}{4\pi \times 8.854 \times 10^{-12} \times \sqrt{17}} = 0.8179\ V.$$

2. If the same charge $Q = 0.4nC$ in the above example is located at $(2,3,3)$ then obtain the absolute Potential of point $A(2,2,3)$.

SOLUTION:

Now Q is located at $(2,3,3)$.

$$\therefore V_A = \frac{Q}{4\pi\epsilon_0 |r - r'|}, \quad = \frac{Q}{4\pi\epsilon_0 R_A}$$

$$R_A = \sqrt{(2-2)^2 + (2-3)^2 + (3-3)^2} = 1$$

$$\therefore V_A = \frac{0.4 \times 10^{-9}}{4\pi \times 8.854 \times 10^{-12}} = 3.595\ V.$$

EQUIPOTENTIAL SURFACES:

In an electric field, there are many points at which the electric potential is same. This is bcoz, the potential is a scalar quantity which depends on the distance b/w the point at which potential is to be obtained and location of the charge.

All such points are at the same electric potential. If a surface is imagined, joining all such points which are at the same potential, then such a surface is called Equipotential surface.

CONSERVATIVE FIELD:

The work done in moving a test charge around any closed path in a static field $\vec{E}$ is zero. This is because starting and terminating point is same for a closed path. Hence upper and lower limit of integration becomes same. Hence the work done becomes zero. such an integral over a closed path is denoted as

$$\oint_{\text{closed path}} \vec{E} \cdot \vec{dL} = 0 \longrightarrow \text{conservative field (or) lamellar field.}$$

POTENTIAL GRADIENT:

Hence an inverse relation namely the change of Potential ΔV, along the elementary length ΔL must be related to $\vec{E}$, as $\Delta L \to 0$

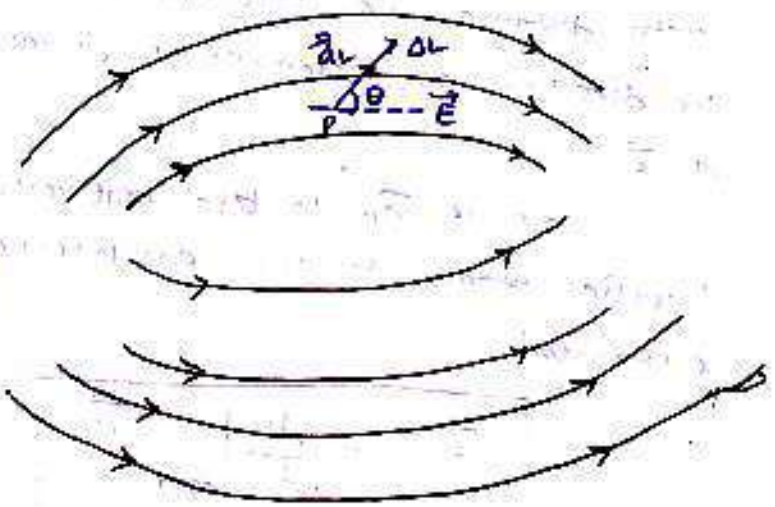
(*) [The rate of change of Potential with respect to the distance is called Potential gradient]

$$\frac{dV}{dL} = \lim_{\Delta L \to 0} \frac{\Delta V}{\Delta L} = \text{Potential gradient}$$

RELATIONSHIP BETWEEN $\vec{E}$ and V

Consider $\vec{E}$ due to a particular charge distributions in space. The Electric field $\vec{E}$ and potential V is changing from point to point in space.

Consider a vector incremental length $\vec{\Delta L}$ making an angle θ W.r.t the direction $\vec{E}$ as shown in figure.



To find incremental Potential we use

$$\Delta V = -\vec{E} \cdot \vec{\Delta L} \quad --①$$

$$\vec{\Delta L} = \Delta L \, \vec{a}_L \quad ---②$$

① ⇒

$$\Delta V = -\vec{E} \cdot \vec{\Delta L}$$

$$= -E \, \Delta L \cos\theta$$

$$\frac{\Delta V}{\Delta L} = -E \cos\theta$$

To find ΔV at a point, take $\lim \Delta L \to 0$

$$\therefore \lim_{\Delta L \to 0} \frac{\Delta V}{\Delta L} = -E \cos\theta$$

But $\lim_{\Delta L \to 0} \frac{\Delta V}{\Delta L} = \frac{dV}{dL}$ = Potential Gradient

$$\therefore \frac{dV}{dL} = -E\cos\theta$$

Hence the Potential gradient $\frac{dV}{dL}$ can be maximum only when $\cos\theta = -1$ i.e. $\theta = +180^\circ$.

This indicates that ΔL must be in the direction opposite to $\vec{E}$

$$\therefore \left.\frac{dV}{dL}\right|_{\substack{max \\ \theta=180}} = E$$

Thus the above eavations shows that,

1. Maximum valve of Potential gradient gives the magnitude of the electric field intensity $\vec{E}$.

2. The maximum valve of rate of change of potential with distance. i.e Potential gradient is possible only when the direction of increment in distance is opposite to the direction of $\vec{E}$.

Thus if $\vec{a}_n$ is the unit vector in the direction of increasing Potential normal to the equipotential surface then $\vec{E}$ can be expressed.

$$\vec{E} = -\left.\frac{dV}{dL}\right|_{max} \vec{a}_n$$

As $\vec{E}$ and Potential gradient are in opposite direction, above equation has -ve sign.

The maximum valve of rate of change of Potential with distance (dV/dL) is called gradient of V.

mathematically

$$\text{Gradient of } V = \text{grad } V = \nabla V$$

$$\therefore \vec{E} = -\nabla V$$

The gradV in various co-ordinates are given as

1. Cartesian $\nabla V = \frac{\partial V}{\partial x}\vec{a}_x + \frac{\partial V}{\partial y}\vec{a}_y + \frac{\partial V}{\partial z}\vec{a}_z$

2. cylindrical $\nabla V = \frac{\partial V}{\partial r}\vec{a}_r + \frac{1}{r}\frac{\partial V}{\partial \phi}\vec{a}_\phi + \frac{\partial V}{\partial z}\vec{a}_z$

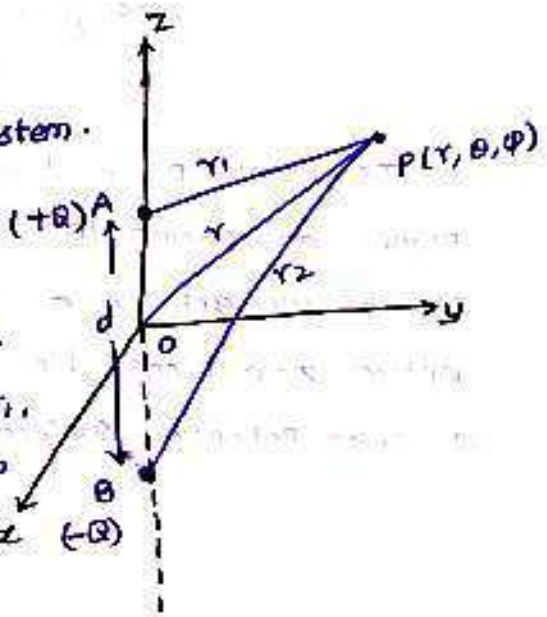
3. spherical $\nabla V = \frac{\partial V}{\partial r}\vec{a}_r + \frac{1}{r}\frac{\partial V}{\partial \theta}\vec{a}_\theta + \frac{1}{r\sin\theta}\frac{\partial V}{\partial \phi}\vec{a}_\phi$

AN ELECTRIC DIPOLE:

Two point charges of equal magnitude but opposite sign, seperated by a very small distance gives rise to an ELECTRIC DIPOLE.

The field produced by such a dipole plays an important role in the engineering electromagnetics.

Consider an Electric dipole as shown in the figure. The two point charges $+Q$ and $-Q$ are seperated by a very small distance d.



consider an ~~electric~~ point 'P' $P(r, \theta, \phi)$ in spherical co-ordinate system. It is required to find $\vec{E}$ due to an electric dipole at point P. Let 'O' be the midpoint of AB. The distance of point P from A is r_1, while distance of point P from B is r_2. The distance of point P from O is r.

The distance of seperation of charges is d, it is very small compared to r_1, r_2 and r.

The co-ordinates of A is $(0, 0, +\frac{d}{2})$ and $B(0, 0, -\frac{d}{2})$.

TO Find $\vec{E}$, we will find out the Potential V at Point P, due to an electric dipole. Then using $\vec{E} = -\nabla V$, we can find $\vec{E}$ due to an electric dipole.

EXPRESSION OF $\vec{E}$ DUE TO AN ELECTRIC DIPOLE:

In spherical co-ordinates, the potential at point P due to the charge $+Q$ is given by,

$$V_1 = \frac{+Q}{4\pi\epsilon_0 r_1} \quad \text{---} (1)$$

The potential at P due to the charge $-Q$ is given by

$$V_2 = \frac{-Q}{4\pi\epsilon_0 r_2} \quad \text{----} (2)$$

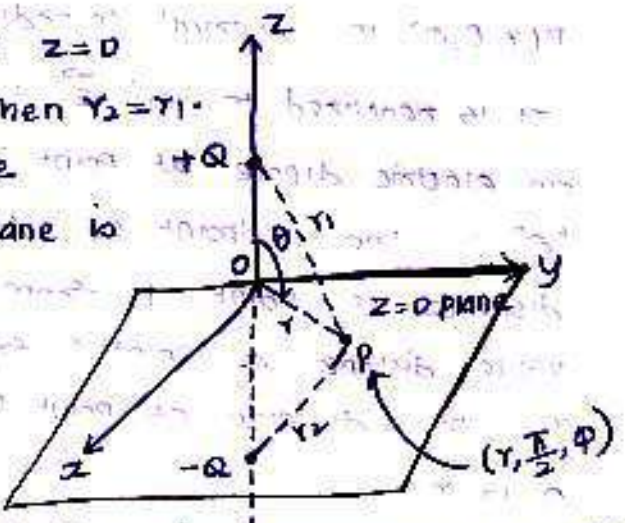
The total potential at point P is the algebraic sum of V_1 and V_2

$$\therefore V = V_1 + V_2$$

$$= \frac{+Q}{4\pi\epsilon_0 r_1} - \frac{Q}{4\pi\epsilon_0 r_2}$$

$$\therefore V = \frac{Q}{4\pi\epsilon_0}\left[\frac{1}{r_1} - \frac{1}{r_2}\right] = \frac{Q}{4\pi\epsilon_0}\left[\frac{r_2 - r_1}{r_1 r_2}\right] \quad \text{---} (3)$$

If Point P is located in $z=0$ Plane as shown in figure, Then $r_2 = r_1$. Hence we get $V=0$. Thus the entire $z=0$ plane i.e xy plane is a zero Potential surface.

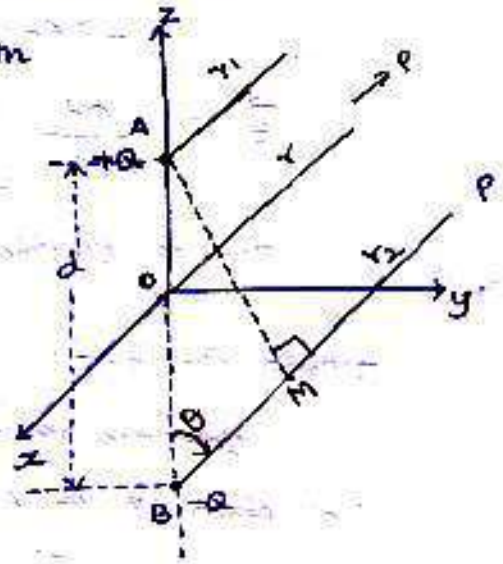


Now consider that P is located far away from the electric dipole. Thus r_1, r_2 and r can be assumed to be $\parallel^{el}$ to each other as shown in figure (b).

$\theta = \pi/2$, $z=0$ Plane.

AM is drawn $\perp^r$ from A on r_2.

The angle made by r_1, r_2 and r with Z axis is θ on all are $\parallel^{el}$.



$\therefore$ BM = AB cosθ

= d cosθ ---- (4)

PB = PM + BM

and PA = PM as AM is $\perp^r$

$PB = r_2$ $PA = r_1$

$\therefore$ BM = PB − PM

$BM = r_2 - r_1$ --- (5)

(4) = (5) $\therefore$ $r_2 - r_1 = d\cos\theta$ } --- (6)

As d is very small, $r_1 \neq r_2 \approx r$ hence $r_1 r_2 = r^2$

Sub (5) in (3) we get

$$V = \frac{Q}{4\pi\epsilon_0}\left[\frac{d\cos\theta}{r^2}\right] \text{ Volts} \quad \text{---- (A)}$$

NOW $\vec{E} = -\nabla V = -\left[\frac{\partial V}{\partial r}\vec{a}_r + \frac{1}{r}\frac{\partial V}{\partial \theta}\vec{a}_\theta + \frac{1}{r\sin\theta}\frac{\partial V}{\partial \phi}\vec{a}_\phi\right]$

$$\frac{\partial V}{\partial r} = \frac{\partial}{\partial r}\left[\frac{Qd\cos\theta}{4\pi\epsilon_0 r^2}\right] = \frac{Qd\cos\theta}{4\pi\epsilon_0}\frac{\partial}{\partial r}\left(\frac{1}{r^2}\right)$$

$$= \frac{Qd\cos\theta}{4\pi\epsilon_0}\frac{\partial}{\partial r}(r^{-2})$$

$$\frac{\partial V}{\partial r} = -\frac{2Qd\cos\theta}{4\pi\epsilon_0} r^{-3} \Rightarrow -\frac{2Qd\cos\theta}{4\pi\epsilon_0 r^3}$$

$$\frac{\partial V}{\partial \theta} = \frac{Qd}{4\pi\epsilon_0 r^2}[-\sin\theta] \qquad \frac{\partial V}{\partial \phi} = 0$$

$$\therefore \vec{E} = -\left[\frac{-2Qd\cos\theta}{4\pi\epsilon_0 r^3}\vec{a}_r - \frac{Qd\sin\theta}{4\pi\epsilon_0 r^3}\vec{a}_\theta\right]$$

$$\vec{E} = \frac{2Qd\cos\theta}{4\pi\epsilon_0 r^3}\vec{a}_r + \frac{Qd\sin\theta}{4\pi\epsilon_0 r^3}\vec{a}_\theta$$

$$\vec{E} = \frac{Qd}{4\pi\epsilon_0 r^3}\left[2\cos\theta\,\vec{a}_r + \sin\theta\,\vec{a}_\theta\right]$$

This is Electric field $\vec{E}$ at Point P due to an electric dipole.

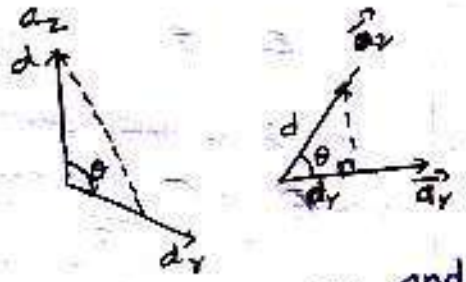
DIPOLE MOMENT:

Let the vector length directed from $-Q$ to $+Q$ i.e from B to A is $\vec{d}$

$$\therefore \vec{d} = d\vec{a}_z \quad ---(1)$$

Its component along $\vec{a}_r$ direction can be obtained as,

$$d_r = \vec{d}\cdot\vec{a}_r \quad ---(2)$$



sub (1) in (2) we get

$$d_r = d\vec{a}_z \cdot \vec{a}_r = d\cos\theta$$

$$\therefore \vec{d} = d\cos\theta\,\vec{a}_r$$

Then the Product of $Q\vec{d}$ is called dipole moment and denoted as $\vec{P}$

$$\therefore \vec{P} = Q\vec{d}$$

The dipole moment is measured in Cm (Coulomb-meter).

Now $\vec{P}\cdot\vec{a}_r = Q\vec{d}\cdot\vec{a}_r = Qd\cos\theta$

Hence the expression of potential V can be expressed as

$$V = \frac{Qd\cos\theta}{4\pi\epsilon_0 r^2} = \frac{\vec{P}\cdot\vec{a}_r}{4\pi\epsilon_0 r^2}\ V$$

from Equation (A) of Page No (43).

Note:

$\vec{a}_r$ is the unit vector in the direction of distance vector joining the point at which moment exists and point at which V is to be obtained. $= \frac{\vec{r}}{|\vec{r}|}$ $\vec{r}$ = vector joining point of dipole moment to P.

Problem

A dipole having moment $\vec{P} = 3\vec{a}_x - 5\vec{a}_y + 10\vec{a}_z$ nCm is located at Q(1,3,-4) in free space. Find V at P(2,3,4)

Solution:

The Potential V in terms of dipole moment is

$$V = \frac{\vec{P} \cdot \vec{a}_r}{4\pi\epsilon_0 r^2}$$

Q(1,2,-4) and P(2,3,4)

$$\vec{r} = (2-1)\vec{a}_x + (3-2)\vec{a}_y + (4-(-4))\vec{a}_z$$

$$= \vec{a}_x + \vec{a}_y + 8\vec{a}_z$$

$$|\vec{r}| = \sqrt{1+1+64} = \sqrt{66}$$

$$\therefore \vec{a}_r = \frac{\vec{r}}{|\vec{r}|} = \frac{\vec{a}_x + \vec{a}_y + 8\vec{a}_z}{\sqrt{66}}$$

$$\vec{P} \cdot \vec{a}_r = (3\vec{a}_x - 5\vec{a}_y + 10\vec{a}_z) \cdot \left(\frac{\vec{a}_x + \vec{a}_y + 8\vec{a}_z}{\sqrt{66}}\right)$$

$$= \frac{3-5+80}{\sqrt{66}} = \frac{78}{\sqrt{66}} \times 10^{-9} \text{ as } \vec{P} \text{ is in nCm.}$$

$$V = \frac{\vec{P} \cdot \vec{a}_r}{4\pi\epsilon_0 r^2} = \frac{(78/\sqrt{66}) \times 10^{-9}}{4\pi \times 8.854 \times 10^{-12} \times (\sqrt{66})^2} = 1.3074 \text{ V.}$$

UNIT-III

CONDUCTORS, DIELECTRICS AND CAPACITORS

CURRENT:

- Flow of charges constitutes an Electric current
- It can be measured by measuring how many charges are passing thro' a specified surface or a point in a material per second.
- It is rate of flow of charge at a specified point or across a specified surface per unit time is called an Electric current.
- It is measured in Ampere, which is coulombs/sec (C/s).

i.e. $$I = \frac{dQ}{dt} \text{ C/s i.e Amps}$$

A current of 1 AMP is said to be flowing across the surface when a charge of one coulomb is passing across the surface in one second.

CURRENT DENSITY:

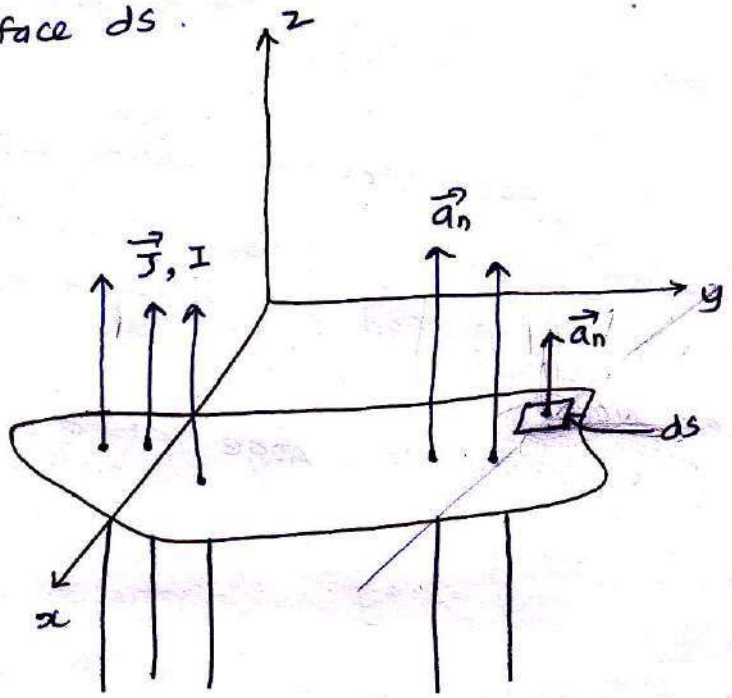
It is defined as the current passing thro' the unit surface area, when the surface is held normal to direction of the current.

- It is a vector quantity and denoted as $\vec{J}$.
- It is measured in Amperes per sq. meters (A/m^2).

RELATIONSHIP BETWEEN I AND J:

Consider a surface S and I is the current passing thro' the surface. The direction of current is normal to the surface S and hence direction of $\vec{J}$ is also normal to the surface S.

Consider an incremental area ds as shown in fig below and $\vec{a}_n$ is the unit vector normal to the incremental surface ds.



A/m^2 m_2

$I = J \times S$

$dI = \vec{J} \cdot \vec{ds}$

$\vec{ds} = ds\, \vec{a}_n$

$\vec{J} = J\, \vec{a}_n$

Then the differential current dI passing thro' the differential surface ds is given by the dot product of the current density vector $\vec{J}$ and $\vec{ds}$

$\therefore \quad dI = \vec{J} \cdot \vec{ds}$ [dot Product]

When $\vec{J}$ and $\vec{ds}$ are at right angles ($\theta = 90^\circ$) then

$dI = \vec{J} \cdot \vec{ds} = |\vec{J}|\,|\vec{ds}| \cos 0^\circ$

$$\boxed{dI = J\, ds}$$

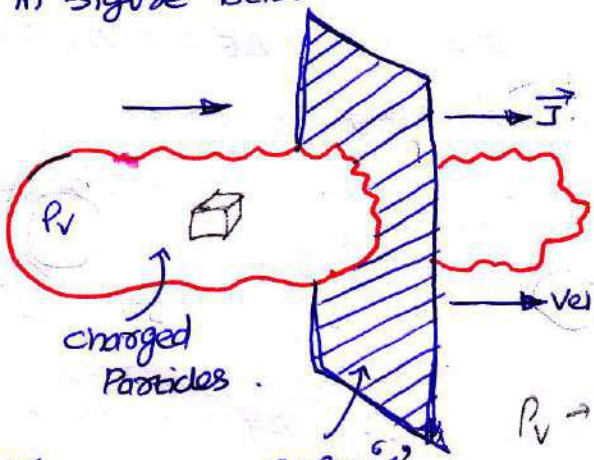
and $I = \oint_S J \cdot ds$. $J \rightarrow$ current density in A/m^2

But if $\vec{J}$ is not normal to $\vec{ds}$ then the total current is obtained by integrating $\vec{J} \cdot \vec{ds}$

$$\boxed{I = \oint_S \vec{J} \cdot \vec{ds}}$$

RELATION BETWEEN $\vec{J}$ & ρ_v

The set of charged particles give rise to a charge density ρ_v in a volume V. The current density $\vec{J}$ can be related to the velocity with the volume charge density. i.e charged particles in volume V. crossed the surface S at a point. This is shown in figure below



The velocity with which the charge is getting transferred is $\vec{v}$ m/s. This is a vector quantity.

To derive the relation between $\vec{J}$ and ρ_v, consider differential volume Δv having charge density ρ_v as show in figure below. The elementary charge that volume carries is,

$$\Delta Q = \rho_v \Delta V \quad \text{---} (1)$$

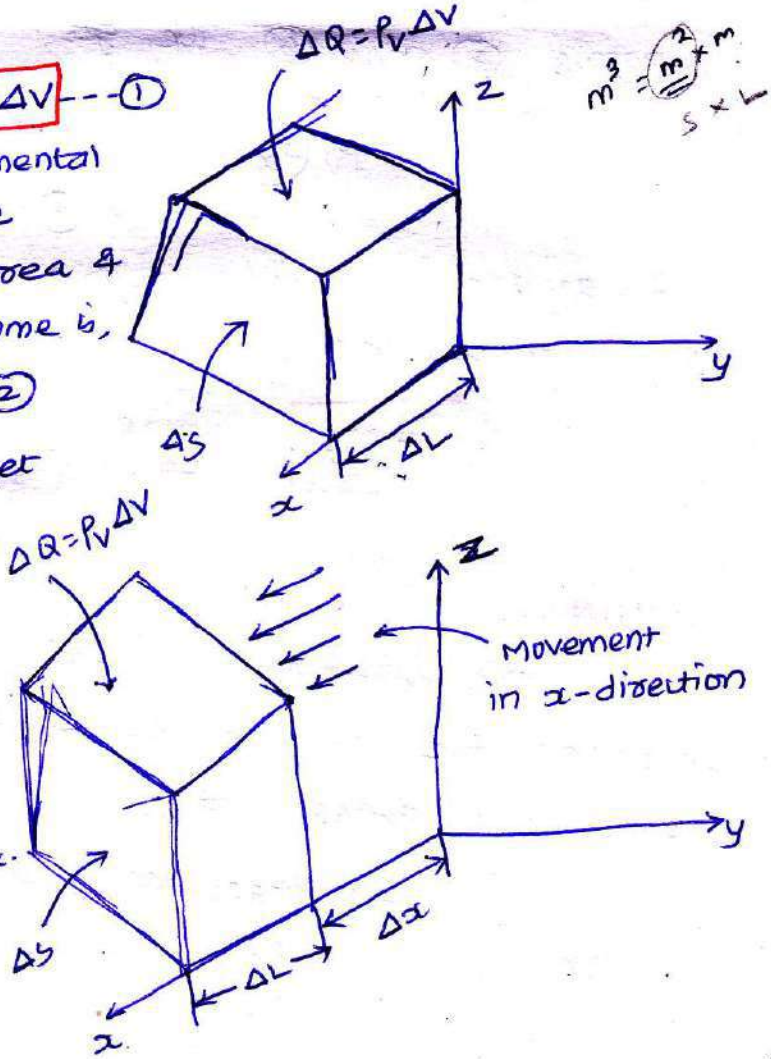
Let ΔL is the incremental length while Δs is the incremental surface area & hence incremental volume is,

$$\Delta V = \Delta s \, \Delta L \quad \text{---} (2)$$

$\therefore$ sub (2) in (1) we set

$$\Delta Q = \rho_v \Delta s \, \Delta L \quad \text{---} (3)$$

Let the charge is moving in x-direction with velocity $\vec{v}$ and thus velocity has only x component v_x.



In the time interval Δt the element of charge has moved through distance Δx, in x direction. The direction is normal to the surface ΔS and hence the resultant current can be expressed as,

$$\Delta I = \frac{\Delta Q}{\Delta t} \quad \text{---} (4)$$

But now, $\Delta Q = \rho_v \Delta S \Delta x$ as the charge corresponding the length Δx is moved and responsible for the current.

$$\therefore \quad \Delta I = \rho_v \Delta S \frac{\Delta x}{\Delta t} \quad \text{----} (5)$$

But $\frac{\Delta x}{\Delta t}$ = Velocity in x-direction i.e. v_x

$$\therefore \quad \Delta I = \rho_v \Delta S v_x \quad \text{---} (6)$$

$\hookrightarrow$ x component of velocity $\vec{v}$

But $\Delta I = \vec{J} \Delta S$ when $\vec{J}$ and ΔS are normal. $\quad \text{---} (7)$

Here $\vec{J}$ and ΔS are normal to each other hence comparing (7) and (6) we get

$$J_x = \rho_v (v_x) = x \text{ component of } \vec{J} \quad \text{------} (8)$$

In general, the relation ship between $\vec{J}$ and ρ_v can be expressed as

$$\vec{J} = \rho_v \vec{v}$$

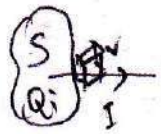
where $\vec{v}$ is the velocity vector.

CONTINUITY EQUATION:

The continuity equation of the current is based on the Principle of conservation of charge. The Principle states that.

The charges can neither be created nor be destroyed.

Consider a closed surface S with a current density $\vec{J}$, then the total current I crossing the surface S is given by,



$$I = \oint_S \vec{J} \cdot \vec{ds} \quad ---(1)$$

- The current flows outwards from the closed surface.
- The current means the flow of positive charges.
- The current I is constituted due to outward flow of +ve charge from the closed surface S.
- According to Principle of conservation of charge, there must be decrease of an equal amount of +ve charge inside the closed surface.
- Hence the outward rate of flow of +ve charge gets balanced by the rate of decrease of charge inside the closed surface.

Let Q_i = charge within the closed surface

$-\frac{dQ_i}{dt}$ = Rate of decrease of charge inside the closed surface.

The Negative sign indicates decrease in charge.

Due to principle of conservation of charge, this rate of decrease is same as rate of outward flow of charge, which is current

$$\therefore I = \oint_S \vec{J} \cdot \vec{ds} = -\frac{dQ_i}{dt} \quad ---(2)$$ [outward flowing current I].

This is the integral form of the continuity equation of the current.

Current entering the volume is

$$\oint_S \vec{J} \cdot \vec{ds} = -I = \frac{dQ_i}{dt} \quad ---(3)$$

The Point form of the continuity equation can be obtained from the integral form.

using divergence theorem, convert the surface integral in integral form to the volume integral.

$$\left[\oint_S \vec{D}.d\vec{s} = \int_{Vol}(\nabla.\vec{D})dV\right] \quad \therefore \quad \oint_S \vec{J}.d\vec{s} = \int_{Vol}(\nabla.\vec{J})dV \quad ----(4)$$

$$\therefore \quad -\frac{dQ_i}{dt} = \int_{Vol}(\nabla.\vec{J})dV$$

But $Q_i = \int_{Vol} \rho_v\, dV$ where $\rho_v \rightarrow$ volume charge density.

$$\therefore \int_{Vol}(\nabla.\vec{J})dV = -\frac{d}{dt}\left[\int_{Vol}\rho_v\, dV\right] = -\int_{Vol}\frac{d\rho_v}{\partial t}\,dV.$$

for constant surface derivative becomes partial derivative

$$\therefore \int_{Vol}(\nabla.\vec{J})dV = -\int_{Vol}\frac{\partial\rho_v}{\partial t}\,dV. \quad ---(5)$$

If the above relation is true for any volume, it must be true for incremental volume ΔV

$$\therefore (\nabla.\vec{J})\Delta V = -\frac{\partial\rho_v}{\partial t}\Delta V$$

$$\therefore \boxed{(\nabla.\vec{J}) = -\frac{\partial\rho_v}{\partial t}} \quad ---(6)$$

↳ Point form or differential form of continuity equation of the current.

For steady currents which are not the function of time $\frac{\partial\rho_v}{\partial t} = 0$ hence

$$(\nabla.\vec{J}) = 0. \text{ for steady state.}$$

CONDUCTORS :

under the effect of applied electric field, the available free electrons starts moving. The moving electrons strikes the adjacent atoms and rebound in the random directions. this is called drifting of electrons.

After some time, the electrons attain the constant average velocity called drift velocity (ϑ_d). The current constituted due to the drifting of such electrons in metallic conductors is called drift current.

The drift velocity is directly proportional to the applied electric field.

$$\vec{\vartheta}_d \propto \vec{E} \quad \text{---} (1)$$

The constant of proportionality is called mobility of the electrons in a given material and denoted as μ_e.

$$\vec{\vartheta}_d = -\mu_e \vec{E} \quad \text{---} (2)$$

-ve sign indicates the velocity of the electrons is against the direction of field $\vec{E}$. [$\mu = 0.0012$ for Al
$= 0.0032$ for W].

According to relation between $\vec{J}$ and $\vec{\vartheta}$ we can write,

$$\vec{J} = \rho_v \vec{\vartheta} \quad \text{---} (3)$$

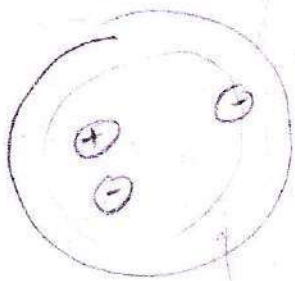
The drift velocity is the velocity of free electrons hence the above relation can be expressed as

$$\vec{J} = \rho_e \vec{\vartheta}_d \quad \text{---} (4)$$

where $\rho_e \rightarrow$ charge density due to free Electrons.

sub (2) in (4) we get

$$\boxed{\vec{J} = -\rho_e \mu_e \vec{E}} \quad \text{--} (5)$$



POINT FORM OF OHM'S LAW:

The relationship between $\vec{J}$ and $\vec{E}$ can also be expressed in terms of conductivity of the material.

Thus for a metallic conductor

$$\vec{J} = \sigma \vec{E} \quad ---(5)$$

σ - sigma

Where σ = conductivity of the material. (σ/m) (mho/metre)

Point form of ohm's law.

$\sigma = 3.82 \times 10^7$ for Al

$= 5.8 \times 10^7$ for Cu.

By comparing (5) and (6)

$$\sigma = -\rho_e N_e \quad ----(7)$$

$\rho_e = ne$

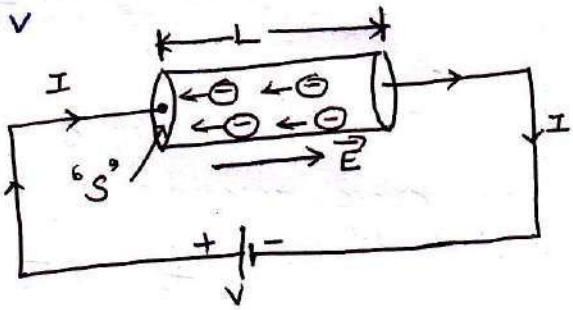
n - no. of electrons

e - charge per electron.

The resistivity is the reciprocal of the conductivity. The conductivity depends on the temperature. As temperature increases, the conductivity decreases and resistivity increases.

RESISTANCE OF A CONDUCTOR:-

Consider that the voltage V is applied to a conductor of length L having uniform cross section 'S' as shown in the figure.



The direction of $\vec{E}$ is same as the direction of conventional current, which is opposite to flow of electrons. The electric field applied is uniform and its magnitude is given by,

$$E = \frac{V}{L} \quad ---- (1)$$

The conductor has uniform cross-section s and hence we can write

$$I = \int_S \vec{J} \cdot \vec{ds} = J\,ds \quad ---(2)$$

The current direction is normal to the surface ds.

Thus $J = \frac{I}{S} = \sigma E$ --- ③

$J = \sigma E$

Sub ① in ③ we get

$E = V/L$

$E = V/L$

$J = \frac{\sigma V}{L}$ where σ = conductivity of the material

$J = \frac{\sigma V}{L}$

$V = \frac{JL}{\sigma} =$

$V = \frac{JL}{\sigma} \left(J = \frac{I}{S}\right)$

$= \frac{IL}{\sigma S}$ $\left[\because J = \frac{I}{S}\right]$

$V = \frac{IL}{\sigma S}$

$V = \left(\frac{L}{\sigma S}\right) I$

$V = \left(\frac{L}{\sigma S}\right) J$

$\therefore R = \frac{V}{I} = \frac{L}{\sigma S}$

$R = \frac{1}{T}$

For nonuniform fields, the resistance R is defined as the ratio V to I where V is the potential difference b/w two specified equipotential surfaces in the material and I is the current crossing the more positive surface of the two, into the material.

$$\therefore R = \frac{V_{ab}}{I} = \frac{-\int_b^a \vec{E} \cdot d\vec{L}}{\int_s \vec{J} \cdot d\vec{s}} = \frac{-\int_b^a \vec{E} \cdot d\vec{L}}{\int_s \sigma \vec{E} \cdot d\vec{s}}$$

PROPERTIES OF CONDUCTOR:

1- under static conditions, no charge and no electric field can exist at any point within the conducting material.

2. The charge can exist on the surface of the conductor giving rise to surface charge density

3. Within a conductor, the charge density is always zero

4. The charge distribution on the surface depends on the shape of the surface.

5. The conductivity of ideal conductor is infinite

6. The conductor surface is an equipotential surface.

Properties of Dielectric materials.

1. The dielectrics donot contain any free charges but contain bound charges

2. Bound charges are under the internal molecular and atomic forces and cannot contribute to the conduction.

3. When subjected to an external field $\vec{E}$, the bound charges shift their relative positions. Due to this, small electric dipoles get induced inside the dielectric. This is called Polarization.

4. Due to the Polarization, the dielectrics can store the energy

5. Due to the Polarization, the flux density of the dielectric increases by amount equal to the Polarization.

6. The induced dipoles Produce their own electric field and align in the direction of the applied electric field.

7. When Polarization occurs, the volume charge density is formed inside the dielectric while the surface charge density is formed over the surface of the dielectric

8. The electric field outside and inside the dielectric gets modified due to the induced electric dipoles.

The medium is called homogeneous when the physical characteristics of the medium dinot vary from Point to Point but remain same everywhere throughout the medium.

If the characteristics vary from Point to point, the medium is called heterogeneous (or) non-homogeneous.

While the medium is called linear with respect to the electric field is the flux density $\vec{D}$ is directly Proportional to the electric field $\vec{E}$. The relationship is thro' the permittivity of the medium

If $\vec{D}$ is not directly proportional to $\vec{E}$, the material is called non-linear

considering a conducting material which is linear and homogeneous. The current density for such a material is,

$$\vec{J} = \sigma \vec{E} \quad \text{where } \sigma \rightarrow \text{conductivity} \quad ---(1)$$

But W.K.T $\vec{D} = \varepsilon \vec{E}$ ---(2)

$$\therefore \vec{E} = \frac{\vec{D}}{\varepsilon} \quad ---(3)$$

sub (3) in (1) we get

$$\vec{J} = \sigma \frac{\vec{D}}{\varepsilon} = \frac{\sigma}{\varepsilon} \vec{D} \quad ---(4)$$

The Point form of continuity equation states that,

$$\nabla . \vec{J} = -\frac{\partial \rho_v}{\partial t} \quad ---(5)$$

sub (4) in (5)

$$\nabla . \left(\frac{\sigma}{\varepsilon} \vec{D}\right) = -\frac{\partial \rho_v}{\partial t}$$

$$\frac{\sigma}{\varepsilon} \nabla . \vec{D} = -\frac{\partial \rho_v}{\partial t} \quad ---(6)$$

But W.K.T $\nabla . \vec{D} = \rho_v$ ---(7) → Point form of Gauss's law Page NO: 18 (Unit II)

∴ sub (7) in (6) we get

$$\frac{\sigma}{\varepsilon} \rho_v = -\frac{\partial \rho_v}{\partial t} \Rightarrow \frac{\partial \rho_v}{\partial t} + \frac{\sigma}{\varepsilon} \rho_v = 0 \quad ---(8)$$

$$\frac{\partial \rho_v}{\partial t} + \frac{\sigma}{\varepsilon}\rho_v = 0 \quad \text{---} (8)$$

The above equation is of the form

$$\frac{\partial x}{\partial t} + a x = 0$$

solution of this equation is $x = x_0 e^{-at}$

where $x_0 \rightarrow$ Initial condition

III^{ly} solution of Equation (8) is

$$\rho_v = \rho_0 e^{-\sigma/\varepsilon t}.$$

$$\boxed{\rho_v = \rho_0 e^{-t/\tau}} \quad \text{where } \rho_0 = \text{charge density at } t = 0.$$

$$\text{---} (9)$$

This shows that if there is a temporary imbalance of electrons inside the given material, the charge density decays exponentially with time constant $\tau = \varepsilon/\sigma$ sec. This time is called relaxation time.

The relaxation time (τ) is defined as the time required by the charge density to decay to 36.8% of its initial value

τ = Relaxation time = $\frac{\varepsilon}{\sigma}$ sec.

DIELECTRIC MATERIALS:

→ It is seen that the conductors have large number of free electrons while insulators and dielectric materials do not have free charges.

→ The charges in dielectrics are <u>bound by</u> the <u>finite forces</u> and hence called <u>bound charges</u>. As they are bound & not free, they cannot contribute to the conduction process.

→ But if subjected to an Electric field $\vec{E}$, they shift their relative positions, against the normal molecular and atomic forces. This shift in the relative positions of bound charges, allows the dielectric to store the energy.

The shifts in positive and negative charges are in opposite directions and under the influence of an applied electric field $\vec{E}$ such charges act like small electric dipoles.

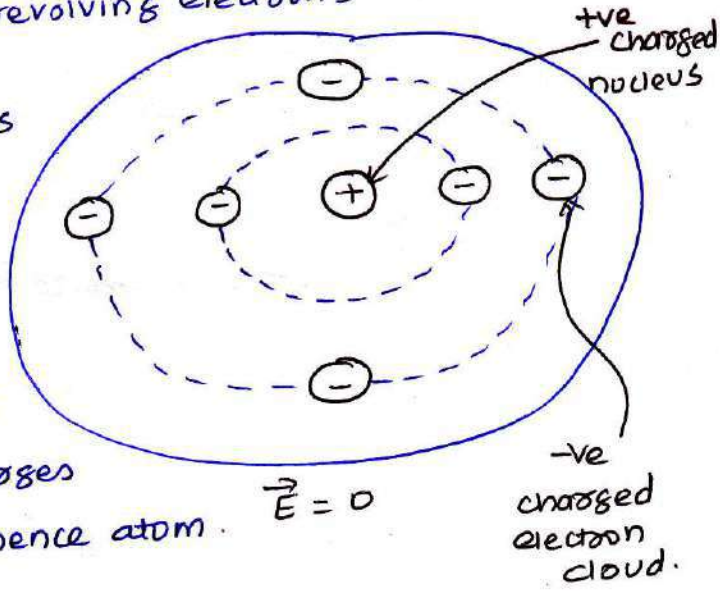
→ These electric dipoles produce an electric field which opposes the externally applied Electric field. This process, due to which seperation of bound charges results to produce electric dipoles, under the influence of electric field $\vec{E}_Y$ is called POLARIZATION.

POLARIZATION:

→ consider an atom of a dielectric

→ This consists of a nucleus with +ve charge and -ve charge in the form of revolving electrons in the orbits.

→ The negative charge is thus considered to be in the form of cloud of electrons. as shown in figure.

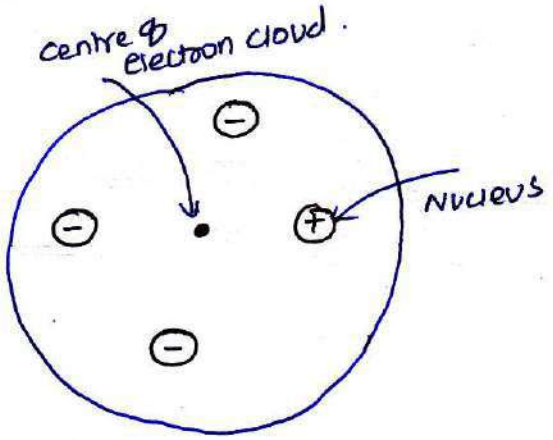


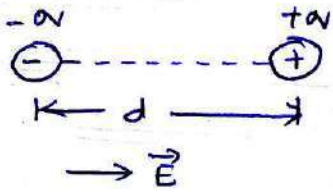
Note that $\vec{E}$ applied is zero. The number of +ve charges is same as -ve charges and hence atom is electrically neutral.

Due to symmetry, both +ve and -ve charges can be assumed to be point charges of equal amount, coinciding at the centre. Hence there cannot exists an electric dipole. This is called unpolarized atom.

When electric field $\vec{E}$ is applied, the symmetrical distribution of charges gets disturbed. The +ve charge experience a force $\vec{F} = Q\vec{E}$ while the -ve charge experience a force $\vec{F} = -Q\vec{E}$ in the opposite direction.

Now there is seperation b/w the nucleus and the centre of the electron cloud as shown in fig below. such an atom is called POLARIZED ATOM.





MATHEMATICAL EXPRESSION FOR POLARIZATION:

When the dipole is formed due to Polarization, there exists an electric dipole moment $\vec{P}$

$$\vec{P} = Q\vec{d} \quad ---(1)$$

where Q = Magnitude of one of the two charges

$\vec{d}$ = Distance vector from -ve to +ve charge

Let

$n \rightarrow$ No. of dipoles per unit volume

$\Delta V \rightarrow$ Total volume of the dielectric

$N \rightarrow$ Total dipole $= n\Delta V$

Then the total dipole moment is to be obtained by using superposition theorem.

$$\vec{P}_{total} = Q_1\vec{d}_1 + Q_2\vec{d}_2 + \cdots + Q_n\vec{d}_n$$

$$\vec{P}_{total} = \sum_{i=1}^{n\Delta V} Q_i\vec{d}_i \quad ---(2)$$

The Polarization $\vec{P}$ is defined as the total dipole moment per unit volume.

$$\therefore \vec{P} = \lim_{\Delta V \to 0} \frac{\sum_{i=1}^{n\Delta V} Q_i\vec{d}_i}{\Delta V} \quad ---(3)$$

It is measured in (C/m^2)

It can be seen that the units of polarization are same as that of flux density $\vec{D}$. Thus polarization increases the electric flux density in a dielectric medium. Hence we can write, flux density in an dielectric as

$$\vec{D} = \varepsilon_0 \vec{E} + \vec{P}$$

DIELECTRIC STRENGTH:

→ The ideal dielectric is non conducting but practically no dielectric can be ideal.

→ As the electric field applied to dielectric increases sufficiently, due to the force exerted on to the molecules, the electroons in the dielectric become free.

→ Under such large Electric field, the dielectric becomes conducting due to presence of large number of free electroons. This condition of dielectric is called dielectric breakdown.

The minimum value of the applied electric field at which the dielectric breaksdown is called dielectric strength of that dielectric.

It is measured in V/m or KV/cm.

BOUNDARY CONDITIONS:

→ When an electric field passes from one medium to another medium, it is important to study the conditions at the boundary b/w the two media.

→ The conditions existing at the boundary of the two media, when field passes from one medium to other are called boundary conditions.

Depending upon the nature of the media, there are two situations of the boundary conditions.

1- Boundary b/w conductor and free space
2. Boundary b/w two dielectrics with different properties.

→ The free space is nothing but a dielectric, hence first case is nothing but the boundary b/w conductors and dielectric.

→ For studying the boundary conditions, the maxwell's equation for Electrostatics are required.

$$\oint \vec{E} \cdot d\vec{L} = 0 \quad \& \quad \oint \vec{D} \cdot d\vec{s} = Q$$

similarly the field intensity $\vec{E}$ is required to be decomposed into two components namely

(i) Tangential to the boundary $[\vec{E}_{tan}]$ &
(ii) Normal to the boundary $[\vec{E}_N]$

$$\therefore \quad \vec{E} = \vec{E}_{tan} + \vec{E}_N$$

III[r] decomposition is required for flux density $\vec{D}$ as well.

BOUNDARY CONDITIONS B/W CONDUCTOR & FREE SPACE

Consider a boundary between conductor and free space. The conductor is ideal having infinite conductivity For ideal conductors it is known that:

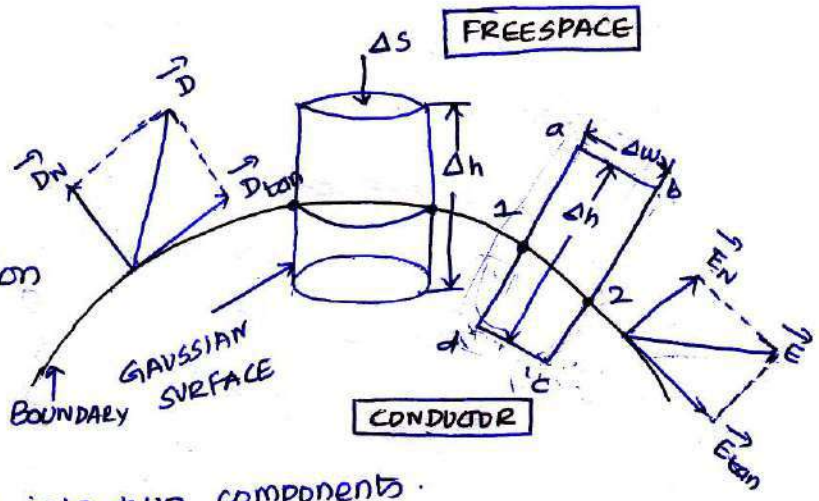
1. The field intensity inside a conductor is zero and the flux density inside a conductor is zero.
2. No charge can exist with in a conductor. The charge appears on the surface in the form of surface charge density.
3. The charge density with in the conductor is zero.

thus $\vec{E}$, $\vec{D}$ and ρ_v within the conductor is zero.

while ρ_s → surface charge density on the surface of the conductor.

To determine the boundary conditions let us use the closed path, and the Gaussian surface.

Consider the conductor free space boundary as shown in fig below.



$\vec{E}$ at BOUNDARY:

Let $\vec{E}$ be the Electric field intensity, in the direction shown in the figure, making some angle with the boundary.

This $\vec{E}$ can be resolved into two components.

1. The component tangential to the surface ($\vec{E}_{tan}$)
2. The component normal to the surface [$\vec{E}_N$]

It is known that

$$\oint \vec{E} \cdot d\vec{L} = 0$$

The integral of $\vec{E} \cdot d\vec{L}$ carried over a closed contour is zero. i.e work done in carrying a unit +ve charge along a closed path is zero.

Consider a rectangular closed path abcda as shown in fig. It is traced in clockwise direction as a-b-c-d-a and hence $\oint \vec{E} \cdot d\vec{L}$ can be divided into four parts.

$$\oint \vec{E} \cdot d\vec{L} = \int_a^b \vec{E} \cdot d\vec{L} + \int_b^c \vec{E} \cdot d\vec{L} + \int_c^d \vec{E} \cdot d\vec{L} + \int_d^a \vec{E} \cdot d\vec{L} = 0.$$

The closed contour is placed in such a way that its two sides a-b and c-d are ||el to tangential direction to the surface while the other two are normal to the surface, at the boundary.

The rectangle is an elementary rectangle with elementary height Δh and elementary width Δw. The rectangle is place in such a way that half of it is in the conductor and remaining half is in the free space.

Thus $\Delta h/2$ is in the conductor and $\Delta h/2$ is in the free space.

Now the portion c-d is in the conductor where $\vec{E} = 0$ hence the corresponding integral is zero

$$\therefore \int_a^b \vec{E}.\vec{dL} + \int_b^c \vec{E}.\vec{dL} + \int_d^a \vec{E}.\vec{dL} = 0 \quad \text{---} \quad (A)$$

As the width Δw is very small, $\vec{E}$ over it can be assumed constant and hence can be taken out for integration.

$$\therefore \int_a^b \vec{E}.\vec{dL} = \vec{E} \int_a^b \vec{dL} = \vec{E}(\Delta w)$$

But Δw is along tangential direction to the boundary in which direction $\vec{E} = \vec{E}_{tan}$

$$\therefore \int_a^b \vec{E}.\vec{dL} = E_{tan}(\Delta w) \quad \text{where } E_{tan} = |E_{tan}| \quad \text{---} \quad (1)$$

Now b-c is $\parallel^{el}$ to the normal components so we have $\vec{E} = \vec{E_N}$ along this direction, Let $E_N = |\vec{E_N}|$

over the small height Δh, E_N can be assumed constant and can be taken out of integration.

$$\therefore \int_b^c \vec{E}.\vec{dL} = \vec{E} \int_b^c \vec{dL} = \vec{E_N} \int_b^c \vec{dL}$$

But out of b-c, b-2 is in free space and 2-c is in the conductor where $\vec{E} = 0$

$$\therefore \int_b^c \vec{dL} = \int_b^2 \vec{dL} + \int_2^c \vec{dL} = \frac{\Delta h}{2} + 0 = \frac{\Delta h}{2}$$

$$\therefore \int_b^c \vec{E}.\vec{dL} = E_N\left(\frac{\Delta h}{2}\right) \text{---} (2)$$

Similarly for path d-a, the condition is same as for the path b-c, only direction is opposite

$$\therefore \int_d^a \vec{E}.\vec{dL} = -E_N\left(\frac{\Delta h}{2}\right) \text{---} (3)$$

Sub (1), (2) and (3) in (A) we get

$$E_{tan}(\Delta W) + E_N\left(\frac{\Delta h}{2}\right) - E_N\left(\frac{\Delta h}{2}\right) = 0$$

$$E_{tan}(\Delta W) = 0 \qquad \because \Delta W \neq 0 \text{ as finite}$$

$$\Rightarrow \boxed{E_{tan} = 0}$$

Thus the tangential component of the electric field intensity is zero at the boundary b/w conductor and free space.

D_N at the BOUNDARY

To find normal component of $\vec{D}$, select a closed Gaussian surface in the form of right circular cylinder as shown in the figure.

It's height is Δh and is placed in such a way that $\Delta h/2$ is in the conductor and remaining $\Delta h/2$ is in the free space. It's axis in the normal direction to the surface.

According to Gauss's law

$$\oint_S \vec{D}.\vec{ds} = Q.$$

The surface integral must be evaluated over three surfaces (i) TOP (ii) Bottom (iii) Lateral.

Let the area of top and bottom is same equal to ΔS

$$\therefore \int_{top} \vec{D} \cdot \vec{ds} + \int_{bottom} \vec{D} \cdot \vec{ds} + \int_{lateral} \vec{D} \cdot \vec{ds} = Q \quad \text{---} (1)$$

The bottom surface is in the conductor where $\vec{D} = 0$ hence corresponding integral is zero

The TOP surface is in the free space and we are interested in the boundary condition, hence top surface can be shifted at the boundary with $\Delta h \to 0$.

$$\therefore \int_{top} \vec{D} \cdot \vec{ds} + \int_{lateral} \vec{D} \cdot \vec{ds} = Q \quad \text{---} (2)$$

The lateral surface area is $2\pi r \Delta h$

where $r \to$ radius of the cylinder

But $\Delta h \to 0$, this area reduces to zero and corresponding integral is zero.

While only component of $\vec{D}$ present is the normal component having magnitude D_N. The top surface is very small over which D_N can be assumed constant and can be taken out of integration.

$$\therefore \int_{top} \vec{D} \cdot \vec{ds} = D_N \int_{top} \vec{ds} = D_N \Delta S \quad \text{---} (3)$$

$$\therefore D_N \Delta S = Q \quad \text{---} (4)$$

But at Boundary, the charge exists in the form of surface charge density ρ_s C/m^2

$$\therefore Q = \rho_s \Delta S \quad \text{---} (5)$$

sub (5) in (4) we get

$$D_N \Delta S = \rho_s \Delta S$$

$$\therefore \boxed{D_N = \rho_s}$$

Thus the flux leaving normally and the normal component of flux density is equal to the surface charge density.

$$\therefore D_N = \varepsilon_0 E_N = \rho_s$$

$$\therefore E_N = \frac{\rho_s}{\varepsilon_0}.$$

BOUNDARY CONDITION B/W CONDUCTOR & DIELECTRIC

The free space is a dielectric with $\varepsilon = \varepsilon_0$. Thus if the boundary is between conductor and dielectric $\varepsilon = \varepsilon_0 \varepsilon_r$.

$$\therefore \boxed{\begin{aligned} E_{tan} &= D_{tan} = 0 \\ D_N &= \rho_s \\ E_N &= \frac{\rho_s}{\varepsilon} = \frac{\rho_s}{\varepsilon_0 \varepsilon_r}. \end{aligned}}$$

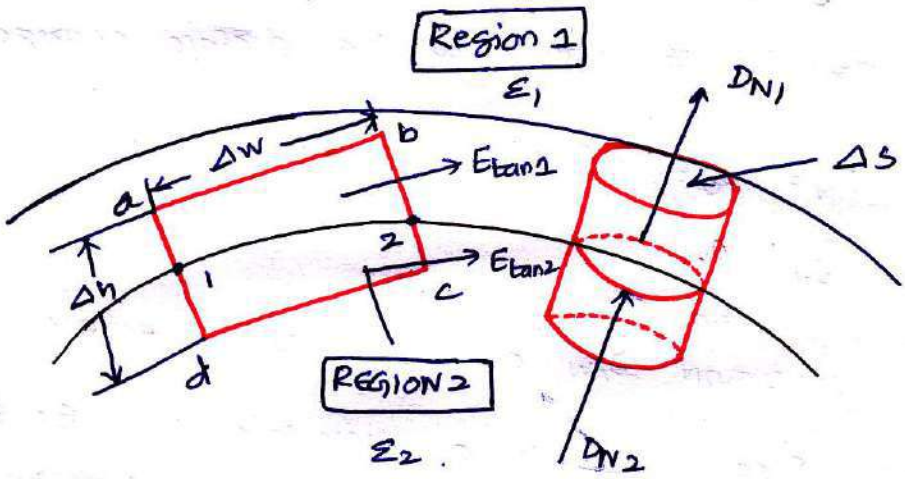
BOUNDARY CONDITIONS BETWEEN TWO PERFECT DIELECTRICS:

Let us consider the boundary b/w two perfect dielectrics. one dielectric has permittivity ε_1 while other has permittivity ε_2. The interface is shown in the figure.

The $\vec{E}$ and $\vec{D}$ are to be obtained again by resolving each into two components, tangential to the boundary and normal to the surface.

Consider a closed loop abcda rectangular in shape having elementary heigh Δh and elemenatry width Δw, as shown in figure.

It is placed in such a way that $\Delta h/2$ is in the dielectric 1 while the remaining is dielectric 2. Let us evaluate the integral $\vec{E}.\vec{dL}$ along this path, tracing it in clockwise direction as a-b-c-d-a.



$$\oint \vec{E}.\vec{dL} = 0 \quad ---(1)$$

$$\therefore \int_a^b \vec{E}.\vec{dL} + \int_b^c \vec{E}.\vec{dL} + \int_c^d \vec{E}.\vec{dL} + \int_d^a \vec{E}.\vec{dL} = 0 \quad ---(2)$$

Now $\vec{E_1} = \vec{E_{1t}} + \vec{E_{1N}}$

$\vec{E_2} = \vec{E_{2t}} + \vec{E_{2N}}$

Both $\vec{E_1}$ and $\vec{E_2}$ in the respective dielectrics have both the components, normal and tangential.

Let $|\vec{E_{1t}}| = E_{tan1}$ $\quad |\vec{E_{2t}}| = E_{tan2}$

$|\vec{E_{1N}}| = E_{1N}$ $\quad |\vec{E_{2N}}| = E_{2N}$.

Now for the rectangle to be reduced at the surface to analyse boundary conditions, $\Delta h \to 0$

As $\Delta h \to 0$ $\int_b^c$ and $\int_d^a$ become zero as these are line integrals along Δh and $\Delta h \to 0$, Hence eqn (2) becomes

$$\int_a^b \vec{E}.\vec{dL} + \int_c^d \vec{E}.\vec{dL} = 0 \quad \text{---} (3)$$

Now a-b is in dielectric 1 hence the corresponding component of $\vec{E}$ is E_{tan1} as a-b direction is tangential to the surface

$$\therefore \int_a^b \vec{E}.\vec{dL} = E_{tan1} \int_a^b \vec{dL} = E_{tan1}(\Delta w) \quad \text{---} (4)$$

while c-d is in dielectric 2 hence the corresponding component of $\vec{E}$ is E_{tan2} as c-d direction is also tangential to the surface. But the direction of c-d is opposite to a-b hence corresponding integral is negative of the integral obtained for path a-b.

$$\therefore \int_c^d \vec{E}.\vec{dL} = -E_{tan2}(\Delta w) \quad \text{----} (5)$$

substituting (4) and (5) in (3) we get

$$E_{tan1}(\Delta w) - E_{tan2}(\Delta w) = 0$$

$$\Rightarrow \boxed{E_{tan1} = E_{tan2}} \quad \text{---} (6)$$

Thus the tangential component of field intensity at the boundary in both the dielectrics remain same

i.e Electric field intensity is continuous across the boundary

The relation b/w $\vec{D}$ and $\vec{E}$ is known as,

$$\vec{D} = \varepsilon \vec{E}$$

Hence if D_{tan1} and D_{tan2} are magnitudes of the tangential components of $\vec{D}$ in dielectric 1 and 2 respectively then,

$$D_{tan1} = \varepsilon_1 E_{tan1}$$

$$D_{tan2} = \varepsilon_2 E_{tan2}$$

$$\frac{D_{tan1}}{\varepsilon_1} = \frac{D_{tan2}}{\varepsilon_2}$$

$$\boxed{\frac{D_{tan1}}{D_{tan2}} = \frac{\varepsilon_1}{\varepsilon_2} = \frac{\varepsilon_{r1}}{\varepsilon_{r2}}} \quad \text{---- (7)}$$

Thus tangential components of $\vec{D}$ undergoes some change across the interface hence tangential $\vec{D}$ is said to be discontinuous across the boundary.

To find the normal components, let us use Gauss's law. Consider a Gaussian surface in the form of right circular cylinder, placed in such a way that half of it lies in dielectric 1 while the remaining half in dielectric 2. The height $\Delta h \to 0$ hence given leaving from its lateral surface is zero. The surface area of its top and bottom is ΔS.

$$\therefore \oint \vec{D} \cdot \vec{ds} = Q \quad \text{--- (8)}$$

$$\therefore \left[\int_{top} + \int_{bottom} + \int_{lateral} \right] \vec{D} \cdot \vec{ds} = Q \quad \text{---- (9)}$$

But $$\int_{lateral} \vec{D} \cdot \vec{ds} = 0 \quad \text{as} \quad \Delta h \to 0 \quad \text{---- (10)}$$

$$\therefore \int_{top} \vec{D} \cdot \vec{ds} + \int_{bottom} \vec{D} \cdot \vec{ds} = Q \quad \text{---- (11)}$$

The flux leaving normal to the boundary is normal to the top and bottom surfaces.

$\therefore |\vec{D}| = D_{N1}$ for dielectric 1.

$= D_{N2}$ for dielectric 2.

As the top and bottom surfaces are elementary, flux density can be assumed constant and can be taken out of integration

$$\therefore \int_{top} \vec{D} \cdot \vec{ds} = D_{N1} \int_{top} \vec{ds} = D_{N1} \Delta S \quad \text{----} (12)$$

For top surface, the direction of D_N is entering the boundary while for bottom surface, the direction of D_N is leaving the boundary.

Both are opposite in direction, at the boundary

$$\therefore \int_{bottom} \vec{D} \cdot \vec{ds} = -D_{N2} \int_{bottom} \vec{ds} = -D_{N2} \Delta S \quad \text{---} (13)$$

Sub (12) and (13) in (11) we get

$$D_{N1} \Delta S - D_{N2} \Delta S = Q$$

But $Q = \rho_S \Delta S$

$$D_{N1} = D_{N2}$$

$$\therefore \boxed{D_{N1} - D_{N2} = \rho_S}$$

There is no free charge available in perfect dielectric and hence no free charge can exist on the surface. All charges in dielectric are bound charges and are not free.

Hence at ideal dielectric media boundary the surface charge density ρ_s can be assumed zero.

$\therefore \rho_s = 0$

$D_{N1} - D_{N2} = 0$

$$\boxed{D_{N1} = D_{N2}}$$

Hence the normal component of flux density $\vec{D}$ is continuous at the boundary b/w the two perfect dielectrics.

$\therefore D_{N1} = \varepsilon_1 E_{N1}$ and $D_{N2} = \varepsilon_2 E_{N2}$

$$\therefore \frac{D_{N1}}{D_{N2}} = \frac{\varepsilon_1}{\varepsilon_2} \frac{E_{N1}}{E_{N2}} = 1.$$

$$\therefore \boxed{\frac{E_{N1}}{E_{N2}} = \frac{\varepsilon_2}{\varepsilon_1} = \frac{\varepsilon_{r2}}{\varepsilon_{r1}}}$$

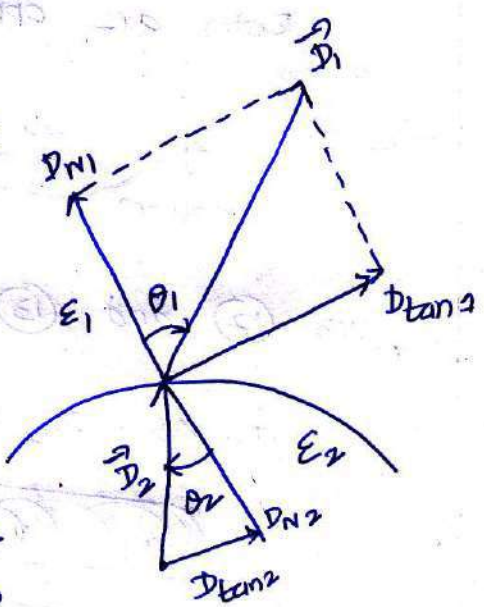
Refraction of $\vec{D}$ at the Boundary:

The directions of $\vec{D}$ and $\vec{E}$ change at the boundary b/w the two dielectrics.

Let $\vec{D_1}$ and $\vec{E_1}$ make an angle θ_1 with the normal to the surface.

$\vec{D_1}$ and $\vec{E_1}$ direction is same as

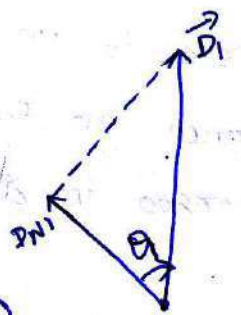
$$\boxed{\vec{D_1} = \varepsilon_1 \vec{E_1}}$$



This is shown in the figure.

Let $|\vec{D_1}| = D_1$

$|\vec{D_2}| = D_2$



from fig

$\cos\theta_1 = \frac{D_{N1}}{D_1}$

$\therefore D_{N1} = D_1 \cos\theta_1$ ---(1)

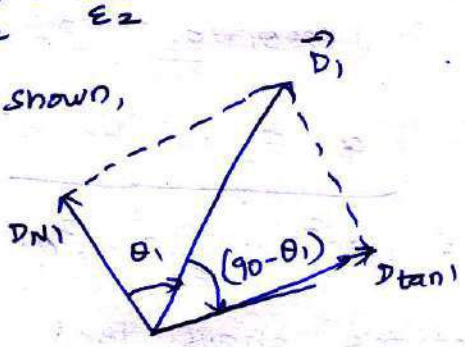
III^{rly} $D_{N2} = D_2 \cos\theta_2$ ---(2)

But W.K.T $D_{N1} = D_{N2}$

$\therefore D_1 \cos\theta_1 = D_2 \cos\theta_2$

III^{rly} W.K.T $\frac{D_{tan1}}{D_{tan2}} = \frac{\varepsilon_1}{\varepsilon_2}$

From the Figure shown,



$\cos(90-\theta_1) = \frac{D_{tan1}}{D_1}$

$\sin\theta_1 = \frac{D_{tan1}}{D_1}$

$\Rightarrow D_{tan1} = D_1 \sin\theta_1$ } --- (3)

III^{rly} $D_{tan2} = D_2 \sin\theta_2$ }

$$\frac{D_1 \sin\theta_1}{D_2 \sin\theta_2} = \frac{\varepsilon_1}{\varepsilon_2} = \frac{D_{tan1}}{D_{tan2}} \quad \text{--- (A)}$$

NOW (3a) ÷ (1)

$$\frac{D_1 \sin\theta_1}{D_1 \cos\theta_1} = \frac{D_{tan1}}{D_{N1}} \Rightarrow \tan\theta_1 = \frac{D_{tan1}}{D_{N1}} \quad \text{--- (4a)}$$

III^{rly} $\tan\theta_2 = \frac{D_{tan2}}{D_{N2}}$ --- (4b)

$$\frac{(4a)}{(4b)} \Rightarrow \frac{\tan\theta_1}{\tan\theta_2} = \frac{D_{tan1}}{D_{tan2}} \frac{D_{N2}}{D_{N1}}$$

But $D_{N1} = D_{N2}$

$$\therefore \frac{\tan\theta_1}{\tan\theta_2} = \frac{D_{tan1}}{D_{tan2}} = \frac{\varepsilon_1}{\varepsilon_2}$$

$$\Rightarrow \boxed{\frac{\tan\theta_1}{\tan\theta_2} = \frac{\varepsilon_1}{\varepsilon_2} = \frac{\varepsilon_{r1}}{\varepsilon_{r2}}}$$

This is called law of refraction. Thus the angles θ_1 and θ_2 are dependent on permittivities of two media and not on $\vec{D}$ or $\vec{E}$.

If $\varepsilon_1 > \varepsilon_2$ then $\theta_1 > \theta_2$

The magnitude of $\vec{D}$ in region 2 can be obtained as

$$D_2^2 = D_{N2}^2 + D_{tan2}^2 = (D_1 \cos\theta_1)^2 + D_{tan2}^2$$

Now $D_{tan_2} = D_2 \sin\theta_2 = \frac{D_1 \sin\theta_1 \varepsilon_2}{\varepsilon_1}$ [from (A)]

$$\therefore D_2^2 = (D_1 \cos\theta_1)^2 + \left(D_1 \sin\theta_1 \frac{\varepsilon_2}{\varepsilon_1}\right)^2$$

$$D_2 = D_1 \sqrt{\cos^2\theta_1 + \left(\frac{\varepsilon_2}{\varepsilon_1}\right)^2 \sin^2\theta_1}.$$

Illy Magnitude of E_2 can be obtained as

$$E_2 = E_1 \sqrt{\sin^2\theta_1 + \left(\frac{\varepsilon_1}{\varepsilon_2}\right)^2 \cos^2\theta_1}$$

the equations shows that

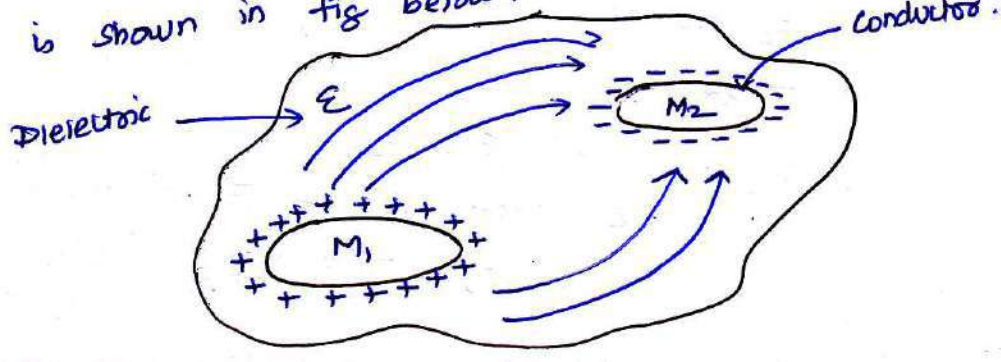
i) $\vec{D}$ is larger in region of larger Permittivity
ii) $\vec{E}$ is larger in region of smaller permittivity
iii) $|\vec{D_1}| = |\vec{D_2}|$ if $\theta_1 = \theta_2 = 0^\circ$
(iv) $|\vec{E_1}| = |\vec{E_2}|$ if $\theta_1 = \theta_2 = 90^\circ$.

To find the angles θ_1 and θ_2, w.r. to normal use the dot Product if normal direction to the boundary is known.

CONCEPT OF CAPACITANCE:

Consider two conducting materials M_1 and M_2 which are Placed in a dielectric medium having Permittivity ε. The material M_1 carries a positive charge Q while the material M_2 carries a negative charge $-Q$ (equal in magnitude). There are no other charges present and the total charge of the system is zero.

In conductors, charge cannot reside within the conductor and it resides only on the surface. Thus for M_1 and M_2 charges $+Q$ and $-Q$ resides on the surfaces of M_1 and M_2 respectively. This is shown in fig below.



Such a system which has two conducting surfaces carrying equal and opposite charges seperated by a dielectric is called **capacitive systems** giving rise to a **capacitance**.

The electric field is normal to the conductor surface and the electric flux is directed from M_1 towards M_2 in such a system. There exists a potential difference b/w the two surfaces M_1 and M_2. Let this potential is V_{12}.

The ratio of magnitudes of the total charge on any one of the two conductors and potential difference b/w the conductors is called the capacitance. It is denoted by 'C'.

$$C = \frac{Q}{V_{12}}$$

$V_{12} = V_2 - V_1$

$V_2 = -ve$

$V_1 = +ve$

In general $C = \frac{Q}{V}$

where Q = charge in coulombs

V = Potential difference in volts.

The capacitance is measured in farads (F) and

$$1 \text{ Farad} = \frac{1 \text{ coulomb}}{1 \text{ volt}}.$$

As charge Q resides only on the surface of the conductor it can be obtained from the Gauss's law as,

$$Q = \oint_S \vec{D} \cdot \vec{ds} = \oint_S \varepsilon_0 \varepsilon_r \vec{E} \cdot \vec{ds} = \oint_S \varepsilon \vec{E} \cdot \vec{ds}$$

while V is the work done in moving unit positive charge from -ve to +ve surface and can be obtained as,

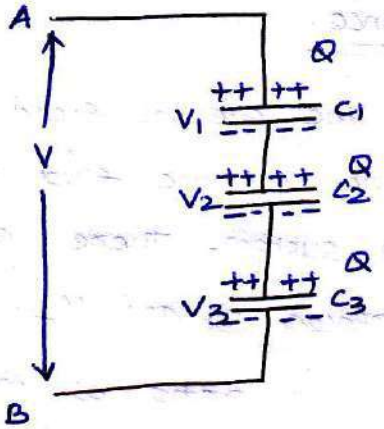
$$V = -\int_L \vec{E} \cdot \vec{dL} = -\int_-^+ \vec{E} \cdot \vec{dL}$$

Hence capacitance can be expressed as.

$$C = \frac{Q}{V} = \frac{\oint_S \varepsilon \vec{E} \cdot \vec{ds}}{-\int_-^+ \vec{E} \cdot \vec{dL}} \text{ F.}$$

CAPACITORS IN SERIES:

consider the three capacitors in series connected across the applied voltage V as shown in figure below.

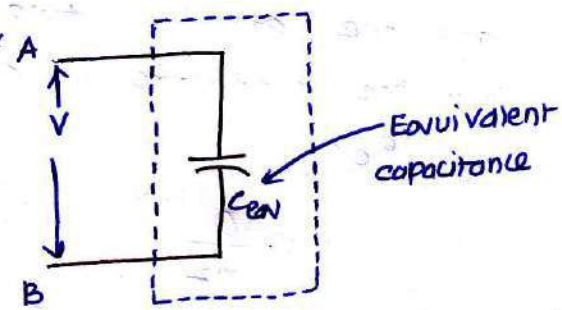


$$Q = C_1 V_1 = C_2 V_2 = C_3 V_3.$$

Giving

$$V_1 = \frac{Q}{C_1}\ ;\ V_2 = \frac{Q}{C_2}\ ;\ V_3 = \frac{Q}{C_3}$$

Is an equivalent capacitor also stores the same charge, when applied with the same voltage, then it is obvious that,



$$C_{eN} = \frac{Q}{V} \quad (\text{or})$$

$$V = \frac{Q}{C_{eN}}$$

But $V = V_1 + V_2 + V_3$

$$\frac{Q}{C_{eN}} = \frac{Q}{C_1} + \frac{Q}{C_2} + \frac{Q}{C_3}$$

$$\therefore \frac{1}{C_{eN}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$$

It is easy to find V_1, V_2 and V_3 if Q is known

for 'n' capacitors in series

$$\boxed{\frac{1}{C_{eN}} = \frac{1}{C_1} + \frac{1}{C_2} + \cdots + \frac{1}{C_n}}$$

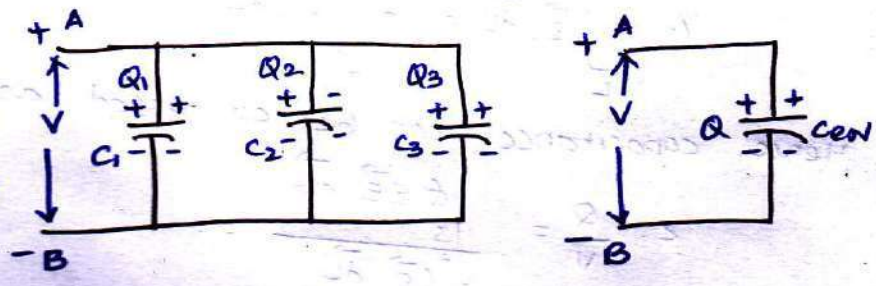
CAPACITORS IN PARALLEL:

When capacitors are in 11^{el}, the same voltage exists across them, but charges are different.

$Q_1 = C_1 V$

$Q_2 = C_2 V$

$Q_3 = C_3 V$



The Total charge stored by the Parallel banks of capacitors Q is given by

$$Q = Q_1 + Q_2 + Q_3$$
$$= C_1V + C_2V + C_3V$$
$$C_{eq}V = (C_1 + C_2 + C_3)V$$

$$\therefore \boxed{C_{eq} = C_1 + C_2 + C_3}$$

For n capacitors in 11^{el}

$$\boxed{C_{eq} = C_1 + C_2 + C_3 + ---- + C_n}$$

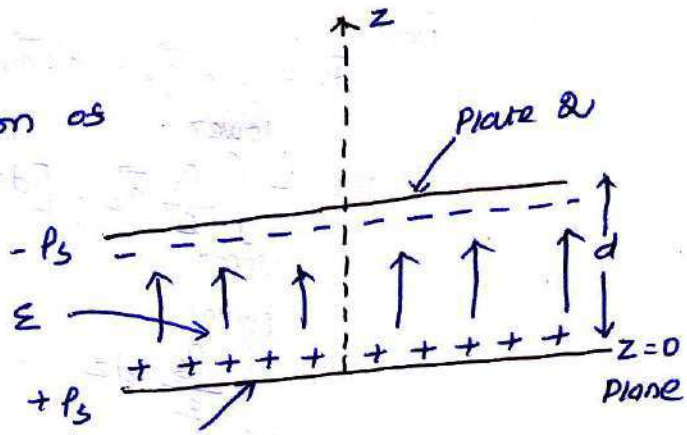
PARALLEL PLATE CAPACITORS :-

A Parallel plate capacitor is shown in figure. It consists of two parallel metallic plates seperated by distance 'd'. The space b/w the plates is filled with a dielectric of Permittivity ε.

The lower plate, plate 1 carries the positive charge and is distributed over it with a charge density $+\rho_s$. The upper plate, plate 2 carries the negative charge and is distributed over its surface with a charge density of $-\rho_s$. The plate 1 is placed in z=0 i.e xy plane hence normal to it is z-direction. while upper plate 2 is in z=d Plane, Parallel to xy plane.

Let A = Area of cross section of the plates in m^2.

$$\therefore \boxed{Q = \rho_s A} \text{ coulombs.}$$



This is magnitude of charge $+\rho_s$ on any one plate as charge carried by both is equal in magnitude.

To find Potential difference, let us obtain $\vec{E}$ b/w the Plates.

Assuming Plate 1 to be infinite sheet of charge

$$\vec{E_1} = \frac{\rho_s}{2\varepsilon}\vec{a_N} \quad [\text{Page No 16 of unit-II}].$$

$$= \frac{\rho_s}{2\varepsilon}\vec{a_z} \text{ V/m}.$$

The $\vec{E_1}$ is normal at the boundary b/w conductor and dielectric without any tangential component.

While for Plate 2, we can write

$$\vec{E_2} = \frac{-\rho_s}{2\varepsilon}\vec{a_N} = \frac{-\rho_s}{2\varepsilon}(-\vec{a_z}) = \text{V/m}.$$

The direction of $\vec{E_2}$ is downwards i.e in $-\vec{a_z}$ direction.

∴ In b/w Plates

$$\vec{E} = \vec{E_1} + \vec{E_2}$$

$$= \frac{\rho_s}{2\varepsilon}\vec{a_z} + \frac{\rho_s}{2\varepsilon}\vec{a_z} \Rightarrow \frac{\rho_s}{\varepsilon}\vec{a_z}$$

$$\boxed{\vec{E} = \frac{\rho_s}{\varepsilon}\vec{a_z}}$$

The Potential difference is given by.

$$V = -\int_{-}^{+} \vec{E}\cdot\vec{dL} = -\int_{\text{upper}}^{\text{lower}} \frac{\rho_s}{\varepsilon}\vec{a_z}\cdot\vec{dL}$$

Now $\vec{dL} = dx\,\vec{a_x} + dy\,\vec{a_y} + dz\,\vec{a_z}$ in cartesian system,

$$V = -\int_{\text{upper}}^{\text{lower}} \frac{\rho_s}{\varepsilon}\vec{a_z}\cdot[dx\,\vec{a_x} + dy\,\vec{a_y} + dz\,\vec{a_z}]$$

$$= -\int_{\text{upper}}^{\text{lower}} \frac{\rho_s}{\varepsilon}\,dz = -\frac{\rho_s}{\varepsilon}[z]_d^0 = -\frac{\rho_s}{\varepsilon}(-d) = \frac{\rho_s d}{\varepsilon}.$$

$$\boxed{V = \frac{\rho_s d}{\varepsilon} \text{ volts}}$$

∴ The capacitance is the ratio of charge Q to voltage V.

$$C = \frac{Q}{V} = \frac{\rho_s A}{\frac{\rho_s d}{\varepsilon}} = \frac{\varepsilon A}{d} \cdot F$$

Thus is $\varepsilon = \varepsilon_0 \varepsilon_r$

$$\boxed{C = \frac{\varepsilon_0 \varepsilon_r A}{d} F}$$

It can be seen that the value of capacitance depends on

(i) The permittivity of the dielectric used
(ii) The area of cross section of the plates
(iii) The distance of seperation of plates.

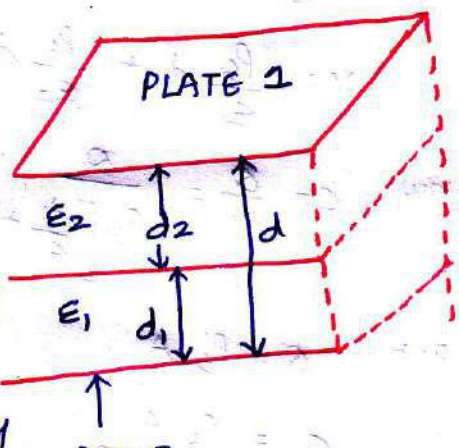
COMPOSITE PARALLEL PLATE CAPACITORS:

The composite parallel plate capacitor is one in which the space b/w the plates is filled with more than one dielectric.

Consider a composite capacitor with space filled with two seperate dielectrics for distance d_1 and d_2

The dielectric interface is parallel to the conducting plates.

The space d_1 is filled with dielectric having permittivity ε_1 while space d_2 is filled with dielectric having permittivity ε_2



Let Q = charge on each plate

$\vec{E}_1$ = Field intensity in region d_1

$\vec{E}_2$ = Field intensity in region d_2

Both the intensities are uniform

$\therefore V_1 = E_1 d_1$

$V_2 = E_2 d_2$

where E_1 and E_2 are the magnitudes of the two intensities.

$$V = V_1 + V_2 = E_1 d_1 + E_2 d_2 \quad \text{---} (1)$$

At a dielectric - dielectric interface, the normal components of flux densities are equal

i.e $D_{N1} = D_{N2}$

Now $D_1 = \varepsilon_1 E_1$ and $D_2 = \varepsilon_2 E_2$

$$\Rightarrow E_1 = \frac{D_1}{\varepsilon_1} \text{ \& } E_2 = \frac{D_2}{\varepsilon_2} \quad \text{---} (2)$$

Sub (2) in (1) we get

$$V = \frac{D_1}{\varepsilon_1} d_1 + \frac{D_2}{\varepsilon_2} d_2 \quad \text{---} (3)$$

The magnitude of surface charge is same on each plate hence

$$\rho_s = D_1 = D_2 \quad \text{---} (4)$$

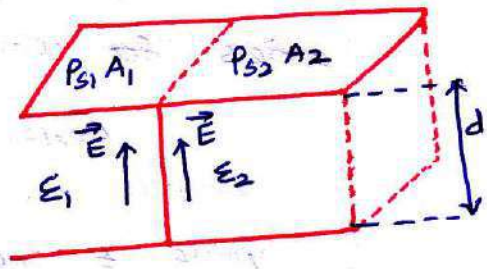
Sub (4) in (3) we get

$$V = \frac{\rho_s}{\varepsilon_1} d_1 + \frac{\rho_s}{\varepsilon_2} d_2 \Rightarrow \rho_s \left[\frac{d_1}{\varepsilon_1} + \frac{d_2}{\varepsilon_2} \right] \quad \text{---} (5)$$

$$\frac{Q}{} \quad \text{---} (6)$$

DIELECTRIC BOUNDARY NORMAL TO THE PLATES:

Consider the composite capacitor in which dielectric boundary is normal to the conducting plates.



The dielectric ε_1 occupying area A_1 of the plates, while dielectric ε_2 occupying area A_2 as shown in the figure.

The total potential across the two plates is V and the distance b/w the plates is d. Hence magnitude of $\vec{E}$ is

$$E = \frac{V}{d}$$

∴ At the boundary, both $\vec{E}_1$ and $\vec{E}_2$ are tangential and for dielectric - dielectric interface tangential components are equal.

$$E_{tan1} = E_{tan2} = E_1 = E_2 = \frac{V}{d} \quad \text{---(1)}$$

Now $D_1 = \varepsilon_1 E_1$ & $D_2 = \varepsilon_2 E_2$ ---(2)

Sub (1) in (2),

$$D_1 = \frac{\varepsilon_1 V}{d} \quad \text{------} \quad D_2 = \frac{\varepsilon_2 V}{d} \quad \text{---(3)}$$

on the plates the charge is divided into two parts

on area A_1, The charge density is $\rho_{s1} = D_1$ while
on area A_2, The charge density is $\rho_{s2} = D_2$ } ---(4)

$$\therefore Q = Q_1 + Q_2 \quad \text{---(5)}$$

$$= \rho_{s1} A_1 + \rho_{s2} A_2 \quad \text{---(6)} \qquad \text{Sub (4) in (6)}$$

$$= D_1 A_1 + D_2 A_2 \quad \text{--(7)}$$

Sub (3) in (7)

$$= \frac{\varepsilon_1 V A_1}{d} + \frac{\varepsilon_2 V A_2}{d}$$

$$C = \frac{Q}{V} = \frac{\frac{\varepsilon_1 V A_1 + \varepsilon_2 V A_2}{d}}{V} \Rightarrow \frac{\varepsilon_1 A}{d} + \frac{\varepsilon_2 A}{d}$$

$$\boxed{C = C_1 + C_2}$$

where $C_1 = \frac{\varepsilon_1 A}{d}$ $C_2 = \frac{\varepsilon_2 A}{d}$.

Thus if dielectric boundary is $\parallel^{el}$ to the plates, the arrangement is equivalent to two capacitors in series for which

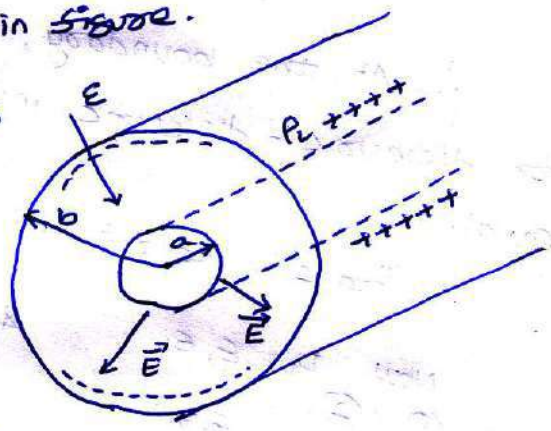
$$C_{eq} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2}}$$

While if the dielectric boundary is normal to the plates, the arrangement is equivalent to two capacitors in $\parallel^{el}$ for which

$$C_{eq} = C_1 + C_2 .$$

CAPACITANCE OF A CO-AXIAL CABLE:-

Consider a co-axial cable or co-axial capacitor as shown in figure.



The two concentric conductors are seperated by dielectric of Permittivity ε.

The length of the cable is L meters.

The inner conductor carries a charge density $+\rho_L$ c/m on its surface then equal and opposite charge density $-\rho_L$ c/m exists on the outer conductor.

$$\therefore Q = \rho_L \times L \quad ---- (1)$$

Assuming cylindrical co-ordinate system, $\vec{E}$ will be radial from inner to outer and for infinite line charge it is given by

$$\vec{E} = \frac{\rho_L}{2\pi\varepsilon r}\,\vec{a}_r \quad --- (2)$$

$\vec{E}$ is directed from inner conductor to outer conductor. The Potential difference is work done in moving unit charge against $\vec{E}$ i.e. from $r = b$ to $r = a$.

To find Potential difference, consider $\vec{dL}$ in radial direction which is $dr\,\vec{a}_r$.

$$\therefore \vec{dL} = dr\,\vec{a}_r \quad \text{---- (3)}$$

$$\therefore V = -\int_{-}^{+} \vec{E}\cdot\vec{dL}$$

$$= -\int_{-}^{+} \frac{\rho_L}{2\pi\varepsilon r}\vec{a}_r \cdot dr\,\vec{a}_r = -\frac{\rho_L}{2\pi\varepsilon}[\ln r]_b^a$$

$$= -\frac{\rho_L}{2\pi\varepsilon}\ln\left[\frac{a}{b}\right]$$

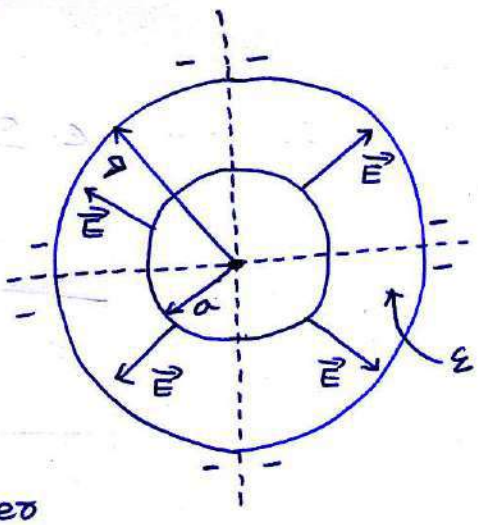
$$\therefore V = \frac{\rho_L}{2\pi\varepsilon}\ln\left(\frac{b}{a}\right)$$

$$\therefore C = \frac{Q}{V} = \frac{\rho_L L}{\frac{\rho_L}{2\pi\varepsilon}\ln\left(\frac{b}{a}\right)} = \frac{2\pi\varepsilon L}{\ln\left(\frac{b}{a}\right)}\ F$$

$$C = \frac{2\pi\varepsilon L}{\ln\left(\frac{b}{a}\right)}\ F \quad \text{---- (4)}$$

SPHERICAL CAPACITOR:-

Consider a spherical capacitor formed of two concentric spherical conducting shells of radius 'a' and 'b'. The capacitor is shown in figure.



The radius of outer sphere is 'b' while that of inner sphere is 'a'. Thus $b > a$. The region b/w the two spheres is filled with a dielectric of permittivity ε.

The inner sphere is given a +ve charge $(+Q)$ while for the outer sphere it is $(-Q)$.

considering, Gaussian surface as a sphere of radius r, it can be obtained that $\vec{E}$ is in radial direction and given by.

$$\vec{E} = \frac{Q}{4\pi\varepsilon r^2}\vec{a}_r \ V/m. \quad ----(1)$$

[Elementary Eqn]

The Potential difference is work done in moving unit positive charge against the direction of $\vec{E}$ i.e from $r=b$ to $r=a$

$$\therefore V = -\int_{-}^{+}\vec{E}.d\vec{L} = -\int_{r=b}^{r=a}\frac{Q}{4\pi\varepsilon r^2}\vec{a}_r.d\vec{L} \quad ---(2)$$

$$\vec{dL} = dr\,\vec{a}_r \quad ---(3)$$

sub (3) in (2) we get

$$V = -\int_{r=b}^{r=a}\frac{Q}{4\pi\varepsilon r^2}\vec{a}_r.dr\,\vec{a}_r$$

$$= -\int_{b}^{a}\frac{Q}{4\pi\varepsilon r^2}dr = -\frac{Q}{4\pi\varepsilon}\left[-\frac{1}{r}\right]_b^a$$

$$\boxed{V = \frac{Q}{4\pi\varepsilon}\left[\frac{1}{a}-\frac{1}{b}\right] \text{ Volts}} \quad ---(4)$$

$\therefore$ Now $C = \frac{Q}{V} = \frac{Q}{\frac{Q}{4\pi\varepsilon}\left[\frac{1}{a}-\frac{1}{b}\right]}$

$$\boxed{C = \frac{4\pi\varepsilon}{\left[\frac{1}{a}-\frac{1}{b}\right]} \ F} \quad ---(5)$$

CAPACITANCE OF SINGLE ISOLATED SPHERE:

Consider a single isolated sphere of radius 'a' given a charge of $+Q$. It forms a capacitance with an outer plate which is infinitely large hence $b = \infty$.

The capacitance of such a single isolated spherical conductor can be obtained by substituting $b = \infty$ in above eqn (5)

$$\therefore \quad C = \frac{4\pi\varepsilon}{\frac{1}{a} - \frac{1}{\infty}} \qquad \text{but } \frac{1}{\infty} = 0$$

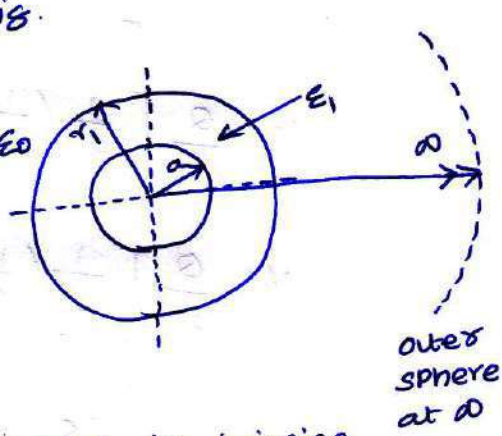
$$\boxed{C \Rightarrow 4\pi\varepsilon a \text{ farads}}$$

(stray capacitance of an isolated body)

ISOLATED SPHERE COATED WITH DIELECTRIC :

Consider a single isolated sphere coated with a dielectric having permittivity ε_1, upto radius r_1. The radius of inner sphere is 'a' as shown in fig.

It is placed in a free space so outside sphere $\varepsilon = \varepsilon_0$. It carries a charge of $+Q$.



So for $a < r < r_1$, $\varepsilon = \varepsilon_1$.

for $r > r_1$, $\varepsilon = \varepsilon_0$.

The Potential difference is work done in bringing unit positive charge from outer sphere $r = \infty$ to inner sphere $r = a$ against $\vec{E}$. This is to be splitted into two as

$$V = -\int_{-}^{+} \vec{E} \cdot \vec{dL} = -\int_{r=\infty}^{r=a} \vec{E} \cdot \vec{dL}$$

$$= -\int_{r=\infty}^{r=r_1} \vec{E} \cdot \vec{dL} - \int_{r=r_1}^{r=a} \vec{E} \cdot \vec{dL} \quad \text{---(1)}$$

Now for $a < r < r_1$ for $r_1 < r < \infty$

$$\vec{E_1} = \frac{Q}{4\pi\varepsilon_1 r^2}\vec{a_r} \qquad \vec{E_2} = \frac{Q}{4\pi\varepsilon_0 r^2}\vec{a_r}$$

while $\vec{dL} = dr\vec{a_r}$

$\therefore$ Eqn ① becomes,

$$V = -\int_{\infty}^{r_1} \frac{Q}{4\pi\varepsilon_0 r^2}\vec{a_r}\cdot dr\,\vec{a_r} - \int_{r_1}^{a} \frac{Q}{4\pi\varepsilon_1 r^2}\vec{a_r}\cdot dr\,\vec{a_r}$$

$$= -\frac{Q}{4\pi}\left[\frac{1}{\varepsilon_0}\int_{\infty}^{r_1}\frac{1}{r^2}dr + \frac{1}{\varepsilon_1}\int_{r_1}^{a}\frac{1}{r^2}dr\right]$$

$$= -\frac{Q}{4\pi}\left[\frac{1}{\varepsilon_0}\left[\frac{-1}{r}\right]_{\infty}^{r_1} + \frac{1}{\varepsilon_1}\left[\frac{-1}{r}\right]_{r_1}^{a}\right]$$

$$V = -\frac{Q}{4\pi}\left[\frac{1}{\varepsilon_0}\left(\frac{-1}{r_1}+\frac{1}{\infty}\right) + \frac{1}{\varepsilon_1}\left[\frac{-1}{a}+\frac{1}{r_1}\right]\right]$$

$$V = \frac{Q}{4\pi}\left[\frac{1}{\varepsilon_0}\left(\frac{1}{r_1}\right) + \frac{1}{\varepsilon_1}\left(\frac{1}{a}\right) - \frac{1}{\varepsilon_1}\left(\frac{1}{r_1}\right)\right]$$

$$V = \frac{Q}{4\pi}\left[\frac{1}{\varepsilon_1}\left(\frac{1}{a}-\frac{1}{r_1}\right) + \frac{1}{\varepsilon_0 r_1}\right] \text{ volts}$$

$$\therefore C = \frac{Q}{V} = \frac{Q}{\frac{Q}{4\pi}\left[\frac{1}{\varepsilon_1}\left(\frac{1}{a}-\frac{1}{r_1}\right)+\frac{1}{\varepsilon_0 r_1}\right]}$$

$$\Rightarrow \frac{1}{C} = \frac{\frac{1}{\varepsilon_1}\left(\frac{1}{a}-\frac{1}{r_1}\right)+\frac{1}{\varepsilon_0 r_1}}{4\pi}$$

$$C = \frac{4\pi}{\left[\frac{1}{\varepsilon_1}\left(\frac{1}{a}-\frac{1}{r_1}\right)+\frac{1}{\varepsilon_0 r_1}\right]}$$

$$\Rightarrow \frac{1}{C} = \frac{\frac{1}{a}-\frac{1}{r_1}}{4\pi\varepsilon_1} + \frac{1}{4\pi\varepsilon_0 r_1}$$

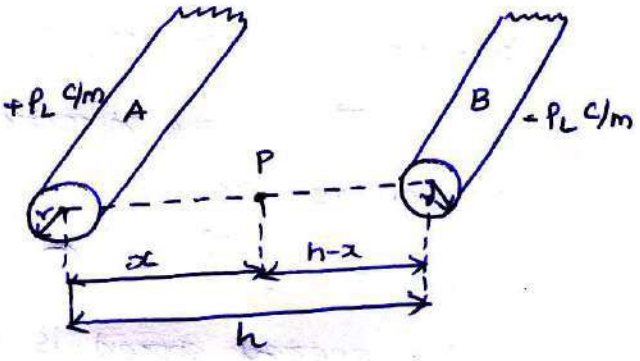
Let $C_1 = \dfrac{4\pi\varepsilon_1}{\frac{1}{a}-\frac{1}{r_1}}$ & $C_2 = 4\pi\varepsilon_0 r_1$

$$\therefore \frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2}$$

$$\boxed{C = \frac{1}{\frac{1}{C_1}+\frac{1}{C_2}}}$$

CAPACITANCE BETWEEN TWO TRANSMISSION LINES:

Let us consider two ||el conductors A and B of radius 'r' seperated by a distance 'h'. If A has charge $+\rho_L$ c/m along its length, it will induce $-\rho_L$ c/m on conductor, B. At any Point P at a distance x from the centre of A, electric field intensity due to A is.



$$\vec{E}_1 = \frac{\rho_L}{2\pi\varepsilon x}\,\vec{a}_x$$

Electric field intensity at P due to B is

$$\vec{E}_2 = \frac{-\rho_L}{2\pi\varepsilon(h-x)}\,(+\vec{a}_x)$$

The TOTAL field Intensity at P is.

$$\vec{E} = \vec{E}_1 + \vec{E}_2 = \frac{\rho_L}{2\pi\varepsilon}\left[\frac{1}{x} \bar{+} \frac{1}{h-x}\right]\vec{a}_x$$

Potential rise from B to A

$$V = -\int_B^A \vec{E}\cdot d\vec{l}$$

At the surface of A, $x = r$

B, $x = h-r$.

$$\therefore V = -\int_{x=h-r}^{x=r} \frac{\rho_L}{2\pi\varepsilon}\left[\frac{1}{x} \bar{+} \frac{1}{h-x}\right] dx = -\frac{\rho_L}{2\pi\varepsilon}\left[\ln x \bar{+} \ln(h-x)\right]_{h-r}^{r}$$

$$V = \frac{-\rho_L}{2\pi\varepsilon}\left[\ln(r) - \ln(h-r) \bar{+} \ln(h-r) + \ln\left[h-(h-r)\right]\right]$$

$$V = -\frac{\rho_L}{2\pi\varepsilon}\left[2\ln(r) - 2\ln(h-r)\right] = \frac{\rho_L}{2\pi\varepsilon} 2\left[\ln(r) - \ln(h-r)\right]$$

$$\therefore V = \frac{\rho_L}{\pi\varepsilon}\left[\ln\left(\frac{h-r}{r}\right)\right]$$

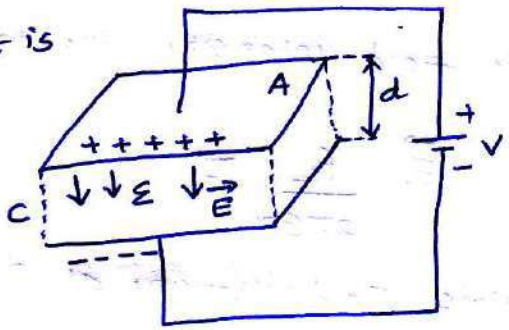
$$\therefore C = \frac{Q}{V} = \frac{\rho_L \cdot l}{\frac{\rho_L}{\pi\varepsilon}\ln\left(\frac{h-r}{r}\right)} = \frac{\pi\varepsilon l}{\ln\left(\frac{h-r}{r}\right)}$$

$$\boxed{\therefore C = \frac{\pi\varepsilon l}{\ln\left(\frac{h-r}{r}\right)}}$$

ENERGY STORED IN A CAPACITOR:

It is seen that capacitor can store the energy. Let's find the expression for the energy stored in a capacitor.

Consider a $\parallel^{el}$ Plate capacitor as shown in the figure. It is supplied with voltage V.



Let $\vec{a}_N$ is the direction normal to the plates

$$\therefore \vec{E} = \frac{V}{d}\vec{a}_N \text{ ---(1)}$$

The energy stored is given by,

$$W_E = \frac{1}{2}\int_{Vol} \vec{D}.\vec{E}\, dV$$

$$= \frac{1}{2}\int_{Vol} \varepsilon \vec{E}.\vec{E}\, dV \quad \text{but } \vec{E}.\vec{E} = |\vec{E}|^2$$

$$= \frac{1}{2}\int_{Vol} \varepsilon |\vec{E}|^2 dV \quad \text{but } |\vec{E}| = \frac{V}{d}$$

$$= \frac{1}{2}\varepsilon \frac{V^2}{d^2}\int_{Vol} dV \quad \text{but } \int_{Vol} dV = \text{volume} = A \times d$$

$$= \frac{1}{2}\varepsilon \frac{V^2 A d}{d^2}$$

$$W_E = \frac{1}{2}\frac{\varepsilon A}{d}V^2 = \frac{1}{2}CV^2 \quad \left[\because C = \frac{\varepsilon A}{d}\right]$$

ENERGY DENSITY:

Energy density is Energy stored per unit volume as volume tends to zero.

$$\therefore W_E = \frac{1}{2}\varepsilon \int_{Vol} |\vec{E}|^2 dV$$

$$W_E = \frac{1}{2}\varepsilon |\vec{E}|^2 \ J/m^3 = \text{Energy density}.$$

Using $|\vec{D}| = \varepsilon |\vec{E}|$ in above expression.

$$W_E = \frac{1}{2}\frac{|\vec{D}|^2}{\varepsilon} = \frac{1}{2}|\vec{D}||\vec{E}| \ J/m^3.$$

POISSON'S & LAPLACE'S EQUATIONS:

From the Gauss's law in the point form, Poisson's equation can be derived.

Consider the Gauss's law in the point form as

$$\nabla . \vec{D} = \rho_v \quad ---(1)$$

$\vec{D}$ → Flux density; ρ_v → volume charge density

W.K.T $$\vec{D} = \varepsilon \vec{E} \quad ---(2)$$

Sub (2) in (1) we get

$$\nabla . \varepsilon \vec{E} = \rho_v \quad ---(3)$$

From the gradient relationship

$$\vec{E} = -\nabla V \quad ---(4)$$

substitute (4) in (3) we get

$$\nabla . \varepsilon(-\nabla V) = \rho_v$$

$$-\varepsilon [\nabla . \nabla V] = \rho_v$$

$$\nabla . \nabla V = \frac{-\rho_v}{\varepsilon} \quad ---(5)$$

But $\nabla . \nabla = \nabla^2$

$\therefore$ (5) $\Rightarrow$ $$\boxed{\nabla^2 V = -\frac{\rho_v}{\varepsilon}} \quad ---(6)$$

Equation (6) is called Poisson's Equation.

If in certain region, $\rho_v = 0$, which is true for dielectric medium then Poisson's Equation takes a form

$$\boxed{\nabla^2 V = 0}$$ (for charge free region).

This is a special case of Poisson's equation called as Laplace's Equation.

∇^2 is called Laplacian of V.

UNIQUENESS THEOREM:

The boundary value problems can be solved by number of methods such as analytical, graphical, experimental etc.

Thus there is a question that, is the solution of Laplace's equation solved by any method, unique? The answer to this question is the uniqueness theorem, which is proved by contradiction method.

Assume that the Laplace's equation has two solutions say V_1 and V_2, both are functions of the co-ordinates of the system used. These solutions must satisfy Laplace's equation. So we can write,

$$\nabla^2 V_1 = 0 \quad \text{and} \quad \nabla^2 V_2 = 0 \cdot \text{----} (1)$$

Both the solutions must satisfy the boundary conditions as well. At the boundary, the potentials at different points are same due to equipotential surface then,

$$V_1 = V_2 \text{ ---} (2)$$

Let the difference b/w the two solutions is V_d

$$\therefore V_d = V_2 - V_1 \text{ ---} (3)$$

Using Laplace's equation for the difference V_d,

$$\nabla^2 V_d = \nabla^2 (V_2 - V_1) = 0 \text{ ----} (4) \Rightarrow \nabla^2 V_2 - \nabla^2 V_1 = 0 \text{ ---} (5)$$

on the boundary $V_d = 0$ [from (2) & (3)]

from divergence theorem,

$$\int_{Vol} (\nabla \cdot \vec{A})\, dv = \oint_S \vec{A} \cdot \vec{ds} \text{ ---} (6)$$

Let $\vec{A} = V_d \nabla V_d$ and from vector algebra

$$\nabla \cdot (\alpha \vec{B}) = \alpha [\nabla \cdot \vec{B}) + \vec{B} \cdot (\nabla \alpha) \text{ ---} (7).$$

Now use this for $\nabla.(V_d \nabla V_d)$ with $d = V_d$ and $\nabla V_d = \vec{B}$

$$\nabla.(V_d \nabla V_d) = V_d(\nabla.\nabla V_d) + \nabla V_d.(\nabla V_d)$$

But $\nabla.\nabla = \nabla^2$ hence

$$\nabla.(V_d \nabla V_d) = V_d \nabla^2 V_d + \nabla V_d.\nabla V_d \quad ---(8)$$

using eqn (4) in (8) ie $\nabla^2 V_d = 0$ we get

$$\nabla.(V_d \nabla V_d) = \nabla V_d.\nabla V_d \quad ---- (9)$$

To use this in equation (6)

Let $V_d \nabla V_d = \vec{A}$ hence

$$\nabla.(V_d \nabla V_d) = \nabla.\vec{A} = \nabla V_d.\nabla V_d$$

$$\int_{Vol} \nabla V_d.\nabla V_d \, dV = \oint_S V_d \nabla V_d.\vec{ds} \quad --- (10)$$

But $V_d = 0$ on boundary, hence RHS of (10) becomes zero

$$\therefore \int_{Vol} (\nabla V_d.\nabla V_d) dV = 0$$

$$\int_{Vol} |\nabla V_d|^2 dV = 0 \text{ as } \nabla V_d \text{ is a vector} \quad --- (11)$$

Now Integration can be zero under two conditions,

(i) The quantity under integral sign is zero

(ii) the quantity is +ve in some regions and -ve in some other regions by equal amount and hence zero.

$$\therefore |\nabla V_d|^2 = 0$$

$$\nabla V_d = 0.$$

As the gradient of $V_d = V_2 - V_1$ is zero means $V_2 - V_1$ is constant and not changing with any co-ordinates.

But considering boundary it can be pooved that

$$V_2 - V_1 = \text{const} = \text{zeoo}.$$

$$V_2 = V_1$$

This pooves that both the solutions are eoual and cannot be different.

UNIQUENESS THEOREM states that

Is the solution of Laplace's eouation satisfies the boundary condition then that solution is uniove, by whatever method it is obtained.

TUTORIAL PROBLEMS

1. Verify that the potential field given below satisfies the Laplace's equation $V = 2x^2 - 3y^2 + z^2$

Given field is in cartesian system

$$\therefore \nabla^2 V = \frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} + \frac{\partial^2 V}{\partial z^2}$$

$$= \frac{\partial^2}{\partial x^2}[2x^2 - 3y^2 + z^2] + \frac{\partial^2}{\partial y^2}[2x^2 - 3y^2 + z^2] + \frac{\partial^2}{\partial z^2}[2x^2 - 3y^2 + z^2]$$

$$= \frac{\partial}{\partial x}[4x] + \frac{\partial}{\partial y}[-6y] + \frac{\partial}{\partial z}[2z]$$

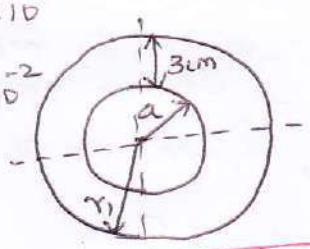
$$\Rightarrow 4 - 6 + 2 = 0$$

$\boxed{\nabla^2 V = 0}$ Thus the field satisfies the Laplace's Equation

2. Find the capacitance of a conducting sphere of 2cm in diameter, covered with a layer of polyethelene with $\varepsilon_r = 2.26$ and 3cm thick.

a = radius of sphere = $\frac{d}{2}$ = 1 cm = 1×10^{-2}

r_1 = a + thickness = 1 + 3 = 4 cm = 4×10^{-2}



$$\therefore C = \frac{4\pi}{\frac{1}{\varepsilon_1}\left(\frac{1}{a} - \frac{1}{r_1}\right) + \frac{1}{\varepsilon_0 r_1}} \quad F$$

$$= \frac{4\pi}{\frac{1}{2.26}\left[\frac{1}{1\times10^{-2}} - \frac{1}{4\times10^{-2}}\right] + \frac{1}{8.854\times10^{-12}\times 4\times10^{-2}}}$$

$\boxed{C = 1.9121 \text{ PF}}$

3. A coil of 500 turns is wound on a closed iron ring of mean radius 10 cm and cross section area of $3\,cm^2$. Find the self inductance of the winding if the relative permeability of iron is 800.

$\mu_r = 800$

$A = 3\,cm^2 = 3 \times 10^{-4}\,m^2$

$R = 10\,cm = 10 \times 10^{-2}\,m$

$N = 500$

$L = \frac{\mu N^2 A}{2\pi R}$

$\mu = \mu_0 \mu_r$

$\mu_0 = 4\pi \times 10^{-7}$

$L = 0.12$ H

$\boxed{L = 120\ mH}$

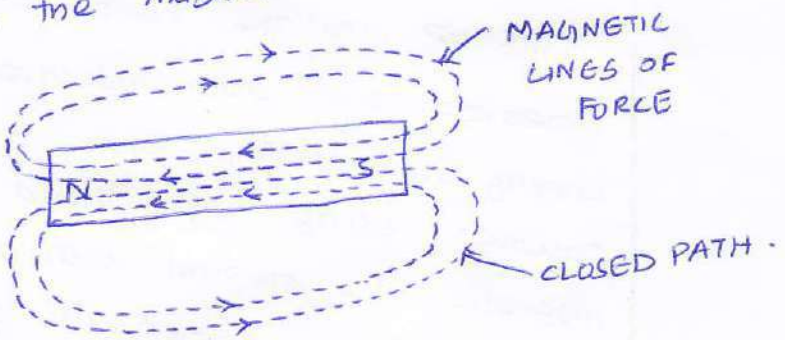
MAGNETIC FIELD & ITS PROPERTIES:

Consider a Permanent magnet, It has two poles North (N) and South (S). The region around a magnet within which the influence of the magnet can be experienced is called magnetic field.

Such a field is represented by imaginary lines around the magnet which are called magnetic lines of force. These lines of force are also called magnetic lines of flux or magnetic flux lines.

An important difference b/w electric flux lines and magnetic flux lines can be observed here. In case of electric flux, the flux lines originate from an isolated positive charge and diverge to terminate at infinity. while for a -ve charge, electric flux lines converge on a charge, starting from infinity. But in case of magnetic flux, the poles exists in pairs only.

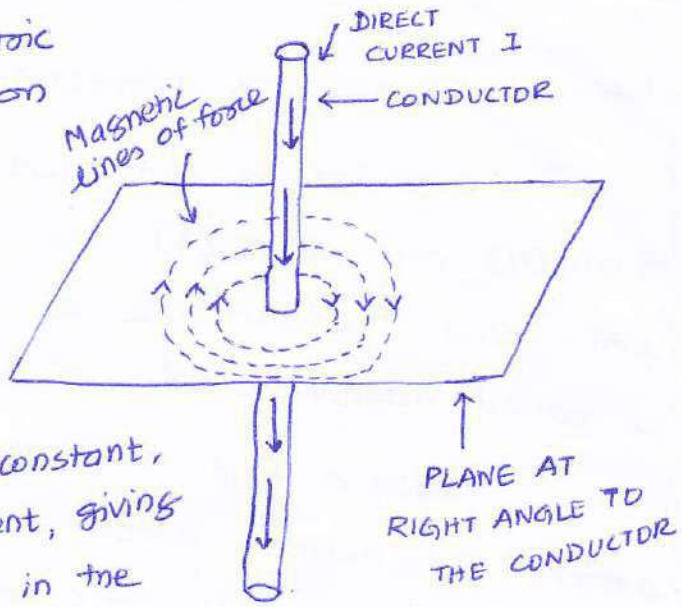
Hence every magnetic flux line starting from North Pole must end at south pole and complete the path from south to north internal to the magnet.



MAGNETIC FIELD DUE TO CURRENT CARRYING CONDUCTOR:

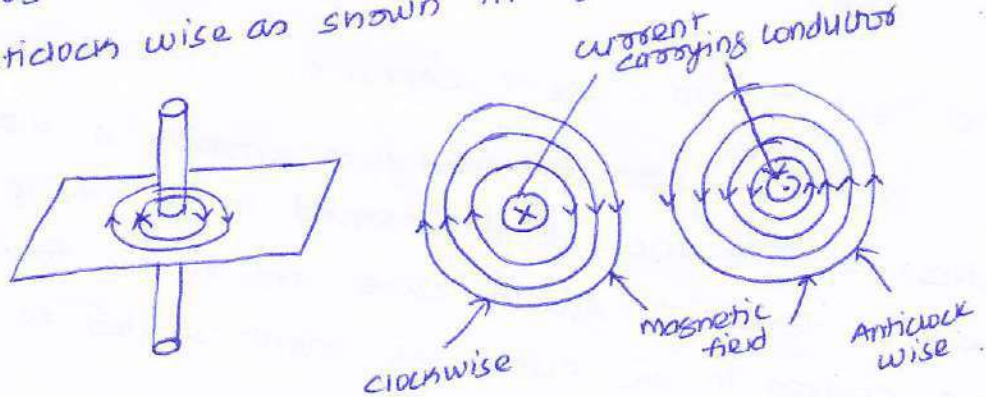
When a straight conductor carries a direct current, it Produces a magnetic field around it, all along its length. The lines of force in such a case are in the form of concentric circles in the planes at right angles to the conductor.

The direction of concentric circles around depends on the direction of current thro' the conductor. As long as the current is constant and current is time independent, magnetic lines of force are also constant, static and time independent, giving a steady magnetic field in the space around the conductor.



A right hand thumb rule is used to determine the direction of magnetic field around a conductor carrying a direct current. It states that, hold the current carrying conductor in right hand such that thumb pointing in the direction of current and $\parallel^{el}$ to the conductor, then coiled fingers point in the direction of the magnetic lines of flux around it.

The cross indicates that the current direction is going ~~up~~ into the plane of the paper away from the observer. The dot indicates that the current direction is coming out of the plane of the paper, coming towards the observer. using right hand thumb rule, the direction of magnetic flux around such a conductor is either clockwise(cs) anticlockwise as shown in figure.



The magnetic lines of force i.e magnetic flux lines always form a closed loop and exist in the form of concentric circles, around a current carrying conductor. The total number of magnetic lines of force is called a magnetic flux denoted as ϕ. It is measured in webers (Wb). one Wb means 10^8 lines of force.

MAGNETIC FIELD INTENSITY: ($\vec{H}$)

The quantitative measure of strongness or weakness of the magnetic field is given by magnetic field intensity or magnetic field strength. The magnetic field intensity at any point in the magnetic field is defined as the force experienced by a unit north Pole of one weber strength, when placed at that point.

The magnetic flux lines are measured in webers (Wb) while magnetic field intensity is measured in Newtons/weber [N/Wb] or amperes per meter [A/m]. or ampere Turns/meter [AT/m]. It is denoted by $\vec{H}$.

MAGNETIC FLUX DENSITY: ($\vec{B}$)

The total magnetic lines of force i.e magnetic flux crossing a unit area in a plane at right angles to the direction of flux is called magnetic flux density. It is denoted by $\vec{B}$. It is measured in Wb/m^2 which is also called Tesla (T).

RELATION BETWEEN $\vec{B}$ & $\vec{H}$.

In magnetostatics, the $\vec{B}$ and $\vec{H}$ are related to each other through the property of the region in which current carrying conductor is placed. It is called Permeability denoted as μ.

For free space

Permability is denoted as $\mu_0 = 4\pi \times 10^{-7}$ H/m

For any other region

a relative permability is specified as μ_r

and $\mu = \mu_0 \mu_r$.

The $\vec{B}$ and $\vec{H}$ are related as

$$\vec{B} = \mu \vec{H} \quad \mu = \mu_0 \mu_r \vec{H}$$

For free space

$$\vec{B} = \mu_0 \vec{H}$$

For nonmagnetic media

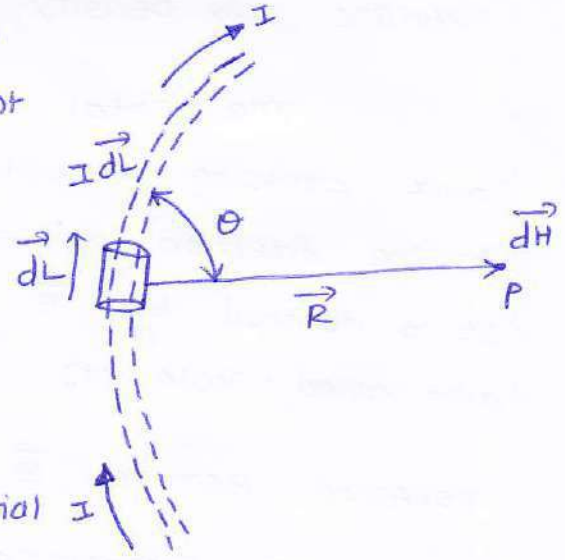
$\mu_r = 0$

For magnetic materials

$\mu_r > 1$.

BIOT-SAVART LAW:

Consider a conductor carrying a direct current I and a steady magnetic field produced around it. The Biot-savart law allows us to obtain the differential magnetic field intensity $d\vec{H}$, produced at point P, due to a differential current element I dL.



consider a differential length dL hence the differential current element is IdL. This is a very small part of the current carrying conductor. The point P is at a distance R from the differential current element. The θ is the angle b/w the differential current element and the line joining point P to the differential current element.

The Biot-Savarts law states that

The magnetic field intensity $\vec{dH}$ produced at a point P due to a differential current element IdL is,

1. Proportional to the product of current I and differential length dL.

2. The sine of the angle b/w the element and the line joining point P to the element

3. And Inversely proportional to the square of the distance R b/w point P and the element.

Mathematically, the Biot-Savarts law can be stated as,

$$\vec{dH} \propto \frac{IdL\sin\theta}{R^2} \quad \text{----(1)}$$

$$\vec{dH} = \frac{kIdL\sin\theta}{R^2} \quad \text{----(2)}$$

k → constant of proportionality

$$k = \frac{1}{4\pi}$$

$$\therefore \vec{dH} = \frac{IdL\sin\theta}{4\pi R^2} \quad \text{----(3)}$$

Let dL = Magnitude of vector length $\vec{dL}$ and

$\vec{a_R}$ = unit vector in the direction from differential current element to point P.

Then from rule of cross product

$$\vec{dL} \times \vec{a_R} = dL\,|\vec{a_R}|\sin\theta = dL\sin\theta \quad \text{---(4)}$$

Using (4) in (3) we get

$$\vec{dH} = \frac{I\,\vec{dL}\times\vec{a_R}}{4\pi R^2} \text{ A/m} \quad \text{---(5)}$$

But $\vec{a_R} = \frac{\vec{R}}{|\vec{R}|} = \frac{\vec{R}}{R}$ $\therefore$

$$\boxed{\vec{dH} = \frac{I\,\vec{dL}\times\vec{R}}{4\pi R^3} \text{ A/m}} \quad \text{---(6)}$$

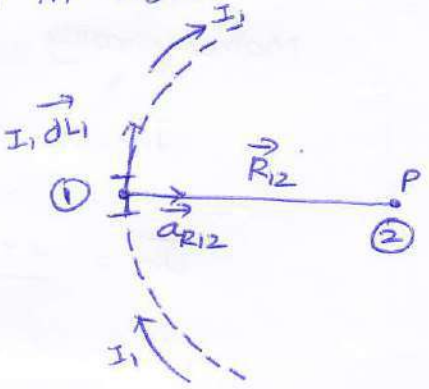
Equations (5) and (6) is the mathematical form of Biot-Savarts law.

The entire conductor is made up of all such differential elements. Hence to obtain total magnetic field Intensity $\vec{H}$, the equation (5) takes the integral form as,

$$\vec{H} = \oint \frac{I\vec{dL} \times \vec{a_R}}{4\pi R^2} \quad \text{---- (7)}$$

The closed line integral is required to ensure that all the current elements are considered. This is because current can flow only in the closed path, provided by the closed circuit.

If the current element is considered at Point 1 and Point P at Point 2, as shown in figure then,



$$\vec{dH_2} = \frac{I_1 \vec{dL_1} \times \vec{a_{R12}}}{4\pi R_{12}^2} \text{ A/m.}$$

$I_1 \rightarrow$ current flowing thro' dL_1 at Point 1

$\vec{dL_1} \rightarrow$ Differential vector length at Point 1

$\vec{a_{R12}} \rightarrow$ unit vector in the direction from element at Point 1 to the Point P at point 2

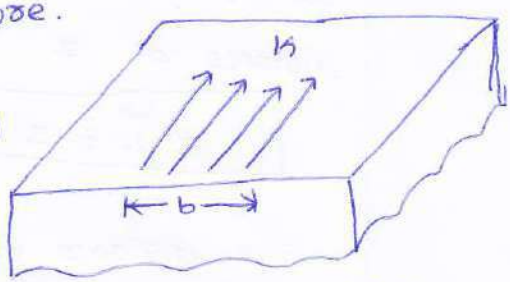
$$\vec{a_{R12}} = \frac{\vec{R_{12}}}{|\vec{R_{12}}|} = \frac{\vec{R_{12}}}{R_{12}}$$

$$\therefore H = \oint \frac{I_1 \vec{dL_1} \times \vec{a_{R12}}}{4\pi R_{12}^2} \text{ A/m} \quad \text{--- (8)}$$

This is called Integral form of Biot-Savart Law.

BIOT-SAVART LAW INTERMS OF DISTRIBUTED SOURCES

Consider a surface carrying a uniform current over its surface as shown in figure. Then the surface current density is denoted as $\vec{K}$ and is measured in (A/m)



Thus for uniform current density, current I in any width b is given by $I = Kb$, where width b is $\perp^r$ to the direction of current flow.

Thus if ds is the differential surface area considered of a surface having current density $\vec{K}$ then

$$I\,d\vec{L} = \vec{K}\,d\vec{s} \quad \text{---- (1)}$$

If the current density in a volume of a given conductor is $\vec{J}$ measured in A/m^2 then the differential volume dv we can write

$$I\,d\vec{L} = \vec{J}\,dv \quad \text{--- (2)}$$

Hence biot-savart's law can be expressed for surface current considering $\vec{K}\,ds$ while for volume current considering $\vec{J}\,dv$.

$$\therefore \vec{H} = \oint_S \frac{\vec{K} \times \vec{a_R}\,ds}{4\pi R^2} \text{ A/m}$$

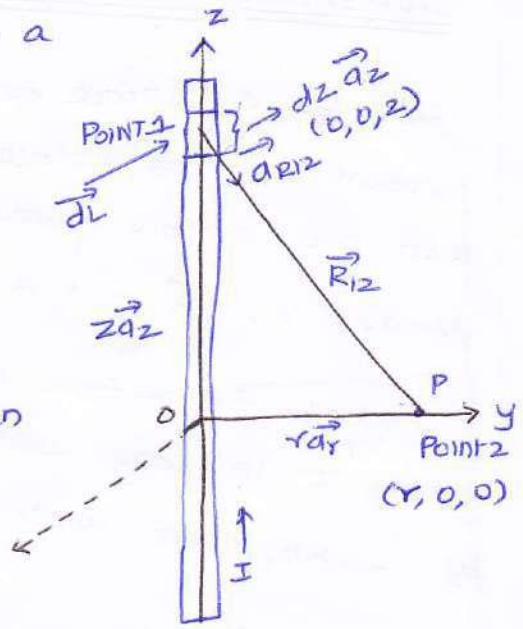
$$\vec{H} = \oint_{Vol} \frac{\vec{J} \times \vec{a_R}\,dV}{4\pi R^2} \text{ A/m} \quad \text{---- (3)}$$

The Biot-savart's law is also called Ampere's law for the current element.

$\vec{H}$ due to infinitely Long straight conductor:

Consider an infinitely long straight conductor, along z-axis the current passing through the conductor is a direct current of I Amp. The field intensity $\vec{H}$ at a Point P is to be calculated, which is at a distance 'r' from the z-axis.

Consider small differential element at Point 1, along the z-axis at a distance of z from origin.



$$\therefore \vec{I\,dL} = I\,dz\,\vec{a}_z \quad \text{---} (1)$$

The distance vector joining Point 1 to Point 2 is $\vec{R}_{12}$ and can be written as

$$\vec{R}_{12} = (r-0)\vec{a}_r + (0-0)\vec{a}_\phi + (0-z)\vec{a}_z$$

$$= r\vec{a}_r + 0\,\vec{a}_\phi - z\vec{a}_z$$

$$\therefore \vec{R}_{12} = r\vec{a}_r - z\vec{a}_z \quad \text{---} (2)$$

$$\vec{a}_{R12} = \frac{\vec{R}_{12}}{|\vec{R}_{12}|} = \frac{-z\vec{a}_z + r\vec{a}_r}{\sqrt{r^2+z^2}} = \frac{r\vec{a}_r - z\vec{a}_z}{\sqrt{r^2+z^2}}$$

$$\vec{dL} \times \vec{a}_{R12} = \begin{bmatrix} \vec{a}_r & \vec{a}_\phi & \vec{a}_z \\ 0 & 0 & dz \\ r & 0 & -z \end{bmatrix} = r\,dz\,\vec{a}_\phi$$

Note: while taking cross product, $|\vec{R}_{12}|$ is neglected for convenience and must be considered for further calculations.

$$\therefore \vec{I\,dL} \times \vec{a}_{R12} = \frac{I r\,dz\,\vec{a}_\phi}{\sqrt{r^2+z^2}}$$

According to Biot-Savart's law, $\vec{dH}$ at Point 2 is

$$\vec{dH} = \frac{\vec{I\,dL} \times \vec{a}_{R12}}{4\pi R_{12}^2} = \frac{I r\,dz\,\vec{a}_\phi}{\sqrt{r^2+z^2}} \cdot \frac{1}{4\pi (\sqrt{r^2+z^2})^2}$$

$$\frac{\vec{I\,dL} \times \vec{a}_{R12}}{4\pi R^2} = \frac{I\,dz\,\vec{a}_z}{4\pi (r^2+z^2)} \times \left(\frac{r\vec{a}_r - z\vec{a}_z}{\sqrt{r^2+z^2}}\right)$$

$$\vec{dH} = \frac{I r\,dz\,\vec{a}_\phi}{4\pi (r^2+z^2)^{3/2}}$$

$a_z \times a_r = a_\phi \qquad a_z \times a_z = 0$

$$d\vec{H} = \frac{I r\,dz}{4\pi (r^2+z^2)^{3/2}}\,a_\phi$$

Thus total field intensity $\vec{H}$ can be obtained by integrating $\vec{dH}$ over the entire length of the conductor

$$\therefore \vec{H} = \int_{z=-\infty}^{\infty} \vec{dH} = \int_{z=-\infty}^{\infty} \frac{I r dz \vec{a_\phi}}{4\pi (r^2+z^2)^{3/2}}$$

Put $z = r\tan\theta$ ← can be obtained by using $z = r\tan\theta$.

$z^2 = r^2\tan^2\theta$

and $dz = r\sec^2\theta\, d\theta$, $z=-\infty$, $\theta = -\pi/2$ & $z = +\infty$, $\theta = +\pi/2$

$$\therefore \vec{H} = \int_{\theta=-\pi/2}^{\theta=\pi/2} \frac{I r\, r\sec^2\theta\, d\theta \vec{a_\phi}}{4\pi (r^2+r^2\tan^2\theta)^{3/2}}$$

$$= \int_{-\pi/2}^{\pi/2} \frac{I r^2 \sec^2\theta\, d\theta \vec{a_\phi}}{4\pi r^3 (\sec^3\theta)} \quad \left[\because (r^2+r^2\tan^2\theta)^{3/2} = [r^2(1+\tan^2\theta)]^{3/2} = r^3\sec^3\theta\right] \quad 1+\tan^2\theta = \sec^2\theta.$$

$$\vec{H} = \int_{-\pi/2}^{\pi/2} \frac{I}{4\pi r} \cdot \frac{1}{\sec\theta} \cdot d\theta \cdot \vec{a_\phi} \Rightarrow \frac{I}{4\pi r} \int_{-\pi/2}^{\pi/2} \cos\theta\, d\theta\, \vec{a_\phi}$$

$$\vec{H} = \frac{I}{4\pi r} [\sin\theta]_{-\pi/2}^{\pi/2} \vec{a_\phi} = \frac{I}{4\pi r} \left[\sin\pi/2 - \sin(-\pi/2)\right] \vec{a_\phi}$$

$$\vec{H} = \frac{I}{4\pi r} [1-(-1)] \vec{a_\phi} = \frac{2I}{4\pi r} \vec{a_\phi}$$

$$\boxed{\vec{H} = \frac{I}{2\pi r} \vec{a_\phi} \ A/m} \qquad \boxed{\vec{B} = \mu\vec{H} = \frac{\mu I}{2\pi r} \vec{a_\phi} \ Wb/m^2}$$

AMPERE'S CIRCUITAL LAW:

In electrostatics, the Gauss's law is useful to obtain the $\vec{E}$ in case of complex problems. similarly in the magneto-statics, the complex problems can be solved using a law called Ampere's circuital law (or) Ampere's work law.

The ampere's circuital law states that,

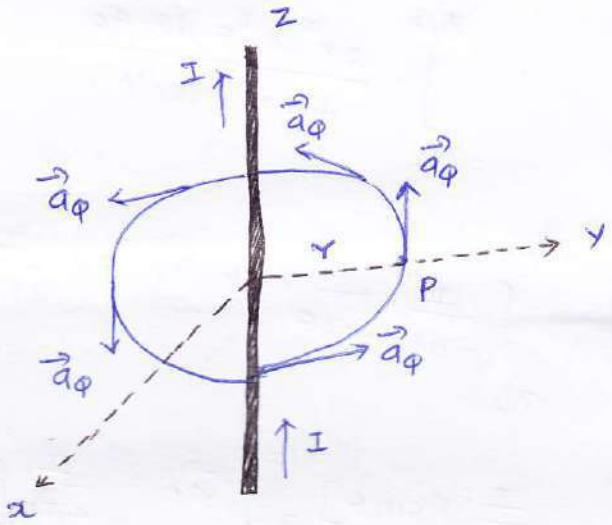
The line integral of magnetic field intensity $\vec{H}$ around a closed path is exactly equal to the direct current enclosed by that path.

The mathematical representation of Ampere's circuital law is,

$$\oint \vec{H} \cdot \vec{dL} = I$$

PROOF FOR AMPERE'S CIRCUITAL LAW:

Consider a long straight conductor carrying direct current I placed along z-axis as shown in figure below.



Consider a closed circular path of radius r which encloses the straight conductor carrying direct current I. The point P is at a distance r from the conductor. Consider $\vec{dL}$ at point P which is in $\vec{a}_\phi$ direction, tangential to circular path at point P.

$$\therefore \vec{dL} = r\, d\phi\, \vec{a}_\phi \quad \text{---} (1)$$

While $\vec{H}$ obtained at point P, from Biot-savart's law due to infinitely long conductor is

$$\vec{H} = \frac{I}{2\pi r}\vec{a}_\phi \quad \text{---} (2)$$

[from (5) of unit IV]

Page NO

$$\therefore \vec{H}.\vec{dL} = \frac{I}{2\pi r}\vec{a_\phi}.r\,d\phi\,\vec{a_\phi}$$

$$\vec{H}.\vec{dL} = \frac{I r\,d\phi}{2\pi r}$$

$$\vec{H}.\vec{dL} = \frac{I\,d\phi}{2\pi} \quad ---(3)$$

Integrating (3) over the entire closed path,

$$\oint \vec{H}.\vec{dL} = \int_{\phi=0}^{2\pi} \frac{I\,d\phi}{2\pi} = \frac{I}{2\pi}[\phi]_0^{2\pi} = I$$

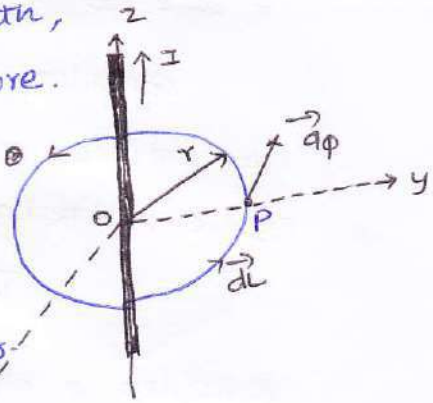
= current carried by conductor.

This proves that the integral $\vec{H}.\vec{dL}$ along closed path gives direct current enclosed by that closed path.

APPLICATION OF AMPERE'S CIRCUITAL LAW:

$\vec{H}$ due to infinitely straight conductor

Consider an infinitely long straight ~~wire~~ conductor placed along z-axis, carrying a direct current I as shown in the figure. consider the Amperian closed path, enclosing the conductor as shown in figure.



consider point P on the closed path at which $\vec{H}$ is to be obtained. The radius of the path is r and hence P is at a $\perp^r$ distance from the conductor.

The magnitude of $\vec{H}$ depends on r and the direction is always tangential to the closed path i.e $\vec{a_\phi}$. So $\vec{H}$ has only component in $\vec{a_\phi}$ direction say H_ϕ.

Consider elementary length $\vec{dL}$ at a point P and in cylindrical co-ordinates it is $r\,d\phi$ in $\vec{a_\phi}$ direction.

$$\therefore \vec{H} = H_\phi \vec{a_\phi} \quad \text{and} \quad \vec{dL} = r\,d\phi\,\vec{a_\phi}$$

$$\therefore \vec{H}.\vec{dL} = H_\phi \vec{a_\phi}.r\,d\phi\,\vec{a_\phi} = H_\phi r\,d\phi$$

According to Ampere's circuital law,

$$\oint \vec{H} \cdot d\vec{L} = I.$$

$$\int_{\phi=0}^{2\pi} H_\phi r \, d\phi = I$$

$$H_\phi r \, [\phi]_0^{2\pi} = I$$

$$H_\phi r 2\pi = I$$

$$\Rightarrow H_\phi = \frac{I}{2\pi r}$$

Hence $\vec{H}$ at Point P is given by

$$\boxed{\vec{H} = H_\phi \vec{a}_\phi = \frac{I}{2\pi r} \vec{a}_\phi \quad A/m}$$

$$\therefore \boxed{\vec{B} = \mu \vec{H} = \frac{\mu I}{2\pi r} \vec{a}_\phi}$$

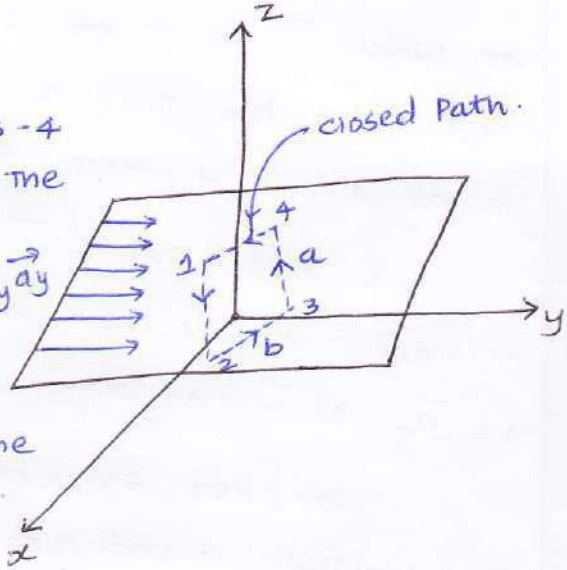
$\vec{H}$ due to infinite sheet of current:

Consider an infinite sheet of current in the z=0 plane. The surface current density is $\vec{K}$. The current is flowing in Positive y direction hence

$$\vec{K} = K_y \vec{a}_y$$

consider a closed path 1-2-3-4 as shown in fig. The width of the Path is 'b' while height is 'a'.

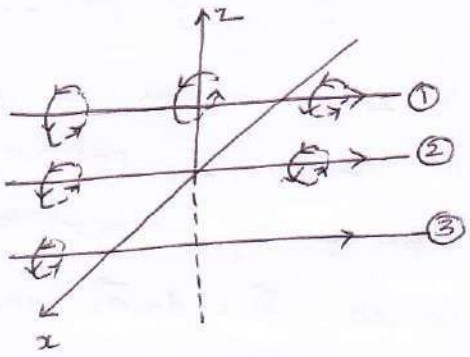
It is $\perp^r$ to the direction of current hence in xz plane.

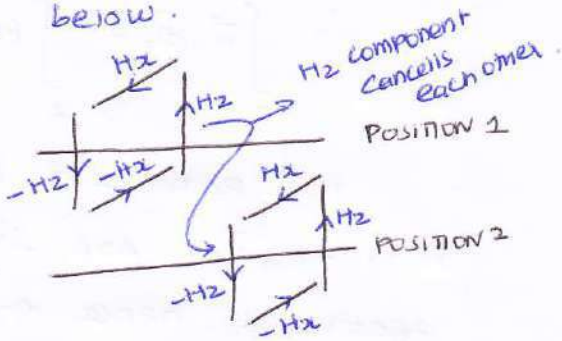


The current flowing across the distance 'b' is given by $K_y b$.

$$\therefore I_{enc} = K_y b \text{ ---- } (1).$$

Consider the magnetic lines of force due to the current in $\vec{a_y}$ direction, according to the right hand thumb rule. These are shown in figure below.





It is clear that in b/w two very closely spaced conductors, the components of $\vec{H}$ in z direction are oppositely directed [$-H_z$ for position 1 and $+H_z$ for position 2 b/w the two opposite positions]. All such components cancel eachother and hence $\vec{H}$ cannot have any component in z-direction.

As current is flowing in y direction, $\vec{H}$ cannot have component in y direction.

So $\vec{H}$ has only component in x direction.

$$\left.\begin{aligned}\vec{H} &= H_x \vec{a_x} \quad \text{for } z > 0 \\ &= -H_x \vec{a_x} \quad \text{for } z < 0\end{aligned}\right\} \text{---- (2)}$$

Applying Ampere's circuital law

$$\oint \vec{H} \cdot \vec{dL} = I_{enc} \text{ ---- (3)} = \int_1^2 + \int_2^3 + \int_3^4 + \int_4^1 [\vec{H} \cdot \vec{dL}]$$

Evaluate the integral along the path 1-2-3-4-1.

For path 1-2, $\vec{dL} = dz\,\vec{a_z}$

3-4, $\vec{dL} = -dz\,\vec{a_z}$

But $\vec{H}$ is in x-direction while $\vec{a_x} \cdot \vec{a_z} = 0$.

Hence along the paths 1-2 and 3-4, the integral

$$\oint \vec{H} \cdot \vec{dL} = 0.$$

consider path 2-3 along which $\vec{dL} = dx\,\vec{a_x}$

$$\therefore \int_2^3 \vec{H}.\vec{dL} = \int_2^3 (H_x \vec{a_x}).(dx\,\vec{a_x}) = -H_x \int_2^3 dx = bH_x \quad ---(4)$$

The path 2-3 is lying in $z<0$ region for which $\vec{H}$ is $-H_x\vec{a_x}$. And limits from 2 to 3, positive x to Negative x hence effective sign of the integral is +ve

consider path 4-1 along which $\vec{dL} = dx\,\vec{a_x}$ and it is in the region $z>0$ hence $\vec{H} = H_x\vec{a_x}$

$$\therefore \int_4^1 \vec{H}.\vec{dL} = \int_4^1 (H_x\vec{a_x}).(dx\,\vec{a_x}) = H_x \int_4^1 dx = bH_x \quad ---(5)$$

$\therefore$ sub (4) and (5) in (3) we get

$$\oint \vec{H}.\vec{dL} = bH_x + bH_x = 2bH_x \quad ---(6)$$

usin (1) in eqn (6) we get

$$\oint \vec{H}.\vec{dL} = 2bH_x = I_{enc} = K_y b$$

$$\therefore 2bH_x = K_y b$$

$$H_x = \frac{1}{2} K_y$$

Hence $\vec{H} = \frac{1}{2} K_y \vec{a_x}$ for $z>0$

$= -\frac{1}{2} K_y \vec{a_x}$ for $z<0$

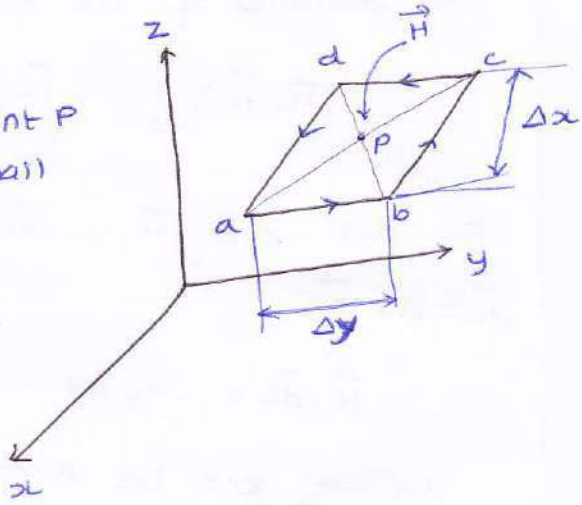
In general for an infinite sheet of current density $\vec{K}$ A/m we can write

$$\vec{H} = \frac{1}{2}\vec{K} \times \vec{a_N}$$

Where $\vec{a_N}$ = unit vector normal from the current sheet to the point at which $\vec{H}$ is to be obtained.

CURL:

Consider the differential surface element having sides Δx and Δy plane, as shown in figure below. The unknown current has produced $\vec{H}$ at the centre of the incremental closed path.



The total magnetic field at point P which is at the centre of the small rectangle is,

$$\vec{H} = H_{x0}\vec{a}_x + H_{y0}\vec{a}_y + H_{z0}\vec{a}_z \quad \text{--- (1)}$$

while the total current density is given by,

$$\vec{J} = J_x\vec{a}_x + J_y\vec{a}_y + J_z\vec{a}_z \quad \text{--- (2)}$$

To apply Ampere's circuital law to this closed path, let us evaluate the closed line integral of $\vec{H}$ about this path in the direction abcda. According to right hand thumb rule the current is in $\vec{a}_z$ direction.

Along path a-b,

$$\vec{H} = H_y\vec{a}_y \;\&\; \vec{dL} = \Delta y\,\vec{a}_y$$

$$\therefore \vec{H}.\vec{dL} = H_y\Delta y \quad \text{---- (3)}$$

The intensity H_y along a-b can be expressed interms of H_{y0} existing at P and the rate of change of H_y in the x-direction with x.

The distance in x direction of a-b from point P is $\left(\frac{\Delta x}{2}\right)$. Hence $\vec{H}.\vec{dL}$ along a-b can be expressed as

$$(\vec{H}.\vec{dL})_{ab} = \left[H_{y0} + \frac{\partial H_y}{\partial x}\left(\frac{\Delta x}{2}\right)\right]\Delta y \quad \text{--- (4)}$$

For Path b-c, $\vec{H}$ is in $-\vec{a}_x$ direction hence $-H_x\vec{a}_x$ and $\vec{dL} = \Delta x\,\vec{a}_x$

$$\therefore \vec{H}.\vec{dL} = -H_x\Delta x \quad \text{--- (5)}$$

Now H_x can be expressed interms of H_{x0} at Point P and rate of change of H_x in y direction and y.

$$H_x = H_{x0} + \frac{\Delta y}{2} \frac{\partial H_x}{\partial y}$$

The distance of bc from P is $\Delta y/2$.

$$\therefore (\vec{H} \cdot \vec{dL})_{b-c} = -\left[H_{x0} + \frac{\partial H_x}{\partial y} \frac{\Delta y}{2}\right] \Delta x \quad \text{--- (6)}$$

For Path c-d $\vec{H}$ is in $-\vec{a_y}$ direction hence $-H_y \vec{a_y}$ and $\vec{dL} = \Delta y \vec{a_y}$

$$\therefore \vec{H} \cdot \vec{dL} = -H_y \Delta y \quad \text{---- (7)}$$

But H_y can be expressed in terms of H_{y0} and rate of change of Hy in negative x direction. The distance of CD from point P is $(\Delta x/2)$ in negative x direction

$$\therefore H_y = H_{y0} - \frac{\Delta x}{2} \frac{\partial H_y}{\partial x}$$

$$\therefore (\vec{H} \cdot \vec{dL})_{c-d} = -\left[H_{y0} - \frac{\Delta x}{2} \frac{\partial H_y}{\partial x}\right] \Delta y \quad \text{--- (8)}$$

For Path d-a, $\vec{H}$ is in $+\vec{a_x}$ direction hence $H_x \vec{a_x}$ and $\vec{dL} = \Delta x \vec{a_x}$

$$\therefore \vec{H} \cdot \vec{dL} = H_x \Delta x \quad \text{--- (9)}$$

But H_x can be expressed interms of H_{x0} and rate of change of H_x in negative y direction. The distance of DA from Point P is $\left(\frac{\Delta y}{2}\right)$ in negative y direction

$$\therefore H_x = \left[H_{x0} - \frac{\Delta y}{2} \frac{\partial H_x}{\partial y}\right] \quad \text{(10)}$$

$$\therefore (\vec{H} \cdot \vec{dL})_{d-a} = \left[H_{x0} - \frac{\Delta y}{2} \frac{\partial H_x}{\partial y}\right] \Delta x \quad \text{--- (10)}$$

Total $\vec{H}.\vec{dL}$ can be obtained by adding equations (4), (6), (8) and (10)

$$\therefore \vec{H}.\vec{dL} = H_{yo}\Delta y + \frac{\Delta x \Delta y}{2}\frac{\partial H_y}{\partial x} - H_{xo}\Delta x - \frac{\Delta x \Delta y}{2}\frac{\partial H_x}{\partial y}$$

$$- H_{yo}\Delta y + \frac{\Delta x \Delta y}{2}\frac{\partial H_y}{\partial x} + H_{xo}\Delta x - \frac{\Delta x \Delta y}{2}\frac{\partial H_x}{\partial y}.$$

$$\therefore \oint \vec{H}.\vec{dL} = \Delta x \Delta y \left[\frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y}\right] \quad \text{---- (11)}$$

According to Ampere's circuital law, this integral must be current enclosed by the differential element.

current enclosed = current density normal to closed path × Area of that closed path

$$I_{encl.} = J_z \Delta x \Delta y \quad \text{--- (12)}$$

where J_z = current density in $\vec{a}_z$ direction as the current enclosed is in $\vec{a}_z$ direction.

From eqn (11) & (12)

$$\oint \vec{H}.\vec{dL} = I_{encl.}$$

$$\oint \vec{H}.\vec{dL} = \Delta x \Delta y \left[\frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y}\right] = J_z \Delta x \Delta y$$

$\div \Delta x \Delta y$

$$\frac{\oint \vec{H}.\vec{dL}}{\Delta x \Delta y} = \left[\frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y}\right] = J_z \quad \text{---(13)}$$

This gives accurate result as the closed path shrinks to a point (ie) $\Delta x \Delta y$ area tends to zero.

$$\therefore \lim_{\Delta x \Delta y \to 0} \frac{\oint \vec{H}.\vec{dL}}{\Delta x \Delta y} = \frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y} = J_z \quad \text{---(14)}$$

considering incremental closed path in yz plane we get the current density normal to it i.e in y-direction. so we can write,

$$\lim_{\Delta y \Delta z \to 0} \frac{\oint \vec{H} \cdot d\vec{L}}{\Delta y \Delta z} = \frac{\partial H_z}{\partial y} - \frac{\partial H_y}{\partial z} = J_x \quad \text{---} (15)$$

and

$$\lim_{\Delta z \Delta x \to 0} \frac{\oint \vec{H} \cdot d\vec{L}}{\Delta z \Delta x} = \frac{\partial H_x}{\partial z} - \frac{\partial H_z}{\partial x} = J_y \quad \text{----} (16)$$

In general we can write,

$$\lim_{\Delta S_N \to 0} \frac{\oint \vec{H} \cdot d\vec{L}}{\Delta S_N} = J_N \quad \text{---} (17)$$

→ curl.

where J_N = current density normal to the surface Δs.

The term on left hand side of the equation is called curl $\vec{H}$. The ΔS_N is area enclosed by the closed line integral.

the total $\vec{J}$ now can be obtained by adding eqn (14), (15) and (16).

$$\therefore \quad \vec{J} = J_x \vec{a}_x + J_y \vec{a}_y + J_z \vec{a}_z$$

$$= \left[\frac{\partial H_z}{\partial y} - \frac{\partial H_y}{\partial z}\right] \vec{a}_x + \left[\frac{\partial H_z}{\partial z} - \frac{\partial H_z}{\partial x}\right] \vec{a}_y + \left[\frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y}\right] \vec{a}_z$$

$$\boxed{\vec{J} = \text{curl } \vec{H} = \nabla \times \vec{H}} \quad \text{---} (18)$$

The curl $\vec{H}$ is indicated by $\nabla \times \vec{H}$ which is cross product of operator 'del' and $\vec{H}$

The equation (18) is called the Point form of Ampere's circuital law.

$$\boxed{\text{curl } \vec{H} = \nabla \times \vec{H} = \vec{J}}$$

This is one of the Maxwell's equations.

The curl of a vector in the direction of the unit vector is the ratio of the line integral of the vector around a closed contour, to the enclosed area bounded by the contour, as the enclosed area diminished to zero.

Properties of curl:

1. The curl of a vector is a vector quantity
2. $\nabla \times (\vec{A} + \vec{B}) = \nabla \times \vec{A} + \nabla \times \vec{B}$
3. $\nabla \times \nabla \times \vec{A} = \nabla(\nabla \cdot \vec{A}) - \nabla^2 A$
4. The divergence of a curl is zero

$$\nabla \cdot (\nabla \times \vec{A}) = 0.$$

5. The curl of a gradient of a vector is zero

$$\nabla \times \nabla V = 0.$$

STROKE'S THEOREM:

Analogous to the divergence theorem in electrostatics, there exists stooke's theorem in magnetostatics. The stooke's theorem relates the line integral to a surface integral.

The stooke's theorem states that,

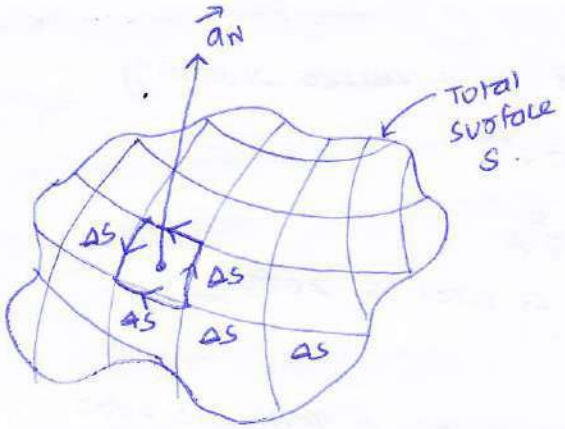
"The line integral of vector $\vec{A}$ around a closed path L is equal to the integral of curl of $\vec{A}$ over the open surface S enclosed by the closed path L".

The Theorem is applicable only when $\vec{A}$ and $\nabla \times \vec{A}$ are continuous on the surface S.

$$\oint_L \vec{H} \cdot \vec{dL} = \int_S (\nabla \times \vec{H}) \cdot \vec{ds}$$

PROOF'S OF STROKE'S THEOREM:

Consider a surface S which is splitted into number of incremental surfaces. Each incremental surface is having area Δs as shown in figure.



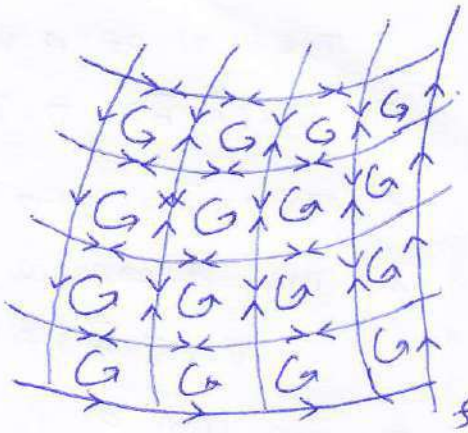


fig (b)

Applying by definition of the curl to any of these incremental surfaces we can write

$$(\nabla \times \vec{H})_N = \frac{\oint \vec{H} \cdot \vec{dL}_{\Delta S}}{\Delta S} \quad \text{--- (1)}$$

where

$N \rightarrow$ Normal to ΔS according to right hand rule

$dL_{\Delta S} \rightarrow$ Perimeter of the incremental surface ΔS.

Now the curl of $\vec{H}$ in the normal direction is the dot product of curl of $\vec{H}$ with $\vec{a}_N$, where $\vec{a}_N$ is unit vector, normal to the surface ΔS, according to right hand rule,

$$\therefore (\nabla \times \vec{H})_N = (\nabla \times \vec{H}) \cdot \vec{a}_N$$

$$\therefore \oint \vec{H} \cdot \vec{dL}_{\Delta S} = (\nabla \times \vec{H}) \cdot \vec{a}_N \, \Delta S$$

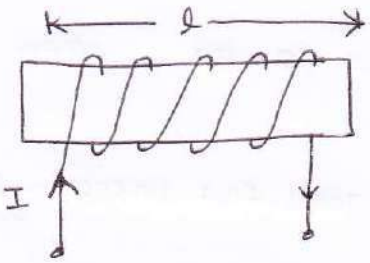
$$\therefore \oint \vec{H} \cdot \vec{dL}_{\Delta S} = (\nabla \times \vec{H}) \cdot \vec{\Delta S}$$

To obtain total curl for every incremental surface, add the closed line integrals for each ΔS. From fig (b), it can be seen that at a common boundary b/w the two incremental surfaces, The line integral is getting cancelled as the boundary is getting traced in two opposite directions.

INDUCTANCE OF A SOLENOID:

Consider a solenoid of N turns as shown in fig.

Let the current flowing through the solenoid be I Amps. Let the length of the solenoid be l and the cross-section area be A.



Magnetic field intensity H inside the solenoid is given by,

$$H = \frac{NI}{l} \ (A/m) \quad \text{--- (1)}$$

Total flux linkage is given by

$$\text{Total flux linkage} = N\phi = N(B)(A)$$

$$[\because \phi = BA \quad Wb = \frac{Wb}{m^2} m^2]$$

$$N\phi = NBA$$

But $B = \mu H$

$$\therefore N\phi = N(\mu H)A$$

$$= N\mu HA$$

$$= N\mu\left[\frac{NI}{l}\right]A \Rightarrow N\phi = \frac{N\mu N^2 IA}{l}$$

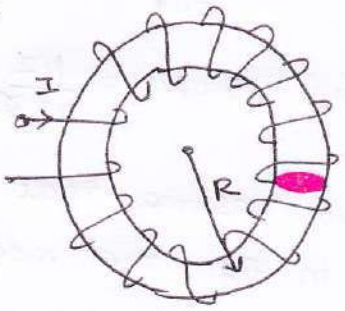
Inductance of a solenoid is given by

$$L = \frac{\text{Total flux linkage}}{\text{Total current}} = \frac{N\mu N^2 IA/l}{I}$$

$$\boxed{L = \frac{\mu N^2 A}{l}}$$

INDUCTANCE OF A TOROID:

Consider a toroid ring with N turns and carrying current I. Let the radius of the toroid be R as shown in fig.



The magnetic flux density inside a toroidal ring is given by

$$B = \frac{\mu NI}{2\pi R} \quad \text{--- (1)}$$

$$[\because B = \mu H = \mu \cdot \left(\frac{NI}{l}\right) \rightarrow \text{Perimeter of circle}$$

$$= \mu\left(\frac{NI}{2\pi R}\right)$$

Total flux of a toroidal ring having N turns is given by,

Total flux linkage $= N\Phi$

But $\Phi = BA$ where $A \rightarrow$ Area of cross-section of a toroidal ring.

$\therefore$ Total flux linkage $= N(B)(A) = N\left[\frac{\mu NI}{2\pi R}\right](A) = \frac{\mu N^2 IA}{(2\pi R)}$

The inductance of a toroid is given by,

$$L = \frac{\text{Total flux linkage}}{\text{Total current}}$$

$$= \frac{\mu N^2 IA}{(2\pi R)I} = \frac{\mu N^2 A}{2\pi R} \text{ H.}$$

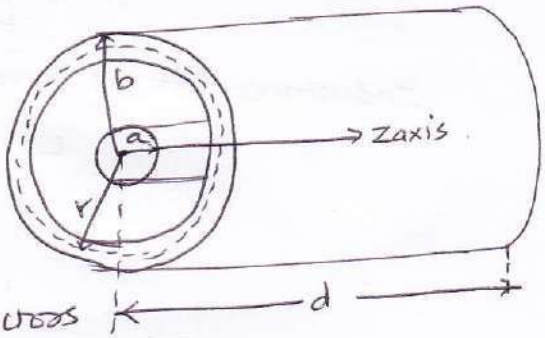
$$\boxed{L = \frac{\mu N^2 A}{2\pi R} \text{ H}}$$

Where $A \rightarrow$ Area of cross section of Toroidal ring $= \pi r^2 m^2$

INDUCTANCE OF A CO-AXIAL CABLE:

Consider a co-axial cable with inner conductor radius 'a' and outer conductor radius 'b'.

Let the current thro' the co-axial cable be I.



For the co-axial cable the magnetic field intensity at any point b/w inner and outer conductors is given by

$$H = \frac{I}{2\pi r} \quad \text{where} \quad a < r < b \quad \text{---} (1)$$

$$B = \mu H = \frac{\mu I}{2\pi r} \quad \text{---} (2)$$

Let $\vec{B} = \frac{NI}{2\pi r}\vec{a_\phi}$ (T)

The total magnetic flux is given by

$$\phi = \int_S \vec{B} \cdot \vec{ds}$$

Now $\vec{ds} = dr\,dz\,\vec{a_\phi}$ [from cylindrical co-ordinate system].

$$\therefore \phi = \int_{z=0}^{z=d} \int_{r=a}^{r=b} \frac{NI}{2\pi r}\vec{a_\phi} \cdot dr\,dz\,\vec{a_\phi}$$

$$= \frac{NI}{2\pi} \int_{z=0}^{z=d} dz \int_{r=a}^{r=b} \frac{1}{r}\,dr$$

$$= \frac{NI}{2\pi} [z]_0^d \; [\ln r]_a^b$$

$$\boxed{\phi = \frac{NI}{2\pi} d \ln\left(\frac{b}{a}\right)} \quad \text{--- (3)}$$

The inductance of a co-axial cable is given by

$$L = \frac{\text{Total flux linkage}}{\text{Total current}}$$

$$\boxed{L = \frac{\frac{NId}{2\pi}\ln\left(\frac{b}{a}\right)}{I} = \frac{Nd}{2\pi}\ln\left(\frac{b}{a}\right) \text{ H.}}$$

The Inductance of a co-axial cable may be expressed per unit length as

$$\boxed{\frac{L}{d} = \frac{N}{2\pi}\ln\left(\frac{b}{a}\right) \text{ H/m.}}$$

MAGNETIC ENERGY - ENERGY STORED IN A MAGNETIC FIELD

Energy stored in a inductor is given by

$$W_m = \frac{1}{2}LI^2$$

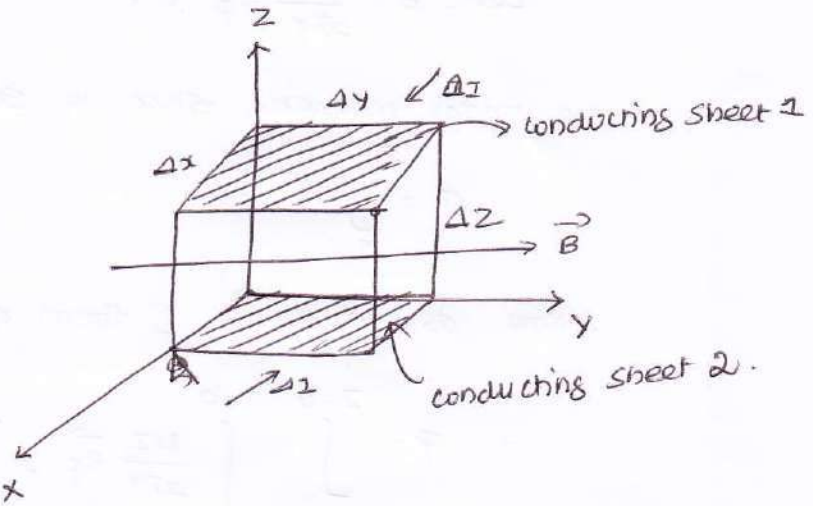
$$L = \frac{\Phi}{I} = \frac{B}{I}$$

$$\Delta L = \frac{\Delta \Phi}{\Delta I} = \frac{B \Delta S}{\Delta I}$$

ΔS = differential surface area

$$= \Delta x \, \Delta z$$

$$\therefore \Delta L = \frac{B (\Delta x \Delta z)}{\Delta I} \quad \text{-- (1)}$$



$$B = \mu H$$

$$\therefore \Delta L = \frac{\mu H \Delta x \Delta z}{\Delta I}$$

$$\Delta I = H (\Delta y) \quad \text{(} \because \text{conducting sheet current is in y direction)} \quad \text{---(2)}$$

$\therefore$ Energy stored

$$\Delta W_m = \frac{1}{2} \Delta L \, \Delta I^2 \quad \text{-- (3)}$$

sub (1) & (2) in (3) we get

$$\Delta W_m = \frac{1}{2} \left[\frac{\mu H \Delta x \Delta z}{\Delta I} \right] \left[H (\Delta y) \right]^2$$

$$= \frac{1}{2} \mu H^2 (\Delta x \Delta y \Delta z)$$

But $\Delta V = \Delta x \Delta y \Delta z$

$$\therefore \Delta W_m = \frac{1}{2} \mu H^2 \Delta V$$

magnetostatics energy density function

$$W_m = \lim_{\Delta V \to 0} \frac{\Delta W_m}{\Delta V} = \frac{1}{2} \mu H^2 \ (J/m^3)$$

different forms

$$W_m = \frac{1}{2} (\mu H) H = \frac{1}{2} B H$$

$$= \frac{1}{2} \mu \left(\frac{B}{\mu} \right)^2 = \frac{B^2}{2\mu}$$

UNIT-V

ELECTROMAGNETIC WAVES.

In previous chapters we delt the concepts of electrostatic and magnetostatic fields, which donot change w.r.to time. Hence these fields are called as static fields or time invariant fields.

In this chapter - time varying or dynamic fields.

Maxwell's eq - describe relationship b/n time varying electric & magnetic fields

FARADAY'S LAW & LENZ'S LAW:

Time varying electric field & magnetic field are interdependent

In 1820, Prof. Hans christian Oersted demonstrated that a compass needle deflected due to an electric current.

After 10 years, Michael Faraday, a British scientist proved that a magnetic field could produce a current.

According to Faraday's experiment, a static magnetic field cannot produce any current flow, but with a time varying field, an electro motive force (emf) is induced, which may drive a current in a closed path or circuit.

This emf is nothing but a voltage that induces from changing magnetic fields or motion of the conductors in a magnetic field.

STATEMENT:

The electromagnetic force (e.m.f) induced in a closed path (or circuit) is proportional to rate of change of magnetic flux enclosed by the closed path [or linked with the circuit]

Faraday's law can be stated as

$$e = -N\frac{d\phi}{dt} \text{ volts}$$

$N \rightarrow$ No. of turns in the circuit

$e \rightarrow$ Induced e.m.f

The minus sign indicates that the direction of the induced e.m.f is such that to produce a current which will produce a magnetic field which will oppose the original field.

DISPLACEMENT CURRENT DENSITY & DISPLACEMENT CURRENT

For static electromagnetic fields, according to ampere's circuital law, we can write

$$\nabla \times \vec{H} = \vec{J} \quad \text{--- (1)}$$

Taking divergence on both sides we get

$$\nabla \cdot (\nabla \times \vec{H}) = \nabla \cdot \vec{J} \quad \text{--- (2)}$$

But according to vector identity, divergence of the curl of any vector field is zero

$$\therefore \nabla \cdot (\nabla \times \vec{H}) = \nabla \cdot \vec{J} = 0 \quad \text{--- (3)}$$

But the equation of continuity is given by,

$$\nabla \cdot \vec{J} = -\frac{\partial \rho_v}{\partial t} \quad \text{[Page No 3 of chapter 3]} \quad \text{--- (4)}$$

From eqn (4) it is clear that when $\frac{\partial \rho_v}{\partial t} = 0$, then only eqn (3) becomes true. Thus equation (3) and (4) are not compatible for time varying fields.

Thus equation (1) must be modified by adding one unknown term say $\vec{N}$

∴ The equation (1) becomes

$$\nabla \times \vec{H} = \vec{J} + \vec{N} \quad \text{--- (5)}$$

Again after taking divergence on both the sides,

$$\nabla \cdot (\nabla \times \vec{H}) = \nabla \cdot \vec{J} + \nabla \cdot \vec{N} = 0 \quad \text{--- (6)}$$

As $\nabla \cdot \vec{J} = -\frac{\partial \rho_v}{\partial t}$, to get correct conditions we must write,

$$\nabla \cdot \vec{N} = \frac{\partial \rho_v}{\partial t} \quad \text{--- (7)}$$

But according to Gauss's law

$$\rho_v = \nabla \cdot \vec{D}$$

Lenz law

The direction of induced emf is such that it opposes the cause producing it.

$e = -N \frac{d\phi}{dt}$ volts

$e = \oint \bar{E} \cdot d\bar{L}$

Induced emf is equal to the voltage in the circuit & changes as the rate of change of magnetic flux passing through a specified area

$\phi = \int \bar{B} \cdot d\bar{s}$ B = Magnetic flux density

$\therefore e = -N \frac{d\phi}{dt} = -\frac{d\phi}{dt}$

$e = -\frac{d}{dt} \int_s \vec{B} \cdot d\vec{s}$

$e = \oint \bar{E} \cdot d\bar{l} = -\frac{d}{dt} \int_s \bar{B} \cdot d\bar{s}$

$$\oint E \cdot dl = -\int \frac{\partial \bar{B}}{\partial t} d\bar{s}$$

Partial derivative as time varying

The emf induced in stationary closed path due to time varying $\bar{B}$ is called stationary induced emf or transformer emf. If time varying closed path, dynamically induced emf or motional emf

Thus replacing ρ_v by $\nabla . \vec{D}$ in (7) we get

$$\nabla . \vec{N} = \frac{\partial}{\partial t} (\nabla . \vec{D}) = \nabla . \frac{\partial \vec{D}}{\partial t}$$

Comparing two sides of the equation,

$$\vec{N} = \frac{\partial \vec{D}}{\partial t}$$

Now we can write Ampere's circuital law in point form as,

$$\nabla \times \vec{H} = \vec{J}_c + \frac{\partial \vec{D}}{\partial t} \quad \text{--- (8)}$$

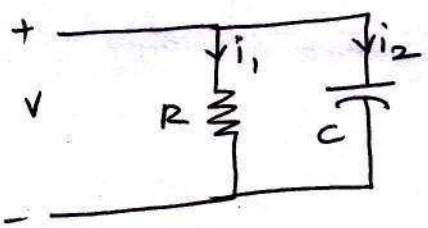
$\vec{J}_c$: Conduction current density. c indicates that the current is due to the moving charges.

$\frac{\partial \vec{D}}{\partial t}$: represents current density (A/m^2). As this quantity is obtained from time varying electric flux density. This is also called displacement density. (or) displacement current density ($\vec{J}_D$)

$$\therefore \quad \nabla \times \vec{H} = \vec{J}_c + \vec{J}_D$$

PHYSICAL SIGNIFICANCE OF DISPLACEMENT CURRENT:

Consider a $\parallel^{el}$ circuit with Resistor 'R' and capacitor 'C'



Consider that this $\parallel^{el}$ combination is driven by the time varying i.e sinusoidal voltage V.

It is obvious that the nature of current flowing through the resistor R i.e i_1 is different than that flowing through capacitor C i.e i_2.

The current flowing through R is due to due to the actual motion of charges. Thus the current through resistor can be written as,

$$i_1 = \frac{V}{R} \quad \text{--- (1)}$$

This is called conduction current as the current is flowing because of actual motion of charges. Let it be denoted by i_c.

Let A be the cross-sectional area of resistor, then the conduction current density is given by,

$$\vec{J_c} = \frac{i_c}{A} = \sigma \vec{E} \quad \text{---} (2)$$

$\frac{i_c}{A}$ $\quad i_c = \frac{V}{R} = \frac{V}{RA} = \sigma \frac{V}{A} = \sigma \vec{E}$ $\quad \sigma = \frac{1}{R}$ $E = \frac{V}{A}$

Now assume that the initial charge on a capacitor is zero. Then for time varying voltage applied across $\parallel^{el}$ plate capacitor, the current thro' the capacitor is given by,

$$i_2 = c\frac{dV}{dt}$$

$$i_2 = \frac{\varepsilon A}{d}\frac{dV}{dt} \quad \left[\because c = \frac{\varepsilon A}{d} \text{ for } \parallel^{el} \text{ plate capacitors}\right]$$

$$\text{---} (3)$$

displacement current denoted by i_D

The Electric field produced by the voltage applied b/w the two plates is given by,

$$\vec{E} = \frac{V}{d}$$

$$V = (d)(\vec{E}) \quad \text{--} (4)$$

sub (4) in (3) we get

$$i_D = i_2 = \frac{\varepsilon A}{d}\frac{d}{dt}(d\vec{E})$$

$$i_D = \frac{\varepsilon A}{d} d \frac{d\vec{E}}{dt} \quad \rightarrow d \text{ (distance) not varying with time}$$

$$\therefore i_D = \varepsilon A \frac{d\vec{E}}{dt}$$

$\therefore$ current density for i_D is

$$\vec{J_D} = \frac{i_D}{A}$$

$$\vec{J_D} = \frac{\varepsilon A}{A}\frac{d\vec{E}}{dt} \rightarrow \left(\frac{\varepsilon A}{A}\frac{d\vec{E}}{dt}\right)$$

$$\vec{J_D} = \varepsilon \frac{d\vec{E}}{dt} = \frac{d}{dt}(\varepsilon \vec{E}) \Rightarrow \varepsilon \vec{E} = \vec{D}$$

$$\boxed{\vec{J_D} = \frac{\partial \vec{D}}{\partial t}}$$

$\vec{J_c}$ – conduction current density

$\vec{J_D}$ → Displacement current density

$$\boxed{J = \vec{J_c} + \vec{J_D}}$$

MAXWELL'S EQUATION:

We have seen that a static electric field $\vec{E}$ can exist without a magnetic field $\vec{H}$ demonstrated by a capacitor with a static charge Q.

Way a conductor with a constant current I has a magnetic field $\vec{H}$ in the absence of an electric field $\vec{E}$.

But in the case of time varying fields, $\vec{E}$ & $\vec{H}$ doesnot exists without each other.

Maxwell's Equations are nothing but a set of four expressions derived from Ampere's circuital law, Faraday's law, Gauss's law for electric field and Gauss's law for magnetic field.

MAXWELL'S EQUATION FOR STATIC FIELDS:

A] MAXWELL'S EQUATION DERIVED FROM FARADAY'S LAW:

According to the basic concept from electrostatic field, the workdone over a closed path (or) closed contour (i.e. starting point same as terminating point) is always zero.

Mathematically it is represented as,

$$\oint \vec{E} \cdot d\vec{L} = 0.$$

The above equation is called integral form of maxwell's equation derived from faraday's law of static field.

Now using stoke's theorem converting the close line integral into the surface integral we get,

$$\oint \vec{E} \cdot d\vec{L} = \int_S (\nabla \times \vec{E}) \cdot d\vec{s} = 0$$

$$\therefore \int_S (\nabla \times \vec{E}) \cdot d\vec{s} = 0$$

But $d\vec{s}$ cannot be zero (i.e $d\vec{s} \neq 0$) that means,

$\boxed{\nabla \times \vec{E} = 0}$ → Point form or differential form of Maxwell's eqn derived from Faraday's law of static fields.

MAXWELL'S EQUATION DERIVED FROM AMPERE'S CIRCUITAL LAW:

According to basic concept of magnetostatics an Ampere's circuital law states that the line integral of magnetic field intensity $\vec{H}$ around a closed path is exactly equal to the direct current enclosed by that path. Mathematically it is given as,

$$\oint \vec{H} \cdot \vec{dL} = I$$

Now the current enclosed is equal to the product of current density normal to the closed path and area of closed path. Hence we get,

$$I = \int_S \vec{J} \cdot \vec{ds} \quad \text{where} \quad \vec{J} = \text{current density}.$$

Hence equating above equations we get,

$$\oint \vec{H} \cdot \vec{dL} = \int_S \vec{J} \cdot \vec{ds}$$

This above expression is called Integral form of maxwell's equation from Ampere circuital law for static field.

Now by applying stoke's theorem, L.H.S of above equation can be converted into surface integral

$$\therefore \oint \vec{H} \cdot \vec{dL} = \int_S (\nabla \times \vec{H}) \cdot \vec{ds} = \int_S \vec{J} \cdot \vec{ds}$$

Hence we get

$$\boxed{\nabla \times \vec{H} = \vec{J}}$$

differential form of Maxwell's eqn derived from Ampere circuital law for static field.

Maxwell's Eqvation derived from Gauss's law for Electrostatic fields.

According to Gauss's law of electrostatic fields, the electric flux passing thro' any closed surface is eqval to the total charge enclosed by that surface. Mathematically we can write,

$$\psi = \oint \vec{D} \cdot \vec{ds} = Q_{enclosed} \quad \text{---} (1)$$

The most common form to represent Gauss's law mathematically is with volume charge density ρ_v. Hence we can write,

$$\oint \vec{D} \cdot \vec{ds} = \int_v \rho_v \, dV \quad \text{---} (2)$$

The above eqvation is called integral form of maxwell's eqvation derived from Gauss's law for static electric field.

To establish relationship b/w $\vec{D}$ and ρ_v, converting closed surface integral into volume integral using divergence theorem as,

$$\oint \vec{D} \cdot \vec{ds} = \int_v (\nabla \cdot \vec{D}) \cdot dV \quad \text{---} (3)$$

comparing (2) and (3) we set

$$\int_v (\nabla \cdot \vec{D}) \cdot dV = \int_v \rho_v \, dV$$

$$\rightarrow \nabla \cdot \vec{D} = \rho_v \longrightarrow$$ Point form or differential form of Maxwell's Eqvation derived from Gauss's law for static electric field.

MAXWELL'S EQVATION DERIVED FROM GAUSS'S LAW FOR MAGNETOSTATIC FIELD:

According to Gauss's law for magnetostatic field, the magnetic flux cannot reside in a closed surface due to non existance of single magnetic pole.

Mathematically we can write,

$$\oint_S \vec{B} \cdot \vec{ds} = 0.$$

The above equation is called Integral form of Maxwell's Equation derived from Gauss's law for static magnetic field.

Now using divergence Theorem, we can write

$$\oint_S \vec{B}.d\vec{s} = \int_V (\nabla.\vec{B})\,dV = 0$$

(ie) $$\int_V (\nabla.\vec{B})\,dV = 0$$

Now dV cannot be zero that means

$$\nabla.\vec{B} = 0$$

↳ Point form or differential form of maxwell's equation derived from Gauss's law for static magnetic field.

MAXWELL'S EQUATION FOR TIME VARYING FIELD:

MAXWELL'S EQUATION DERIVED FROM FARADAY'S LAW:

Now consider faraday's law which relates e.m.f induced in a circuit to a circuit to the time rate of change or decrease of total magnetic flux linking the ckt. Thus we can write.

$$\oint \vec{E}.d\vec{L} = -\int_S \frac{\partial \vec{B}}{\partial t}.d\vec{s} \rightarrow \text{Maxwell's Eqn derived from Faraday's law expressed in Integral form.} \quad \text{---(1)}$$

The total electromotive force (e.m.f) induced in a closed path is equal to the negative surface integral of the rate of change of flux density w.r.to time over an entire surface bounded by the same closed path.

using stokes theorem, we get

$$\int_S (\nabla \times \vec{E}).d\vec{s} = -\int_S \frac{\partial \vec{B}}{\partial t}.d\vec{s}$$

$$\therefore \quad \nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \rightarrow \text{Point form or differential form derived from faraday's law.}$$

MAXWELL'S EQUATION DERIVED FROM AMPERE'S CIRCUITAL LAW:

According to Ampere's circuital law, the line integral of magnetic field intensity $\vec{H}$ around a closed path is equal to current enclosed by the path.

$$\oint \vec{H} \cdot \vec{dL} = I_{enclosed}.$$

$$I_{enclosed} = \int_S \vec{J} \cdot \vec{ds}$$

$$\therefore \oint \vec{H} \cdot \vec{dL} = \int_S \vec{J} \cdot \vec{ds}$$

Above expression can be made further general by adding displacement current density to conduction current density as follows,

$$\oint \vec{H} \cdot \vec{dL} = \int_S \left[\vec{J_c} + \frac{\partial \vec{D}}{\partial t}\right] \cdot \vec{ds} \rightarrow \text{Integral form}$$

Applying stokes theorem.

$$\oint \vec{H} \cdot \vec{dL} = \int_S (\nabla \times \vec{H}) \cdot \vec{ds} = \int_S \left[\vec{J_c} + \frac{\partial \vec{D}}{\partial t}\right] \cdot \vec{ds}$$

$$\therefore (\nabla \times \vec{H}) = \vec{J_c} + \frac{\partial \vec{D}}{\partial t} \rightarrow \text{Point form.}$$

Statement:

The total MMF around any closed path is equal to the surface integral of the conduction and displacement current densities over the entire surface bounded by the same closed path.

Total flux leaving out of a closed surface is equal to the total charge enclosed by a finite volume.

The surface integral of magnetic flux density over a closed surface is always equal to zero.

Differential form	Integral form	Significance
$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}$	$\oint \vec{E} \cdot d\vec{L} = -\int_S \frac{\partial \vec{B}}{\partial t} \cdot d\vec{s}$	Faraday's law
$\nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t}$	$\oint \vec{H} \cdot d\vec{L} = I + \int_S \frac{\partial \vec{D}}{\partial t} \cdot ds$	Ampere circuital law
$\nabla \cdot \vec{D} = \rho_v$	$\oint \vec{D} \cdot d\vec{s} = \int_S \rho_v \, dV$	Gauss's law
$\nabla \cdot \vec{B} = 0$	$\oint_S \vec{B} \cdot d\vec{s} = 0$	No isolated magnetic charges.

MAXWELL'S EQUATION FOR FREE SPACE:

Free space is a non-conducting medium in which volume charge density $\rho_v = 0$ and conductivity $\sigma = 0$

Point form	Integral form
$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}$	$\oint \vec{E} \cdot d\vec{L} = -\int_S \frac{\partial \vec{B}}{\partial t} \cdot d\vec{s}$
$\nabla \times \vec{H} = \frac{\partial \vec{D}}{\partial t}$ $[\because \vec{J} = \sigma \vec{E}]$	$\oint \vec{H} \cdot d\vec{L} = \int_S \frac{\partial \vec{D}}{\partial t} \cdot d\vec{s}$
$\nabla \cdot \vec{D} = 0$	$\oint \vec{D} \cdot d\vec{s} = 0$
$\nabla \cdot \vec{B} = 0$	$\oint \vec{B} \cdot d\vec{s} = 0$.

MAXWELL'S EQUATION FOR GOOD CONDUCTORS :

For good conductor $\vec{J} >> \frac{\partial \vec{D}}{\partial t}$ & $\rho_v = 0$.

$\therefore \nabla \times \vec{E} = \frac{\partial \vec{B}}{\partial t}$	$\oint \vec{E} \cdot d\vec{L} = -\int_S \frac{\partial \vec{B}}{\partial t} \cdot d\vec{s}$
$\nabla \times \vec{H} = \vec{J}$	$\oint \vec{H} \cdot d\vec{L} = \int_S \vec{J} \cdot d\vec{s}$
$\nabla \cdot \vec{D} = 0$	$\oint \vec{B} \cdot d\vec{s} = 0$
$\nabla \cdot \vec{B} = 0$	$\oint \vec{B} \cdot d\vec{s} = 0$.

Comparison b/w Electric circuit and Magnetic circuit.

Electric circuit	Magnetic circuit
1. The Path traced by the current is called electric circuit	1. The path traced by the magnetic flux is called Magnetic circuit
2. In electric ckt, emf is the driving force. It is measured in volts.	2. In magnetic circuit mmf is the driving force, it is measured in Ampere-turns.
3. Resistance R opposes the flow of current. $R = \frac{emf}{current} = \frac{l}{\sigma s}\ \Omega$	3. Reluctance $\mathcal{R}$ is opposed by the magnetic path. $\mathcal{R} = \frac{l}{\mu s} = \frac{mmf}{flux}$ A.t/Wb.
4. conductivity σ	4. Permiability μ.
5. Field Intensity E	5. Field intensity H.
6. current density $J = \frac{\sigma E}{s}$ A/m^2	6. Flux density $B = \frac{\phi}{s} = \mu H$ Wb/m^2
7. Reciprocal of resistance is conductance (G)	7. Reciprocal of reluctance is Permeance (R).
8. ohms law $e = IR$	8. ohms law $e_m = \phi R$.
9. Kirchoff's law: $\Sigma I = 0$ $\Sigma EMF = 0$	9. Kirchoff's law $\Sigma \phi = 0$ $\Sigma MMF = \Sigma \phi S = \Sigma H.l$.

ELECTROMAGNETIC WAVES:

The waves are the means of transporting energy (or) information from source to destination. The waves consisting of electric and magnetic fields are called electromagnetic waves.

The electromagnetic waves are said to be in existance is all the four Maxwell's equations are satisfied at the source point [where they are generated], at any point in the medium (through which they travel) and at the destination or load Point [where they are received).

Basically the waves radiated from the source are with spherical wavefront, but at large distances from source the spherical waves become practically plane waves.

In general, the wave is a function of time & space.
eg: radio waves, light rays, radar beams, television signals etc.

GENERAL WAVE EQUATION:

To obtain general wave equations, let us assume that the electric and magnetic fields exist in a linear, homogeneous & isotropic medium with the parameters μ, ε and σ.

Also assume that the medium is source free which clearly gives the idea about the charge free medium.

Assume that the medium obeys the ohm's law i.e $\vec{J} = \sigma \vec{E}$. Then the Maxwell's equation is given by,

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \implies \vec{B} = \mu \vec{H} \Rightarrow \nabla \times \vec{E} = -\mu \frac{\partial \vec{H}}{\partial t} \quad \text{---} (1)$$

$$\nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} \implies \vec{D} = \varepsilon \vec{E}, \ \vec{J} = \sigma \vec{E} \Rightarrow \nabla \times \vec{H} = \sigma \vec{E} + \varepsilon \frac{\partial \vec{E}}{\partial t} \quad \text{--} (2)$$

$$\nabla \cdot \vec{B} = 0 \implies \vec{B} = \mu \vec{H} \Rightarrow \nabla \cdot \vec{H} = 0 \quad \text{---} (3)$$

$$\nabla \cdot \vec{D} = 0 \implies \vec{D} = \varepsilon \vec{E} \Rightarrow \nabla \cdot \vec{E} = 0 \quad \text{---} (4)$$

[$\because \rho_v = 0$ for free space].

To eliminate $\vec{H}$ from (1), taking curl on both sides of equation (1), we get

$$\nabla \times (\nabla \times \vec{E}) = -\frac{\partial}{\partial t}(\nabla \times \vec{H}) \quad \text{--} (5)$$

$\nabla \rightarrow$ indicates differentiation w.r.to space

while $\frac{\partial}{\partial t} \rightarrow$ indicates differentiation w.r.to time.

Both are independent of each other, the operations can be interchanged.

So we get

$$\nabla \times (\nabla \times \vec{E}) = -\mu \frac{\partial}{\partial t}(\nabla \times \vec{H}) \quad \text{--- (6)}$$

sub (2) in (6) we get

$$\nabla \times \nabla \times \vec{E} = -\mu \frac{\partial}{\partial t}\left[\sigma \vec{E} + \varepsilon \frac{\partial \vec{E}}{\partial t}\right]$$

$$\nabla \times \nabla \times \vec{E} = -\mu\sigma \frac{\partial \vec{E}}{\partial t} - \mu\varepsilon \frac{\partial^2 E}{\partial t^2} \quad \text{---- (7)}$$

Now accooding to vector identity,

$$\nabla \times \nabla \times \vec{E} = \nabla(\nabla \cdot \vec{E}) - \nabla^2 \vec{E} \quad \text{--- (8)}$$

sub (4) in (8) we get

$$\nabla \times \nabla \times \vec{E} = -\nabla^2 \vec{E} \quad \text{--- (9)}$$

sub (9) in (7) we get

$$+\nabla^2 \vec{E} = +\mu\sigma \frac{\partial \vec{E}}{\partial t} + \mu\varepsilon \frac{\partial^2 \vec{E}}{\partial t^2} \quad \text{--- (10)}$$

This is the wave eavation ~~foo~~ the electoic field $\vec{E}$. Now multiplying both the sides of (10) by ε, we get

$$\nabla^2(\varepsilon \vec{E}) = \mu\sigma \frac{\partial \varepsilon \vec{E}}{\partial t} + \mu\varepsilon \frac{\partial^2 \varepsilon \vec{E}}{\partial t^2}$$

$$\nabla^2 \vec{D} = \mu\sigma \frac{\partial \vec{D}}{\partial t} + \mu\varepsilon \frac{\partial^2 \vec{D}}{\partial t^2} \quad \left[\because \vec{D} = \varepsilon \vec{E}\right] \quad \text{--- (11)}$$

This is the wave eavation ~~for~~ $\vec{D}$ in unifoom medium.

To obtain wave eavation of $\vec{H}$, take curl on both sides of (2), we get

$$\nabla \times (\nabla \times \vec{H}) = \nabla \times \sigma \vec{E} + \varepsilon \nabla \times \frac{\partial \vec{E}}{\partial t}$$

$$\nabla \times \nabla \times \vec{H} = \sigma(\nabla \times \vec{E}) + \varepsilon \frac{\partial}{\partial t}(\nabla \times \vec{E}) \quad \text{--- (12)}$$

Sub (1) in (12) we get

$$\nabla \times \nabla \times \vec{H} = \sigma\left(-\mu \frac{\partial \vec{H}}{\partial t}\right) + \varepsilon \frac{\partial}{\partial t}\left[-\mu \frac{\partial \vec{H}}{\partial t}\right]$$

$$= -\mu\sigma \frac{\partial \vec{H}}{\partial t} - \mu\varepsilon \frac{\partial^2 \vec{H}}{\partial t^2} \quad \text{---} (13)$$

using vector identity

$$\nabla \times \nabla \times \vec{H} = \nabla(\nabla \cdot \vec{H}) - \nabla^2 \vec{H} \quad \text{---} (14)$$

Sub (3) in (14) we get

$$\nabla \times \nabla \times \vec{H} = -\nabla^2 \vec{H} \quad \text{---} (15)$$

Equivating (15) and (13) we get

$$-\nabla^2 \vec{H} = -\mu\sigma \frac{\partial \vec{H}}{\partial t} - \mu\varepsilon \frac{\partial^2 \vec{H}}{\partial t^2}$$

$$\boxed{\nabla^2 \vec{H} = \mu\sigma \frac{\partial \vec{H}}{\partial t} + \mu\varepsilon \frac{\partial^2 \vec{H}}{\partial t^2}} \quad \text{---} (16)$$

This is the wave equation for magnetic field $\vec{H}$. Now multiplying both sides by μ we get

(16) $\times \mu$

$$\nabla^2(\mu\vec{H}) = \mu\sigma \frac{\partial \mu\vec{H}}{\partial t} + \mu\varepsilon \frac{\partial^2 \mu\vec{H}}{\partial t^2}$$

$\because \mu\vec{H} = \vec{B}$

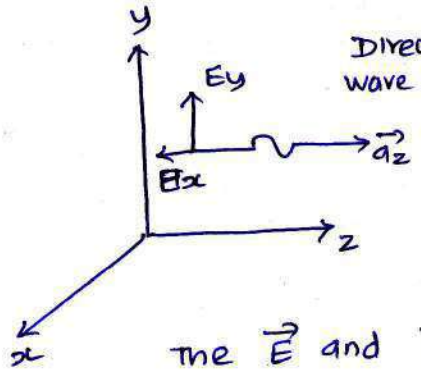
$$\boxed{\nabla^2 \vec{B} = \mu\sigma \frac{\partial \vec{B}}{\partial t} + \mu\varepsilon \frac{\partial^2 \vec{B}}{\partial t^2}} \quad \text{---} (18)$$

This is the wave equation of $\vec{B}$ in the uniform medium.

UNIFORM PLANE WAVES IN FREE SPACE:

Consider an electromagnetic wave propagating thro' the free space. For free space $\sigma = 0$, consider that the electric field in the wave in x-direction only while the magnetic field in the y-direction only.

Both the fields i.e, electric and magnetic field do not vary with x and y but vary only with z. The fields also vary with time as wave propagates in the free space.



Basically plane waves means, the electric field vector $\vec{E}$ and the magnetic field vector $\vec{H}$ lie on the same plane.

The uniform plane wave means the $\vec{E}$ and $\vec{H}$ field vector are in same plane. moreover the amplitude and phase of field vectors $\vec{E}$ & $\vec{H}$ is constant over the planes $\parallel^{el}$ to each other.

Electric field vector is in $\vec{a}_x$ direction, while magnetic field vector is in $\vec{a}_y$ direction. That means $\vec{E}$ & $\vec{H}$ lie in x-y plane. So in any of the planes in the wave, the vectors $\vec{E}$ and $\vec{H}$ are independent of x and y. Thus we can conclude that $\vec{E}$ and $\vec{H}$ are functions of z and t only. Moreover as $\vec{E}$ and $\vec{H}$ are mutually $\perp^r$ to each other, the electromagnetic waves are also called as transverse electromagnetic waves.

Let us consider wave equations for $\vec{E}$ & $\vec{H}$ fields given by,

$$\nabla^2 \vec{E} = \mu\sigma \frac{\partial \vec{E}}{\partial t} + \mu\varepsilon \frac{\partial^2 \vec{E}}{\partial t^2} \quad \text{---} (1)$$

$$\nabla^2 \vec{H} = \mu\sigma \frac{\partial \vec{H}}{\partial t} + \mu\varepsilon \frac{\partial^2 \vec{H}}{\partial t^2} \quad \text{----} (2)$$

But for free space $\sigma = 0$, $\mu = \mu_0$ and $\varepsilon = \varepsilon_0$

Sub these values in (1) & (2) we get

$$\nabla^2 \vec{E} = \mu_0 \varepsilon_0 \frac{\partial^2 \vec{E}}{\partial t^2} \quad ---(3)$$

$$\nabla^2 \vec{H} = \mu_0 \varepsilon_0 \frac{\partial^2 \vec{H}}{\partial t^2} \quad ----(4)$$

Consider eqn (3)

$$\nabla^2 \vec{E} = \frac{\partial^2 \vec{E}}{\partial x^2} + \frac{\partial^2 \vec{E}}{\partial y^2} + \frac{\partial^2 \vec{E}}{\partial z^2} = \mu_0 \varepsilon_0 \frac{\partial^2 \vec{E}}{\partial t^2} \quad ---(5)$$

But the wave travels in the z-direction, hence $\vec{E}$ is independent of x and y. Hence first two differential terms in above eqn are zero. Hence we can write

$$\frac{\partial^2 \vec{E}}{\partial z^2} = \mu_0 \varepsilon_0 \frac{\partial^2 \vec{E}}{\partial t^2} \quad ----(6)$$

$$\frac{\partial^2 \vec{E}}{\partial t^2} = \frac{1}{\mu_0 \varepsilon_0} \frac{\partial^2 \vec{E}}{\partial z^2} \quad ---(7)$$

Now according to the results in physics,

$$v = \frac{1}{\sqrt{\mu_0 \varepsilon_0}} = c \quad \text{i.e. } v^2 = \frac{1}{\mu_0 \varepsilon_0} = c^2 \quad \text{where}$$

$c = 3 \times 10^8$ m/s = velocity of light

Sub above relations in (7) we get

$$\boxed{\frac{\partial^2 \vec{E}}{\partial t^2} = v^2 \frac{\partial^2 \vec{E}}{\partial z^2}} \quad ---(8)$$

Above equation is other form of wave equation.

III^{ly} to this we can write.

$$\boxed{\frac{\partial^2 \vec{H}}{\partial t^2} = v^2 \frac{\partial^2 \vec{H}}{\partial z^2}} \quad ----(9)$$

Reconsidering eqn (6)

$$\frac{\partial^2 \vec{E}}{\partial z^2} = \mu_0 \varepsilon_0 \frac{\partial^2 E}{\partial t^2}$$

For the wave Propagating in z-direction, $\vec{E}$ may have E_x & E_y component definately not E_z. According to assumption, $\vec{E}$ is in $\vec{a}_x$ direction, so let us consider that only E_x is Present. Then we can rewrite above equation as,

$$\frac{\partial^2 E_x}{\partial z^2} = \mu_0 \varepsilon_0 \frac{\partial^2 E_x}{\partial t^2} \quad \text{----(10)}$$

Let $E_x = E_m e^{j\omega t}$

where $E_m \rightarrow$ Amplitude of the electric field

$\omega \rightarrow$ Angular freq.

Partially differentiating E_x twice w.r.to t, we get

$$\frac{\partial^2 E_x}{\partial t^2} = E_m (j\omega)(j\omega) e^{j\omega t} = -\omega^2 E_m e^{j\omega t}$$

But $E_m e^{j\omega t} = E_x$

$$\therefore \frac{\partial^2 E_x}{\partial t^2} = -\omega^2 E_x$$

Sub above eqn in (10) we set

$$\frac{\partial^2 E_x}{\partial z^2} = \mu_0 \varepsilon_0 [-\omega^2 E_x] = -\omega^2 \mu_0 \varepsilon_0 E_x \quad \text{----(11)}$$

Let $\frac{\partial}{\partial z} = D$ i.e $\frac{\partial^2}{\partial z^2} = D^2$ $\therefore$ (11) becomes.

$$D^2 E_x + \omega^2 \mu_0 \varepsilon_0 E_x = 0$$

Thus Auxillary Equation becomes,

$$(D^2 + \omega^2 \mu_0 \varepsilon_0) E_x = 0.$$

Hence equating bracket terms to zero, we get

$$D^2 + \omega^2 \mu_0 \varepsilon_0 = 0$$

(or) $$D^2 = -\omega^2 \mu_0 \varepsilon_0$$

(or) $$D = \pm j\omega \sqrt{\mu_0 \varepsilon_0} = \pm j\beta$$

where $\beta = \omega \sqrt{\mu_0 \varepsilon_0}$ which is called Phase shift constant measured in rad/m.

Hence the solution of eqn (11) can be written as,

$$E_x = K_1 e^{-j\omega\sqrt{\mu_0\varepsilon_0}\,z} + K_2 e^{j\omega\sqrt{\mu_0\varepsilon_0}\,z}.$$

$$E_x = K_1 e^{-j\beta z} + K_2 e^{+j\beta z} \quad \text{----(12)}$$

Let K_1 and K_2 be the constants w.r.to z but are functions of t. Let us assume K_1 and K_2 as.

$$K_1 = E_m^+ e^{+j\omega t} \quad \&$$

$$K_2 = E_m^- e^{+j\omega t}.$$

sub K_1 and K_2 in (12) we get

$$E_x = E_m^+ e^{j\omega t} e^{-j\beta z} + E_m^- e^{+j\omega t} e^{+j\beta z}$$

$$= E_m^+ e^{j(\omega t-\beta z)} + E_m^- e^{j(\omega t+\beta z)}. \quad \text{---(13)}$$

To find the electric field in the time domain, taking real part of (13), we get

$$E_x = Re\left[E_m^+ e^{j(\omega t-\beta z)} + E_m^- e^{j(\omega t+\beta z)}\right]$$

$$E_x = \underbrace{E_m^+}_{\text{Travelling in } +z \text{ direction}} \cos(\omega t-\beta z) + \underbrace{E_m^-}_{\text{Travelling in -ve z-direction.}} \cos(\omega t+\beta z)\ V/m.$$

Above eqvation is the sinusoidal function consisting of two components. one in forward direction and other in backward direction

POYNTING VECTOR & POYNTING THEOREM:

By means of Electromagnetic (EM) waves, an energy can be transported from transmitter to receiver. The energy stored in an electric field and magnetic field is transmitted at a certain rate of energy flow which can be calculated with the help of Poynting theorem.

As we know $\vec{E}$ & $\vec{H}$ are basic fields, $\vec{E}$ is electric field expressed in V/m ; while $\vec{H}$ is magnetic field measured in A/m. so if we take dot product of the two fields, dimensionally we get a unit $V \cdot A/m^2$ (or) $\frac{watt}{m^2}$. So this product of $\vec{E}$ & $\vec{H}$ gives a new quantity which is expressed as $watt/m^2$. This quantity is called Power density.

As $\vec{E}$ & $\vec{H}$ are vectors, to get power density we may carry out either dot product or cross product. The result of dot product is always a scalar quantity. But as power flows in certain directions, it is a vector quantity. To illustrate this, consider that the field is transmitted in the form of an electromagnetic waves from an antenna. Both the fields are sinusoidal in nature.

The power radiated from antenna has a particular direction. Hence to calculate a power density, we must carry out a cross product of $\vec{E}$ and $\vec{H}$.

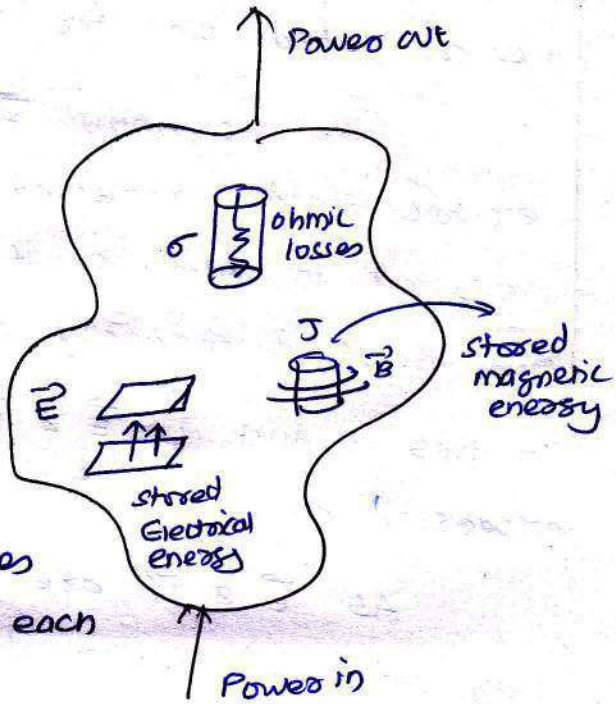
The power density is given by

$$\vec{P} = \vec{E} \times \vec{H}.$$

Where $\vec{P}$ is called Poynting vector.

Poynting theorem is based on the law of conservation of energy in electromagnetism. Poynting theorem can be stated as,

The net power flowing out of a given volume V is equal to the time rate of decrease in the energy stored within volume 'V' minus the ohmic power dissipated.



Suppose

$\vec{E} = E_x \vec{a}_x$

$\vec{H} = H_y \vec{a}_y$ then

$\vec{P} = \vec{E} \times \vec{H}$

$= E_x \vec{a}_x \times H_y \vec{a}_y$

$$\boxed{\vec{P} = E_x H_y \vec{a}_z}$$

The above equation indicates $\vec{E}, \vec{H}$ and $\vec{P}$ are mutually $\perp^r$ to each other.

Consider that the electric field propagates in free space given by

$$\vec{E} = [E_m \cos(\omega t - \beta z)] \vec{a}_x$$

In the medium, the ratio of magnitudes of $\vec{E}$ & $\vec{H}$ depends on its intrinsic impedance η, for free space.

$$\eta = \eta_0 = \frac{E_m}{H_m} = 120\pi = 377\,\Omega.$$

Moreover in free space, electromagnetic wave travels at a speed of light,

Thus we can write,

$$\vec{H} = [H_m \cos(\omega t - \beta z)] \vec{a}_y$$

$$= \left[\frac{E_m}{\eta_0} \cos(\omega t - \beta z)\right] \vec{a}_y$$

According to Poynting theorem.

$$\vec{P} = \vec{H} \times \vec{E}$$

$$= [E_m \cos(\omega t - \beta z)]\vec{a}_x \times \left[\frac{E_m}{\eta_0}\cos(\omega t - \beta z)\right]\vec{a}_y$$

$$\vec{P} = \frac{E_m^2}{\eta_0}\cos^2(\omega t - \beta z)\,\vec{a}_z \quad W/m^2$$

This is nothing but the power density measured in Watt/m^2. Thus the power passing particular area is given by,

Power = Power density × Area.

AVERAGE POWER DENSITY (P_{avg}).

To find average power density, let us integrate by the power density in z-direction over one cycle and divide the period T of one cycle.

$$\therefore P_{avg} = \frac{1}{T}\int_0^T \frac{E_m^2}{\eta}\cos^2(\omega t - \beta z)\,dt.$$

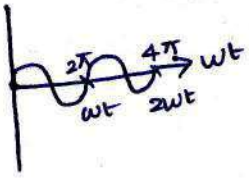
$$= \frac{E_m^2}{\eta T}\int_0^T \cos^2(\omega t - \beta z)\,dt$$

$$= \frac{E_m^2}{\eta T}\int_0^T \frac{1+\cos 2(\omega t - \beta z)}{2}\,dt$$

$$= \frac{E_m^2}{\eta T}\left[\frac{t}{2} + \frac{\sin 2(\omega t - \beta z)}{(2\omega)\,2}\right]_0^T$$

$$= \frac{E_m^2}{\eta T}\left[\frac{t}{2} + \frac{\sin(2\omega t - 2\beta z)}{4\omega}\right]_0^T$$

$$= \frac{E_m^2}{\eta T}\left[\frac{T}{2} + \frac{\sin(2\omega T - 2\beta z)}{4\omega} - \frac{\sin(-2\beta z)}{4\omega}\right]$$



$$= \frac{E_m^2}{T\eta}\left[\frac{T}{2} + \frac{\sin(4\pi - 2\beta z)}{4\omega} + \frac{\sin(2\beta z)}{4\omega}\right]$$

$$= \frac{E_m^2}{T\eta}\left[\frac{T}{2} - \frac{\sin 2\beta z}{4\omega} + \frac{\sin 2\beta z}{4\omega}\right] = \frac{E_m^2 \cdot T}{2T\eta} = \frac{E_m^2}{2\eta}$$

Hence the average power is given by,

$$P_{avg} = \frac{1}{2} \frac{E_m^2}{\eta} \text{ W/m}^2$$

INTEGRAL & POINT FORMS OF POYNTING THEOREM:

Consider Maxwell's equations as given below,

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} = -\mu \frac{\partial \vec{H}}{\partial t} \quad \text{---- (1)}$$

$$\nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} = \sigma \vec{E} + \varepsilon \frac{\partial \vec{E}}{\partial t} \quad \text{--- (2)}$$

Doting both the sides of eqn (2) with $\vec{E}$, we get

$$\vec{E} \cdot (\nabla \times \vec{H}) = \vec{E} \cdot (\sigma \vec{E}) + \vec{E} \cdot \left(\varepsilon \frac{\partial \vec{E}}{\partial t}\right) \quad \text{--- (3)}$$

Let us make use of vector identity as given below

$$\nabla \cdot (\vec{A} \times \vec{B}) = \vec{B} \cdot (\nabla \times \vec{A}) - \vec{A} \cdot (\nabla \times \vec{B})$$

applying the above identity to equation (3) with $\vec{A} = \vec{E}$ & $\vec{B} = \vec{H}$ we get

$$\vec{H} \cdot (\nabla \times \vec{E}) - \vec{E} \cdot (\nabla \times \vec{H}) = \nabla \cdot (\vec{E} \times \vec{H})$$

$$\vec{H} \cdot (\nabla \times \vec{E}) - \nabla \cdot (\vec{E} \times \vec{H}) = \vec{E} \cdot (\nabla \times \vec{H})$$

sub (3) in above equation we get

$$\vec{H} \cdot (\nabla \times \vec{E}) - \nabla \cdot (\vec{E} \times \vec{H}) = \vec{E} \cdot (\sigma \vec{E}) + \vec{E} \cdot \left(\varepsilon \frac{\partial \vec{E}}{\partial t}\right)$$

$$\vec{H} \cdot (\nabla \times \vec{E}) - \nabla \cdot (\vec{E} \times \vec{H}) = \sigma E^2 + \vec{E} \cdot \left(\varepsilon \frac{\partial \vec{E}}{\partial t}\right) \quad \text{--- (4)}$$

consider the first term of (4) we get, & by substituting (1) we get

$$\vec{H} \cdot (\nabla \times \vec{E}) = \vec{H} \cdot \left(-\mu \frac{\partial \vec{H}}{\partial t}\right)$$

$$\vec{H} \cdot (\nabla \times \vec{E}) = -\mu \vec{H} \cdot \frac{\partial \vec{H}}{\partial t} \quad \text{----- (i)}$$

Now consider term,

$$\frac{\partial}{\partial t}(\vec{H}\cdot\vec{H}) = \vec{H}\cdot\frac{\partial \vec{H}}{\partial t} + \vec{H}\cdot\frac{\partial \vec{H}}{\partial t}$$

$$\frac{\partial}{\partial t}H^2 = 2\vec{H}\cdot\frac{\partial \vec{H}}{\partial t}$$

$$\frac{1}{2}\frac{\partial}{\partial t}\vec{H}^2 = \vec{H}\cdot\frac{\partial \vec{H}}{\partial t} \quad \text{--- (ii)}$$

Similarly we can write

$$\frac{1}{2}\frac{\partial}{\partial t}E^2 = \vec{E}\cdot\frac{\partial \vec{E}}{\partial t} \quad \text{---- (iii)}$$

Substituting (i), (ii) & (iii) in (4) we get

$$\vec{H}\cdot(\nabla\times\vec{E}) - \nabla\cdot(\vec{E}\times\vec{H}) = \sigma E^2 + \vec{E}\cdot\left(\varepsilon\frac{\partial \vec{E}}{\partial t}\right)$$

$$-N\vec{H}\cdot\frac{\partial \vec{H}}{\partial t} - \nabla\cdot(\vec{E}\times\vec{H}) = \sigma E^2 + \varepsilon\left[\vec{E}\cdot\frac{\partial \vec{E}}{\partial t}\right]$$

$$-\frac{N}{2}\frac{\partial}{\partial t}H^2 - \nabla\cdot(\vec{E}\times\vec{H}) = \sigma E^2 + \frac{\varepsilon}{2}\frac{\partial}{\partial t}E^2$$

$$-\nabla\cdot(\vec{E}\times\vec{H}) = \sigma E^2 + \frac{\varepsilon}{2}\frac{\partial}{\partial t}E^2 + \frac{N}{2}\frac{\partial}{\partial t}H^2$$

$$-\nabla\cdot(\vec{E}\times\vec{H}) = \sigma E^2 + \frac{1}{2}\frac{\partial}{\partial t}\left[NH^2 + \varepsilon E^2\right]$$

But $\vec{E}\times\vec{H} = \vec{P}$

$$\therefore -\nabla\cdot(\vec{P}) = \sigma E^2 + \frac{1}{2}\frac{\partial}{\partial t}\left[NH^2 + \varepsilon E^2\right] \quad \text{---(5)}$$

The above equation represents Poynting theorem in Point form.

If we integrate this power over a volume, we can get energy distribution as,

$$-\int_V \nabla\cdot\vec{P}\,dV = \int_V \sigma E^2 dV + \frac{\partial}{\partial t}\int_V \frac{1}{2}\left[NH^2 + \varepsilon E^2\right]dV$$

Applying divergence theorem to left of above equation we get

$$-\oint \vec{P}\cdot\vec{ds} = \int_V \sigma E^2 dV + \frac{\partial}{\partial t}\int_V \frac{1}{2}\left[NH^2 + \varepsilon E^2\right]dV.$$

Above equation represents Poynting theorem in integral form.

REFLECTION OF UNIFORM PLANE WAVES:

We have so far, studied the uniform plane waves travelling in unbounded and homogeneous media. But practically, very often, wave propagates in boundary regions consisting several media of different constitutive parameters such as $\varepsilon, \mu, \sigma, \eta$ etc.

Before we actually start with the reflection of the uniform plane wave, let us consider simple example of a transmission line.

Consider a transmission line having a characteristics impedance Z_0. Assume that the line is terminated in load impedance Z_L.

If the load impedance Z_L equals the characteristic impedance Z_0 (i.e $Z_L = Z_0$), then the line is said to be properly terminated.

If $Z_L \neq Z_0$, then there is a mismatch b/w the two impedances and the line is not properly terminated. Consider that the wave travelling along the line incidents at the load. The part of the wave gets absorbed by the load, while the other part is reflected back to the generator.

So we can say reflection occurs at the load if $Z_L \neq Z_0$. If there are two waves, one incident in forward direction, while other reflected back in backward direction, then the standing waves are said to be produced along the line.

When a uniform plane wave travels from one medium to other having different intrinsic impedances, the reflection takes place at the boundaries.

The part of the wave is transmitted in medium 2 and remaining part is reflected back to medium 1, depending upon the consecutive parameters of media.

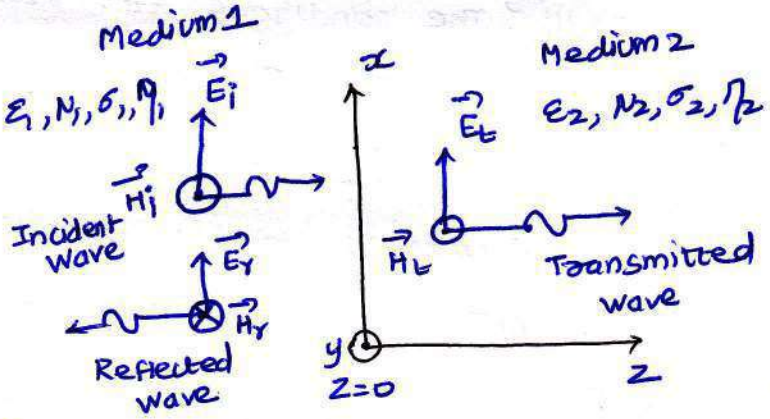
Depending upon the manner in which the uniform plane wave is incident on the boundary, there are two cases of incidence.

(i) Normal incidence

(ii) Oblique incidence.

NORMAL INCIDENCE AT PLANE DIELECTRIC BOUNDARY:

Consider a uniform plane wave striking the interface b/w the two dielectrics at right angles as shown in the figure.



Assume that the uniform plane wave travels along +z direction and incidence at right angles at the boundary b/w two dielectric media i.e. at z=0.

Below z=0, let the properties of medium 1 be $\varepsilon_1, \mu_1, \sigma_1, \eta_1$ and above z=0, the properties of medium 2 be $\varepsilon_2, \mu_2, \sigma_2, \eta_2$

So depending upon the properties of two media, part of the wave will be transmitted in medium 2 while other part will be reflected back in medium 1

Let E_i & H_i be the field strengths of the incident wave striking at the boundary.

E_t & H_t be the field strengths of the transmitted wave in the medium 2.

E_r & H_r be the field strengths of the reflected wave in the medium 1 returning back from the interface.

From figure it is clear that in medium 1, the total field composes of both the incident and reflected fields. But in medium 2 only transmitted field gives the total field.

So the conditions for the total field in medium 1 are given by,

$$\vec{E_1} = \vec{E_i} + \vec{E_r} \quad \&$$

$$\vec{H_1} = \vec{H_i} + \vec{H_r}$$

Similarly the conditions for total field in medium 2 is given by,

$$\vec{E_2} = \vec{E_t} \quad \&$$

$$\vec{H_2} = \vec{H_t}$$

According to the boundary condition, the tangential components of $\vec{E}$ & $\vec{H}$ must be continuous at the interface $z=0$.

$$\therefore \quad \vec{E_{1tan}} = \vec{E_{2tan}}$$

$$\vec{H_{1tan}} = \vec{H_{2tan}}$$

Thus at interface $z=0$, we can write

$$\vec{E_i} + \vec{E_r} = \vec{E_t} \quad \&$$

$$\vec{H_i} + \vec{H_r} = \vec{H_t}$$

The relationships b/w the magnitude of $\vec{E}$ & $\vec{H}$ at $z=0$ are given by the following expressions

$E_i = \eta_1 H_i$

$E_r = -\eta_1 H_r$ .... as direction of reflected wave is opposite to that of incident wave

$E_t = \eta_2 H_t$

Interms of magnitudes of the fields $\vec{E}$ & $\vec{H}$ at the interface, we can write

$$E_i + E_r = E_t \quad \text{---- (1)}$$

$$H_i + H_r = H_t \quad \text{---- (2)}$$

In eqn (2), putting the values of H_i, H_r and H_t interms of E_i, E_r & E_t we get

$$\frac{E_i}{\eta_1} - \frac{E_r}{\eta_1} = \frac{E_t}{\eta_2}$$

$$\therefore E_i - E_r = \frac{\eta_1}{\eta_2} E_t \quad \text{---- (3)}$$

Adding eqn (1) & (3), we get

$$2E_i = \left(1 + \frac{\eta_1}{\eta_2}\right) E_t$$

$$2E_i = \left(\frac{\eta_1 + \eta_2}{\eta_2}\right) E_t$$

$$\boxed{E_t = \frac{2\eta_2}{\eta_1 + \eta_2} E_i} \quad \text{--- (4)}$$

The Transmission co-efficient is denoted by τ and it is given by,

$$\boxed{\tau = \frac{E_t}{E_i} = \frac{2\eta_2}{\eta_1 + \eta_2}} \quad \text{--- (5)}$$

Eliminating E_t from eqn (1) & (3), we get

$$\frac{(1)}{(3)} \Rightarrow \frac{E_i + E_r}{E_i - E_r} = \frac{\eta_2}{\eta_1} \Rightarrow E_i + E_r = \frac{\eta_2}{\eta_1} E_i - E_r$$

$$\eta_2(E_i + E_r) = \eta_2(E_i - E_r)$$

$$\eta_1 E_i + \eta_2 E_r = \eta_2 E_i - \eta_2 E_r$$

$$(\eta_1 - \eta_2) E_i = -E_r(\eta_1 + \eta_2)$$

$$E_i(\eta_1 - \eta_2) = -E_r(\eta_1 + \eta_2)$$

$$E_r = \frac{\eta_1 - \eta_2}{-(\eta_1 + \eta_2)} E_i$$

$$\boxed{E_r = \frac{\eta_2 - \eta_1}{\eta_1 + \eta_2} E_i} \quad \text{--- (6)}$$

The reflection co-efficient is denoted as Γ and it is given by,

$$\boxed{\Gamma = \frac{E_r}{E_i} = \frac{\eta_2 - \eta_1}{\eta_1 + \eta_2}} \quad \text{--- (7)}$$

from eqn (5) and (7), we can draw some important results as

(a) $1 + \Gamma = \tau$

(b) $0 \leq |\Gamma| \leq 1$

(c) Both the co-efficients ; Γ and τ are dimensionless and may be complex in nature.

According to Poynting Theorem, The average Power density is given by,

$$P_{avg} = \frac{1}{2} \frac{E_m^2}{\eta} \text{ W/m}^2$$

where $E_m \rightarrow$ Amplitude of the Electric field intensity

$\eta \rightarrow$ Intrinsic impedance of a medium

The average Power ~~transmitted~~ incident in medium-1 is given by

$$P_{iavg} = \frac{1}{2} \frac{E_i^2}{\eta_1} \text{ W/m}^2$$

The average Power reflected in medium-1 is given by

$$P_{ravg} = \frac{1}{2} \frac{E_r^2}{\eta_1} \text{ W/m}^2$$

The ratio of Power transmitted to Power incident is given by

$$\frac{P_{tavg}}{P_{iavg}} = \frac{1/2\, E_t^2/\eta_2}{1/2\, E_i^2/\eta_1} = \frac{\eta_1}{\eta_2}\left[\frac{E_t}{E_i}\right]^2 = \frac{\eta_1}{\eta_2}\left[\frac{2\eta_2}{\eta_2+\eta_1}\right]^2 = \frac{4\eta_1\eta_2}{(\eta_1+\eta_2)^2}$$

Arranging terms we can write,

$$P_{tavg} = \frac{4\eta_1\eta_2}{(\eta_1+\eta_2)^2} P_{iavg} \quad \text{---} \quad (1)$$

$$= \frac{\eta_1^2 + 2\eta_1\eta_2 + \eta_2^2 - (\eta_2^2 - 2\eta_1\eta_2 + \eta_1^2)}{(\eta_1+\eta_2)^2} P_{iavg}$$

$$= \frac{(\eta_1+\eta_2)^2 - (\eta_2-\eta_1)^2}{(\eta_1+\eta_2)^2} P_{iavg}$$

$$= \left[\frac{(\eta_1+\eta_2)^2}{(\eta_1+\eta_2)^2} - \frac{(\eta_2-\eta_1)^2}{(\eta_1+\eta_2)^2}\right] P_{iavg}$$

$$\boxed{P_{tavg} = \left[1 - |\Gamma|^2\right] P_{iavg}} \quad \text{---} \quad (2)$$

The ratio of Power reflected to Power incident is given by,

$$\frac{P_{ravg}}{P_{iavg}} = \frac{1/2\, E_r^2/\eta_1}{1/2\, E_i^2/\eta_1} = \left[\frac{E_r}{E_i}\right]^2 = \left[\frac{\eta_2-\eta_1}{\eta_2+\eta_1}\right]^2 = \frac{(\eta_2-\eta_1)^2}{(\eta_1+\eta_2)^2} \quad \text{---} \quad (3)$$

Rearranging terms we get

$$P_{ravg} = \frac{(\eta_2 - \eta_1)^2}{(\eta_2 + \eta_1)^2} P_{iavg}.$$

$$\therefore \boxed{P_{ravg} = (\Gamma)^2 P_{iavg}} \quad \text{--- (4)}$$

Adding (1) and (3) we get

$$\frac{P_{tavg}}{P_{iavg}} + \frac{P_{ravg}}{P_{iavg}} = \frac{4\eta_1\eta_2}{(\eta_1+\eta_2)^2} + \frac{(\eta_2-\eta_1)^2}{(\eta_1+\eta_2)^2}$$

$$= \frac{\eta_1^2 + \eta_2^2 + 2\eta_1\eta_2}{(\eta_1+\eta_2)^2} = \frac{(\eta_1+\eta_2)^2}{(\eta_1+\eta_2)^2}$$

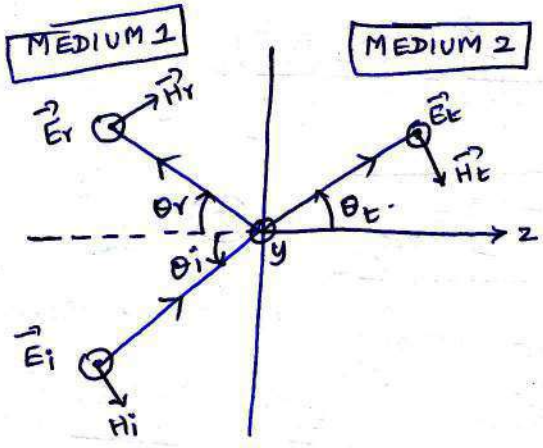
$$= 1$$

$$\therefore \boxed{P_{tavg} + P_{ravg} = P_{iavg}} \quad \text{--- (5)}.$$

OBLIQUE INCIDENCE:-

When a uniform plane wave strikes obliquely on the surface (either conductor or dielectric), the behaviour of the reflected wave is decided by the polarization of the incident wave. There are two cases for the oblique incidence as given below.

case (i): The electric field vector $\perp^r$ to the plane of incidence. In other words, the Electric field vector is aligned $\parallel^{el}$ to the boundary surface as shown below. This is called Horizontal Polarization.



According to Poynting Theorem, The average Power density is given by,

$$P_{avg} = \frac{1}{2} \frac{E_m^2}{\eta} \text{ W/m}^2$$

where $E_m \rightarrow$ Amplitude of the Electric field intensity

$\eta \rightarrow$ Intrinsic impedance of a medium

The average Power ~~transmitted~~ incident in medium-1 is given by

$$P_{iavg} = \frac{1}{2} \frac{E_i^2}{\eta_1} \text{ W/m}^2$$

The average Power reflected in medium-1 is given by

$$P_{ravg} = \frac{1}{2} \frac{E_r^2}{\eta_1} \text{ W/m}^2$$

The ratio of Power transmitted to Power incident is given by

$$\frac{P_{tavg}}{P_{iavg}} = \frac{1/2\, E_t^2/\eta_2}{1/2\, E_i^2/\eta_1} = \frac{\eta_1}{\eta_2}\left[\frac{E_t}{E_i}\right]^2 = \frac{\eta_1}{\eta_2}\left[\frac{2\eta_2}{\eta_2+\eta_1}\right]^2 = \frac{4\eta_1\eta_2}{(\eta_1+\eta_2)^2}$$

Arranging terms we can write,

$$P_{tavg} = \frac{4\eta_1\eta_2}{(\eta_1+\eta_2)^2} P_{iavg} \quad \text{---} \quad (1)$$

$$= \frac{\eta_1^2 + 2\eta_1\eta_2 + \eta_2^2 - (\eta_2^2 - 2\eta_1\eta_2 + \eta_1^2)}{(\eta_1+\eta_2)^2} P_{iavg}$$

$$= \frac{(\eta_1+\eta_2)^2 - (\eta_2-\eta_1)^2}{(\eta_1+\eta_2)^2} P_{iavg}$$

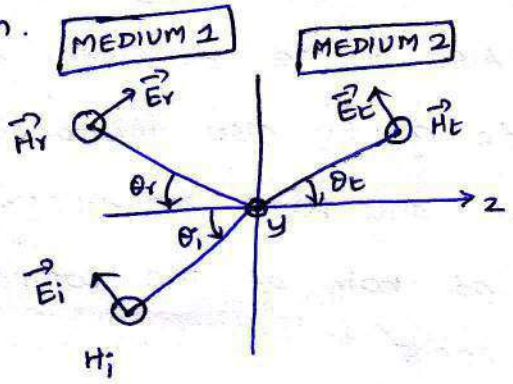
$$= \left[\frac{(\eta_1+\eta_2)^2}{(\eta_1+\eta_2)^2} - \frac{(\eta_2-\eta_1)^2}{(\eta_1+\eta_2)^2}\right] P_{iavg}$$

$$\boxed{P_{tavg} = \left[1 - |\Gamma|^2\right] P_{iavg}} \quad \text{---} \quad (2)$$

The ratio of Power reflected to Power incident is given by,

$$\frac{P_{ravg}}{P_{iavg}} = \frac{1/2\, E_r^2/\eta_1}{1/2\, E_i^2/\eta_1} = \left[\frac{E_r}{E_i}\right]^2 = \left[\frac{\eta_2-\eta_1}{\eta_2+\eta_1}\right]^2 = \frac{(\eta_2-\eta_1)^2}{(\eta_1+\eta_2)^2} \quad \text{---} \quad (3)$$

CASE(ii) : The magnetic field vector is aligned $\parallel^{el}$ to the boundary surface. In other words, the magnetic field vector is $\perp^{r}$ to the plane of incidence while electric field vector is aligned $\parallel^{el}$ to the plane of incidence as shown below. This is called vertical Polarization.



PLANE OF INCIDENCE:-

A plane of incidence is a plane containing the vector in the direction of Propagation of the incident wave and the normal to the boundary surface.

POLARIZATION OF ELECTROMAGNETIC WAVES:

The Polarization of uniform plane waves is defined as time varying behaviour of the Electric field intensity vector $\vec{E}$ at some fixed point in space, along the direction of Propagation.

There are three different types of Polarization of a uniform plane wave as given below

(a) Linear Polarization
(b) Elliptical Polarization
(c) Circular Polarization.

In other words Polarization is nothing but the way in which the magnitude and direction of the electric field varies.

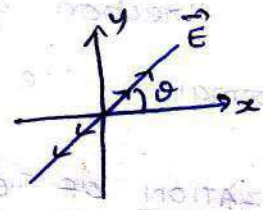
LINEAR POLARIZATION:

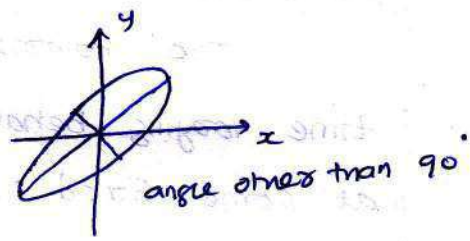
Let the components of $\vec{E}$ be $\vec{E_x}$ and $\vec{E_y}$ along x and y-direction respectively. Both these components are in phase having different amplitudes. As $\vec{E_x}$ and $\vec{E_y}$ are in phase they will have their amplitudes reaching max or min value simultaneously. Also if the amplitude of $\vec{E_x}$ increases or decreases the amplitude of $\vec{E_y}$ also increases or decreases.

In other words, at any point along +ve z-axis the ratio of amplitudes of both of the components is constant as both of them are in phase having same wavelength

The electric field $\vec{E}$ is the resultant of $\vec{E_x}$ & $\vec{E_y}$ and the direction of it depends on the relative magnitude of $\vec{E_x}$ & $\vec{E_y}$. Thus the angle made by $\vec{E}$ with x-axis is given by,

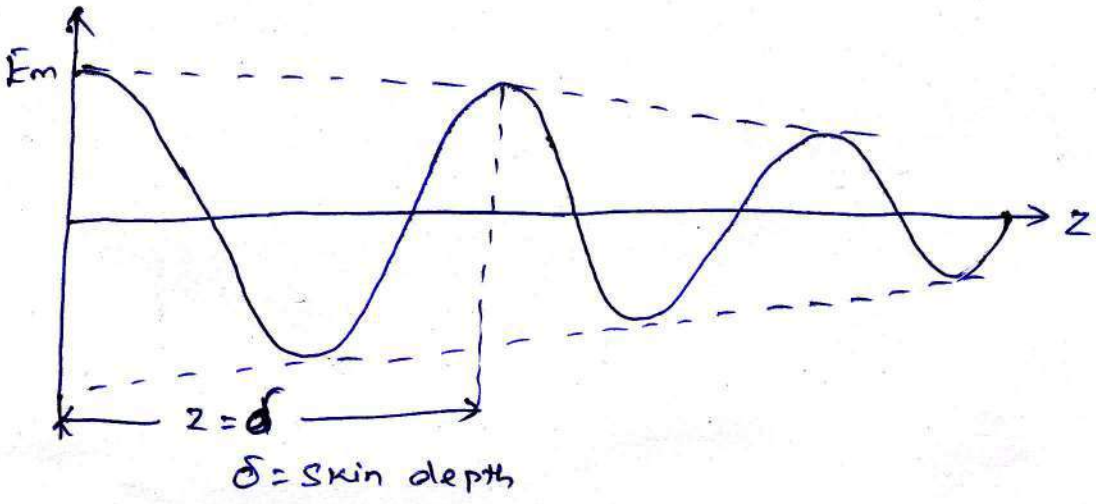
$$\theta = \tan^{-1} \frac{E_y}{E_x}.$$





SKIN DEPTH:

The skin depth is defined as the depth in which the wave has attenuated to 1/e ie, approximately 37% of its original value. It is also called as depth of Penetration.



Problem:

(1) A 300 Hz uniform plane wave propogate through fresh water for which sigma = 0, $\mu_r = 1$, $\varepsilon_r = 78$. Calculate wavelength.

Given $f = 300$ Hz, sigma = 0, $\mu_r = 1$, $\varepsilon_r = 78$

$$\beta = \omega\sqrt{\mu\varepsilon} = \omega\sqrt{(\mu_0\mu_r)(\varepsilon_0\varepsilon_r)}$$

$$\omega = 2\pi f$$

$$\beta = (2 \times \pi \times 300) \times \sqrt{(4\pi \times 10^{-7})(1)(8.854 \times 10^{-12})(78)}$$

$$\beta = 5.54 \times 10^{-4} \text{ rad/m}$$

$$\lambda = \frac{2\pi}{\beta} = \frac{2\pi}{5.54 \times 10^{-4}}$$

$$\lambda = 1.13 \times 10^{-4} \text{ mere}$$

UNIT I INTRODUCTION

Electromagnetic model, Units and constants, Review of vector algebra, Rectangular, cylindrical and spherical coordinate systems, Line, surface and volume integrals, Gradient of a scalar field, Divergence of a vector field, Divergence theorem, Curl of a vector field, Stoke's theorem, Null identities, Helmholtz's theorem

PART - A

Q. No.	Questions
1.	List the source quantities in the electromagnetic model.
2.	Describe line, surface and volume charge density.
3.	State divergence theorem.
4.	Define Stokes theorem.
5.	Name the universal constants in the electromagnetic model.
6.	What are surface and volume integrals?
7.	Give the relationship between potential and electric field intensity.
8.	Identify the unit vector and its magnitude corresponding to the given vector $\boldsymbol{A}=5\,\hat{\mathbf{a}}_x + \hat{\mathbf{a}}_y + 3\,\hat{\mathbf{a}}_z$.
9.	Estimate the distance between the given vectors $\boldsymbol{A}$ (1, 2,3) and $\boldsymbol{B}$ (2,1,2).
10.	Outline the relationship between magnetic flux density and field density.
11.	Calculate the values of universal constants of free space.
12.	Analyze a differential volume element in spherical coordinates (r,θ,φ) resulting from differential charges in the orthogonal coordinate systems.
13.	Specify the unit vector extending from the origin towards the point G (2,-2,-1).
14.	Compare orthogonal and non-orthogonal coordinate systems.
15.	Point out the role of vector algebra in electromagnetics.
16.	Convert the point P (5, 1, 3) from Cartesian to spherical coordinates.
17.	Show the transformation between spherical and Cartesian coordinates.
18.	Justify that electric field is conservative.
19.	Obtain the gradient of $V=10\, r \sin^2\theta \cos\varphi$.
20.	Assess the measurement of strength of flow and vortex source.

PART - B

1. What is electromagnetics? Give the advantages and disadvantage of fieldand circuit theory. (13)
2. Tabulate the various field, source and universal quantities ofelectromagnetic model and explain. (13)
3. (i) Write short notes on vector algebra. (5)
   (ii) Given the two vectors A and B , How do you find
   a) The component of A in the direction of B
   b) The component of B in the direction of A (8)
4. Explain how an orthogonal co-ordinate system describes the position of thepoint in free space.(13)
5. Summarize about the curl of a vector field in cylindrical and sphericalcoordinates.(13)

6. Obtain the expressions for differential area and volume element incylindrical coordinate system.(13)

7. Analyze the geometrical position of the point in Cartesian coordinatesystem and obtain the algebraic equations.(13)

8. Express the space rate of change of a scalar in a given direction in terms ofits gradient. (13)

9. Apply divergence theorem to find the divergence of the vector field in curvilinear coordinate system.(13)

10. State and prove divergence theorem for a given differential volumeelement. (13)

11. Assess the position of the vector field in spherical coordinate system andderive the expressions for differential areas.(13)

12. Explain the difference between irrotational and solenoidal field usingHelmholtz theorem. (13)

13. (i) Verify the null identities using general orthogonal curvilinearcoordinates. (7)
(ii) How do you transform the vectors between Cartesian and cylindricalsystems? (6)

14. Elaborate the Stokes theorem with their applications. (13)

PART - C

1. Given the two points A (x=2, y=3,z=-1) and B ($r=4,\theta=25^0,\varphi=120^0$). Solvethe spherical coordinates of A and Cartesian coordinates of B. (15)

2. The equation of the straight line in the XY plane is given by 2x+y=4.

   a) Find the vector equation of a unit normal from the origin to the line.
   b) Find the equation of the line passing through the point P (0,2) andperpendicular to the given line. (15)

3. Validate stokes theorem for a vector field $\overline{F} = r^2\cos\varphi a_{\bar{r}} + z\sin\varphi\, a_{\bar{z}}$ and the path L defined by $0\leq r\leq 3$, $0\leq\varphi\leq 45^{\cdot}$ and z=0. (15)

4. Estimate the position of the point in Cartesian and spherical coordinates ifthe position of the point in cylindrical coordinates is given as $(4, 2\pi/3, 3)$. (15)

UNIT II ELECTROSTATISTICS

Electric field, Coulomb's law, Gauss's law and applications, Electric potential, Conductors in static electric field, Dielectrics in static electric field, Electric flux density and dielectric constant, Boundary conditions, Capacitance, Parallel, cylindrical and spherical capacitors, Electrostatic energy, Poisson's and Laplace's equations, Uniqueness of electrostatic solutions, Current density and Ohm's law, Electromotive force and Kirchhoff's voltage law, Equation of continuity and Kirchhoff's current law

PART – A

Q.No	Questions
1.	Define electric field intensity.
2.	Write the significance of Columbs law.
3.	What is the difference between permittivity and dielectric constant of amedium?
4.	Why the electrostatic potential is continuous at boundary?
5.	Describe the boundary conditions for electrostatic fields.
6.	State Gauss law.
7.	Calculate the values of *D* and *P* for a certain linear, homogeneous, isotropic dielectric material having relative permittivity of 1.8 and electric field intensity of $4000a_y$V/m.
8.	Give the relationship between electric flux density and polarization.
9.	Differentiate between homogeneous and non-homogeneous medium.
10.	List the properties of conductor and dielectric materials.
11.	Describe about capacitance and capacitors.
12.	Solve the energy stored in a 10 μF capacitor which has been charged to a voltage of 400v.
13.	How do you find the equivalent capacitance of series and parallel-connected capacitors?
14.	Obtain the relation between current and current density.
15.	Identify equation of Ohm’s law in point form.
16.	Compare Poisson’s and Laplace’s equation.
17.	Evaluate the unique solution of electrostatic fields.
18.	Calculate the value of capacitance between two square plates having cross sectional area of 1 sq.cm separated by 1 cm placed in a liquid whose dielectric constant is 6 and the relative permittivity of free space is 8.854 pF/m.
19.	Formulate a mathematical expression for electrostatic energy.
20.	Derive the continuity equation in integral and differential form.

PART - B

1. (i) List out the properties of dielectric materials. (3)
   (ii) Brief note on conductors and dielectrics in a static electric field. (10)
2. Derive the boundary conditions of the normal and tangential components ofelectric field at the interface of two media with different dielectrics. (13)
3. Obtain a formula for the electric field intensity on the axis of a circular discof radius b and carries uniform charge density ρ_s. (13)
4. Describe the electric potential due to electric dipole in spherical coordinatesystem.(13)

5. Explain about any two applications of Gauss law with neat diagrams. (13)

6. Determine the electric field intensity at P(-0.2,0,-2.3) due to a point chargeof +5nC at Q(0.2,0.1,-2,5) in air. All dimensions are in meter. (13)

7. The region y<0 contains a dielectric material for which ε_{r1}=2.5, while the region y>0 is characterized by ε_{r2}=4. Let $\boldsymbol{E_1}$=-30 $\hat{\mathbf{a}}_x$+ 50 $\hat{\mathbf{a}}_y$+70 $\hat{\mathbf{a}}_z$ V/m. Interpret (a)E_{N1}, (b) $|E_{tan1}|$, (c)E_1, (d) θ_1 (13)

8. Explain the importance of Poisson's and Laplace's equation inelectromagnetics with necessary equations. (13)

9. (i) Find the total current in a circular conductor of radius 4 mm if the current density varies according to J = (10^4/r) A/m^2. (8)

   (ii) Calculate the capacitance of a parallel plate capacitor having a mica dielectric, ε_r=6, a plate area of 10 $inch^2$, and a separation of 0.01inch. (5)

10. Formulate the expression for electrostatic energy required to assemble agroup of charges at rest. (13)

11. A cylindrical capacitor consists of an inner conductor of radius 'a' & an outer conductor whose inner radius is 'b'. The space between the conductors is filled with a dielectric permittivity ε_r & length of the capacitor is L. Estimate the value of the Capacitance. (13)

12. (i) Write the equation of continuity in integral and differential form. (8)

    (ii) Discuss the energy stored and energy density in a capacitor withsupporting expressions. (5)

13. (i) Analyze the capacitance of a parallel plate capacitor with dielectric ε_{r1} =1.5 and ε_{r2} = 3.5 each occupy one half of the space between the plates ofarea 2 m^2 and d = 10^{-3}m. (10)

    (ii) State Kirchoff 's current and voltage law. (3)

14. A capacitor with two dielectrics as follows: Plate area 100 cm^2, dielectric 1 thickness = 3 mm, ε_{r1}=3dielectric 2 thickness = 2 mm, ε_{r2}=2. If a potential of 100 V is applied across the plates, evaluate the Capacitance and the energy stored. (13)

PART - C

1. (i) Determine the dc resistance of 1km of wire having a 1mm radius a) ifthe wire is made of copper b) if the wire is made of aluminum. (10)

   (ii) A metallic sphere of radius 10 cm has a surface charge density of 10nC/m^2. Calculate the energy stored in the system. (5)

2. A capacitor consists of two coaxial metallic cylindrical surfaces of a length 30mm and radius 5mm& 7mm. the dielectric material between the surfaces has a relative permittivity ε_r =2+(4/r), where r is measured in mm. Determine the capacitance of the capacitor. (15)

3. Formulate the energy required to assemble a uniform sphere of charge with radius b and volume charge density ρ C/m^3. (15)

4. Determine the E field both inside and outside a spherical cloud of electrons with a uniform volume charge density $\rho = -\rho_0$ for $0 \leq R \leq b$ and $\rho = 0$ for R>b by solving laplace and poisons equations for V. (15)

UNIT III MAGNETOSTATICS

Lorentz force equation, Law of no magnetic monopoles, Ampere's law, Vector magnetic potential, Biot- Savart law and applications, Magnetic field intensity and idea of relative permeability, Magnetic circuits, Behaviour of magnetic materials, Boundary conditions, Inductance and inductors, Magnetic energy, Magnetic forces and torques

PART - A

Q.No	Questions
1.	Define magnetic dipole moment.
2.	State Biot-Savart's law.
3.	Describe Ampere's circuital law.
4.	What is scalar magnetic potential & vector magnetic potential?
5.	Write the relation between magnetic flux and flux density.
6.	List the applications of Ampere's circuital law.
7.	Point out the relation between magnetic flux density and magnetic fieldintensity.
8.	Outline the concept of self-inductance.
9.	Infer the Lorentz force equation for a moving charge?
10.	Explain the hall effect.
11.	Identify the relationship between magnetic field intensity and permeability.
12.	Classify the different types of magnetic materials.
13.	Derive the expression of H for a solenoid having N turns of finite length d.
14.	Express the inductance of a toroid for the coil of N turns.
15.	Examine the magnetic flux density in vector form for the given vector magnetic potential $\boldsymbol{A} = 10/(x^2+y^2+z^2)\ \hat{\mathbf{a}}_x$.
16.	An inductive coil of 10mH is carrying a current of 10A. Analyze the energystored in the magnetic field.
17.	An infinitesimal length of wire is located at (1,0,0) and carries a current 2A in the direction of the unit vector $\mathbf{a}_z$. Find the Magnetic Flux Density $\boldsymbol{B}$ due to the current element at the field point (0,2,2).
18.	A ferrite material has $\mu_r = 50$ operating with sufficiently low flux densities and $\boldsymbol{B}$=0.05 Tesla. Compute magnetic field intensity.
19.	Show the permeability of the material whose magnetic susceptibility is 49.
20.	Propose the two basic equations for the analysis of magnetic circuits.

PART – B

1. From the Biot Savart's law, write the expression for magnetic field intensity at a point P and distance R from the infinitely long straight current carrying conductor. (13)
2. Derive the equations for magnetic field intensity and magnetic flux density atthe centre of the square current loop with side *w* using Biot Savart's law. (13)
3. Write short notes on
   i) Magnetic circuits (5)
   ii) Magnetic forces and torques (8)

4. State about magnetization? Describe the classification of magnetic materialswith examples. (13)

5. Determine the magnetic field intensity at the origin due to currentelement Idl = $3\pi(\hat{\mathbf{a}}_x + 2\,\hat{\mathbf{a}}_y + 3\hat{\mathbf{a}}_z)$ μA at(3,4,5)m in free space. (13)

6. (i) Discuss about the forces and torques acting on a current carrying conductorin a uniform magnetic field. (8)

   (ii) Illustrate how Vector Magnetic potential is obtained from Biot Savart law. (5)

7. (i) Using Biot-Savart's law, illustrate the magnetic field intensity on the axis ofa circular loop of radius R carrying a steady current I. (8)

   (ii) A circular loop located on $x^2 + y^2 = 9$, z = 0 carries a direct current of 10 A along a_φ. Calculate **H** at (0,0,4) and (0,0,-4). (5)

8. Discover the expression of magnetic energy in terms of B and H. (13)

9. Solve the magnetic field at a point P(0.01, 0, 0)m if current through a co-axialcable is 6 A. which is along the z-axis and a=3mm, b=9mm, c=11mm. (13)

10. Analyze the expression for inductance of a toroidal coil carrying current I, withN turns and the radius of toroid 'r'. (13)

11. Examine the magnetic field intensity within a magnetic material where a)M=150A/m and $\mu=1.5\times10^{-5}$ H/m (b)B=300μT and χ_m=15. (13)

12. Describe about the magnetic boundary condition at the interface between two magnetic medium. (13)

13. A solenoid with N_1=2000, r_1=2 cm and l_1= 100cm is concentric within a second coil of N_2= 4000, r_2= 4cm and l_2=100cm.Calculate mutual inductance assuming free space conditions. (13)

14. Formulate the magnetic flux density around infinitely long straight conductorby magnetic vector potential. (13)

PART – C

1. Validate the expression which relates Magnetic Flux density B and Magnetic vector potential A. Demonstrate the expression with the supporting laws. (15)

2. (i) At a point P(x,y,z) the components of vector magnetic potential $\vec{A}$ are given as A_z = (4x + 3y+2 z) , A_y =(5x +6y +3 z) and A_z= (2x+3y+5z). Invent $\vec{B}$ at point P. (8)

   (ii) A solenoid has an inductance of 20mH. If the length of the solenoid is increased by two times and the radius is decreased to half of its original value, Compute the new inductance. (7)

3. Region 1 is the semi-infinite space in which 2x-5y>0, while region 2 is definedby 2x-5y<0. Let μ_{r1}=3, μ_{r2}=4 and $\bar{H}_1=30\bar{a}_x$ A/m. Calculate
   (a) $|\bar{B}_1|$, (b)$|\bar{B}_{N1}|$, (c) $|\bar{H}_{tan1}|$, (d) $|\bar{H}_2|$. (15)

4. (i) A solenoid is 50 cm long, 2 cm in diameter and contains 1500 turns. The cylindrical core has a diameter of 2 cm and a relative permeability of 75. This coil is co-axial with second solenoid which is 50 cm long, 3 cm diameter and 1200 turns. Solve the inductance L for inner and outer solenoid. (7)

   (ii) Propose the solution for energy stored in the solenoid having 50cm long and 5 cm in diameter and is wound with 2000 turns of wire, carrying a current of 10 A. (8)

UNIT IV TIME-VARYING FIELDS AND MAXWELL's EQUATIONS

Faraday's law, Displacement current and Maxwell-Ampere law, Maxwell's equations, Potential functions, Electromagnetic boundary conditions, Wave equations and solutions, Time-harmonic fields

PART - A

1 State lenz's law?
2 What are the characteristics of an ideal transformer?
3 Write the source free wave equations for E and H in free space?
4 Why are the frequencies below the VLF range rarely used for wireless transmission?
5 Show the expression for time harmonic retarded scalar and vector potentialsin terms of charge and current distributions
6 Why are materials having high permeability and low conductivity preferred as transformer cores?
7 Infer the electromagnetic boundary conditions.
8 Summarize the differential form of Maxwell's Equation.
9 Outline the difference between phasor and vector?
10 Illustrate the non-homogenous wave equation for scalar potential V and for vector potential A.
11 Develop the expression for retarded potential?
12 Identify the significance on loss tangent of a medium.
13 Find the Poynting vector on the surface of a long straight conducting wire of radius 'b' and conductivity σ that carries a direct current I.
14 Analyze the Lorentz condition for potentials? What is its physical significance?
15 Point out the coefficient of coupling in inductive circuits.
16 Develop the expression for wave number.
17 Explain the significance of displacement current.
18 Fundamental postulates of electromagnetic induction, and examine how itleads to Faraday's law.
19 Are conduction and displacement currents in phase for time harmonic fields? Justify.
20 A wave propagates from a dielectric medium to the interface with free space if the angle of incidence is the critical angle 20^0. Solve for relative permittivity of the medium.

PART B

1 Write the boundary conditions that exist at the interface of free space and a magnetic material of infinite permeability. (13)
2 A circular loop of N turns of conducting wire lies in the XY plane with its center at the origin og magnetic field specified by $B= a_z B_0 \cos(\pi r/2b) * \sin wt$ where, b is the radius of the loop and w is the angular frequency. Find the emf induced in the loop. (13)
3 i) Write short notes about displacement current and displacement current density. (8)
(ii) In a given lossy dielectric medium, conduction current density $J_c=0.02 \sin 10^9 t$ (A/m^2). Find the displacement current density if $\sigma=10^3$ S/m and $\varepsilon_r=6.5$

(5)

4 Show Maxwell's equation for static fields. Explain how they are modified for time varying electric and magnetic fields. (13)

5 Derive the expressions for time harmonic retarded scalar and vector potentialsin terms of charge and current distributions. (13)

6 Illustrate the integral and point form of Maxwell's equations from Faraday'slaw and Ampere's law. (13)

7 Express the transformer EMF induced in a stationary loop in terms of time varying vector potential A. (13)

8 Discuss about the propagation of the plane waves in free space and in a homogeneous material. (13)

9 Demonstrate the detailed steps for the derivation of electromagnetic boundary conditions. (13)

10 Illustrate the two divergence equations from the two curl equations and the equation of continuity. (13)

11 Point out the set of Maxwell's equations as eight scalar equations

(i) In Cartesian Coordinates

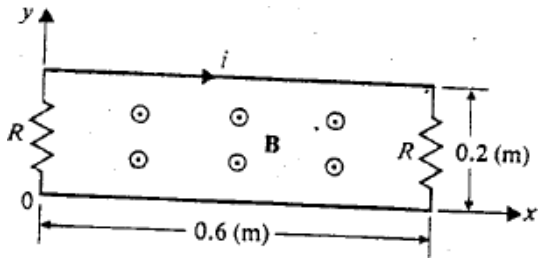
(ii) In Cylindrical Coordinates

(iii) In Spherical Coordinates (13)

12 Calculate the general wave equations for E and H in a non-conducting simple medium where a charge distribution ρ and a current distribution J exist. Convert the wave equations to Helmholtz's equations for sinusoidal time dependence. (13)

13 Prove that the Lorentz condition for potentials are consistent with the equation of continuity. (13)

14 The circuit is situated in a magnetic field assuming R= 15 ohm. Find the current i?
$B= a_z 3\cos(5\pi 10^7 t - \frac{2}{3}\pi x)$ (μT) (13)



PART - C

1 Evaluate the general wave equations for E and H in a non-conducting simple medium where a charge distribution ρ and a current distribution J exist. Convert the wave equations to Helmholtz's equations for sinusoidal time dependence. Write the general solutions for E(R,t) and H(R,t) in terms of ρ and J. (15)

2 Deduce the intrinsic impedance equation from the relation between $\bar{E}$ and $\bar{H}$ in free space. (15)

3 Calculations concerning the Electromagnetic effect of currents in a good conductor usually neglect the displacement current even at microwave frequencies.

(a) Assuming $\varepsilon_r = 1$, $\sigma = 5.7 * 10^7$ s/m for copper compare the magnitude of displacement current density with that of the conduction current density at 100 GHz. (8)

(b) (b) Write the governing differential equations for magnetic field intensity H in a source free good conductor. (7)

4 (i) Estimate the value of k such that following pairs of field satisfies Maxwell's equation in the region where $\sigma = 0$, $\sigma_v = 0$

(a) $\bar{E} = [kx - 100t]\,\bar{a}_y$ V/m, $\bar{H} = [x + 20t]\,\bar{a}_z$ A/m and $\mu = 0.25$H/m, $\varepsilon = 0.01$F/m

(b) $\bar{D} = 5x\bar{a}_x - 2\bar{a}_y + kz\bar{a}_z$ μC/m^2, $\bar{B} = 2\bar{a}_y$ mT and $\mu = \mu_0$, $\varepsilon = \varepsilon_0$. (8)

(ii) If the magnetic field $\bar{H} = [3x \cos\beta + 6y \sin\alpha]\,\bar{a}_z$, find current density $\bar{\mathbf{J}}$ if fields are invariant with time. **(7)**

UNIT V PLANE ELECTROMAGNETIC WAVES

Plane waves in lossless media, Plane waves in lossy media (low-loss dielectrics and good conductors), Group velocity, Electromagnetic power flow and Poynting vector, Normal incidence at a plane conducting boundary, Normal incidence at a plane dielectric boundary.

PART - A

1 Define uniform plane wave.
2 State pointing theorem.
3 Describe the characteristics of uniform plane wave?
4 What is the significance of plasma frequency?
5 Give the relation between group velocity Vs phase velocity
6 Show the constitution of ionosphere.
7 Demonstrate Doppler effect.
8 Point out the difference between reflection and transmission coefficient
9 Infer about polarization of a wave. When a wave is linearly polarized and circularly polarized.
10 Explain the significance of pointing vector?
11 Identify the relationship between SWR and reflection coefficient.
12 Construct the phasor expressions for E and H field intensity vectors of an x-polarized uniform plane wave propagating in the +z direction.
13 Derive the condition for parallel and perpendicular polarization?
14 Express the values of the reflection and transmission coefficients at an interfacewith a perfectly conducting boundary?
15 Examine the wave impedance of the total magnetic field.
16 Analyze the polarization of AM and FM broadcasting stations
17 Find the value of free space intrinsic impedance.
18 Compute the skin depth of a conductor? How it is related to attenuation constant?
19 Show the phasor expressions of normal incidence of a plane dielectricboundary.
20 Develop the expressions in terms of electric and magnetic field intensity vectors for a) instantaneous Poynting vector b)time average Poynting vector

PART – B

1 Find the wave equations governing the E and H field in a source free conducting medium with parameters ε,μ,σ (13)
2 Show that the instantaneous pointing vector of a circularly polarized wave propagating in a lossless medium is independent of time and distance. (13)
3 Write short notes on plane waves in lossy and lossless medium. (13)

4 State and prove Poynting theorem. (8)
Describe the Poynting vector, average power and instantaneous power. (5)

5 Determine the condition under which the magnitude of the reflection coefficient equals that of the transmission coefficient for a uniform wave at normal incidence on an interface between two lossless dielectric medium. (13)

6 Explain the use of Doppler effect in radar applications. (13)

7 Demonstrate the equations for a plane wave incident normally on a plane dielectric boundary. (13)

8 A uniform plane wave in a lossless medium with intrinsic impedance Ƞ1 is incident normally onto another lossless medium with intrinsic impedance Ƞ2 through a plane boundary. Develop the expressions for the time average powerdensities. (13)

9 Generalize and prove the electric field intensity in lossy media satisfies the homogeneous Helmholtz's equation. (13)

10 Determine and compare the intrinsic impedance, attenuation constant and skindepth of a conducting medium. (13)

11 Calculate the polarization of the reflected wave for a right hand circularly polarized plane wave. (13)

12 Demonstrate the pointing vector on the surface of a long straight conductingwire of radius b that carries a direct current I. Verify poynting's theorem. (13)

13 Examine the general expressions of the attenuation and phase constant for conducting medium. (13)

14 Estimate the group velocity of a signal that propagates in a lossy dielectric medium. (13)

PART – C

1 A uniform plane wave with $E= a_x E_x$ propagates in a lossless simple medium ($\varepsilon_r = 4, \mu_r=1, \sigma=0$) in the +Z direction. Assume that E_x is sinusoidal with a frequency of 100 MHz and has a maximum value of $+10^{-4}$ V/m at t=0 and Z= 1/8 m

a. write the instantaneous expression for E & H for any t and Z

b. determine the locations where E_x is a positive maximum when $t=10^{-8}$ sec (15)

2 A narrow band signal propagates in a lossy dielectric medium which has a loss tangent 0.2 at 550 KHz, the career frequency of the signal. The dielectric constant of the medium is 2.5

a. Compute α and β
b. Calculate phase velocity and group velocity.
c. Evaluate the medium is dispersive (15)

3 A y- polarized uniform plane wave (E_i, H_i) with a frequency 100 MHz propagates in the +X direction and impinges normally on a perfectly conducting plane at x=0. Assume E_i = 6mV/m.
Develop the phasor and instantaneous expressions for
a. E_i, H_i of the incident wave
b. E_r, H_r of the reflected wave
c. E_1,H_1 of the total wave in air (15)

4 Given that the skin depth for graphite at 100 MHz is 0.16 mm. Estimate
a. Conductivity of graphite,
b. The distance that 1 GHz wave travels in graphite such that it's field intensity is reduced by 30 dB (15)

MADHA
Expertise | Empathy | Excellence
ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

EC3354 SIGNALS AND SYSTEMS

Semester - 03

Notes

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Vision

To excel in providing value based education in the field of Electronics and Communication Engineering, keeping in pace with the latest technical developments through commendable research, to raise the intellectual competence to match global standards and to make significant contributions to the society upholding the ethical standards.

Mission

- ✓ To deliver Quality Technical Education, with an equal emphasis on theoretical and practical aspects.
- ✓ To provide state of the art infrastructure for the students and faculty to upgrade their skills and knowledge.
- ✓ To create an open and conducive environment for faculty and students to carry out research and excel in their field of specialization.
- ✓ To focus especially on innovation and development of technologies that is sustainable and inclusive, and thus benefits all sections of the society.
- ✓ To establish a strong Industry Academic Collaboration for teaching and research, that could foster entrepreneurship and innovation in knowledge exchange.
- ✓ To produce quality Engineers who uphold and advance the integrity, honour and dignity of the engineering.

PROGRAMEDUCATIONALOBJECTIVES(PEOs)

1. To provide the students with a strong foundation in the required sciences in order to pursue studies in Electronics and Communication Engineering.
2. To gain adequate knowledge to become good professional in electronic and communication engineering associated industries, higher education and research.
3. To develop attitude in lifelong learning, applying and adapting new ideas and technologies as their field evolves.
4. To prepare students to critically analyze existing literature in an area of specialization and ethically develop innovative and research oriented methodologies to solve the problems identified.
5. To inculcate in the students a professional and ethical attitude and anability to visualize the engineering issues in a broader social context.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Design, develop and analyze electronic systems through application of relevant electronics, mathematics and engineering principles.

PSO2: Design, develop and analyze communication systems through application of fundamentals from communication principles, signal processing, and RF System Design & Electromagnetics.

PSO3: Adapt to emerging electronics and communication technologies and develop innovative solutions for existing and newer problems.

EC3354 SIGNALS AND SYSTEMS L T P C
3 1 0 4

COURSE OBJECTIVES :

- To understand the basic properties of signal & systems
- To know the methods of characterization of LTI systems in time domain
- To analyze continuous time signals and system in the Fourier and Laplace domain
- To analyze discrete time signals and system in the Fourier and Z transform domain

UNIT I CLASSIFICATION OF SIGNALS AND SYSTEMS 6+6

Standard signals- Step, Ramp, Pulse, Impulse, Real and complex exponentials and Sinusoids_Classification of signals – Continuous time (CT) and Discrete Time (DT) signals, Periodic & Aperiodic signals, Deterministic & Random signals, Energy & Power signals -Classification of systems- CT systems and DT systems- – Linear & Nonlinear, Time-variant& Time-invariant,Causal & Non-causal, Stable & Unstable.

UNIT II ANALYSIS OF CONTINUOUS TIME SIGNALS 6+6

Fourier series for periodic signals - Fourier Transform – properties- Laplace Transforms and Properties

UNIT III LINEAR TIME INVARIANT CONTINUOUS TIME SYSTEMS 6+6

Impulse response - convolution integrals- Differential Equation- Fourier and Laplace transforms in Analysis of CT systems - Systems connected in series / parallel.

UNIT IV ANALYSIS OF DISCRETE TIME SIGNALS 6+6

Baseband signal Sampling–Fourier Transform of discrete time signals (DTFT)– Properties of DTFT - Z Transform & Properties

UNIT V LINEAR TIME INVARIANT-DISCRETE TIME SYSTEMS 6+6

Impulse response–Difference equations-Convolution sum- Discrete Fourier Transform and Z Transform Analysis of Recursive & Non-Recursive systems-DT systems connected in series and parallel.

TOTAL: 30+30 PERIODS

COURSE OUTCOMES:

At the end of the course, the student will be able to:

CO1:determine if a given system is linear/causal/stable
CO2: determine the frequency components present in a deterministic signal
CO3:characterize continuous LTI systems in the time domain and frequency domain
CO4:characterize continuous LTI systems in the time domain and frequency domain
CO5:compute the output of an LTI system in the time and frequency domains

TEXT BOOKS:

1. Oppenheim, Willsky and Hamid, “Signals and Systems”, 2nd Edition, Pearson Education, New Delhi, 2015.(Units I - V)
2. Simon Haykin, Barry Van Veen, “Signals and Systems”, 2nd Edition, Wiley, 2002

REFERENCES :

1. B. P. Lathi, “Principles of Linear Systems and Signals”, 2nd Edition, Oxford, 2009.
2. M. J. Roberts, “Signals and Systems Analysis using Transform methods and MATLAB”, McGraw- Hill Education, 2018.
3. John Alan Stuller, “An Introduction to Signals and Systems”, Thomson, 2007.

UNIT – I
CLASSIFICATION OF SIGNALS AND SYSTEMS

INTRODUCTION:

A signal, as stated before is a function of one or more independent variables. A signal is a quantitative description of a physical phenomenon, event or process. More precisely, a signal is a function, usually of one variable in time. However, in general, signals can be functions of more than one variable, e.g., image signals. Signals are functions of one or more variables.

Systems respond to an input signal by producing an output signal .
Examples of signals include:

1. A voltage signal: voltage across two points varying as a function of time.
2. A force pattern: force varying as a function of 2-dimensional space.
3. A photograph: color and intensity as a function of 2-dimensional space.
4. A video signal: color and intensity as a function of 2-dimensional space and time.

A continuous-time signal is a quantity of interest that depends on an independent variable, where we usually think of the independent variable as time. Two examples are the voltage at a particular node in an electrical circuit and the room temperature at a particular spot, both as functions of time.

A discrete-time signal is a sequence of values of interest, where the integer index can be thought of as a time index, and the values in the sequence represent some physical quantity of interest.

A signal was defined as a mapping from a set of the independent variable (domain) to the set of the dependent variable (co-domain). A system is also a mapping, but across signals, or across mappings. That is, the domain set and the co-domain set for a system are both sets of signals, and corresponding to each signal in the domain set, there exists a unique signal in the co-domain set.
System description

The system description specifies the transformation of the input signal to the output signal. In certain cases, a system has a closed form description. E.g. the continuous-time system with description y (t) = x(t) + x(t-1); where x(t) is the input signal and y(t) is the output signal.

Continuous-time and discrete-time systems

- Physically, a system is an interconnection of components, devices, etc., such as a computer or an aircraft or a power plant.
- Conceptually, a system can be viewed as a black box which takes in an input signal x(t) (or x[n]) and as a result generates an output signal y(t) (or (y[n]).
- A system is continuous-time (discrete-time) when its I/O signals are continuous-time (discrete-time).

Elementary Signals:

The elementary signals are used for analysis of systems. Such signals are,

- Step
- Impulse
- Ramp
- Exponential
- Sinusoidal

Unit step signal:

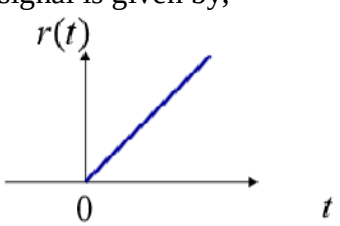
- Unit Step Sequence: The unit step signal has amplitude of 1 for positive value and amplitude of 0 for negative value of independent variable.
- It have two different parameter such as CT unit step signal u(t) and DT unit step signal u(n).
- The mathematical representation of CT unit step signal u(t) is given by,

Ramp Signal:

- The amplitude of every sample is linearly increased with the positive value of independent variable.
- Mathematical representation of CT unit ramp signal is given by,

The Ramp function

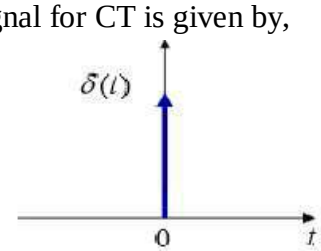
$$r(t) = t \cdot u(t)$$



Unit impulse function:

- Amplitude of unit impulse approaches 1 as the width approaches zero and it has zero value at all other values.
- The mathematical representation of unit impulse signal for CT is given by,

$$\delta(0) = \infty$$
$$\delta(t) = 0, t \neq 0$$
$$\int_{-\infty}^{t} \delta(t)dt = \begin{cases} 1, & t > 0 \\ 0, & t < 0 \end{cases}$$



- It is used to determine the impulse response of system.

Sinusoidal signal:

- A continuous time sinusoidal signal is given by,

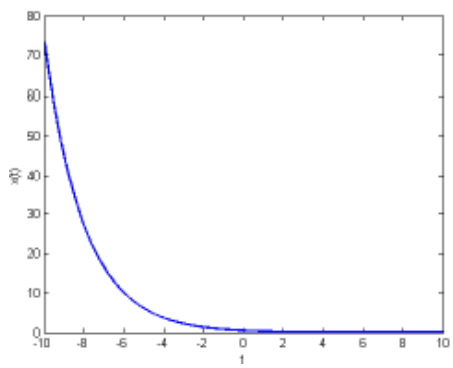
$$x(t) = A\cos(\Omega_0 t + \alpha)$$

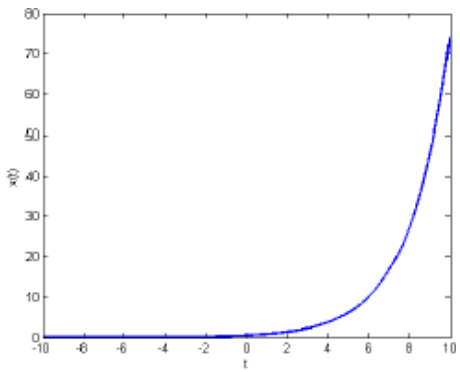
Where, A – amplitude α- phase angle in radians

Exponential signal:

- It is exponentially growing or decaying signal.
- Mathematical representation for CT exponential signal is,

$$x(t) = Ce^{at}, \quad where\ C, a \in \mathbb{C}$$





Classification of CT and DT signals:

- **Periodic and non-periodic Signals**

A periodic function is one which has been repeating an exact pattern for an infinite period of time and will continue to repeat that exact pattern for aninfinite time. That is, a periodic function x(t) is one for which

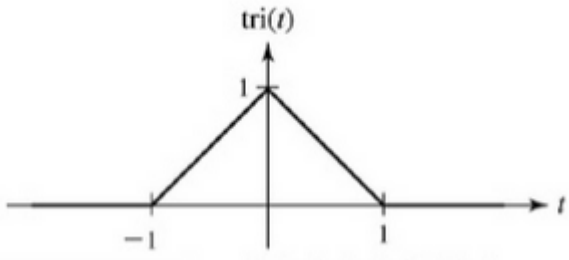
$$x(t) = x(t+nT)$$

for any integer value of n, where T >0 is the period of the function and $-\infty < t < \infty$. The signal repeats itself every T sec. Of course, it also repeats every 2 T,3T and nT. Therefore, 2T, 3T and nT are all periods of the function because the function repeats over any of those intervals. The minimum positive interval over which a function repeats itself is called the fundamental period T0.T0 is the smallest value that satisfies the condition x (t) = x (t+T0). The fundamental frequency f 0 of a periodic function is the reciprocal of the fundamental period f 0=1/T0. It is measured in Hertz and is the number of cycles (periods) per second. The fundamental angular frequency ω0 measured in radians per second is ω0=2πT0= 2πf0. A signal that does not satisfy the condition in (2.1) is said to be a periodic or non-periodic.

- **Deterministic and Random Signals**

Deterministic Signals are signals who are completely defined for any instant of time, there is no uncertainty with respect to their value at any point of time. They can also be described mathematically, at least approximately. Let a function be defined as

$$\mathrm{tri}(t) = \begin{cases} 1-|t|, & -1 < t < 1 \\ 0, & otherwise \end{cases}$$



A random signal is one whose values cannot be predicted exactly and cannot be described by any exact mathematical function, they can be approximately described.

- **Energy and Power Signals:**

Consider v(t) to be the voltage across a resistor R producing a current i(t). The instantaneous power p(t) per ohm is defined as, Total energy E and average power P on a per-ohm basis are

$$p(t) = \frac{v(t)i(t)}{R} = i^2(t)$$

For an arbitrary continuous-time signal x (t), the normalized energy content E of x(t) is defined as,

$$E = \int_{-\infty}^{\infty} i^2(t)\,dt \quad \text{joules}$$

$$P = \lim_{T\to\infty} \frac{1}{T}\int_{-T/2}^{T/2} i^2(t)\,dt \quad \text{watts}$$

The normalized average power P of x (t) is defined as,

$$E = \int_{-\infty}^{\infty} |x(t)|^2\,dt$$

Similarly, for a discrete-time signal x[n], the normalized energy content ***E*** of x[n] is defined as,

$$E = \sum_{n=-\infty}^{\infty} |x[n]|^2$$

The normalized average power P of x[n] is defined as,

$$P = \lim_{N\to\infty} \frac{1}{2N+1} \sum_{n=-N}^{N} |x[n]|^2$$

CT Systems and DT Systems:

A system is defined as a physical device which contains set of elements or functional blocks and that generates a response or output signal for a given input.

Classification of system:

The systems are classified as,

- Static & dynamic system
- Time invariant and variant system
- Linear and non linear system
- Causal and non causal system
- Stable and unstable system

Static and dynamic system:

- Static system is said to be a memoryless system.
- The output does not depend the past or future input.
- It only depends the present input for an output.

Eg, y(n) = x(n)

- Dynamic system is said to be as system with memory.
- Its output depend the past values of input for an output.

Eg. Y(n) = x(n) + x(n - 1)

- This static and dynamic systems are otherwise called as memoryless and system with memory.

Systems with and without memory:

- A system is called memory less if the output at any time t (or n) depends only on the input at time t (or n); in other words, independent of the input at times before of after t (or n). Examples of memory less systems:

$$y(t) = Rx(t) \qquad \text{or} \qquad y[n] = \left(2x[n] - x^2[n]\right)^2$$

Examples of systems with memory:

$$y(t) = \frac{1}{C}\int_{-\infty}^{t} x(\tau)d\tau \qquad \text{or} \qquad y[n] = x[n-1].$$

Time invariant and time variant system:

- If the time shifts in the input signals results in corresponding time shift in the output, then the system is called as time invariant.
- The input and output characteristics do not change with time.
- For a continuous time system,

f[x(t1 – t2)] = y(t1 – t2)

- For a discrete time system,

F[x(n - k)] = y(n - k)

- If the above relation does not satisfy, then the system is said to be a time variant system.
- A system is called time-invariant if the way it responds to inputs does not change over time:

$$x(t) \to y(t) \quad \Rightarrow \quad x(t-t_0) \to y(t-t_0), \quad \text{for any } t_0$$

$$x[n] \to y[n] \quad \Rightarrow \quad x[n-n_0] \to y[n-n_0], \quad \text{for any } n_0.$$

Examples of time-invariant systems:

- The RC circuit considered earlier provided the values of R or C are constant.

$$y[n] = x[n-1].$$

Examples of time-varying systems:

- The RC circuit considered earlier if the values of R or C change over time.

$$y(t) = x(2t) \text{ since}$$

$$x(t) \to x(2t) \quad \text{but} \quad x(t-t_0) \to x(2t-t_0).$$

- Most physical systems are slowly time-varying due to aging, etc. Hence, they can be considered time-invariant for certain time periods in which its behavior does not change significantly.

Linear and non linear system:

- A system is said to be linear if it satisfies the superposition principle.
- Superposition principle states that the response to a weighted sum of input signal be equal to the weighted sum of the output corresponding to each of the individual input signal
- The continuous system is linear if,

F[a1x1(t) + a2x2(t)] = a1y1(t) + a2y2(t)

- The discrete system is linear if,

F[a1x1(n) + a2x2(n)] = a1y1(n) + a2y2(n)

- Otherwise the system is non linear.
- A system is called linear if its I/O behavior satisfies the additivity and homogeneity properties:

$$\left.\begin{array}{l} x_1(t) \to y_1(t) \\ x_2(t) \to y_2(t) \end{array}\right\} \quad \Rightarrow \quad \begin{array}{c} (x_1(t) + x_2(t)) \to (y_1(t) + y_2(t)) \\ (ax_1(t)) \to (ay_1(t)) \end{array}$$

for any complex constant a.

- Equivalently, a system is called linear if its I/O behavior satisfies the superposition property:

$$\left.\begin{array}{l} x_1(t) \rightarrow y_1(t) \\ \\ x_2(t) \rightarrow y_2(t) \end{array}\right\} \quad \Rightarrow \quad (ax_1(t) + bx_2(t)) \rightarrow (ay_1(t) + by_2(t))$$

where any complex constants a and b.

Causal and non causal system:

- A causal system is one whose output depends upon the present and past input values.
- If the system depends the future input values, the system is said to be non causal.

Eg. for causal system.

$$Y(t) = x(t) + x(t - 1)$$
$$Y(n) = x(n) + x(n - 3)$$

Eg. For non causal system,

$$Y(t) = x(t+3) + x2(t)$$
$$Y(n) = x(2n)$$

- A system is called causal or non-anticipative if the output at any time t (or n) depends only on the input at times t or before t (or n or before n); in other words, independent of the input at times after t (or n). All memory less systems are causal. Physical systems where the time is the independent variable are causal.
- Non-causal systems may arise in applications where the independent variable is not the time such as in the image processing applications.

Examples of causal systems:

$$y(t) = \frac{1}{C}\int_{-\infty}^{t} x(\tau)d\tau \qquad \text{or} \qquad y[n] = x[n-1].$$

Examples of non-causal systems:

$$y(t) = x(-t) \qquad \text{or} \qquad y[n] = \frac{1}{3}\big(x[n-1] + x[n] + x[n+1]\big)$$

Stable and unstable system:

- When every bounded input produces bounded output then the system is called as stable system or bounded input bounded output (BIBO stable).
- Otherwise the system is unstable.
- A system is called stable if it produces bounded outputs for all bounded inputs.
- Stability in a physical system generally results from the presence of mechanisms that dissipate energy, such as the resistors in a circuit, friction in a mechanical system, etc.

Sample Problems:

1. **Determine whether the following systems are: i) Memoryless, ii) Stable iii) Causal iv) Linear and v) Time-invariant.**

i) y(n)= nx(n)

ii) y(t)= $e^{x(t)}$

Solution:-

(i) $y[n] = n\,x[n]$

A. output depends only on the present value of the input

∴ Memoryless

B. $|x[n]| \leq M_x < \infty$ Bounded input

$|y[n]| = |n||x[n]|$ as $n \to \infty$ output is unbounded

∴ Unstable

C. system o/p does not depend on future values

∴ Causal

D. System satisfies both superposition & homogeneity conditions. $H\{a_1 x_1[n] + a_2 x_2[n]\} = a_1 y_1[n] + a_2 y_2[n]$.

∴ Linear

E. $y[n-n_0] = (n-n_0)\,x[n-n_0] \neq H\{x[n-n_0]\}$

∴ Time-variant

ii) $y(t) = e^{x(t)}$

A. Memoryless, B. stable, C. Causal

D. Non-linear E. Time-invariant.

2. **Determine whether the following systems are time invariant or not. [**
   - **i) Y(t) = tx(t)**
   - **ii) Y(n) = x(2n)**

Solution:

i) Y(t) = tx(t)

Y(t) = T[x(t)] = tx(t)

The output due to delayed input is,

Y(t,T) = T[x(t - T)] = tx(t - t)

If the output is delayed by T, we get

Y(t -T) = (t - T) x(t - T)

The system does not satisfy the condition, y(t,T) = y(t – T).

Then the system is time invariant.

ii) $Y(n) = x(2n)$

$Y(n) = x(2n)$

$Y(n) = T[x(n)] = x(2n)$

If the input is delayed by K units of time then the output is,

$Y(n,k) = T[x(n-k)] = x(2n-k)$

The output delayed by k units of time is,

$Y(n-k) = x[2(n-k)]$

Therefore, y(n,k) is not equal to y(n-k). Then the system is time variant.

2 mark question and answer

1. **Define unit impulse and unit step signals.** **[May 2010]**

Unit Impulse signal:

Amplitude of unit impulse is 1 as its width approaches zero. Then it has zero value at all other values.

Unit Step Signal:

The unit step signal has amplitude of 1 for positive values of independent variable and amplitude of 0 for negative of independent variable.

2. **Give the mathematical and graphical representation of CT (continuous time) and DT (discrete time) impulse function.** **[Dec 2013]**

CT and DT impulse function:

Continuous time unit impulse is defined as

$$\delta(t) = \begin{cases} 1, & t=0 \\ 0, & t \neq 0 \end{cases}$$

Discrete time Unit impulse is defined as

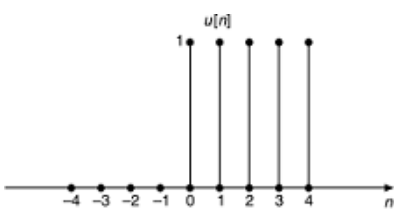
$$\delta[n] = \begin{cases} 0, & n \neq 0 \\ 1, & n=0 \end{cases}$$

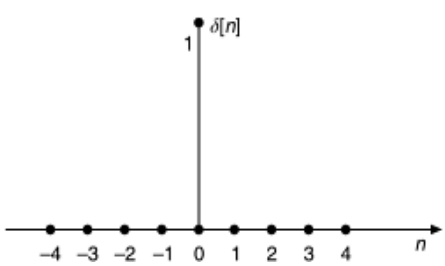
Unit impulse is also known as unit sample.

3. **Define step and impulse function in discrete signals.** **[May 2012]**

Unit step sequence is defined as

$$u[n] = \begin{cases} 1 & \text{for } n \geq 0 \\ 0 & \text{for } n < 0 \end{cases}$$





The unit sample function is defined as

$$\delta[n] = \begin{cases} 1 & \text{for } n=0 \\ 0 & \text{for } n \neq 0 \end{cases}$$

4. **State the two properties of unit impulse function.** **[Dec 2014]**

i) Shifting property:

$$\int_{-\infty}^{+\infty} x(t)\delta(t)\,dt = x(0)$$

ii) Replication property:

$$\int_{-\infty}^{+\infty} x(\tau)\,\delta(t-\tau)\,dt = x(t)$$

5. **Find the fundamental period of signal** **[Dec 2010]**

$$\mathrm{x} = \sin\left(\frac{7\pi}{3} + t\right)$$

Solu:

$$x(t) = \sin\left(\frac{7\pi}{3} + t\right)$$

$$time\ period\ T = \frac{2\pi}{\omega}$$

$$\omega = \frac{7\pi}{3}$$

$$= \frac{6}{7}\ \text{sec}$$

6. **Check e time whether the discrete signal sin 3n is periodic?** **[June 2013]**
   - The frequency of the discrete time signal is 3, because it is not a multiple of π.
   - Therefore the signal is aperiodic.

7. **Distinguish between deterministic and random signals.** **[May 2011]**

(or)

Define random signal and deterministic signal. **[May 2013]**

Random Signal:

It has some degree of uncertainty before it actually occurs. The random signal cannot be defined by mathematical expressions.

Deterministic Signal:

There is no uncertainty occurrence. It is completely represented by mathematical expressions.

8. **Determine the period of the signal** **[Dec 2011]**

$$\mathrm{x} = 2cos(n\pi/4)$$

Solu:

$$2\pi fn = n\pi/4$$

$$\mathrm{f} = \frac{\pi}{4} \times \frac{1}{2\pi} = 1/8$$

We know that, f=1/T

So T = 8sec

9. When is a system said to be memory less? Give an example. [May 2010]

If the system output does not depend the previous input, it only depends the present input. Then the system is called memory less or static system.

Eg:

$$y(t) = 2\mathrm{x}(t) + \mathrm{x}(t)$$
$$y(n) = \mathrm{x}(n) + \sqrt{\mathrm{x}(n)}$$

10. Define energy and power signals. [Dec 2010]

Energy Signal:

- A signal is said to be an energy signal if its normalized energy is non zero and finite.
- For an energy signal, P = 0.

i.e., $0 < E < \infty$

Power Signal:

- A signal is said to be the power signal if it satisfies $0 < P < \infty$
- For a power signal, $E = \infty$

11. What is the classification of system? [Dec 2009]

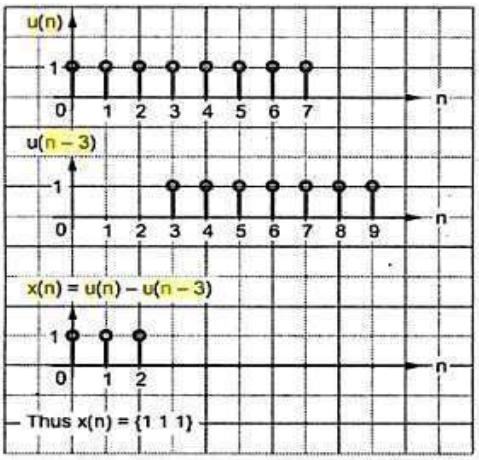
The classification of systems is,

(i). Linear and Non-Linear systems
(ii). Time invariant and Time varying systems.
(iii). Causal and Non causal systems.
(iv). Stable and unstable systems.
(v). Static and dynamic systems.
(vi). Invertible and non invertible systems.

12. Verify whether the system described by the equation $y(t) = x(t)^2$ is linear and time invariant.

- The system is linear since output is direct function of input.
- The system is time variant since time parameter is squared in the given equation.

13. Draw the signal x(n) = u(n) – u(n-3) **[may 2011]**



14. Check whether the following system is static/dynamic and casual/non casual y(n) = x(2n).

- If n=1, y(1) = x(2). This means system requires memory. Hence it is dynamic system.
- Since y(1) = x(2), the present output depends upon future input. Hence the system is non casual.

15. Distinguish between static and dynamic system.

Static system:

- Does not require memory
- Impulse response is of the form $h(t) = c\omega(t)$

Dynamic system:

- Requires memory
- Impulse response can be any form except $h(t) = c\omega(t)$

Unit – II
Analysis of Continuous Time Signals

2. Fourier series analysis:

Fourier series: a complicated waveform analyzed into a number of harmonically related sine and cosine functions

A two parts tutorial on Fourier series. In the first part an example is used to show how Fourier coefficients are calculated and in a second part you may use an applet to further explore Fouries series of the same function.

Fourier series may be used to represent periodic functions as a linear combination of sine and cosine functions. If f(t) is a periodic function of period T, then under certain conditions, its Fourier series is given by:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} [a_n \cos\frac{2n\pi t}{T} + b_n \sin\frac{2n\pi t}{T}]$$

where n = 1 , 2 , 3 , ... and T is the period of function f(t). an and bn are called Fourier coefficients and are given by

$$a_0 = \frac{2}{T}\int_0^T f(t)dt$$

$$a_n = \frac{2}{T}\int_0^T f(t)\cos(\frac{2n\pi t}{T})dt$$

$$b_n = \frac{2}{T}\int_0^T f(t)\sin(\frac{2n\pi t}{T})dt$$

Continuous Time Fourier Transform:

The Fourier expansion coefficient $X[k]$ (in a_k OWN) of a periodic signal is $x_T(t) = x_T(t+T)$ is

$$X[k] = \frac{1}{T}\int_T x_T(t)e^{-jk\omega_0 t}dt \qquad (k = 0, \pm 1, \pm 2, \cdots)$$

and the Fourier expansion of the signal is:

$$x_T(t) = \sum_{k=-\infty}^{\infty} X[k] e^{jk\omega_0 t}$$

which can also be written as:

$$x_T(t) = \frac{1}{T} \sum_{k=-\infty}^{\infty} (TX[k]) e^{jk\omega_0 t} = \frac{\omega_0}{2\pi} \sum_{k=-\infty}^{\infty} X(k\omega_0) e^{jk\omega_0 t} \qquad (a)$$

where $X(k\omega_0)$ is defined as

$$X(k\omega_0) \triangleq T\ X[k] = \int_T x_T(t) e^{-jk\omega_0 t} dt \qquad (b)$$

When the period of approaches infinity $T \to \infty$, the periodic signal becomes a non-periodic signal and the following will result: $x_T(t) x_T(t) x(t)$

Interval between two neighboring frequency components becomes zero:

$$T \to \infty \Longrightarrow \omega_0 = 2\pi/T \to 0$$

Discrete frequency becomes continuous frequency:

$$k\omega_0 \big|_{\omega_0 \to 0} \Longrightarrow \omega$$

Summation of the Fourier expansion in equation (a) becomes an integral:

$$x(t) \triangleq \lim_{T\to\infty} x_T(t) = \lim_{\omega_0 \to 0} \frac{1}{2\pi} \sum_{k=-\infty}^{\infty} X(k\omega_0) e^{jk\omega_0 t} \omega_0 = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(\omega) e^{j\omega t} d\omega$$

the second equal sign is due to the general fact:

$$\lim_{\Delta x \to 0} \sum_{k=-\infty}^{\infty} f(k\Delta x)\Delta x = \int_{-\infty}^{\infty} f(x) dx$$

Time integral over in equation (b) becomes over the entire time axis:

$$X(\omega) \triangleq \lim_{T\to\infty} X(k\omega_0) = \lim_{T\to\infty} \int_T x_T(t) e^{-jk\omega_0 t} dt = \int_{-\infty}^{\infty} x(t) e^{-j\omega t} dt$$

In summary, when the signal is non-periodic $x(t) = \lim_{T\to\infty} x_T(t)$, the Fourier expansion becomes Fourier transform. The forward transform (analysis) is:

$$X(\omega) = \int_{-\infty}^{\infty} x(t) e^{-j\omega t} dt \quad \text{or} \quad X(f) = \int_{-\infty}^{\infty} x(t) e^{-j2\pi f t} dt$$

and the inverse transform (synthesis) is:

$$x(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(\omega) e^{j\omega t} d\omega = \int_{-\infty}^{\infty} X(f) e^{j2\pi f t} df$$

Note that $X(\omega)$ is denoted by $X(j\omega)$ in OWN.

Comparing Fourier coefficient of a periodic signal $x_T(t)$ with with Fourier spectrum of a non-periodic signal $x(t)$

$$X[k] = \frac{1}{T} \int_T x_T(t) e^{-jk\omega_0 t} dt, \qquad X(\omega) = \int_{-\infty}^{\infty} x(t) e^{-j\omega t} dt$$

we see that the dimension of $X(\omega)$ is different from that of $X[k]$:

$$[X(\omega)] = [X[k]][t] = \frac{[X[k]]}{[\omega]}$$

If $|X[k]|^2$ represents the *energy* contained in the kth frequency component of a periodic signal $x_T(t)$, then $|X(\omega)|^2$ represents the energy *density* of a non-periodic signal

$x(t)$ distributed along the frequency axis. We can only speak of the energy contained in a particular frequency band $\omega_1 < \omega < \omega_2$:

Inverse Transforms

If we have the full sequence of Fourier coefficients for a periodic signal, we can reconstruct it by multiplying the complex sinusoids of frequency ω0k by the weights Xk and summing:

$$x(n) = \sum_{k=0}^{p-1} X_k e^{ik\omega_0 n} \qquad x(t) = \sum_{k=-\infty}^{\infty} X_k e^{ik\omega_0 t}$$

We can perform a similar reconstruction for aperiodic signals

$$x(n) = \frac{1}{2\pi} \int_{}^{\pi} X(\omega) e^{i\omega n}\, d\omega \qquad x(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(\omega) e^{i\omega t}\, d\omega$$

These are called the **inverse transforms**.

Parseval's theorem:

Parseval's theorem states that,

If $x(n) \xleftrightarrow{DTFT} X(\Omega)$

Then energy of the signal is given as,

$$E = \frac{1}{2\pi} \int_{-\pi}^{\pi} |X(\Omega)|^2\, d\Omega$$

Proof : We know that energy of the signal is given as,

$$E = \sum_{n=-\infty}^{\infty} |x(n)|^2$$

$|x(n)|^2$ is also equal to $x(n)\, x^*(n)$. Hence energy becomes,

$$E = \sum_{n=-\infty}^{\infty} x(n)\, x^*(n)$$

From equation 4.2.2, we can write the inverse DTFT of $x^*(n)$ as,

$$x^*(n) = \frac{1}{2\pi} \int_{-\pi}^{\pi} X^*(\Omega)\, e^{-j\Omega n}\, d\Omega$$

Laplace Transform

► Lapalce transform is a generalization of the Fourier transform in the sense that it allows "complex frequency" whereas Fourier analysis can only handle "real frequency". Like Fourier transform, Lapalce transform allows us to analyze a "linear circuit" problem, no matter how complicated the circuit is, in the frequency domain in stead of in he time domain.

► Mathematically, it produces the benefit of converting a set of differential equations into a corresponding set of algebraic equations, which are much easier to solve. Physically, it produces more insight of the circuit and allows us to know the bandwidth, phase, and transfer characteristics important for circuit analysis and design.

► Most importantly, Laplace transform lifts the limit of Fourier analysis to allow us to find both the steady-state and "transient" responses of a linear circuit. Using Fourier transform, one can only deal with he steady state behavior (i.e. circuit response under indefinite sinusoidal excitation).

► Using Laplace transform, one can find the response under any types of excitation (e.g. switching on and off at any given time(s), sinusoidal, impulse, square wave excitations, etc.

$$\mathcal{L}[f(t)] = \mathbf{F}(s) = \int_0^\infty f(t)e^{-st}\,dt$$

$f(t)$	Property	$\mathbf{F}(s)$
$f(t)$	Definition	$\int_0^\infty f(t)e^{-st}\,dt$
$f_1(t) + f_2(t)$	Linearity	$\mathbf{F}_1(s) + \mathbf{F}_2(s)$
$Kf(t)$	Linearity	$K\mathbf{F}(s)$
$\frac{df(t)}{dt}$	Differentiation	$s\mathbf{F}(s) - f(0)$
$\frac{d^2f(t)}{dt^2}$	Differentiation	$s^2\mathbf{F}(s) - sf(0) - \frac{df(0)}{dt}$
$\int_0^t f(t)\,dt$	Integration	$\frac{1}{s}\mathbf{F}(s)$
$tf(t)$	Complex differentiation	$-\frac{d\mathbf{F}(s)}{ds}$
$e^{-at}f(t)$	Complex translation	$\mathbf{F}(s + a)$
$f(t - a)\,u(t - a)$	Real translation	$e^{-as}\mathbf{F}(s)$

Application of Laplace Transform to Circuit Analysis

Properties of ROC of Laplace Transform:

1. The ROC of X(s) consists of strips parallel to the jω axis in the s-plane.
2. The ROC does not contain any poles.
3. If x(t) is of finite duration and is absolutely integrable, then the ROC is the entire s-plane.
4. It x(t) is a right sided signal, that is x(t) = 0 for $t<t_0<\infty$ then the ROC is of the form $Re(s)>\alpha_{max}$, where α_{max} equals the maximum real part of any of the poles of X(s).
5. If x(t) is a left sided, that is x(t) = 0 for $t>t_1>-\infty$, then the ROC is of the form $Re(s)<\alpha_{min}$, where α_{min} equals the minimum real part of any of the poles of X(s).
6. If x(t) is a two sided signal, than the ROC is of the form $\alpha_1<Re(s)<\alpha_2$.

(2 mark questions)

1. **What are the Dirichlet's conditions of Fourier series? [June 2014, Dec 2009,2013]**

(i).The function x(t) should be single valued within the interval T0
(ii). The function x(t) should have atmost a finite number of discontinuities in the interval T0
(iii). The function x(t) should have finite number of maxima and minima in the interval T0
(iv). The function should have absolutely integrable.

2. **State any two properties of continuous time Fourier transform.**

[May 2010, Dec 2009]

Convolution (Time) Property:

It states that,

$$x(t) * y(t) \overset{FT}{\leftrightarrow} X(j\Omega)Y(j\Omega)$$

Modulation Property (or) Frequency Shifting:

It states that,

$$x(t)e^{jn_0 t} \overset{FT}{\leftrightarrow} X(j\Omega - jfi_0)$$

3. **Find the laplace transform of the signal** $x(t) = e^{-at}u(t)$ **[may2010]**

Given $x(t) = te^{-at}u(t)$

We know that,

$$X(\Omega) = \int_{-\infty}^{\infty} x(t)e^{-jnt}\,dt = \int_{-\infty}^{\infty} e^{-at}u(t)e^{-jnt}\,dt = \int_{0}^{\infty} e^{-at}e^{-jnt}\,dt$$

$$= \int_0^{\infty} e^{-(a+jn)t}\,dt = \left[\frac{e^{-\infty}}{-(a+jn)} - \frac{e^0}{-(a+jn)}\right] = \frac{1}{a+jn}$$

$$X(\Omega) = \frac{1}{a+jn}$$

4. **What are the difference between Fourier series and Fourier transform? [OCT/NOV 2002,NOV/DEC 2004,DEC 2009,MAY/JUNE 2010]**

S.NO	Fourier Series	Fourier Transform
1	Fourier series is calculated for periodic signals.	Fourier Transform is calculated for non-periodic as well as periodic signals.
2	Expands the signals in time domain.	Represents the signal in frequency domain
3	Three types of Fourier series such as trigonometric, Polar and Complex Exponential	Fourier transform has no such types.

5. **State initial and final value theorem of Laplace transform.[DEC 2009,MAY-11]**

Initial value theorem: $x(0) = \lim_{S\to\infty} SX(S)$

Final value theorem: $x(t) = \lim_{S\to 0} SX(S)$

6. **Define the Fourier transform pair for continuous time signal. (Or) Give synthesis and analysis equations of CT Fourier Transform. [NOV/DEC 2012]**

Fourier Transform: $X(\Omega) = \int_{-\infty}^{\infty} x(t)e^{-jnt}\ dt$

Inverse Fourier Transform: $x(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} X(fi)e^{jnt}\ dfi$

7. **Find inverse Fourier transform of X(ω)=2πδ (ω). [MAY/JUNE 2010]**

Inverse Fourier Transform: $x(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} X(fi)e^{jnt}\ dfi$ **[Note: ω=Ω]**

$$x(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} 2\pi\delta(\Omega)e^{jnt}\ dfi$$

$= 1.$ Since $\delta(\Omega) = \begin{cases} 1 \text{ for } \Omega = 0 \\ 0 \text{ for } \Omega \neq 0 \end{cases}$

8. **State the time scaling property of Laplace Transform. [MAY/JUNE 2013]**

It states that,

If $L[x(t)] = X(S)$ then, $L[x(at)] = \frac{1}{|a|}X\left(\frac{S}{a}\right)$

9. **What is the Fourier Transform of a DC signal of amplitude 1? [MAY/JUNE 2013]**

$$\text{W.K.T } X(j\Omega) = \int_{-\infty}^{\infty} x(t)e^{-jnt}\ dt$$

Here x(t) = 1 then, $F[1] = 2\pi\delta(\Omega)$

10. **Define region of convergence of the Laplace Transform. [NOV/DEC 2012]**

For a given signal the range of values of s, for which the integral $\int_{-\infty}^{\infty}|x(t)|\ dt$converges is called the region of convergence.

i.e., $\int_{-\infty}^{\infty}|x(t)e^{\sigma t}|\ dt < \infty$

11. State the relationship between fourier transform and laplace transform.[may 2015]

- The laplace transform is given by,

$$X(s) = \int_{-\infty}^{\infty} x(t)e^{-st}\,dt$$

- The fourier transform is given by,

$$X(j\omega) = \int_{-\infty}^{\infty} x(t)e^{-j\omega t}\,dt$$

- The laplace transform is same as fourier transform when $s = j\omega$

12. State any two properties of ROC of laplace transform X(s) of a signal x(t).
[jun 2014]

Properties of ROC:

- No poles lie in ROC.
- ROC of the causal signal is right hand sided. It is of the form Re(s)>a.
- ROC of the non causal signal is left hand sided. It is of the form Re(s) < a.
- The system is stable if its ROC includes jω axis of s-plane.

13. Determine fourier series coefficients for signal cos πt [may 2012]

$$\cos \pi t = \frac{e^{j\pi t} + e^{-j\pi t}}{2}$$

Fourier series is given as,

$$x(t) = \sum_{k=-\infty}^{\infty} X(K)e^{jk\pi t}$$

14. Give analysis and synthesis equations of fourier transform. [dec 2012]

- Fourier transform,
  Analysis equation => $X(\omega) = \int_{-\infty}^{\infty} x(t)e^{-j\omega t}\,dt$

- Inverse fourier transform,
  Synthesis equation => $X(f) = 1/2\pi \int_{-\infty}^{\infty} x(\omega)e^{j\omega t}\,d\omega$

15. Obtain the fourier transform of X(f) = $e^{-at}u(t)$ **, a > 0**

$$X(f) = \int_{-\infty}^{\infty} x(t)e^{-j2\pi ft}\,dt$$

$$= \int_{-\infty}^{\infty} e^{-at} e^{-j2\pi ft}\, dt$$

$$= 1/(a + j2\pi f)$$

16. What is the condition to be satisfied for the existence of fourier transform for CT periodic signals? [dec 2011]

The function x(t) should be absolutely integrable for the existence of fourier transform.

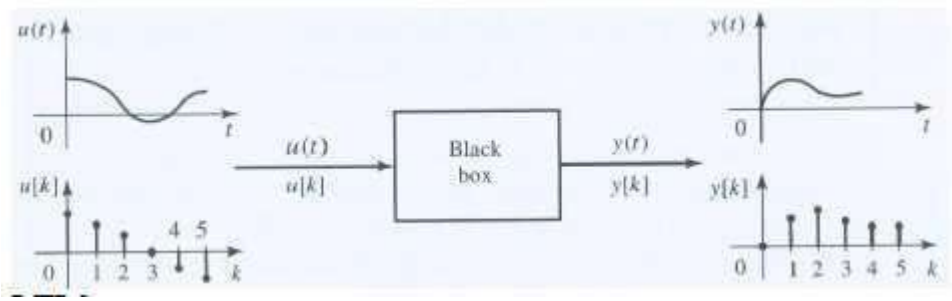
i.e., $\int_{-\infty}^{\infty} |x(t)| dt < \infty$

UNIT III

LINEAR TIME INVARIANT –CONTINUOUS TIME SYSTEMS

System:

A system is an operation that transforms input signal *x* into output signal *y*.



LTI Systems

• Time Invariant

– X(t)□ y(t) & x(t-to) □ y(t-to)

• Linearity

– a1x1(t)+ a2x2(t)□ a1y1(t)+ a2y2(t)

– a1y1(t)+ a2y2(t)= T[a1x1(t)+a2x2(t)]

• Meet the description of many physical systems

• They can be modeled systematically

– Non-LTI systems typically have no general mathematical procedure to obtain solution

Differential equation:

• This is a linear first order differential equation with constant coefficients (assuming a and b are constants)

$$\frac{d}{dt}y(t) - ay(t) = bx(t)$$

The general nth order linear DE with constant equations is

$$a_0 y(t) + a_1 \frac{d}{dt}y(t) + \ldots + a_{n-1}\frac{d^{n-1}}{dt^{n-1}}y(t) + a_n \frac{d^n}{dt^n}y(t) =$$

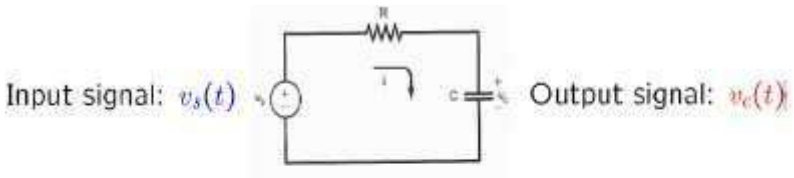
$$b_0 x(t) + b_1 \frac{d}{dt}x(t) + \ldots + b_{m-1}\frac{d^{m-1}}{dt^{m-1}}x(t) + b_m \frac{d^m}{dt^m}x(t)$$

which we can write as:

$$\sum_{k=0}^{n} a_k \frac{d^k}{dt^k}y(t) = \sum_{k=0}^{m} b_k \frac{d^k}{dt^k}x(t).$$

Linear constant-coefficient differential equations In RC circuit

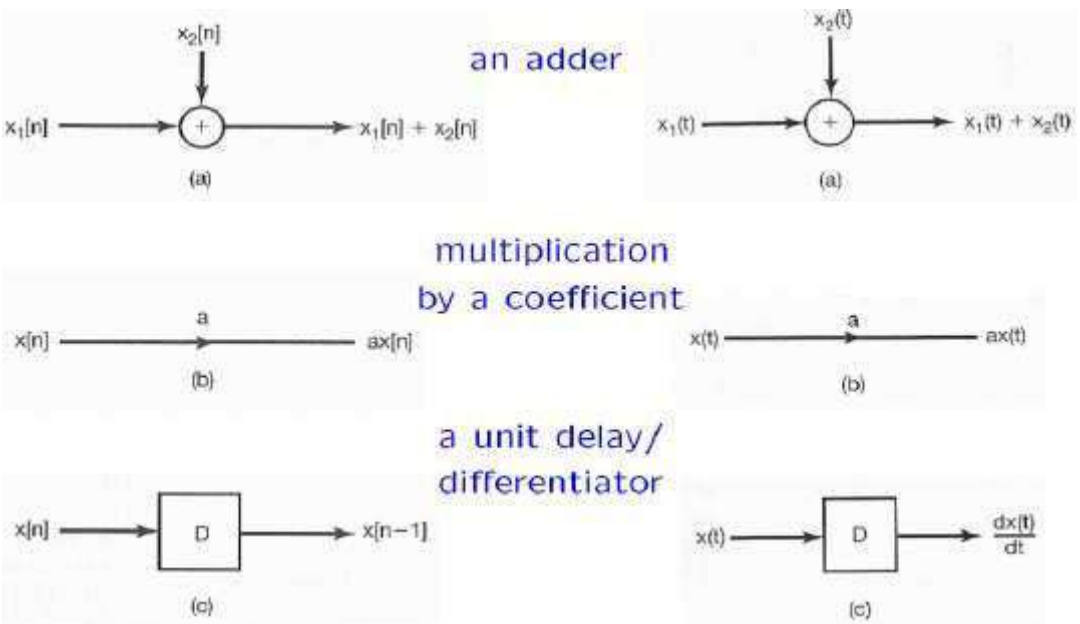
- To introduce some of the important ideas concerning systems specified by linear constant-coefficient differential equations ,let us consider a first-order differential equations:



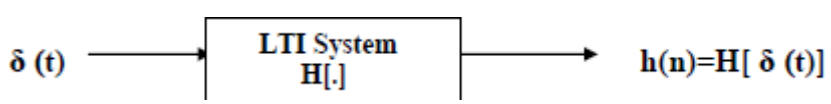
$$\Rightarrow \frac{dv_c(t)}{dt} + \frac{1}{RC}v_c(t) = \frac{1}{RC}v_s(t)$$

Block diagram representations

Block diagram representations of first-order systems described by differential and difference equations



Impulse Response



This impulse response signal can be used to infer properties about the system's structure (LHS of difference equation or unforced solution). The system impulse response, $h(t)$ completely characterises a linear, time invariant system

Properties of System Impulse Response

Stable

A system is stable if the impulse response is absolutely summable

Causal

A system is causal if $h(t)=0$ when $t<0$

Finite/infinite impulse response

The system has a finite impulse response and hence no dynamics in $y(t)$ if there exists $T>0$, such that: $h(t)=0$ when $t>T$

Linear

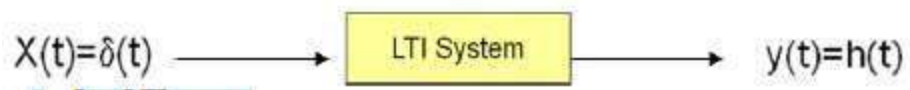
$ad(t) \square ah(t)$

Time invariant

$d(t-T) \square h(t-T)$

Convolution Integral

• An approach (available tool or operation) to describe the input-output relationship for LTI Systems



• In a LTI system
– d(t)□ h(t)
– Remember h(t) is T[d(t)]
– Unit impulse function □ the impulse response
• It is possible to use h(t) to solve for any input-output relationship
• Any input can be expressed using the unit impulse function

Convolution Integral - Properties

- Commutative $x(t)*h(t)=h(t)*x(t)$
- Associative $[x(t)*h_1(t)]*h_2(t)=x(t)*[h_1(t)*h_2(t)]$
- Distributive $x(t)*[h_1(t)+h_2(t)]=[x(t)*h_1(t)]+[x(t)*h_2(t)]$
- Thus, using commutative property:

$$x(t)=\int_{-\infty}^{\infty}x(\tau)h(t-\tau)d\tau=\int_{-\infty}^{\infty}h(\tau)x(t-\tau)d\tau$$

D.1.1 Commutativity Property

By making the change of variable, $\lambda = t - \tau$, in one form of the definition of CT convolution,

$$x(t) * h(t) = \int_{-\infty}^{\infty} x(\tau) h(t-\tau) d\tau$$

it becomes

$$x(t) * h(t) = -\int_{\infty}^{-\infty} x(t-\lambda) h(\lambda) d\lambda = \int_{-\infty}^{\infty} h(\lambda) x(t-\lambda) d\lambda = h(t) * x(t)$$

proving that convolution is commutative.

D.1.2 Associativity Property

Associativity can be proven by considering the two operations

$$[x(t) * y(t)] * z(t) \quad \text{and} \quad x(t) * [y(t) * z(t)].$$

Using the definition of convolution

$$x(t) * h(t) = \int_{-\infty}^{\infty} x(\tau) h(t-\tau) d\tau$$

we get

$$[x(t) * y(t)] * z(t) = \left[\int_{-\infty}^{\infty} x(\tau_{xy}) y(t-\tau_{xy}) d\tau_{xy} \right] * z(t)$$

D.1.3 Distributivity Property

Convolution is also distributive,

$$x(t) * [h_1(t) + h_2(t)] = x(t) * h_1(t) + x(t) * h_2(t).$$

$$x(t) * [h_1(t) + h_2(t)] = \int_{-\infty}^{\infty} x(t) [h_1(t-\tau) + h_2(t-\tau)] d\tau$$

$$x(t) * [h_1(t) + h_2(t)] = \int_{-\infty}^{\infty} x(t) h_1(t-\tau) d\tau + \int_{-\infty}^{\infty} x(t) h_2(t-\tau) d\tau$$

$$x(t) * [h_1(t) + h_2(t)] = x(t) * h_1(t) + x(t) * h_2(t)$$

Properties of Laplace Transform:

	Properties	Time Domain	Laplace Transform
1	Linearity	$a_1x_1(t)+a_2x_2(t)+\ldots+a_nx_n(t)$	$a_1X_1(s)+a_2X_2(s)+\ldots+a_nX_n(s)$
2	Frequency Shifting	$e^{-\alpha t}x(t)$	$F(s+\alpha)$
3	Time Delay	$x(t-a)u(t-a)$	$e^{-as}X(s)$
4	Time Scaling	$x(\alpha t)$	$\frac{1}{\alpha}X\left(\frac{s}{\alpha}\right)$
5	Time Differentiation	$\frac{d}{dt}x(t)$	$sX(s)-x(0^-)$
6	Time Integration	$\int_{-\infty}^{t}x(\tau)d\tau$	$\frac{X(s)}{s}+\frac{1}{s}\int_{-\infty}^{0^-}x(\tau)d\tau$
7	Initial Value Theorem	$\lim_{t\to 0^+}x(t)$	$\lim_{s\to\infty}sX(s)=x(0^+)$
8	Final Value Theorem	$\lim_{t\to\infty}x(t)$	$\lim_{s\to 0}sX(s)=x(\infty)$
9	Time Convolution	$x(t)*y(t)$	$X(s)Y(s)$

1. *Linearity*

Assume $x(t)=a_1x_1(t)+a_2x_2(t)$ (a_1 and a_2 are time independent)

$X_1(s)=L[x_1(t)]$, $X_2(s)=L[x_2(t)]$

then $X(s)=L[x(t)]=a_1X_1(s)+a_2X_2(s)$

Proof:

$$\begin{aligned} L[a_1x_1(t)+a_2x(t)] &= \int_0^\infty (a_1x_1(t)+a_2x(t))e^{-st}dt \\ &= \int_0^\infty a_1x_1(t)e^{-st}+a_2x(t)e^{-st}dt \\ &= a_1\int_0^\infty x_1(t)e^{-st}dt+a_2\int_0^\infty x(t)e^{-st}dt \\ &= a_1X_1(s)+a_2X_2(s) \end{aligned}$$

2. *Complex Frequency shift (s-shift) Theorem*

Assume $y(t)=x(t)e^{-\alpha t}$

$X(s)=L[x(t)]$ $\qquad Y(s)=L[y(t)]$

Then $Y(s)=X(s+\alpha)$

3. *Time Delay Theorem*

Assume $L[x(t)]\equiv L[x(t)u(t)]=X(s)$

Then $L[x(t-t_0)u(t-t_0)]=e^{-st_0}X(s)$ $\qquad (t_0>0)$

4. *Scaling*

Assume $X(s) = L[x(t)]$ then $L[x(at)] = \frac{1}{a} X(\frac{s}{a})$

Restriction: $a>0$

$x(at)$ ← a times fast (if $a>1$) or slow (if $a<1$) as $x(t)$

Proof:

$$\begin{aligned} L[x(at)] &= \int_0^\infty x(at)e^{-st}dt \\ &= \frac{1}{a}\int_0^\infty x(\tau)e^{-(s/a)\tau}d\tau, \quad \text{set } \tau = at \\ &= \frac{1}{a}X(\frac{s}{a}) \end{aligned}$$

5. *Time Differentiation*

Assume $X(s) = L[x(t)]$

Then $L\left(\frac{dx(t)}{dt}\right) = sX(s) - x(0^-)$

Proof:

(1) Definition $L\left[\frac{dx(t)}{d(t)}\right] = \int_0^\infty \frac{dx(t)}{dt} e^{-st}dt = \int_0^\infty e^{-st}dx(t)$

(2) Integration by parts:

$$\int_a^b u(t)dv(t) = u(t)v(t)\Big|_{t=a}^{t=b} - \int_a^b v(t)du(t)$$

Make the following substitution:

$x(t) \Rightarrow v(t)$

$e^{-st} \Rightarrow u(t)$

$$\begin{aligned} L\left[\frac{d}{dt}x(t)\right] &= \int_0^\infty e^{-st}dx(t) \\ &= e^{-st}x(t)\Big|_{t=0}^{t=\infty} - \int_0^\infty x(t)de^{-st} \\ &= 0 - x(0^-) - (-s)\int_0^\infty x(t)e^{-st}dt \\ &= sX(s) - x(0^-) \end{aligned}$$

In the ROC of X(s), we must have $\lim_{t\to\infty}[e^{-st}x(t)] = 0$ otherwise the Laplace integral which is the area under $e^{st}x(t)$ from 0 to $t=\infty$, will become ∞.

State variables and Matrix representation

• State variables represent a way to describe ALL linear systems in terms of a common set of equations involving matrix algebra.

• Many familiar properties, such as stability, can be derived from this common representation. It forms the basis for the theoretical analysis of linear systems.

• State variables are used extensively in a wide range of engineering problems, particularly mechanical engineering, and are the foundation of control theory.

• The state variables often represent internal elements of the system such as voltages across capacitors and currents across inductors.

• They account for observable elements of the circuit, such as voltages, and also account for the initial conditions of the circuit, such as energy stored in capacitors. This is critical to computing the overall response of the system.

• Matrix transformations can be used to convert from one state variable representation to the other, so the initial choice of variables is not critical.

• Software tools such as MATLAB can be used to perform the matrix manipulations required.

• Let us define the state of the system by an *N*-element column vector, $x(t)$:

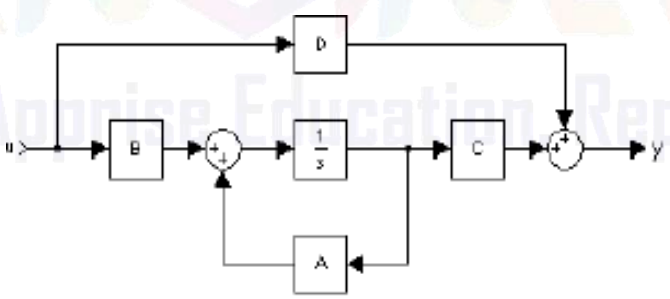
$$\mathbf{x}(t) = \begin{bmatrix} x_1(t) \\ x_2(t) \\ \vdots \end{bmatrix} = \begin{bmatrix} x_1(t) & x_2(t) & \cdots & x_N(t) \end{bmatrix}^T$$

Note that in this development, $v(t)$ will be the input, $y(t)$ will be the output, and $x(t)$ is used for the state variables.

• Any system can be modeled by the following state equations:

• This system model can handle single input/single output systems, or multiple inputs and outputs.

• The equations above can be implemented using the signal flow graph shown to the *below*



- Consider the CT differential equations:

$$\ddot{y}(t) + a_1\dot{y}(t) + a_0 y(t) = b_0 v(t)$$

- A second-order differential equation requires two state variables:

$$x_1(t) = y(t) \qquad x_2(t) = \dot{y}(t)$$

- We can reformulate the differential equation as a set of three equations:

$$\dot{x}_1(t) = x_2(t)$$
$$\dot{x}_2(t) = -a_0 x_1(t) - a_1 x_2(t) + b_0 v(t)$$
$$y(t) = x_1(t)$$

$y(t) = x_1(t)$

- We can write these in matrix form as:

$$\begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -a_0 & -a_1 \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} + \begin{bmatrix} 0 \\ b_0 \end{bmatrix} v(t)$$

$$y(t) = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix}$$

- This can be extended to an N^{th} order differential equation of this type:

$$y^{(N)}(t) + \sum_{i=0}^{N-1} a_i y^{(i)}(t) = b_0 v(t)$$

The state variables are defined as $x_i(t) = y^{(i-1)}(t), \quad i = 1, 2, \ldots, N$

The resulting state equation is

$$\begin{aligned} \dot{x}_1(t) &= x_2(t) \\ \dot{x}_2(t) &= x_3(t) \\ &\vdots \\ \dot{x}_{N-1}(t) &= x_N(t) \\ \dot{x}_N(t) &= -\sum_{i=0}^{N-1} a_i x_{i+1}(t) + b_0 v(t) \\ y(t) &= x_1(t) \end{aligned}$$

Matrix representation

$$\mathbf{A} = \begin{bmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \\ -a_0 & -a_1 & -a_2 & \cdots & -a_{N-1} \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ b_0 \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 \end{bmatrix} \qquad \mathbf{D} = 0$$

(2 mark questions)

1. **What is the overall impulse response h(t) when two systems with impulse response $h_1(t)$ and $h_2(t)$ are in parallel and in series? [MAY-10].**
   (or)
   State the properties needed for interconnecting LTI systems. [MAY-09]

For parallel connection, h(t)=$h_1(t)+h_2(t)$
For series connection, h(t)= $h_1(t)$ $*h_2(t)$.

2. **Write convolution integral of x(t) (or) Define convolution integral of continuous time systems. [DEC-10,MAY-10,MAY-11]**

The convolution integral is given as,y(t)=$\int_{-\infty}^{\infty} x(r)h(t-r)\mathrm{d}r$.

3. **Check whether the causal system with transfer function H(s) = 1/(s-2) is stable [dec 2013]**

Here the pole lies at s = 2. Since the pole of causal system does not lie on the left side of jω axis, the system is not stable.

4. **The impulse response of the LTI – CT system is given as $h(t) = \mathrm{e}^{-t}u(t)$. Determine transfer function and check whether the system is causal and stable.**

$$h(t) = \mathrm{e}^{-t}u(t)$$

Taking laplace transform,
H(s) = 1/(s+1)

Here the pole lies at s = -1, i.e. located in left half of s-plane. Hence this system is causal and stable.

5. **What are the conditions for a system to be LTI system? [dec 2013]**
   Input and output of an LTI system are related by,
   $y(t) = \int_{-\infty}^{\infty} x(r)h(t-r)dr$ i.e. convolution

6. **What is the impulse response of two LTI systems connected in parallel? [may 2010]**
   If the system are connected in parallel, having responses $h_1(t)$ and $h_2(t)$, then their overall response is given as,

$$h(t) = h_1(t) + h_2(t)$$

7. **Write N^{th} order differential equation. [DEC-10]**

The N^{th} order differential equation can be written as,

$$\sum_{k=0}^{N} a_k \frac{d^k y(t)}{dt^k} = \sum_{k=0}^{M} b_k \frac{d^k x(t)}{dt^k}$$

Here N≥ M.

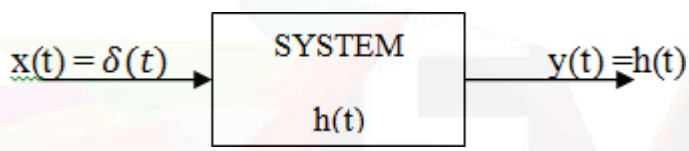
8. What is the condition for LTI system to be stable? [may 2013]

An LTI system is stable if the impulse response is absolutely integrable.

$$\int_{-\infty}^{\infty} |h(t)| < \infty$$

9. What is meant by impulse response of any system? [MAY-11]

When the unit impulse function is applied as input to the system, the output is nothing but impulse response h(t). The impulse response is used to study various properties of the system such as causality, stability, dynamicity etc.



10. Determine the response of the system with impulse response h(t)= t u(t) for the input x(t)= u(t) [DEC-11]

The response is given as,

y(t)=$\int_{-\infty}^{\infty} h(r)u(t-r)\mathrm{d}r$.

y(t)=$\int_{-\infty}^{\infty} ru(r)u(t-r)\mathrm{d}r$.

Here $u(r)u(t-r)$=1 for 0 to t. hence above equation will be,

y(t)=$\int_{0}^{t} r\mathrm{d}r = \frac{1}{2}t^2$.

11. State the properties of convolution. (DEC 2009).

1) Commutative property:x(t)*h(t) = h(t)*x(t)
2) Associative property: [x(t)*h_1(t)]*h_2(t) = x(t)*[h_1(t)*h_2(t)]
3) Distributive property:x(t)*h_1(t)+x(t)*h_2(t) = x(t)*[h_1(t)+h_2(t)]

12. What are the three elementary operations in block diagram representation of continuous time system? [dec 2012,2013]

- Scalar multiplication

X(t) ⟶ y(t) = ax(t)

UNIT IV

ANALYSIS OF DISCRETE TIME SIGNALS

Sampling theory

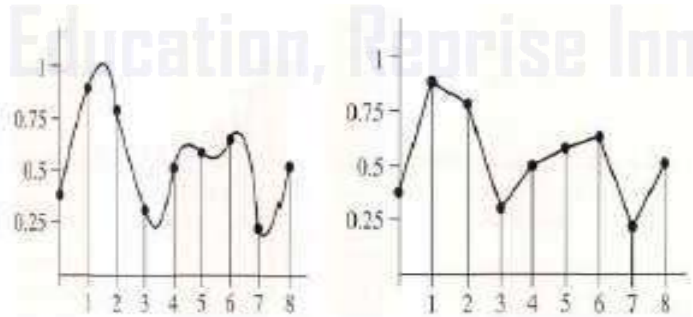
Let $x(t)$ be a continuous signal which is to be sampled, and that sampling is performed by measuring the value of the continuous signal every T seconds, which is called the sampling interval. Thus, the sampled signal $x[n]$ given by**:** $x[n] = x(nT)$, with $n = 0, 1, 2, 3, ...$

The sampling frequency or sampling rate fs is defined as the number of samples obtained in one second, or $fs = 1/T$. The sampling rate is measured in hertz or in samples per second.

The frequency equal to one-half of the sampling rate is therefore a bound on the highest frequency that can be unambiguously represented by the sampled signal. This frequency (half the sampling rate) is called the Nyquist frequency of the sampling system. Frequencies above the Nyquist frequency fN can be observed in the sampled signal, but their frequency is ambiguous. That is, a frequency component with frequency f cannot be distinguished from other components with frequencies $NfN + f$ and $NfN – f$ for nonzero integers N. This ambiguity is called aliasing. To handle this problem as gracefully as possible, most analog signals are filtered with an anti-aliasing filter (usually a low-pass filter with cutoff near the Nyquist frequency) before conversion to the sampled discrete representation.

► The theory of taking discrete sample values *(grid of color pixels)* from functions defined over continuous domains *(incident radiance defined over the film plane)* and then using those samples to reconstruct new functions that are similar to the original (reconstruction).

► **Sampler**: selects sample points on the image plane
► **Filter**: blends multiple samples together



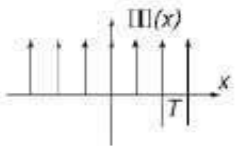
► **Sampling theory**

Sampling Theorem: bandlimited signal can be reconstructed exactly if it is sampled at a rate atleast twice the maximum frequencycomponent in it."

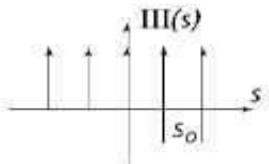
► Consider a signal g(t) that is bandlimited.

► **Sampling theory**

$$\text{III}(x) = \sum_{n=-\infty}^{\infty} \delta(x - nT)$$



$$\text{III}(s) = \sum_{n=-\infty}^{\infty} \delta(s - ns_o)$$

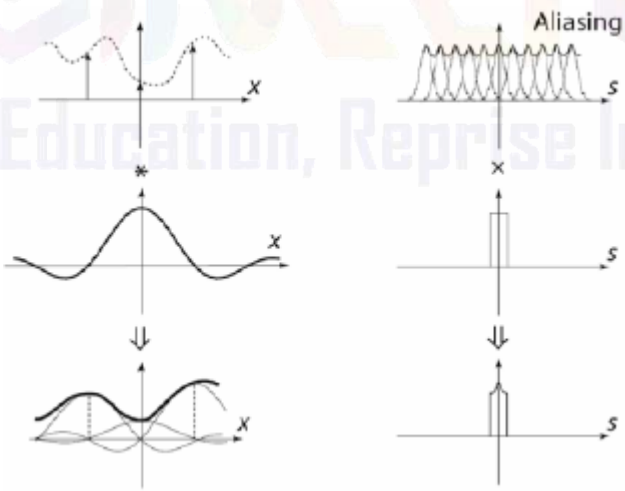


The maximum frequency component of g(t) is fm. To recover the signal g(t) exactly from its samples it has to be sampled ata rate fs _ 2fm. The minimum required sampling rate fs = 2fm is called nyquist rate

A continuous time signal can be processed by processing its samples through a discrete time system. For reconstructing the continuous time signal from its discrete time samples without any error, the signal should be sampled at a sufficient rate that is determined by the sampling theorem.

Aliasing

Aliasing is a phenomenon where the high frequency components of the sampled signal interfere with each other because of inadequate sampling ωs < 2ωm. Aliasing



Aliasing leads to distortion in recovered signal. This is the reason why sampling frequency should be atleast twice the bandwidth of the signal.

Sampling of Non-bandlimited Signal: Anti-aliasing Filter

Anti aliasing filter is a filter which is used before a signal sampler, to restrict the bandwidth of a signal to approximately satisfy the sampling theorem. The potential defectors are all the frequency components beyond $f_s/2$ Hz. We should have to eliminate these components from $x(t)$ before sampling $x(t)$. As a result of this we lose only the components beyond the folding frequency $f_s/2$ Hz. These frequency components cannot reappear to corrupt the components with frequencies below the folding frequency. This suppression of higher frequencies can be accomplished by an ideal filter of bandwidth $f_s/2$ Hz. This filter is called the **anti-aliasing filter**. The anti aliasing operation must be performed before the signal is sampled. The anti aliasing filter, being an ideal filter is unrealizable. In practice, we use a steep cutoff filter, which leaves a sharply attenuated residual spectrum beyond the folding frequency $f_s/2$.

DISCRETE TIME FOURIER TRANSFORM

In mathematics, the **discrete-time Fourier transform (DTFT)** is one of the specific forms of Fourier analysis. As such, it transforms one function into another, which is called the *frequency domain* representation, or simply the "DTFT", of the original function (which is often a function in the time-domain). But the DTFT requires an input function that is *discrete*. Such inputs are often created by sampling a continuous function, like a person's voice.

Given a discrete set of real or complex numbers: $x[n],\ n \in \mathbb{Z}$ (integers), the **discrete-time Fourier transform** (or **DTFT**) of $x[n]$ is usually written**:**

$$X(\omega) = \sum_{n=-\infty}^{\infty} x[n]\, e^{-i\omega n}.$$

Often the $x[n]$ sequence represents the values (aka *samples*) of a continuous-time function, $x(t)$, at discrete moments in time: $t = nT$, where T is the sampling interval (in seconds), and $1/T = f_s$ is the sampling rate (samples per second). Then the DTFT provides an approximation of the continuous-time Fourier transform:

$$X(f) = \int_{-\infty}^{\infty} x(t) \cdot e^{-i2\pi f t}\, dt.$$

To understand this, consider the Poisson summation formula, which indicates that a periodic summation of function $X(f)$ can be constructed from the samples of function $x(t)$. The result is:

$$X_T(f) \stackrel{\text{def}}{=} \sum_{k=-\infty}^{\infty} X(f - kf_s) \equiv T \sum_{n=-\infty}^{\infty} x(nT)\, e^{-i2\pi fTn}. \quad \text{(Eq.2)}$$

The right-hand sides of Eq.2 and Eq.1 are identical with these associations:

$$x[n] = T \cdot x(nT)$$
$$\omega = 2\pi fT = 2\pi \left(\frac{f}{f_s}\right).$$

$$X(\omega) = \sum_{n=-\infty}^{\infty} x[n]\, e^{-i\omega n}.$$

Often the $x[n]$ sequence represents the values (aka *samples*) of a continuous-time function, $x(t)$, at discrete moments in time: $t = nT$, where T is the sampling interval (in seconds), and $1/T = f_s$ is the sampling rate (samples per second). Then the DTFT provides an approximation of the continuous-time Fourier transform:

$$X(f) = \int_{-\infty}^{\infty} x(t) \cdot e^{-i2\pi ft}\, dt.$$

To understand this, consider the Poisson summation formula, which indicates that a periodic summation of function $X(f)$ can be constructed from the samples of function $x(t)$. The result is:

$$X_T(f) \stackrel{\text{def}}{=} \sum_{k=-\infty}^{\infty} X(f - kf_s) \equiv T \sum_{n=-\infty}^{\infty} x(nT)\, e^{-i2\pi fTn}. \quad \text{(Eq.2)}$$

The right-hand sides of Eq.2 and Eq.1 are identical with these associations:

$$x[n] = T \cdot x(nT)$$
$$\omega = 2\pi fT = 2\pi \left(\frac{f}{f_s}\right).$$

$X_T(f)$ comprises exact copies of $X(f)$ that are shifted by multiples of f_s and combined by addition. For sufficiently large f_s, the $k=0$ term can be observed in the region $[-f_s/2, f_s/2]$ with little or no distortion (aliasing) from the other terms.

Inverse transform

The following inverse transforms recover the discrete-time sequence**:**

$$x[n] = \frac{1}{2\pi} \int_{-\pi}^{\pi} X(\omega) \cdot e^{i\omega n}\, d\omega$$
$$= T \int_{-\frac{1}{2T}}^{\frac{1}{2T}} X_T(f) \cdot e^{i2\pi fnT}\, df.$$

The integrals span one full period of the DTFT, which means that the x[n] samples are also the coefficients of a Fourier series expansion of the DTFT.

Infinite limits of integration change the transform into a continuous-time Fourier transform [inverse], which produces a sequence of Dirac impulses. That is**:**

$$\int_{-\infty}^{\infty} X_T(f) \cdot e^{i2\pi ft}\, df = \int_{-\infty}^{\infty} \left(T \sum_{n=-\infty}^{\infty} x(nT)\ e^{-i2\pi fTn} \right) \cdot e^{i2\pi ft}\, df$$
$$= \sum_{n=-\infty}^{\infty} T \cdot x(nT) \int_{-\infty}^{\infty} e^{-i2\pi fTn} \cdot e^{i2\pi ft}\, df$$
$$= \sum_{n=-\infty}^{\infty} x[n] \cdot \delta(t - nT).$$

4.6 Properties

- *is the convolution between two signals
- $x[n]^*$ is the complex conjugate of the function *x[n]*
- $\rho_{xy}[n]$ represents the correlation between *x[n]* and *y[n]*.

x[n]^*\!

Property	Time domain $x[n]$	Frequency domain $X(\omega)$
Linearity	$ax[n] + by[n]$	$aX(e^{i\omega}) + bY(e^{i\omega})$
Shift in time	$x[n-k]$	$X(e^{i\omega})e^{-i\omega k}$
Shift in frequency (modulation)	$x[n]e^{ian}$	$X(e^{i(\omega-a)})$
Time reversal	$x[-n]$	$X(e^{-i\omega})$
Time conjugation	$x[n]^*$	$X(e^{-i\omega})^*$
Time reversal & conjugation	$x[-n]^*$	$X(e^{i\omega})^*$
Derivative in frequency	$\frac{n}{i}x[n]$	$\frac{dX(e^{i\omega})}{d\omega}$
Integral in frequency	$\frac{i}{n}x[n]$	$\int_{-\pi}^{\omega} X(e^{i\vartheta})d\vartheta$
Convolve in time	$x[n] * y[n]$	$X(e^{i\omega}) \cdot Y(e^{i\omega})$
Multiply in time	$x[n] \cdot y[n]$	$\frac{1}{2\pi}X(e^{i\omega}) * Y(e^{i\omega})$
Correlation	$\rho_{xy}[n] = x[-n]^* * y[n]$	$R_{xy}(\omega) = X(e^{i\omega})^* \cdot Y(e^{i\omega})$
Parseval's theorem	$E = \sum_{n=-\infty}^{\infty} x[n]y^*[n]$	$E = \frac{1}{2\pi}\int_{-\pi}^{\pi} X(e^{i\omega})Y^*(e^{i\omega})d\omega$

SYMMETRY PROPERTIES

The Fourier Transform can be decomposed into a real and imaginary part or into an even and odd part.

$$X(e^{i\omega}) = X_R(e^{i\omega}) + iX_I(e^{i\omega})$$

or

$$X(e^{i\omega}) = X_E(e^{i\omega}) + X_O(e^{i\omega})$$

Time Domain	Frequency Domain
$x[n]$	$X(e^{i\omega})$
$x^*[n]$	$X^*(e^{-i\omega})$
$x^*[-n]$	$X^*(e^{i\omega})$

Z-transforms

► **Definition:** The *Z* – transform of a discrete-time signal *x(n)* is defined as the power series:

$$X(z) = \sum_{k=-\infty}^{\infty} x(n) z^{-k} \qquad X(z) = Z[x(n)]$$

where *z* is a complex variable. The above given relations are sometimes called **the direct *Z* - transform** because they transform the time-domain signal *x(n)* into its complex-plane representation *X(z)*. Since *Z* – transform is an infinite power series, it exists only for those values of *z* for which this series converges.

The **region of convergence** of *X(z)* is the set of all values of *z* for which *X(z)* attains a finite value.

► For discrete-time systems, *z*-transforms play the same role of Laplace transforms do in continuous-time systems

Bilateral forward Z transform

$$H[z] = \sum_{n=-\infty}^{\infty} h[n] z^{-n}$$

Bilateral inverse Z transform

$$h[n] = \frac{1}{2\pi j} \oint_R H[z] z^{-n+1} dz$$

Z-transform Pairs

► $h[n] = d[n]$

Region of convergence: entire z-plane

$$H[z] = \sum_{n=-\infty}^{\infty} \delta[n] z^{-n} = \sum_{n=0}^{0} \delta[n] z^{-n} = 1$$

► $h[n] = d[n-1]$

Region of convergence: entire z-plane

$h[n-1] \Leftrightarrow z^{-1} H[z]$ $H[z] = \sum_{n=-\infty}^{\infty} \delta[n-1] z^{-n} = \sum_{n=1}^{1} \delta[n-1] z^{-n} = z^{-1}$

► Inverse z-transform

$$f[n] = \frac{1}{2\pi j} \oint_{c-j\infty}^{c+j\infty} F[z] z^{n-1} dz$$

► Using the definition requires a contour integration in the complex z-plane.
► Fortunately, we tend to be interested in only a few basic signals (pulse, step, etc.) Virtually all of the signals we'll see can be built up from these basic signals.

4.9 Z transform properties

Z-transform Properties

Properties of z - transform

1. Linearity

$$Z(x_1(nT) + x_2(nT)) = Z(x_1(nT)) + Z(x_2(nT))$$

2. Initial Value $x(0) = \lim_{z \to \infty} X(z)$

$$X(z) = x(0) + x(1) z^{-1} + \cdots$$

3. Final value $x(\infty) = \lim_{z \to 1} (1 - z^{-1}) X(z)$

$$x(\infty) = \lim_{s \to 0} sX(s)$$

$$
\begin{array}{ccc}
s \to 0 & \Leftrightarrow & z \to 1 \\
\frac{1}{s} & \Leftrightarrow & \frac{1}{1-z^{-1}} \\
s & \Leftrightarrow & 1-z^{-1} \\
sX(s) & \Leftrightarrow & (1-z^{-1})X(z) \\
\lim\limits_{s\to 0} sX(s) & \Leftrightarrow & \lim\limits_{z\to 1}(1-z^{-1})X(z)
\end{array}
$$

1. **Periodicity:**

$$X(e^{j(\omega+2\pi)}) = X(e^{j\omega})$$

2. **Linearity:**

$$ax_1[n] + bx_2[n] \longleftrightarrow aX_1(e^{j\omega}) + bX_2(e^{j\omega})$$

3. **Time Shift:**

$$x[n-n_0] \longleftrightarrow e^{-j\omega n_0}X(e^{j\omega})$$

4. **Phase Shift:**

$$e^{j\omega_0 n}x[n] \longleftrightarrow X(e^{j(\omega-\omega_0)})$$

5. **Conjugacy:**

$$x^*[n] \longleftrightarrow X^*(e^{-j\omega})$$

6. **Time Reversal**

$$x[-n] \longleftrightarrow X(e^{-j\omega})$$

7. **Differentiation**

$$nx[n] \longleftrightarrow j\frac{dX(e^{j\omega})}{d\omega}$$

8. **Parseval Equality**

$$\sum_{n=-\infty}^{\infty} |x[n]|^2 = \frac{1}{2\pi}\int_{2\pi} |X(e^{j\omega})|^2 d\omega$$

9. **Convolution**

$$y[n] = x[n] * h[n] \longleftrightarrow Y(e^{j\omega}) = X(e^{j\omega})H(e^{j\omega})$$

10. **Multiplication**

$$y[n] = x_1[n]x_2[n] \longleftrightarrow Y(e^{j\omega}) = \frac{1}{2\pi}\int_{2\pi} X_1(e^{j\omega})X_2(e^{j(\omega-\theta)})d\theta$$

Sample Problem:

1. **Obtain the z transform of,**

$$X(z)=\frac{1}{z^2(z-0.5)}$$

We expand $X(z)/z$ into simple fractions as

$$\frac{X(z)}{z}=\frac{1}{z^3(z-0.5)}=\frac{K_1}{z^3}+\frac{K_2}{z^2}+\frac{K_3}{z}+\frac{K_4}{z-0.5}$$

where

$$\begin{aligned}
K_1 &= z^3\frac{X(z)}{z}|_{z=0}=\frac{1}{z-0.5}|_{z=0}=-2\\
K_2 &= \frac{1}{1!}\frac{d}{dz}z^3\frac{X(z)}{z}|_{z=0}=\frac{d}{dz}\frac{1}{z-0.5}|_{z=0}=\frac{-1}{(z-0.5)^2}|_{z=0}=-4\\
K_3 &= \frac{1}{2!}\frac{d^2}{dz^2}z^3\frac{X(z)}{z}|_{z=0}=\frac{1}{2}\frac{d}{dz}\frac{-1}{(z-0.5)^2}|_{z=0}=\frac{1}{2}\frac{(-1)(-2)}{(z-0.5)^3}|_{z=0}=-8\\
K_4 &= (z-0.5)\frac{X(z)}{z}|_{z=0.5}=\frac{1}{z^3}|_{z=0.5}=8
\end{aligned}$$

Thus, $X(z)$ is expanded as

$$X(z)=-2z^{-2}-4z^{-1}-8+\frac{8}{1-0.5z^{-1}}$$

---

2. **Find the inverse z transform of,**

$$X(z)=\frac{z^2+z+2}{(z-1)(z^2-z+1)}$$

by use of the partial-fraction expansion method.

With complex conjugate poles ($z_{2,3}=0.5\pm j0.866$ with $|z_{2,3}|=1$) in the quadratic factor z^2-z+1, we expand $X(z)$ in simple partial fractions as

$$X(z)=\frac{4}{z-1}+\frac{-3z+2}{z^2-z+1}\quad\text{or}\quad X(z)=\frac{4z^{-1}}{1-z^{-1}}+\frac{-3z^{-1}+2z^{-2}}{1-z^{-1}+z^{-2}}$$

Recalling that the z transform of damped cosine and sine functions are given by

$$\begin{aligned}
Z[e^{-akT}\cos\omega kT] &= \frac{1-e^{-aT}z^{-1}\cos\omega T}{1-2e^{-aT}z^{-1}\cos\omega T+e^{-2aT}z^{-2}}\\
Z[e^{-akT}\sin\omega kT] &= \frac{e^{-aT}z^{-1}\sin\omega T}{1-2e^{-aT}z^{-1}\cos\omega T+e^{-2aT}z^{-2}},
\end{aligned}$$

we observe that the second expanded term in the expression of $X(z)$ above can be viewed as the z transform of a damped sinusoid. Actually, $X(z)$ can be rewritten as

$$\begin{aligned}
X(z) &= \frac{4z^{-1}}{1-z^{-1}}-3\left(\frac{z^{-1}-0.5z^{-2}}{1-z^{-1}+z^{-2}}\right)+\frac{0.5z^{-2}}{1-z^{-1}+z^{-2}}\\
&= 4z^{-1}\frac{1}{1-z^{-1}}-3z^{-1}\frac{1-0.5z^{-1}}{1-z^{-1}+z^{-2}}+z^{-1}\frac{0.5z^{-1}}{1-z^{-1}+z^{-2}}
\end{aligned}$$

2 mark questions

1. **What is the relation between Z transform and fourier transform of discrete time signal. (APR/MAY 2010).**

   X(m)=X(Z)|z=$e^{j\omega}$.This means Z transform is same as fourier transform when evaluated on unit circle.

2. **Define region of convergence with respect to Z transform. [MAY-11, 2015].**

   Region of convergence (ROC) is the area in Z plane where Z transform convergence .In other word, it is possible to calculate the X(z) in ROC.

3. **State the initial value theorem of Z transforms. (APR/MAY 2010).**

   The initial value of the sequence is given as, **X(0)=**$\lim_{z\to 1} X(z)$.

4. **What is meant by aliasing? (MAY/JUN 2010).**

   When the high frequency interferes with low frequency and appears as low then the phenomenon is called aliasing.

5. **Define Nyquist rate and Nyquist interval. (MAY/JUN 2010).**

   When the sampling rate becomes exactly equal to '2W' samples/sec,for a give bandwidth of W hertz, then it is called Nyquist rate .'

   Nyquist interval is the time interval between any two adjacent samples.

   Nyquist rate =2W hz&Nyquist interval=1/2W seconds.

6. **Define unilateral Z-Transform or one sided Z-transform [MAY-10]**

   The unilateral Z-Transform of signal x(t) is given as,

$$X(z) = \sum_{n=0}^{\infty} x(n)z^{-n}$$

   The unilateral and bilateral Z-Transforms are same for causal signals.

7. **State the final value theorem for z-transform. [may 2012]**

   The final value of a sequence is given as,

$$x(\infty) = \lim_{z\to 1}(1 - Z^{-1})X(z)$$

8. Define DTFT pair. **[dec 2012]**

DTFT,

$X(m) = \sum_{n=-\infty}^{\infty} x(n)e^{-jmn}$ (analysis equation)

$x(n) = 1/2\pi \int_{-\pi}^{\pi} X(m)e^{jmn}dm$ (Synthesis equation)

9. State the sampling theorem.

- A bandwidth signal of finite energy, which has no frequency components higher than W hertz, is completely described by specifying the values of the signal at instants of time separated by 1/2W seconds.
- A band limited signal of finite energy, which has no frequency components higher than W hertz, may be completely recovered from the knowledge of its samples taken at the rate of 2W samples per second.

10. Define two sided Z transform. **[may 2010,2013]**

The z- transform of the DT signal is given by,

$$X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$$

Here 'z' is the complex variable. The z- transform pair is denoted by,

$x(n) \longleftrightarrow X(Z)$

$$y(t) = \int_{-\infty}^{t} x(r)$$

11. State the convolution property of z transform. **[dec 2012]**

The convolution states that,

If $x_1(n) \longleftrightarrow X_1(z)$

$x_2(n) \longleftrightarrow X_2(z)$

then $x_1(n) * x_2(n) \longleftrightarrow X_1(z)X_2(z)$

That is the convolution of two sequences in time domain is equivalent to multiplication of their z-transforms.

12. State parseval"s theorem.

Consider the complex valued sequences x(n) and y(n).If

x(n)□----_X(k)

y(n)□----_Y(k)

then x(n)y*(n)=1/N X(k)Y*(k)

13. Find Z transform of x(n)={1,2,3,4}

x(n)= {1,2,3,4}

X(z)= x(n)z-n

= 1+2z-1+3z-2+4z-3.
= 1+2/z+3/z2+4/z3.

14. What z transform of (n-m)?

By time shifting property

Z[A (n-m)]=AZ-m sinZ[(n)] =1

15. Obtain the inverse z transform of X(z)=1/z-a,|z|>|a|

Given X(z)=z-1/1-az-1

By time shifting property

X(n)=an.u(n-1)

UNIT V

LINEAR TIME INVARIANT DISCRETE TIME SYSTEMS

5.1 Introduction

A discrete-time system is anything that takes a discrete-time signal as input and generates a discrete-time signal as output.1 The concept of a system is very general. It may be used to model the response of an audio equalizer . In electrical engineering, continuous-time signals are usually processed by electrical circuits described by differential equations.

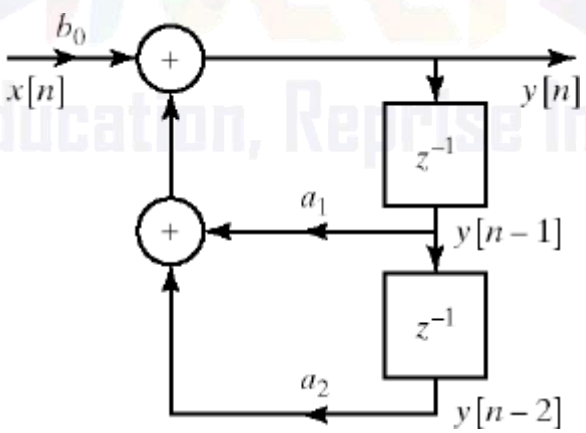
For example, any circuit of resistors, capacitors and inductors can be analyzed using mesh analysis to yield a system of differential equations. The voltages and currents in the circuit may then be computed by solving the equations. The processing of discrete-time signals is performed by discrete-time systems. Similar to the continuous-time case, we may represent a discrete-time system either by a set of difference equations or by a block diagram of its implementation.

For example, consider the following difference equation. y(n) = y(n-1)+x(n)+x(n-1)+x(n-2) This equation represents a discrete-time system. It operates on the input signal x(n)x(n) to produce the output signal y(n).

5.2 BLOCK DIAGRAM REPRESENTATION

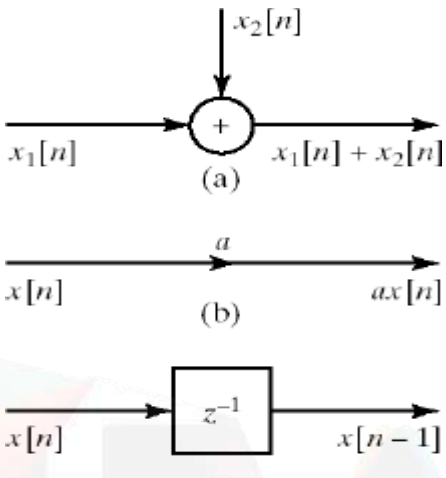
Block diagram representation of

$$y[n] = a_1 y[n-1] + a_2 y[n-2] + b_0 x[n]$$



LTI systems with rational system function can be represented as constant-coefficient difference equation

• The implementation of difference equations requires delayed values of the
– input
– output
– intermediate results
• The requirement of delayed elements implies need for storage



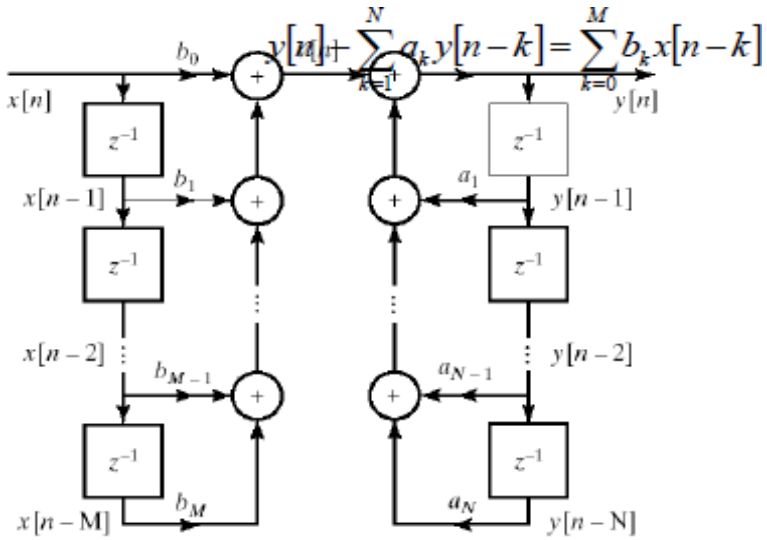
• We also need means of
– addition
– multiplication

Direct Form I

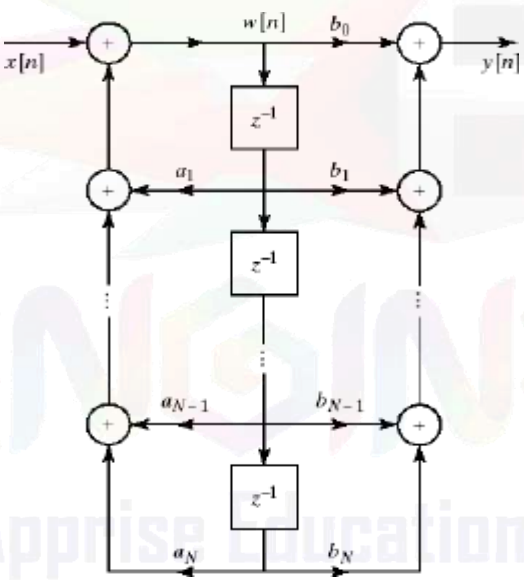
General form of difference equation

$$\sum_{k=0}^{N} \hat{a}_k y[n-k] = \sum_{k=0}^{M} \hat{b}_k x[n-k]$$

Alternative equivalent form



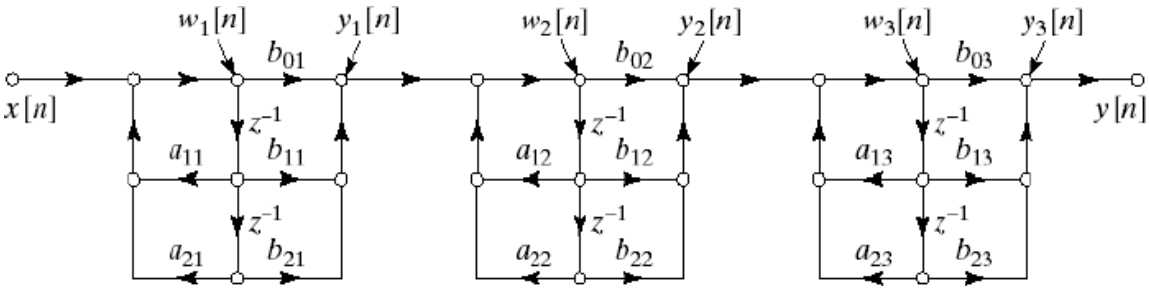
Direct Form II



- Cascade form

General form for cascade implementation

$$H(z)=A\frac{\prod_{k=1}^{M_1}\left(1-f_k z^{-1}\right)\prod_{k=1}^{M_2}\left(1-g_k z^{-1}\right)\left(1-g_k^* z^{-1}\right)}{\prod_{k=1}^{N_1}\left(1-c_k z^{-1}\right)\prod_{k=1}^{N_2}\left(1-d_k z^{-1}\right)\left(1-d_k^* z^{-1}\right)}$$



Parallel form

► Represent system function using partial fraction expansion

CONVOLUTIO N SUM

The convolution sum provides a concise, mathematical way to express the output of an LTI system based on an arbitrary discrete-time input signal and the system's response. The convolution sum is expressed as,

$$y[n] = \sum_{k=-\infty}^{\infty} x[k]\, h[n-k]$$

- Convolution is commutative

$$x[n] * h[n] = h[n] * x[n]$$

- Convolution is distributive

$$x[n] * (h_1[n] + h_2[n]) = x[n] * h_1[n] + x[n] * h_2[n]$$

- Cascade connection:

$$y[n] = h_1[n] * [\, h_2[n] * x[n] \,] = [\, h_1[n] * h_2[n] \,] * x[n]$$

- Parallel connection

$$y[n] = h_1[n] * x[n] + h_2[n] * x[n] \,] = [\, h_1[n] + h_2[n] \,] * x[n]$$

- LTI systems are stable iff

$$\sum_{k=-\infty}^{\infty} |h[k]| < \infty$$

LTI systems are causal if

$h[n] = 0$ $n < 0$

LTI SYSTEMS ANALYSIS USING DTFT

- Consider $X(e^{j\omega}) = |X(e^{j\omega})|e^{j\angle X(e^{j\omega})}$ and $H(e^{j\omega}) = |H(e^{j\omega})|e^{j\angle H(e^{j\omega})}$, then
  - magnitude

$$|Y(e^{j\omega})| = |X(e^{j\omega})||H(e^{j\omega})|$$

  - phase

$$\angle Y(e^{j\omega}) = \angle X(e^{j\omega}) + \angle H(e^{j\omega})$$

Frequency response at $H(e^{j\omega}) = H(z)|_{|z|=1}$ is valid if ROC includes $|z| = 1$.

$$Y(e^{j\omega}) = X(e^{j\omega})H(e^{j\omega})$$

LTI SYSTEMS ANALYSIS USING Z-TRANSFORM

- The z-transform of impulse response is called transfer or system function $H(z)$.

$$Y(z) = X(z)H(z)$$

- General form of LCCDE

$$\sum_{k=0}^{N} a_k y[n-k] = \sum_{k=0}^{M} b_k x[n-k]$$

$$\sum_{k=0}^{N} a_k z^{-k} Y(z) = \sum_{k=0}^{M} b_k z^{-k} X(z)$$

- Compute the z-transform

$$H(z) = \frac{Y(z)}{X(z)} = \frac{\sum_{k=0}^{M} b_k z^{-k}}{\sum_{k=0}^{N} a_k z^{-k}}$$

System Function: Pole/zero Factorization

- Stability requirement can be verified.
- Choice of ROC determines causality.
- Location of zeros and poles determines the frequency response and phase

$$H(z)=\frac{b_0}{a_0}\frac{\prod_{k=1}^{M}\left(1-c_k z^{-1}\right)}{\prod_{k=1}^{N}\left(1-d_k z^{-1}\right)}$$

Sample Problems:

1. Consider the system described by the difference equation.

$$y[n]=x[n]+\frac{1}{3}x[n-1]+\frac{5}{4}y[n-1]-\frac{1}{2}y[n-2]+\frac{1}{16}y[n-3]$$

Here $N=3,\ M=1$. Order 3 homogeneous equation:

$$y[n]-\frac{5}{4}y[n-1]+\frac{1}{2}y[n-2]-\frac{1}{16}y[n-3]=0 \qquad n\geq 2$$

The characteristic equation:

$$1-\frac{5}{4}a^{-1}+\frac{1}{2}a^{-2}-\frac{1}{16}a^{-3}=0$$

The roots of this third order polynomial is: $a_1=a_2=1/2 \quad a_3=1/4$ and

$$y_h[n]=h[n]=A_1(\frac{1}{2})^n+A_2 n(\frac{1}{2})^n+A_3(\frac{1}{4})^n, \quad n\geq 2$$

Let us assume $y[-1]=0$ then (3.52) for this case becomes:

$$\begin{bmatrix}a_0 & 0\\ a_1 & a_0\end{bmatrix}\cdot\begin{bmatrix}y[0]\\ y[1]\end{bmatrix}=\begin{bmatrix}b_0\\ b_1\end{bmatrix} \quad\Rightarrow\quad \begin{bmatrix}1 & 0\\ -5/4 & 1\end{bmatrix}\cdot\begin{bmatrix}y[0]\\ y[1]\end{bmatrix}=\begin{bmatrix}1\\ 1/3\end{bmatrix} \quad\Rightarrow y[0]=1;\ y[1]=19/12$$

with these we have the impulse response of this system:

$$h[n]=-\frac{4}{3}(\frac{1}{2})^n+\frac{10}{3}n(\frac{1}{2})^n+\frac{7}{3}(\frac{1}{4})^n, \quad n\geq 0$$

2. **Given y[-1]=1 and y[-2]=0. Compute recursively a few terms of the following 2nd order DE:**

$$y[n]=\frac{3}{4}y[n-1]-\frac{1}{8}y[n-2]+(\frac{1}{2})^n$$
$$y[0]=\frac{3}{4}y[-1]-\frac{1}{8}y[-2]+(\frac{1}{2})^0=\frac{3}{4}+0+1=\frac{7}{4}$$
$$y[1]=\frac{3}{4}y[0]-\frac{1}{8}y[-1]+(\frac{1}{2})^1=\frac{27}{16}$$
$$y[2]=\frac{3}{4}y[1]-\frac{1}{8}y[0]+(\frac{1}{2})^2=\frac{83}{64}$$
$$\vdots$$

3. **Compute the impulse response of the system described by,**

$$y[n]-\frac{1}{2}y[n-1]=x[n].$$

Solution: if $x[n]=\delta[n]$, then $y[n]=h[n]$ is the impulse response.

$$y[n]=\frac{1}{2}y[n-1]+x[n]$$
$$\Rightarrow h[n]=\frac{1}{2}h[n-1]+\delta[n]$$
$$h[0]=\frac{1}{2}h[-1]+\delta[0]$$

If we assume condition of initial rest $h[-1]=0$, then

$$h[0]=1$$
$$h[1]=\frac{1}{2}h[0]+\delta[1]=\frac{1}{2}+0=\frac{1}{2}$$
$$h[2]=\frac{1}{2}h[1]+\delta[2]=(\frac{1}{2})^2$$
$$\vdots$$
$$h[n]=(\frac{1}{2})^n, \text{for } n\geq 0$$
$$h[n]=0, \text{ for } n<0$$
$$\Rightarrow h[n]=(\frac{1}{2})^n u[n]$$

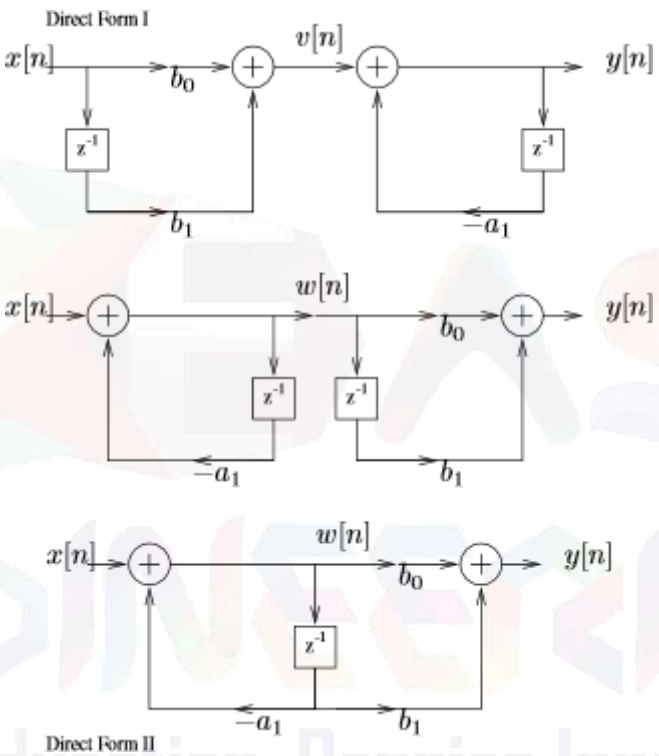
- The response of the system is not limited to a finite time interval. This is called an infinite impulse response (IIR) system.

4. Obtain the structures realization of LTI system

$$y[n] = -a_1\, y[n-1] + b_0\, x[n] + b_1\, x[n-1]$$

$$\begin{aligned} y[n] &= -a_1\, y[n-1] + v[n] \\ v[n] &= b_0\, x[n] + b_1\, x[n-1] \end{aligned}$$

$$\begin{aligned} w[n] &= -a_1\, w[n-1] + x[n] \\ y[n] &= b_0\, w[n] + b_1\, w[n-1] \end{aligned}$$



Generalizes to higher order systems described by difference equations.

$$y[n] = -\sum_{k=1}^{N} a_k\, y[n-k] + \sum_{k=0}^{M} b_k\, x[n-k]$$

$$\begin{aligned} v[n] &= \sum_{k=0}^{M} b_k\, x[n-k] \\ y[n] &= -\sum_{k=1}^{N} a_k\, y[n-k] + v[n] \end{aligned}$$

The first system $v[n] = \ldots$ is nonrecursive, where as the second system is recursive.

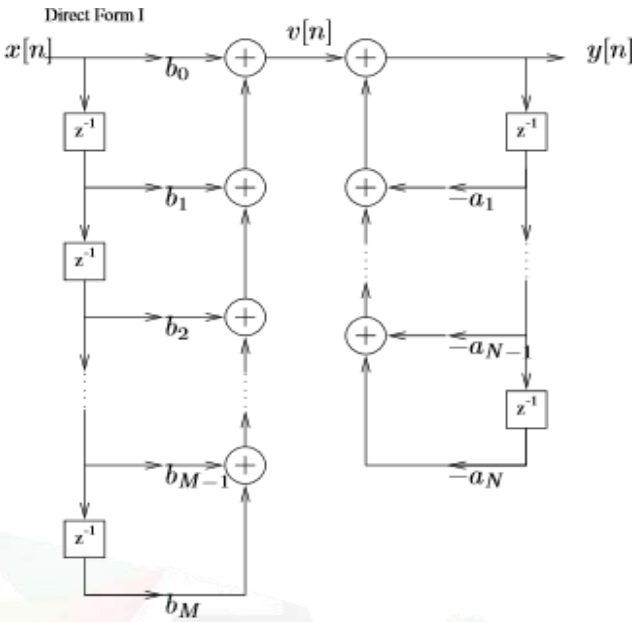
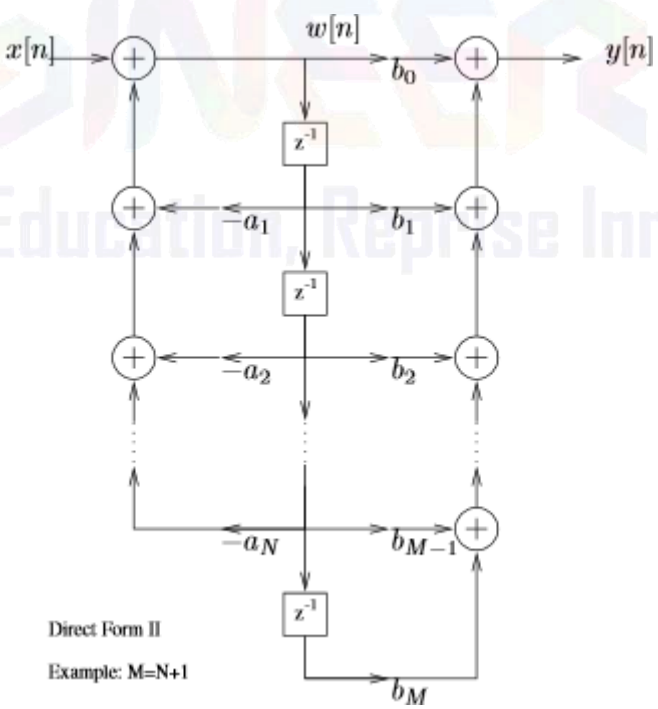


Figure 2.3: General Direct Form I.

$$w[n] = -\sum_{k=1}^{N} a_k\, w[n-k] + x[n]$$

$$y[n] = \sum_{k=0}^{M} b_k\, w[n-k]$$



5. Find the convolution of x(n)=[1,1,1,1,2,2,2,2] with h(n)=[3,3,0,0,0,0,3,3] by using matrix method.

Solution: By using matrix method, N=8

$$\begin{bmatrix} y(0) \\ y(1) \\ y(2) \\ y(3) \\ y(4) \\ y(5) \\ y(6) \\ y(7) \end{bmatrix} = \begin{bmatrix} h(0) & h(7) & h(6) & h(5) & h(4) & h(3) & h(2) & h(1) \\ h(1) & h(0) & h(7) & h(6) & h(5) & h(4) & h(3) & h(2) \\ h(2) & h(1) & h(0) & h(7) & h(6) & h(5) & h(4) & h(3) \\ h(3) & h(2) & h(1) & h(0) & h(7) & h(6) & h(5) & h(4) \\ h(4) & h(3) & h(2) & h(1) & h(0) & h(7) & h(6) & h(5) \\ h(5) & h(4) & h(3) & h(2) & h(1) & h(0) & h(7) & h(6) \\ h(6) & h(5) & h(4) & h(3) & h(2) & h(1) & h(0) & h(7) \\ h(7) & h(6) & h(5) & h(4) & h(3) & h(2) & h(1) & h(0) \end{bmatrix} \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ x(3) \\ x(4) \\ x(5) \\ x(6) \\ x(7) \end{bmatrix}$$

Substituting the values, we get

$$\begin{bmatrix} y(0) \\ y(1) \\ y(2) \\ y(3) \\ y(4) \\ y(5) \\ y(6) \\ y(7) \end{bmatrix} = \begin{bmatrix} 3 & 3 & 3 & 0 & 0 & 0 & 0 & 3 \\ 3 & 3 & 3 & 3 & 0 & 0 & 0 & 0 \\ 0 & 3 & 3 & 3 & 3 & 0 & 0 & 0 \\ 0 & 0 & 3 & 3 & 3 & 3 & 0 & 0 \\ 0 & 0 & 0 & 3 & 3 & 3 & 3 & 0 \\ 0 & 0 & 0 & 0 & 3 & 3 & 3 & 3 \\ 3 & 0 & 0 & 0 & 0 & 3 & 3 & 3 \\ 3 & 3 & 0 & 0 & 0 & 0 & 3 & 3 \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \\ 2 \\ 2 \\ 2 \\ 2 \end{bmatrix}$$

$$\begin{bmatrix} y(0) \\ y(1) \\ y(2) \\ y(3) \\ y(4) \\ y(5) \\ y(6) \\ y(7) \end{bmatrix} = \begin{bmatrix} 3\times1+3\times1+3\times1+0\times1+0\times2+0\times2+0\times2+3\times2 \\ 3\times1+3\times1+3\times1+3\times1+0\times2+0\times2+0\times2+0\times2 \\ 0\times1+3\times1+3\times1+3\times1+3\times2+0\times2+0\times2+0\times2 \\ 0\times1+0\times1+3\times1+3\times1+3\times2+3\times2+0\times2+0\times2 \\ 0\times1+0\times1+0\times1+3\times1+3\times2+3\times2+3\times2+0\times2 \\ 0\times1+0\times1+0\times1+0\times1+3\times2+3\times2+3\times2+3\times2 \\ 3\times1+0\times1+0\times1+0\times1+0\times2+3\times2+3\times2+3\times2 \\ 3\times1+3\times1+0\times1+0\times1+0\times2+0\times2+3\times2+3\times2 \end{bmatrix} = \begin{bmatrix} 15 \\ 12 \\ 15 \\ 18 \\ 21 \\ 24 \\ 21 \\ 18 \end{bmatrix}$$

Therefore, the convoluted sum is $y(n)$ = [15, 12, 15, 18, 21, 24, 21, 18].

2 mark questions and answers

1. States the properties of convolution.**(DEC 2009).**

i).Commutative property of convolution

x(n) $*$**h(n)=h(n)** $*$**x(n)=y(n**)

ii).Associative property of convolution

[x(n) $*h_1(n)$**]** $*h_2(n)$ **=x(n**)$*$**[**$h_1(n)$ $*h_2(n)$]

iii).Distributive property of convolution

x(n) $*$[$h_1(n)$**+**$h_2(n)$] **=x(n)** $*h_1(n)$**+x(n)** $*h_2(n)$**.**

2. Define non recursive and recursive of the following system.(MAY/JUN 2010).

When the output y(n) of the system depends upon present and past inputs then it is called non-recursive system. When the output y(n) of the system depends upon present and past inputs as well as past outputs, then it is called recursive system.

3. Define convolution sum?

If x(n) and h(n) are discrete variable functions, then its convolution sum y(n) is given by,

$$y(n)=\_\ x(k)\ h(n-k)$$

4. If x(n) and y(n) are discrete variable functions, what is its convolution sum. **[dec 2013]**

The convolution sum is,

$$\sum_{k=-\infty}^{\infty} x(k)y(n-k)$$

5. Determine the system function of the discrete time system described by the difference equation.

Y(n) = 0.5y(n-1)+x(n) **[may 2012]**

Taking z-transform of both sides,

$Y(z) = 0.5z^{-1}Y(z)+X(z)$

$H(z) = Y(z)/X(z) = 1/(1 – 0.5z^{-1})$

6. A causal LTI system has impulse response h(n), for which the z-transform is $H(z) = (1+z^{-1})/(1-0.5z^{-1})(1+0.25z^{-1})$. Is the system stable? Explain.

H(z) can be written in terms of positive powers of z as follows:

$$H(z) = z(z+1)/(z-0.5)(z+0.25)$$

Poles are at p_1 =0.5 and p_2 = -0.25. Since both the poles are inside unit circle. This system is stable.

7. Check whether the system with system function H(Z) = $(1/1-0.5z^{-1})+(1/1-2z^{-1})$ with ROC |z| < 0.5 is causal and stable? [dec 2013]

H(z) = z/(z – 0.5) + z/(z - 2). Poles of this system are located at z = 0.5 and z = 2. This system is not causal and stable, since all poles are not located inside unit circle.

8. Is the discrete time system described by the difference equation y(n) = x(-n) is causal? [may 2013]

Here y(-2) = x(-(-2)) = x(2). This means output at n=-2 depends upon future inputs. Hence this system is not causal.

9. Consider a system whose impulse is h(t) = $e^{-|t|}$. Is this system is causal or non causal? [dec 2011]

Here h(t) = $e^{-|t|}$

= e^{-t} for t>=0

= e^{t} for t<0

Since h(t) is not equal to zero for t<0, the system is non causal.

10. Find the step response of the system if the impulse response [may 2011]

$$h(n) = ð(n-2) - ð(n-1)$$

Solution:

Y(n) = h(n)*u(n), since x(n) = u(n), step input.

$= ð(n-2) * u(n) - ð(n-1) * u(n)$

= u(n - 2) – u(n - 1)

11. Obtain the convolution of

a) X(n) * $ð(n)$

b) X(n) * [h_1(n)+h_2(n)]

Solution:

x(n)* $ð(n)$ = $ð(n)$

x(n)*[h_1(n)+h_2(2)] = x(n)*h_1(n) + x(n)*h_2(n)

12. List the steps involved in finding convolution sum?

- o folding
- o Shifting
- o Multiplication
- o Summation

13. Consider an LTI system with impulse response **h(n)= δ(n-n_0)** for an input x(n), find the **Y(**e^{jm}**).(NOV/DEC 2003).**

Here is the spectrum of output. By convolution theorem we can write,

$$\mathbf{Y(}e^{jm}\mathbf{)=H(}e^{jm}\mathbf{)X(}e^{jm}\mathbf{)}$$

Here $\mathbf{H(}e^{jm}\mathbf{)=DTFT\{\ \delta(n-}n_0\mathbf{)\}}=e^{-jmn0}$

$$\mathbf{Y(}e^{jm}\mathbf{)=}\ e^{-jmn0}\ \mathbf{X(}e^{jm}).$$

14. List the properties of convolution?

o Commutative property of convolution

x(n) * h(n) = h(n) * x(n) = y(n)

o Associative property of convolution

[x(n) * h1(n)] * h2(n) = x(n) * [h1(n) * h2(n)]

o Distributive property of convolution

x(n) * [h1(n) + h2(n)] = x(n) * h1(n) + x(n) * h2(n)

15. Define system function?

H(z)= Y(z) is called system function.It is the z transform of the unit sample X(Z) response h(n) of the system.

MADHA
Expertise | Empathy | Excellence
ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

EC3354 SIGNALS AND SYSTEMS

Semester - 03

Question Bank

MADHA
Expertise | Empathy | Excellence
ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Vision

To excel in providing value based education in the field of Electronics and Communication Engineering, keeping in pace with the latest technical developments through commendable research, to raise the intellectual competence to match global standards and to make significant contributions to the society upholding the ethical standards.

Mission

- ✓ To deliver Quality Technical Education, with an equal emphasis on theoretical and practical aspects.
- ✓ To provide state of the art infrastructure for the students and faculty to upgrade their skills and knowledge.
- ✓ To create an open and conducive environment for faculty and students to carry out research and excel in their field of specialization.
- ✓ To focus especially on innovation and development of technologies that is sustainable and inclusive, and thus benefits all sections of the society.
- ✓ To establish a strong Industry Academic Collaboration for teaching and research, that could foster entrepreneurship and innovation in knowledge exchange.
- ✓ To produce quality Engineers who uphold and advance the integrity, honour and dignity of the engineering.

PROGRAMEDUCATIONALOBJECTIVES(PEOs)

1. To provide the students with a strong foundation in the required sciences in order to pursue studies in Electronics and Communication Engineering.
2. To gain adequate knowledge to become good professional in electronic and communication engineering associated industries, higher education and research.
3. To develop attitude in lifelong learning, applying and adapting new ideas and technologies as their field evolves.
4. To prepare students to critically analyze existing literature in an area of specialization and ethically develop innovative and research oriented methodologies to solve the problems identified.
5. To inculcate in the students a professional and ethical attitude and un ability to visualize the engineering issues in a broader social context.

PROGRAMSPECIFICOUTCOMES(PSOs)

PSO1: Design, develop and analyze electronic systems through application of relevant electronics, mathematics and engineering principles.

PSO2: Design, develop and analyze communication systems through application of fundamentals from communication principles, signal processing, and RF System Design & Electromagnetics.

PSO3: Adapt to emerging electronics and communication technologies and develop innovative solutions for existing and newer problems.

EC3354 SIGNALS AND SYSTEMS L T P C
3 1 0 4

COURSE OBJECTIVES :

- To understand the basic properties of signal & systems
- To know the methods of characterization of LTI systems in time domain
- To analyze continuous time signals and system in the Fourier and Laplace domain
- To analyze discrete time signals and system in the Fourier and Z transform domain

UNIT I CLASSIFICATION OF SIGNALS AND SYSTEMS 6+6

Standard signals- Step, Ramp, Pulse, Impulse, Real and complex exponentials and Sinusoids_Classification of signals – Continuous time (CT) and Discrete Time (DT) signals, Periodic & Aperiodic signals, Deterministic & Random signals, Energy & Power signals -Classification of systems- CT systems and DT systems- – Linear & Nonlinear, Time-variant& Time-invariant,Causal & Non-causal, Stable & Unstable.

UNIT II ANALYSIS OF CONTINUOUS TIME SIGNALS 6+6

Fourier series for periodic signals - Fourier Transform – properties- Laplace Transforms and Properties

UNIT III LINEAR TIME INVARIANT CONTINUOUS TIME SYSTEMS 6+6

Impulse response - convolution integrals- Differential Equation- Fourier and Laplace transforms in Analysis of CT systems - Systems connected in series / parallel.

UNIT IV ANALYSIS OF DISCRETE TIME SIGNALS 6+6

Baseband signal Sampling–Fourier Transform of discrete time signals (DTFT)– Properties of DTFT - Z Transform & Properties

UNIT V LINEAR TIME INVARIANT-DISCRETE TIME SYSTEMS 6+6

Impulse response–Difference equations-Convolution sum- Discrete Fourier Transform and Z Transform Analysis of Recursive & Non-Recursive systems-DT systems connected in series and parallel.

TOTAL: 30+30 PERIODS

COURSE OUTCOMES:

At the end of the course, the student will be able to:

CO1:determine if a given system is linear/causal/stable
CO2: determine the frequency components present in a deterministic signal
CO3:characterize continuous LTI systems in the time domain and frequency domain
CO4:characterize continuous LTI systems in the time domain and frequency domain
CO5:compute the output of an LTI system in the time and frequency domains

QUESTION BANK

EC3354 - SIGNALS AND SYSTEMS

UNIT – I: CLASSIFICATION OF SIGNALS AND SYSTEMS

PART –A

1. **Define power signal.**

   The signal x(t) is said to be power signal, if and only if the normalized average power p is finite and non-zero. i.e., $0<p<\infty$.

2. **How the impulse response of a discrete time system is useful in determining its stability and causality?**

   an LTI system with impulse response h[n] and it is causal if and only if h[n]=0 for all n<0.

   an LTI system with impulse response h[n] and it is BIBO stable if and only if $\sum|h[n]|$ is finite.

3. **Give the relation between continuous time unit impulse function f(t), step function u(t), and ramp function r(t).**

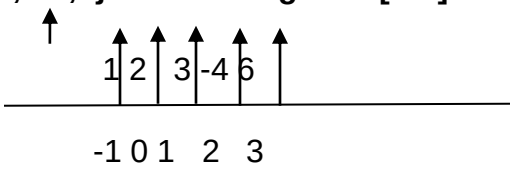
   The relationship between unit step and unit delta function is $\int\delta(t)\,dt= u(t)$

   The relationship between delta and unit ramp function is $\iint(\delta(t)) = r(t)$

4. **Find the value of the integral $\int e^{-2t} f(t+2)\,dt$.**

   e^4

5. **Given x(n) = {1,2,3, -4 ,6}. Plot the signal x [n-1].**



6. **State the properties of unit impulse function.**

   The integral of the impulse is one

   Infinite height and zero width

   It has shifting and convolution property.

6. **Define Signal.**

   A signal is a function of one or more independent variables which contain some information. Eg: Radio signal, TV signal, Telephone signal etc.

7. **Define System.**

A system is a set of elements or functional block that are connected together and produces an output in response to an input signal. Eg: An audio amplifier, attenuator, TV set etc.

8. Define CT signals.

Continuous time signals are defined for all values of time. It is also called as an analog signal and is represented by x(t). Eg: AC waveform, ECG etc.

9. Define DT signal.

Discrete time signals are defined at discrete instances of time. It is represented by x(n). Eg: Amount deposited in a bank per month.

10. Give few examples for CT signals.

AC waveform, ECG, Temperature recorded over an interval of time etc.

11. Give few examples of DT signals.

Amount deposited in a bank per month

12. Define step and impulse function in discrete time signal.

the discrete-time unit step, denoted by u[n] and defined by

$$u[n] = \begin{cases} 1, & n \geq 0 \\ 0, & n < 0 \end{cases}$$

Unit step function are mostly used t sample the continues signal.

The discrete-time unit sample r impulse signal is defined to be

$$\delta[n] = \begin{cases} 1, & n = 0 \\ 0, & n \neq 0 \end{cases}$$

13. Define unit step, ramp and delta functions for CT.

Unit step function is defined as

U(t)= 1for t ≥ 0

0 otherwise

Unit ramp function is defined as

r(t)= t for t ≥ 0

0 for t<0

Unit delta function is defined

as δ(t)= 1 for t=0

0 otherwise

14. Define random signal.

A random signal is one which cannot be represented by any mathematical equation.

Eg: Noise generated in electronic components, transmission channels, cables etc.

15. State the classification of CT signals**.**

The CT signals are classified as follows

(i) Periodic and non periodic signals

(ii) Even and odd signals

(iii) Energy and power signals

(iv) Deterministic and random signals.

16. Distinguish between deterministic and random signals.

A deterministic signal is one which can be completely represented by Mathematical equation at any time. In a deterministic signal there is no uncertainty with respect to its value at any time.

Eg: $x(t)=\cos\omega t$

$x(n)=2\pi fn$

A random signal is one which cannot be represented by any mathematical equation. Eg: Noise generated in electronic components, transmission channels, cables etc.

17. Define power and energy signals.

The signal x(t) is said to be power signal, if and only if the normalized average power p is finite and non-zero. i.e., $0<p<\infty$

A signal x(t) is said to be energy signal if and only if the total normalized energy is finite and non-zero. i.e., $0<E<\infty$

18. Compare power and energy signals.

S.No	POWER SIGNAL	ENERGY SIGNALS
1.	The normalized average power is finite and non-zero	Total normalized energy is finite and non- zero.
2.	Practical periodic signals are power signals	Non-periodic signals are energy signals

19. Define odd and even signal.

A DT signal x(n) is said to be an even signal if x(-n) = x(n) and an odd signal if

x(-n) = - x(n).

A CT signal is x(t) is said to be an even signal if x(t)= x(-t) and an odd signal if

x(-t) = - x(t).

20. Define periodic and aperiodic signals.

A signal is said to be periodic signal if it repeats at equal intervals.

Aperiodic signals do not repeat at regular intervals.

A CT signal which satisfies the equation $x(t)=x(t+ T_0)$ is said to be periodic and a DT signal which satisfies the equation x(n)=x(n+N)is said to be periodic.

21. State the classification or characteristics of CT and DT systems. (NOV/DEC 2010)

The DT and CT systems are classified according to their characteristics as follows

(i). Linear and Non-Linear systems

(ii). Time invariant and Time varying systems

(iii). Causal and non causal systems

(iv). Stable and unstable systems

(v). Static and dynamic systems

(vi). Inverse systems

22. Define memory less system.

A system is said to be a causal if its output at anytime depends upon present and past inputs only. Eg. y(t) = 3cosx(t)

23. Define linear and non-linear systems.

A system is said to be linear if superposition theorem applies to that system. If it does not satisfy the superposition theorem, then it is said to be a nonlinear system.

24. Define Causal and non-Causal systems.

A system is said to be a causal if its output at anytime depends upon present and past inputs only. Eg. y(t) = 3cosx(t)

A system is said to be non-causal system if its output depends upon future inputs also.

Eg. y(t) = x(t+3)

25. Define time invariant and time varying systems.

A system is time invariant if the time shift in the input signal results in corresponding time shift in the output. Eg. y(t)= x(t)x(t-1)

A system which does not satisfy the above condition is time variant system.eg. $y(t)= x(t^2)$

26. What is the mean by stability of the system?

A system is said to be stable if produces bounded output for bounded input

27. Define stable and unstable systems.

When the system produces bounded output for bounded input, then the system is called bounded input, bounded output stable.eg. y(t) = cos3t |x(t)|

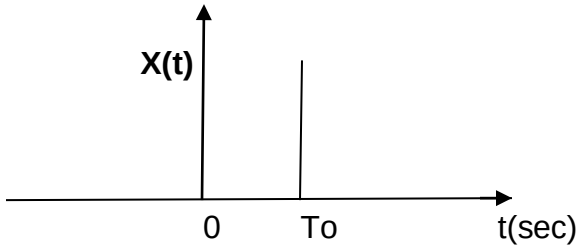
A system which does not satisfy the above condition is called a unstable system.

28. Define Static and Dynamic system.

A system is said to be static or memory less if its output depends upon the present input only. Eg y(t) =2x(t)+3

The system is said to be dynamic with memory if its output depends upon the present and past input values y(t) = x(t/4)

29. Sketch the signal $x(t) = \delta(t - t_o)$



30. Find whether the system is time invariant or not y(n)=nx(n) (Apr/May2019)

It is time variant signal because the delayed input is not equal to delayed system

PART-B

1. (i) Find the odd and even components of the signal $x(n) = (1,0,-1,2,3)$ (NOV/DEC 2018)

   (ii) Find the fundamental period of the signal $x(t) = e^{j\frac{7\Pi n}{3}}$

2. Given x[n]={1,4,3,-1,2}. Plot the following signals. (Nov/Dec 2015)

   (i) $x[-n-1]$ (ii) $x\left[-\frac{n}{2}\right]$ (iii) $x[-2n+1]$ (iv) $x\left[-\frac{n}{2}+2\right]$.

3. Check whether the following signals are periodic/aperiodic signals. (Nov/Dec 2014)

(i) $x(t) = \cos 2t + \sin\left(\frac{4}{5}\right)$

(ii) $x(t) = 3 + \cos\left(\frac{\pi}{2}\right)n + \cos 2n$

4. Given the input-output relationship of a continuous time system $y(t) = tx(-t)$. Determine whether the system is causal, stable, linear and time invariant. (Nov/Dec 2015)
5. Check whether the following system is linear, causal, time invariant and / or stable

   (i) $y(n) = x(n) - x[n-1]$

   (ii) $y(t) = \frac{d}{dt}x(t)$.

6. (i) Determine whether the signal x(t)=sin20πt+sin5πt is periodic and if it is periodic find the fundamental period

   (ii)Define energy and power signals. Find whether the signal $x(n)=(1/2)^n u(n)$ is energy or power signal and calculate their power or energy.

   (iii)Discuss various forms of real and complex exponential signals with graphical representations.

7. Determine whether the discrete time system y(n)=x(n)cos(wn) is

   (i) Memoryless (ii) Stable (iii) Causal (iv)Time invariant

   (v)Linear

7. Find whether the signal is energy or power signal and calculate their power or energy.

   (i) x(t)= rect(t/To)

   (ii) $x(t)=\cos^2(\omega_o t)$

8. a) Define Unit step , Ramp, Pulse , Impulse and Exponential signals .Obtain the relationship between the unit step function and unit ramp function

   b) Find the fundamental period of the signal

   x(n) = cos(nπ/2)-sin(nπ/8)+3cos(nπ/4+π/3)

9. Determine whether the system described by the following input output equations are linear , dynamic, causal and time invariant.

   (i) $y(t) = x(t-3) + x(3-t)$

   (ii) $y(t) = \frac{dx(t)}{dt}$

   (iii) $y(n) = nx(n) + bx^2(n)$

   (iv) Even [x(n-1)]

   (v) $y(n) = x(n) + nx(n+1)$

10. A discrete time system is given as $y(n)=y^2(n-1)-x(n)$. A bounded input of $x(n)=2\delta(n)$ Is applied to the system. Assume that the system is initially relaxed. Check whether system is stable or unstable.

11. (i) Determine whether the system described by the following input output equations are linear , dynamic, causal and time invariant.

$$y(n)=\log_{10}|x(n)|$$

(ii) Find the summation of $\sum_{n=0}^{\infty}\delta(n+1)2^n$

12. (i) A continuous time signal x(t) is shown below. Sketch and label the following signal.

(i) X(t-2)

(ii) X(2t)

(iii) X(t/2)

(iv) X(-t)

(ii)Determine Whether or not each of the following signal is periodic or not. Also find the fundamental period

a) $x(t)=\sin\frac{2\Pi}{3}t$

b) $x(n)=\cos(\frac{n}{8}-\Pi)$

UNIT II- ANALYSIS OF CONTINUOUS TIME SIGNALS

1. **State Dirichlet's conditions**.

   (i). The function x(t) should be single valued within the interval T_0

   (ii). The function x(t) should have at most a finite number of discontinuities in the interval T_0

   (iii). The function x(t) should have finite number of maxima and minima in the interval T_0

   (iv). The function should have absolutely integrable.

2. **Give the relation between Fourier transform and Laplace transform.**

   Fourier transforms map a function to a new function on the real line, whereas Laplace maps a function to a new function on the complex plane.

   Laplace transform is used to shift the system transfer function from time domain to the frequency domain. In Fourier transform we get the frequency spectrum of the signal.

3. **Draw the spectrum of CT rectangular pulse.**

4. **State any two properties of continues time Fourier Transform.)**

   i. Linearity
   ii. Time shift
   iii. Frequency shift
   iv. Time reversal
   v. Time and frequency scaling
   vi. Complex Conjugation

5. **Find the Laplace transform f the signal $x(t) = e^{-2t} u(t)$.**

   1/(s+2)

6. **Find the ROC of the Laplace transform x(t) = u(t).**

   ROC does not include the imaginary axis. ROC> σ

7. **State the condition of convergence Fourier series representation of continues time signal.**

   the condition of convergence Fourier series representation of continues time signal the signal should define in particular interval of time

8. **Define CT signal.**

Continuous time signals are defined for all values of time. It is also called as an analog signal and is represented by x(t).Eg: AC waveform, ECG etc.

9. Compare double sided and single sided spectrums.

The methods of representing spectrums of positive as well as negative frequencies are called double sided spectrums.

The method of representing spectrums only in the positive frequencies is known as single sided spectrums.

10. Define Trigonometric Fourier series.

Consider x(t) be a periodic signal. The Fourier series can be written for this signal as follows

$$x(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos n\omega_0 t + b_n \sin n\omega_0 t \quad \text{Where } a_0 = \frac{1}{T_0}\int_{T_0} x(t)dt$$

$$a_n = \frac{2}{T_0}\int_{T_0} x(t)\cos n\omega_0 t dt$$

$$b_n = \frac{2}{T_0}\int_{T_0} x(t)\sin n\omega_0 t dt$$

. **Define polar Fourier Series.**

$$x(t) = C_0 + \sum_{n=1}^{\infty} C_n \cos\left(n\omega_0 t - \theta_n\right)$$

Where $C_0 = \frac{1}{T_0}\int_{T_0} x(t)dt$

$C_n = \sqrt{a_n^2 + b_n^2}$ where $a_n = \frac{2}{T_0}\int_{T_0} x(t)\cos n\omega_0 t dt$ and $b_n = \frac{2}{T_0}\int_{T_0} x(t)\sin n\omega_0 t dt$

$$\theta_n = \tan^{-1}\frac{b}{a}$$

The above form of representing a signal is known as Polar Fourier series.

11.. Define exponential Fourier series.

$$x(t) = \sum_{n=-\infty}^{\infty} D_n e^{jn\omega_0 t}$$

Where $D_n = \frac{1}{T_0}\int_{T_0} x(t)e^{-jn\omega_0 t}dt$

12. Define Fourier Transform pair for continues time signal.

For every time domain waveform there is corresponding frequency domain waveform. For example delta function pairs and sinc function pairs etc.

13. State Parseval's power theorem.

Parseval's power theorem states that the total average power of a periodic signal x(t) is equal to the sum of the average powers of its phasor components.

14. Define Fourier Transform.

Let x(t) be the signal which is the function of time t. The Fourier transform of x(t) is given by

$$X(j\Omega) = \int_{-\infty}^{\infty} x(t)e^{-j\Omega t}dt$$

15. Find the Fourier transform of function x(t)=δ(t)

Ans: 1

16. State Rayleigh's energy theorem.

Rayleigh's energy theorem states that the energy of the signal may be written in frequency domain as superposition of energies due to individual spectral frequencies of the signal.

17. Define Laplace transform.

Laplace transform is another mathematical tool used for analysis of continuous time signals and systems. It is defined as

$$X(s) = \int_{-\infty}^{\infty} x(t)e^{-st}dt$$

18. Obtain the Laplace transform of ramp function.

Ans: $1/s^2$

19. What are the methods for evaluating inverse Laplace transform? (NOV/DEC 2013)

The two methods for evaluating inverse Laplace transform are

(i). By Partial fraction expansion method.

(ii). By convolution integral.

20. State initial value theorem.

If x(t)----- LT ------- X(s), then value of x(t)is given as, lim t->0x(t) = lim s->∞ [sX(s)] provided that the first derivative of x(t) should be Laplace transformable.

21. State final value theorem.

If x(t) and X(s) are Laplace transform pairs, then the final value of x(t) is given as ,Lim t->∞x(t)= Lim s->0[sX(s)]

22. State the convolution property of Fourier transforms.

If $x_1(t)$ and $X_1(f)$ are Fourier transform pairs and $x_2(t)$ and $X_2(f)$ are Fourier transform pairs, then $\int x_1(t)x_2(f-t)dt$ is Fourier transform pair with $X_1(f)$ $X_2(f)$

23. What is the relationship between Fourier transform and Laplace transform?

X(s)=X(jw) when s=jw

This states that Laplace transform is same as Fourier transform when s=jw.

24. Find the Fourier transform of sgn function.

Ans: 2/j W

25. Find out the Laplace transform of $f(t)=e^{at}u(t)$.

Ans: 1/(s-a)

26. Find out the Laplace transform of $x(t) = e^{-at}u(t)$

Ans: 1/(s+a)

PART-B

1. Find the Fourier series coefficient of the following signal : (Nov/Dec 2015)
   Plot the spectrum of the signal.

2. State and prove any four properties of Fourier transform.
3. Find the spectrum of $x(t) = e^{-2|t|}$. Plot the spectrum of the signal.
4. Find the Laplace transform and its associated ROC for the signal $x(t) = te^{-2|t|}$.(Nov/Dec 2014)
5. (i) Find the Exponential Fourier series of the waveform

   (iii) Find the Fourier transform of signal $x(t) = e^{-a|t|}$
6. (i) Find the Laplace transform of the signal $f(t) = e^{-at}\sin \omega t$

   (ii)Find the inverse Fourier transform of the rectangular spectrum given by

X(jw)= 1 $-W<\omega<W$

0 $-W>\omega>W$

7. a) Compute the Laplace transform of $x(t) = e^{-b|t|}$ for the cases of b<0 and b>0

   b) State and prove parsevals theorem of Fourier transform.

8. A) Determine the Fourier series representation of half wave rectifier output shown in figure below.

   b) Write the properties of ROC of Laplace transform.

9. a) Prove the scaling and time shifting properties of Laplace transform

   b) Determine the Laplace transform of $x(t) = e^{-at} cow\omega tu(t)$

10. a) State and prove the Fourier transform of the following signal in terms of X(jw); $x(t-t_o)$, $x(t)e^{jwt}$.

    b) Find the complex exponential Fourier series coefficient of the signal $x(t)=\sin 3\pi t+2\cos 4\pi t$.

13. Find the exponential Fourier series of the waveform

14. Find the exponential fourier series of the waveform

15. (i)Find the Fourier transform of the signal $x(t) = e^{-at}u(-t)$,a>0

    (ii)Find the inverse laplace transform of the following signal

    (a) $X(s) = \frac{s}{s^2 + 4}$ Re(s)>0

    (b) $X(s) = \frac{s+1}{(s+2)^2 + 4}$ Re(s)>-1

UNIT-III: Linear Time Invariant- Continuous Time Systems

1. **List and draw the basic elements for the block diagram representation of the continuous time system.**

   a. summer

   b. multiplier

   c. integrators

2. **Check the causality of the system with impulse response**

   The system is causal because the output depends on the present and previous values of inputs only.

3. **What is u(t-2)*f(t-1)? Where * represents convolution.**

   Function is not specified

4. **State sampling theorem.**

   A band limited continues time signal with highest frequency can be uniquely recovered from its samples provided that the sampling rate Fs is greater than r equal to 2Fm sample per seconds.

5. **Define LTI-CT systems.**

   In a continuous time system if the time shift in the input signal results in the corresponding time shift in the output, then it is called the LTI-CT system

6. **What are the tools used for analysis of LTI-CT systems?** The tools used for the analysis of the LTI-CT system are

   Fourier transform

   Laplace transform

5. **Define convolution integral.**

   The convolution of two signals is given by

   y(t)= x(t)*h(t)

   where $x(t) * h(t) = \int_{-\infty}^{\infty} x(\tau)h(t-\tau)d\tau$

This is known as convolution integral.

6. List the properties of convolution integral.

a. commutative property
b. distributive property
c. associative property
d. shift property
e. convolution with an impulse
f. width property

7. State commutative property of convolution.

The commutative property of convolution states that

$x_1(t)*x_2(t) = x_2(t)*x_1(t)$

8. **State the associative property of convolution.**

Associative property of convolution states

that $x_1(t)*[x_2(t)*x_3(t)]=[x_1(t)*x_2(t)]*x_3(t)$

9.State distributive property of convolution.

The distributive property states that

$x_1(t)*[x_2(t)+x_3(t)]=[x_1(t)*x_2(t)]+[x_1(t)*x_3(t)]$

10. When the LTI-CT system is said to be dynamic?

In LTI CT system, the system is said to be dynamic if the present output depends only on the present input.

11. When the LTI-CT system is said to be causal?

An LTI continuous time system is causal if and only if its impulse response h(t) = 0 for negative values of t.

12.When the LTI-CT system is said to be stable?

A LTI-CT system is said to be stable if the impulse response of the system is absolutely integrable.

(i) All the poles of H(s) should lie in the LHP of S- plane
(ii) No repeated pole should be in the imaginary axis.
(iii) The ROC of H(s) should include jw axis.

13.What is the impulse response of two LTI systems connected in parallel?

When two systems are connected in parallel the impulse response is given by

$h(t)= h_1(t)+h_2(t)$

14. What is the impulse response of two LTI systems connected in cascade?

The impulse response of two LTI systems connected in cascade are

$h(n)= h_1(t)*h_2(t)$

15. Define complete response.

The complete response of a LTI-CT system is obtained by adding the natural response and forced response

$y(t)= y_n(t)+ y_f(t)$

16. Define Causality and stability using poles.

For a system to be stable and causal, all the poles must be located in the left half of the s plane

17. Find the impulse response of the system y(t)=x(t-t0) using Laplace transform.

Ans:

$H(s)X(s)e^{sto}$

18. The impulse response of the LTI CT system is given as $h(t)=e^{-t}u(t)$.

Determine transfer function and check whether the system is causal and stable.

Ans: H(s)=1/(s+1)

The system is causal & stable.

19. Find the system function for the given LTI differential equation

$$\frac{dy(t)}{dt} + 2y(t) = x(t) + \frac{dx(t)}{dt}$$

System transfer function H(s)= Y(s)/X(s)=s+1/s+2

20. Show that $x(t) * \delta(t - t_o) = x(t - t_0)$

$\delta(t - t_o) = 1 : t = t_o$ when you substitute t=to then we get x(t-to)

PART-B

1. Convolve the following signals: $x(t) = e^{-2t}u(t-2)$ and $h(t) = e^{-3t}u(t)$.
2. Find the overall impulse response of the following system.

Here $h_1(t) = e^{-2t}u(t)$, , $h_3(t) = \delta(t)$. Also find the output of the system for the input $x(t) = u(t)$ using convolution integral.

3. An LTI system is represented by $\frac{d^2}{dt^2}y(t)+4\frac{dy(t)}{dt}+4y(t)=x(t)$ with initial conditions $y(0)=0$; $y'(0)=1$. Find the output of the system, when the input is $x(t)=e^{-t}u(t)$.(Nov/Dec 2014)

4. The input-output of a causal LTI system are related by the differential equation $\frac{d^2}{dt^2}y(t)+6\frac{dy(t)}{dt}+8y(t)=2x(t)$. .

   (i) Find the impulse response $h(t)$.

   (ii) Find the response $y(t)$ of this system if $x(t)=u(t)$. Hint: Use Fourier transforms.

5. (i) Derive convolution integral and derive its equation.

   (ii)A stable LTI system is characterized by the differential equation

   $$\frac{d^2y(t)}{dt^2}+4\frac{dy(t)}{dt}+3y(t)=\frac{dx(t)}{dt}+2x(t)$$

   Find the frequency response and impulse response using Fourier transform.

6. (i) Draw the direct form, parallel form and cascade form of a function with system function

   $$H(s)=\frac{1}{(s+1)(s+2)}$$

7. A)Determine the impulse response h(t) of the system given by Differential equation

   $\frac{d^2y(t)}{dt^2}+3\frac{dy(t)}{dt}+2y(t)=x(t)$ with all initial conditions to be zero.

   b)Obtain direct form I realization of

   $$\frac{d^2y(t)}{dt^2}+5\frac{dy(t)}{dt}+4y(t)=\frac{dx(t)}{dt}$$

8. The system produces the output $y(t)= e^{-t}u(t)$ for an input $x(t)= e^{-2t}u(t)$.

   Determine (i) Frequency response

   (i) Magnitude and phase response

   (ii) Impulse response

9. A) Compute and plot the convolution y(t) of the given signals

   (i) X(t) = u(t-3)-u(t-5), $h(t) = e^{-3t}u(t)$

   (ii) X(t)=u(t) , $h(t)= e^{-t}u(t)$.

10. The LTI system is characterized by impulse response function given by $H(s)=\frac{1}{(s+10)}\ ROC:\mathrm{Re}>-10$. Determine the output of a system when it is excited by the input x(t) = $-2e^{-2t}u(-t)-3e^{-3t}u(t)$.

11. (i)Consider an continuous time LTI system described by $\frac{dy(t)}{dt}+2y(t)=x(t)$ **.**Using Fourier transform find the output y(t) for the given input signal $x(t)=e^{-at}u(t)$

(ii)The output y(t) of a continuous time LTI system is found to be $2e^{-3t}u(t)$ when the input x(t) is u(t). Determine the impulse response h(t) of the system.

12. A unit step input applied to an LTI system at rest results in the equation

$$y(t)=\frac{1}{2}tu(t)-\frac{1}{20}(1-e^{-10t})u(t)$$

Determine the following

(i) Transfer function of the system

(ii) Impulse response of the system

(iii) Response of the system to x(t)=2 cos(10t)u(t)

Use Laplace transform Analysis.

UNIT-IV: ANALYSIS OF DISCRETE TIME SIGNALS

1. **State the need for sampling.**

   Sampling is required to convert a continues time signal t discrete time signal.

2. Find the Z – transform and its associated ROC for x[n] = {1,-1,2,3,4}

   X (z) = $z^3-z^2+2z+3+4/z$ ↑

3. **Define DTFT.**

   Let us consider the discrete time signal x(n). Its DTFT is denoted as X(w). It is given as

$$X(\omega)=\sum_{n=-\infty}^{\infty}x(n)e^{-jwn}$$

4. **State the condition for existence of DTFT?**

The conditions are If x(n)is absolutely summable

then $\sum_{n=-\infty}^{\infty}|x(n)|<\infty$

If x(n) is not absolutely summable then it should have finite energy for DTFT to exit.

5. List the properties of DTFT.

Periodicity

Linearity

Time shift

Frequency shift

Scaling

Differentiation in frequency domain

Time reversal

Convolution

Multiplication in time domain

Parseval's theorem

6. What is the DTFT of unit sample?

The DTFT of unit sample is 1 for all values of w.

7. Define DFT.

DFT is defined as

$X(k)=\sum_{n=0}^{N-1}x(n)e^{-j2\pi kn/N}$ where k = 0,1,….N-1

8. Define Twiddle factor.

The Twiddle factor is defined as $W_N^{nk}=e^{-j2\pi nk/N}$

9. Define Zero padding.

The method of appending zero in the given sequence is called as Zero padding.

10. Define circularly even sequence.

A Sequence is said to be circularly even if it is symmetric about the point zero on the circle.

11. Define circularly odd sequence.

A Sequence is said to be circularly odd if it is anti-symmetric about point x(0) on the circle.

12. Define circularly folded sequences.

A circularly folded sequence is represented as x((-n))N. It is obtained by plotting x(n) in clockwise direction along the circle.

13. State circular convolution.

This property states that multiplication of two DFT is equal to circular convolution of their sequence in time domain.

14. State Parseval's theorem.

Consider the complex valued sequences x(n) and y(n).

If x(n) –DFT -- X(k)

y(n) ---DFT-- Y(k)

then x(n) y * (n)=1/N(X(k)Y*(k))

15. Define Z transform.

The Z transform of a discrete time signal x(n) is denoted by X(z) and is given by

$$X(Z) = \sum_{n=-\infty}^{\infty} x(n) Z^{-n}$$

16.. Define ROC.

The value of Z for which the Z transform converges is called region of convergence.

17. Find Z transform of x(n)={1,2,3,4}

$$X(Z) = \sum_{n=-\infty}^{\infty} x(n) Z^{-n}$$

= 1+2z-1+3z-2+4z-3.

= 1+2/z+3/z2+4/z3.

18. State the convolution property of Z transforms.

The convolution property states that the convolution of two sequences in time domain is equivalent to multiplication of their Z transforms.

x(n)*y(n)=X(Z)Y(Z)

19. What is z transform of x(n-m)?

By time shifting property

$Z[x(n-m)]=Z^{-m} X[Z]$

20. State initial value theorem.

If x(n) is causal sequence then its initial value is given by

lim t---> 0 x(t) = lim z--->∞ [X(z)]

21. List the methods of obtaining inverse Z transform.

Inverse z transform can be obtained by using

Partial fraction expansion.

Contour integration

Power series expansion

Convolution.

22. Obtain the inverse z transform of X(z)=1/z-a,|z|>|a|

Given $X(z)=z^{-1}/1-az^{-1}$

By time shifting property

$x(n)=a^n.u(n-1)$

23. State final value theorem (NOV/ DEC 2018)

If x(n) is causal sequence then its final value is given by

$$\lim t \to \infty x(t) = \lim z \to 1(z-1)X(z)$$

24. State the condition for baseband Sampling.

A continuous time signal can be represented in its samples and can be recovered back when sampling frequency f_s is greater than or equal to the twice the highest frequency component of message signal. i. e.

$$f_s \geq 2f_m.$$

Fs=sampling frequency

Fm=Message frequency

25. State the frequency shifting theorem of DTFT(Apr/May2019)

$$e^{j\Omega_o n}x(n) \to DTFT \to X(\Omega - \Omega_O)$$

PART-B

1. State and explain sampling theorem both in time and frequency domains with necessary quantitative analysis and illustrations.
2. State and prove sampling theorem for a band limited signal and its reconstruction

3. State and prove any two properties of DTFT and any two properties of z-transform.

4. Find the inverse z-transform of $X(z)=\frac{z^{-1}}{1-0.25z^{-1}-0.375z^{-2}}$. For

(iii) ROC $|z|>0.75$ and (ii) ROC $|z|<0.5$

5. a Determine the discrete Fourier transform of $x(n)=a^{|n|}, |a|<1$

b) Find the ROC and Z transform of the sequence $x(n)=r^n \cos(n\Theta)u(n)$

6.a) State and prove the following properties of Z transform

(i) Linearity (ii) Time shifting (iii) Differentiation (iv) Correlation

b) Find the inverse Z transform of the function

$$X(Z)=\frac{1+Z^{-1}}{\left(1-\frac{2}{3}z^{-1}\right)^2} ROC|Z|>\frac{2}{3}$$

8. A) Determine Z transform of $x(n)= a^n \cos(\omega_o n).u(n)$.

b) Determine the inverse Z transform of

$$X(Z)=\frac{1}{\left(1-1.5z^{-1}+0.5z^{-2}\right)} ROC|Z|>1$$

9. (i) State and prove the time shift and frequency shift property of DTFT.

(ii)Determine DTFT of $(1/2)^n u(n)$. Plot its Spectrum

10. Determine the Z transform and sketch the pole zero plot with the ROC for each of the following signal.

(i) $x(n)=0.5^n u(n)-(1/3)^n u(n)$

(ii) $x(n)=0.5^n u(n)+(1/3)^n u(n-1)$

11. (i) Find the Inverse Z-transform of the $\frac{1}{[z^2-1.2Z+0.2]}$

(ii)Express the Fourier transform of the following signals in terms of $X(e^{jw})$

a) $X_1(n)=X(1-n)$

b) $X_2(n)=-(n-1)^2 x(n)$.

12. (i)Find the Z-transform of the sequence $x(n)=\cos\theta(n)u(n)$

(ii)Determine the Z transform of the following expression using partial fraction

method $X(Z) = \dfrac{1}{(1-\frac{1}{3}Z^{-1})(1-\frac{1}{6}Z^{-1})}$ ROC $|Z|$>1/3

13. State and prove the following properties of DTFT.

    a) Linearity

    b) Time shifting

    c) Frequency shifting

    d) Complex conjugation

    e) Time reversal

14. (i)Find the Z-Transform and associated ROC for each of the following sequences.

$x[n] = \delta(n - n_o)$

$x[n] = u(n - n_{o)})$

$x[n] = u(-n)$

$x[n] = a^{-n}u(-n)$

14. (ii)Verify the convolution property of Z-Transform.

UNIT -5: LINEAR TIME INVARIANT DISCRETE TIME SYSTEMS

1. Define convolution sum.

If x(n) and h(n) are discrete variable functions, then its convolution sum y(n) is given by

$$y(n) = \sum_{n=-\infty}^{\infty} x(k)h(n-k)$$

2. List the steps involved in finding convolution sum.

folding

Shifting

Multiplication

Summation

3. List the properties of convolution?

Commutative property of convolution x(n)

* h(n) = h(n) * x(n) = y(n)

Associative property of convolution

[x(n) * h_1(n)] * h_2(n) = x(n) * [h_1(n) *h $_2$(n)]

Distributive property of convolution

x(n) * [h_1(n) + h_2(n)] = x(n) * h_1(n) + x(n) * h_2(n)

4. Define LTI causal system?

A LTI system is causal if and only if, h(n) = 0 for n<0.This is the sufficient and necessary condition for causality of the system.

5. Define LTI stable system?

The bounded input x(n) produces bounded output y(n) in the LTI system only if,

$\sum_{k=-\infty}^{\infty} h(k) < \infty$ When this condition is satisfied, the system will be stable.

6. Define FIR system.

The systems for which unit step response h(n) has finite number of terms, they are called Finite Impulse Response (FIR) systems.

7. Define IIR system.

The systems for which unit step response h(n) has infinite number of terms, they are called Infinite Impulse Response (IIR) systems.

8. Define non recursive and recursive systems.

When the output y(n) of the system depends upon present and past inputs then it is called non-recursive system.

When the output y(n) of the system depends upon present and past inputs as well as past outputs is called recursive system.

9. State the relation between Fourier transform and z transform.

The Fourier transform is basically the z-transform of the sequence evaluated on unit circle. i.e., $X(z)|z=e^{jw} = X(w)$ at $|z|=1$ i.e., unit circle.

10. Define system function.

$H(z)= Y(z) /X(z)$ is called system function. It is the z transform of the unit sample response h(n) of the system.

11. What is the advantage of direct form 2 over direct form 1 structure?

The direct form 2 structure has reduced memory requirement compared to direct form 1 structure.

12. What is an advantage of FFT over DFT?

FFT algorithm reduces number of computations.

13. List the applications of FFT.

Filtering

Spectrum analysis

Calculation of energy spectral density

14. How unit sample response of discrete time system is defined?

The unit step response of the discrete time system is output of the system to unit sample sequence. i.e., $T[\delta(n)]=h(n)$. Also $z[h(n)]= H(z$

15. When a causal DT system is BIBO stable?

A causal DT system is stable if all the poles of the system function H[Z] lie within the unit circle.

16. If u(n) is the impulse response of the system, What is its step response?

Here $h(n) = u(n)$ and the input is $x(n) = u(n)$.

Hence the output $y(n) = h(n) * x(n)$

$= u(n) * u(n)$

17. Convolve the two sequences x(n)={1,2,3} and h(n)={5,4,6,2}

y(n)={5,14,29,26,22,6}

18. Determine the range of values of the parameter „a" for which the linear time invariant system with impulse response h(n)=a^n u(n) is stable?

H(z)= z / (z-a) , There is one pole at z=a. The system is stable, if all its

poles lies within the unit circle. Hence |a| < 1 for stability.

19. What are the different structures of realization of IIR system?

(i) Direct form I

(ii) Direct form II

(iii) Cascade form

(iv) Parallel form

20. State the final value theorem.

In discrete time

$$\lim_{k\to\infty} f[k] = \lim_{z\to 1} (z-1)F(z)$$

where $F(z)$ is the (unilateral) Z-transform of $f[k]$.

21. What are the methods to obtain linear convolution?

(i) Graphical method

(ii) Tabulation method

(iii) Multiplication method

22. Is the discrete time system described by the difference equation $y(n) = x(-n)$ is causal

Yes the system is causal since the output of the systems depends on present and previous values only

23. Write down the expression of convolution sum operation of two signals $x_1[n]$ and $x_2[n]$

Convolution of two signals $x_1[n]$ and $x_2[n]$ are

Y(n)= $x_1[n]$ * $x_2[n]$

$$y(n) = \sum_{k=-\infty}^{\infty} h(k)x(n-k)$$

PART-B

1. Convolve the following signals: $x[n]=\left(\frac{1}{2}\right)^{n-2}u[n-2]$ and

2. Compute $y[n]=x(n)*h(n)$ where $x[n]=\left(\frac{1}{2}\right)^{-n}u[n-2]$ and $h[n]=u[n-2]$.

3. Consider an LTI system with impulse response $h[n]=\alpha^n u[n]$ and the input to this system is $h[n]=\beta^n u[n]$ with $|\alpha|$ & $|\beta|$ <1. Determine the response $y[n]$

   (i) When $\alpha=\beta$

   (ii) When $\alpha\neq\beta$. Using DTFT.

4. LTI discrete time system $y[n]=\frac{3}{2}y[n-1]-\frac{1}{2}y(n-2)+x(n)+x(n-1)$ is given an input $x[n]=u(n)$

   (i) Find the transfer function of the system

   (ii) Find the impulse response of the system

5. a.Compute convolution sum of following sequence

   x(n)= 1 , 0<=n<=4 and

   0, otherwise

   h(n) = α^n, 0<=n<=6

   0, otherwise

   b) Draw direct form I and Direct form II implementations of the system described by difference equation

   $$y(n)+\frac{1}{4}y(n-1)+\frac{1}{8}y(n-2)=x(n)+x(n-1)$$

6. a) Determine the transfer function and impulse response form the causal LTI system described by the difference equation using Z transform

   $$y(n)-\frac{1}{4}y(n-1)-\frac{3}{8}y(n-2)=-x(n)+2x(n-1)$$

7. (i) Obtain the impulse response of the system given by difference equation

   $$y(n)-\frac{5}{6}y(n-1)+\frac{1}{6}y(n-2)=x(n)$$

   (ii)Determine the range of values of the parameter “a” for which the LTI system

With impulse response $h[n]=\alpha^n u[n]$ is stable.

8. Compute the response of the system

$y(n)=0.7y(n-1)-0.12y(n-2)+x(n-1)+x(n-2)$ to the input x(n) = nu(n). Is the system stable.

9. A) Find the impulse response of the difference equation

$y(n)-2y(n-2)+y(n-1)+3y(n-3)=x(n)+2x(n-1)$

10. (i) Draw the direct form II block diagram representation for the system function

$$H(Z)=\frac{1+2Z^{-1}-20Z^{-2}-20Z^{-3}-5Z^{-4}+6Z^{-6}}{[1+0.5Z^{-1}-0.25Z^{-2}]}$$

(ii)Find the input x(n) which produces out[put y(n)={3,8,14,8,3} when passed through the system having h(n)={1,2,3}.

11. A Causal LTI discrete time system $y[n]-\frac{3}{4}y[n-1]+\frac{1}{8}y(n-2)=x(n)$ where x(n) and y(n) are the input and output of the system respectively.

(iii) Find the transfer function of the system H(Z).

(iv) Find the impulse response h(n) of the system

12. (i) Find the convolution sum of the given sequences using Z transform

x[n]=[1,1,1,1] and h[n]=[1,1,1]

(ii) A recursive DT LTI system function H(Z) is given by

$$H(Z)=\frac{z(3z-4)}{(z-\frac{1}{2})(z-3)} \quad \text{ROC } \frac{1}{2}\prec|z|\prec 3$$

Determine whether the system is causal or not.

13. Find the output of a recursive DT system described by the following Difference Equation $y[n]-\frac{3}{4}y[n-1]+\frac{1}{8}y(n-2)=x(n)$, the intial conditions are y[-1]=0,y[-2]=1 and the input x[n] is $x[n]=\left[\frac{1}{2}\right]^n$. Use Z- transform Analysis.

MADHA
Expertise | Empathy | Excellence
ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

EC3351 CONTROL SYSTEM

Semester - 03

Question Bank

MADHA
Expertise | Empathy | Excellence
ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Vision

To excel in providing value based education in the field of Electronics and Communication Engineering, keeping in pace with the latest technical developments through commendable research, to raise the intellectual competence to match global standards and to make significant contributions to the society upholding the ethical standards.

Mission

- ✓ To deliver Quality Technical Education, with an equal emphasis on theoretical and practical aspects.
- ✓ To provide state of the art infrastructure for the students and faculty to upgrade their skills and knowledge.
- ✓ To create an open and conducive environment for faculty and students to carry out research and excel in their field of specialization.
- ✓ To focus especially on innovation and development of technologies that is sustainable and inclusive, and thus benefits all sections of the society.
- ✓ To establish a strong Industry Academic Collaboration for teaching and research, that could foster entrepreneurship and innovation in knowledge exchange.
- ✓ To produce quality Engineers who uphold and advance the integrity, honour and dignity of the engineering.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

1. To provide the students with a strong foundation in the required sciences in order to pursue studies in Electronics and Communication Engineering.
2. To gain adequate knowledge to become good professional in electronic and communication engineering associated industries, higher education and research.
3. To develop attitude in lifelong learning, applying and adapting new ideas and technologies as their field evolves.
4. To prepare students to critically analyze existing literature in an area of specialization and ethically develop innovative and research oriented methodologies to solve the problems identified.
5. To inculcate in the students a professional and ethical attitude and an ability to visualize the engineering issues in a broader social context.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Design, develop and analyze electronic systems through application of relevant electronics, mathematics and engineering principles.

PSO2: Design, develop and analyze communication systems through application of fundamentals from communication principles, signal processing, and RF System Design & Electromagnetics.

PSO3: Adapt to emerging electronics and communication technologies and develop innovative solutions for existing and newer problems.

EC3351 CONTROL SYSTEM

Syllabus

UNIT I SYSTEMS COMPONENTS AND THEIR REPRESENTATION

Control System: Terminology and Basic Structure- forward and Feedback control theory-Electrical and Mechanical Transfer Function Models- diagram Models-Signal flow graphs models-DC and AC servo Systems-Synchronous -Multivariable control system

UNIT II TIME RESPONSE ANALYSIS

Transient response-steady state response-Measures of performance of the standard first order and second order system-effect on an additional zero and an additional pole-steady error constant and system- type number-PID control-Analytical design for PD, PI,PID control systems

UNIT III FREQUENCY RESPONSE AND SYSTEM ANALYSIS

Closed loop frequency response-Performance specification in frequency domain-Frequency response of standard second order system- Bode Plot – Polar Plot- Nyquist plots-Design of compensators using Bode plots-Cascade lead compensation-Cascade lag compensation-Cascade lag-lead compensation

UNIT IV CONCEPTS OF STABILITY ANALYSIS

Concept of stability-Bounded – Input Bounded – Output stability-Routh stability criterion-Relative stability-Root locus concept-Guidelines for sketching root locus-Nyquist stability criterion.

UNIT V CONTROL SYSTEM ANALYSIS USING STATE VARIABLE METHODS

State variable representation-Conversion of state variable models to transfer functions-Conversion of transfer functions to state variable models-Solution of state equations-Concepts of Controllability and Observability-Stability of linear systems-Equivalence between transfer function and state variable representations-State variable analysis of digital control system-Digital control design using state feedback.

Total: 45 Periods

UNIT I SYSTEMS COMPONENTS AND THEIR REPRESENTATION

1. **Define the control system.**

A control system manages commands, directs, or regulates the behavior of other devices or systems using control loops. A control system is a system, which provides the desired response by controlling the output

2. **Define open-loop and closed-loop systems.**

Open loop system:
An open-loop system is a type of control system in which the output of the system depends on the input but the input or the controller is independent of the output of the system. These systems do not contain any feedback loop and thus are also known as non-feedback systems. In the presence of disturbances, an open loop control system will not perform the desired task because when the output changes due to disturbances, it is not followed by changes in input to correct the output.

Closed loop system:
The control system in which the output quantity affects the input quantity to maintain the desired output value is called a closed-loop control system. In a closed-loop system (also a feedback control system), the error signal is the difference between the input signal, and the feedback signal is fed to the controller to reduce the error and bring the output of the system to the desired value.

3. **Give the comparison between (Differentiate) open loop system and closed loop system.**

S.No.	**Open loop system**	**Closed-loop system**
1	The output quantity does not affect the input quantity.	The output affects the input quantity to maintain the desired output value
2	Inaccurate and unreliable	Accurate and reliable
3	Simple and economical	Complex and costlier
4	The changes in output due to external disturbances are not corrected automatically.	The changes in output due to external disturbances are corrected automatically
5	They are generally stable	Great efforts are needed to design a stable system.
6	In the case of Bandwidth, the the frequency at which the gain falls by 3 dB	The Frequency at which the magnitude of the closed-loop gain does not fall below -3dB
7	Examples: Stepper Motor, Traffic light	Temperature control system, Pressure control system, speed control system

4. What are the properties of signal flow graphs?

- The Linear algebraic equations that are used to construct signal flow graphs must be in the form of cause-and-effect relationships.
- Signal flow graph applies to linear systems only.
- Applicable only for Time-Invariant systems

5. What is a Signal Flow Graph?

A node in the signal flow graph represents the variable or signal. A node adds the signals of all incoming branches and transmits the sum to all outgoing branches. A mixed node that has both incoming and outgoing signals can be treated as an output node by adding an outgoing branch of unity transmittance

6. **What is the principle of operation of closed-loop systems**

The closed loop system compares the actual output measured by the sensor with the set point and produces the error signal or actuating signal. The controlled variable has to be kept at a certain value regardless of any disturbing influences acting on the system.

7. **How are feedback control systems classified?**

(i) Negative feedback system where output and setpoint values are subtracted used in Amplifiers
(ii)Positive feedback system where output and setpoint values are added used in oscillators

8. What are the characteristics of negative feedback?

The characteristics of negative feedback are as follows:

- Accuracy in tracking steady state value
- Rejection of disturbance signals
- Low sensitivity to parameter variations
- Reduction in gain at the expense of better stability

9. **Give two advantages of closed-loop control over open-loop control.**

Advantages/Merits

- More Accurate
- It compensates for disturbances
- It greatly improves the speed of its response

10. What is called a feedback control system? Give an example.
(Or) Define a closed-loop control system with a suitable example.

The feedback control system is also known as a closed-loop control system or Automatic control system. The output is feedback to the input for correction. The feedback path element samples the output and converts it to a signal of the same type of reference signal.
Example: Automatic Traffic control system

11. Distinguish between the feed-forward control system and the feedback control system.

S.NO	FEED FORWARD CONTROL SYSTEM	FEEDBACK CONTROL SYSTEMS.
1.	Feedforward control does not check how the adjustments of inputs worked in the process. So, it is referred to as OPEN LOOP CONTROL.	Feedback control measures the output and verifies the adjustment results. So, it is called CLOSED LOOP CONTROL.

2.	Feedforward control takes corrective action before the disturbances enter into the process.	Feedback control takes corrective action only after the disturbances have affected the process and generated an error.
3.	Feedforward control has to predict the output as it does not measure output. So, it is sometimes called PREDICTIVE CONTROL.	The feedback control reacts only to the process error (the deviation between the measured output value and set point). So, it is called REACTIVE CONTROL.

12. Name any two dynamic models used to represent control systems.

Dynamic models used to represent control systems are

- Differential Equation Modeling
- Transfer function model which uses Laplace transformation with differential Equations which does not use initial values.
- State space model which also uses differential models that use initial values

13. Define the Transfer function of a system and mention its applicability in a control system

The Transfer function of a system is defined as the ratio between the Laplace transform of the output and the Laplace transform of the input when initial conditions are zero. It is used to analyze the system characteristics.

14. State the properties of a linear system.

It obeys the principle of superposition and homogeneity. The principle of superposition implies that if a system model has responses $Y1(t)$, and $Y2(t)$ to any two inputs $X1(t)$, and $X2(t)$ respectively, then the system response to the linear combination of these inputs $X1(t)+ X2(t)$ is given by the linear combination of the individual outputs, i.e., $Y1(t)+ Y2(t)$ where 1, 2 are constants. Homogeneity states that the output of a linear system is always directly proportional to the Input of the system

15. What are the basic elements of a closed-loop control system? (Or) What are the basic components of an automatic control system?

- Error detector or comparator
- Amplifier and Controller
- Plant or System to be controlled
- Sensor or feedback system

16. State the laws governing mechanical rotational elements.

The laws governing mechanical rotational elements are Newton's law and D'Alembert's principle. Newton's law states that the sum of torques acting on a body is zero. Alembert's law states that the sum of all Torque acting on the inertial is equal to zero. with J as the moment of Inertia, K as the torsional spring, and B as the Dashpot

17. What are the basic elements used for modeling mechanical translational systems?

The basic elements used for modeling mechanical translational systems that move along a straight line are Mass(M), Damper (B), and Spring(K)

18. **What are the basic elements used for modeling mechanical rotational systems?**

The basic elements used for modeling mechanical rotational systems are Moment of inertia (J), dashpot with rotational frictional coefficient (B), and torsional spring with stiffness (K).

19**. Define the order of the system**.

The highest power of the complex variables in the denominator of the transfer function determines the order of the system.

20. **What is the need for block diagram reduction?**

Block diagrams of some of the control systems turn out to be complex. Such that the evaluation of their performance requires simplification (or reduction) of block diagrams which is carried out by block diagram rearrangements.

21 **List the advantages of a block diagram**.

- Individual as well as overall performance of the system can be studied by using transfer functions shown in the block diagram.
- Overall closed-loop transfer function can be easily calculated by using block diagram rules.
- The function of individual elements can be visualized from the block diagram.
- Very simple to construct the block diagram for complicated systems.

22. **List the disadvantages of a block diagram.**

- The source of energy is generally not shown in the block diagram. So, the block diagram for a given system is not unique.
- The block diagram does not include any information about the physical construction of the system.
- Block diagram reduction technique is a time-consuming process for complicated Systems (higher order systems).

23. **What do you mean by a branch in the signal flow graph?**

A signal travels along a branch from one node to another in the direction indicated by the branch arrow and in the process gets multiplied by the gain or transmittance of the branch.

25. **Define chain node**.

A node having incoming and outgoing branches is known as a chain node .

26. **Define self loop.**

A feedback loop consisting of only one node is called self loop .

27. **Define Loop gain.**

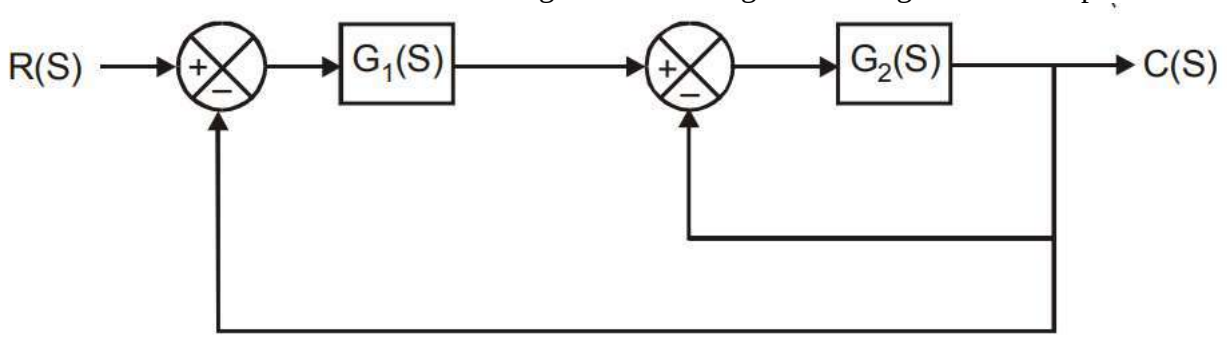
The product of all the gains of the branches forming a loop is called loop gain.

28. **Define the forward path.**

A path from the input to the output node is defined as a forward path.

PART-B

1. Describe the feed forward and feedback controller with an example.
2. Describe Multivariable Control Systems.
3. Derive the Transfer Function of DC Motors.
4. Derive Transfer Function of Field controlled DC Motor.
5. Using the block diagram reduction technique find the closed-loop transfer function of the system.
6. Write down the properties and construction of the signal flow graph.
7. Write down the Procedure for Converting the Block Diagram to a Signal Flow Graph.



UNIT-2 TIME RESPONSE ANALYSIS

1. What is the necessity for standard test signals in the analysis of control systems?

In many control systems, the command signals are not known fully ahead of time. It is difficult to express the actual input signals mathematically by simple functions. To know the behavior of the system in advance the standard test signals are used in the analysis of control systems. The standard signals are Impulse, Step, ramp, and Parabolic

2. **List the standard test signals used in time domain analysis.**

The standard test signals used in time domain analysis are

- Unit step input
- Unit Impulse input
- Unit ramp input
- Unit parabolic input

3. What are type 0 and type 1 systems?

- Type 0 systems – there are no poles of the loop transfer function that lie at the origin.
- Type 1 system – it has only one pole of loop transfer function that lies at the origin.

4. **What is the positional error coefficient?**

The positional error constant $K_p = \lim G(s)H(s)$. Here G(s) H(s) is the loop transfer function.

The steady-state error in type – 0 systems for unit step input is given by 1/ 1+Kp

5. **Distinguish between steady-state response and transient response.**

Transient response:
Transient response is the time response of the system when the input changes from one state to another. Transient response is temporary and will die out soon

Steady State Response:
Steady-state response is the time response of the system when time tends to infinity. It is the behavior of the system after an external input is applied to that system

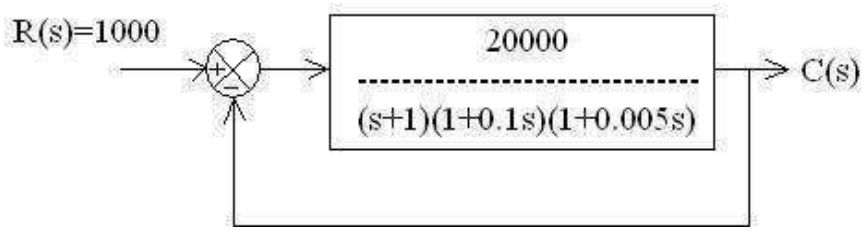
6. **What are time domain specifications?**

The time domain specifications are Peak time (t_p), Delay time (t_d), Rise time (t_r), Maximum overshoot ($\%M_p$), and Settling time (t_s)

7. **Define delay time.**

Delay time is the time taken for the response to reach 50% of its final value, for the very first time.

8. **The block diagram shown in fig. represents a heat-treating oven. The set point is 1000ºC. What is the steady state temperature?**



At steady state the system reaches its final value which is the set point. Here the set point is 1000ºC

9. **Define rise time. (or) What is meant by rise time?**

For an underdamped system: Rise time is the time taken for the response to rise from 0% to 100% for the very first time.
For an overdamped system: Rise time is the time taken by the response to rise from 10% to 90%.
For a critically damped system: Rise time is the time taken for the response to rise from 5% to 95%.

10. **Define Peak time (T_p)**

Peak time is the time taken for the response to reach the peak value for the very first time. (or) it is the time taken for the response to reach the peak overshoot.

$$t_p = \frac{\pi}{\omega n\sqrt{1-\delta^2}}$$

11. **What are static error constants?**

The K_p, K_v and K_a are called static error constants. These constants are associated with Steady State error in a particular type of system and for a standard input.

12. **Define maximum peak overshoot.**

Maximum Peak overshoot is defined as the ratio of the maximum value measured from the steady state value to the steady state value.

13. **How the system is classified depending on the value of damping?**

Case 1: Undamped system, $\epsilon = 0$
Case 2: Underdamped system, $0 < \epsilon < 1$
Case 3: Critically damped system, $\epsilon = 1$
Case 4: Overdamped system, $\epsilon > 1$

14 **Why is 'under damping' preferred to over damping in control systems?**

'Under damping' is preferred over damping, to achieve high response speed. That is the settling time is less for an under-damped system compared to over-damped systems, even though the oscillations are less in the later

15. **Why derivative control action is never used alone?**

Since the derivative controller's output is directly proportional to the rate of change of the error signal if it is used alone for a constant error signal it will not give any corrective action. With sudden changes in the system, the derivative controller will compensate for the output fast. A derivative controller will in general have the effect of increasing the stability of the system, reducing the overshoot, and improving the transient response.

16. What is the effect of the Pl controller on the system performance?

The PI controller increases the order of the system by one, which results in reducing the steady-state error. However, the system becomes less stable than the original system. It Eliminates Offset

17. **What is the effect of the PD controller on the system performance?**

The effect of the PD controller is to increase the damping ratio of the system and so the peak overshoot is reduced. P controller is to decrease the steady-state error of the system. As the proportional gain factor K increases, the steady state error of the system decreases. However, despite the reduction, P control can never manage to eliminate the steady state error of the system

18. **What is the type and order of the system?**

Order: The order of a system is the order of the differential equation governing the system. The order of the system can be obtained from the transfer function of the given system.

Type: The type number of a system indicates the number of poles at the origin.

19. **Define steady state error**

The difference between the desired output and the actual output of the system is called steady-state error, which indicates the accuracy and plays an important role in designing the system

20. **What is meant by the type number of the system? What is its significance?**

The type number is given by a number of poles of the loop transfer function at the origin. The type number of the system decides the steady-state error.

21**. Define step signal.**

It is the sudden application of the input at a specified time.

Mathematically it can be expressed as

R(t) = At for t > 0
R(t) = 0 for t <0

If A = 1, then it is called a unit step function denoted by u(t)

22. **Define ramp signal.**

It is the constant rate of change in input. i.e. gradual application of the input. The magnitude of ramp input is nothing but its slope. Mathematically it can be expressed as

R (t) = At for t > 0
R (t) = 0 for t< 0.

If A = 1, then it is called t unit ramp function.

23. **Define peak overshoot**.

Peak overshoot M: It is defined as the difference between the peak value of the response and the steady state value. It is usually expressed in percent of the steady-state value.

24**. Write the equation in Laplace for a test signal analogous to a shock and a signal with linear variation of time.**

Laplace Equation: Test signal analogous to a shock: R(S) = 1 (impulse signal)
Laplace Equation: Signal with linear variation of time: R(S) = A/ s^2 (Ramp signal)

25. **What are the differences between steady state and generalized error coefficients?**

The steady-state error is defined as the value of error as time tends to infinity. They are the coefficients of a generalized series. The generalized error series is given by $e(t) = C_0\, r(t)+C_1\, dr\,(t)/dt +(C_2/2!)\, dr^2\,(t)/dt^2+.....+(Cn/n!)\, dr^n\,(t)/dt^n$ ...The coefficients C_0, C_1, C_2,.. "C_n are called generalized error coefficients or dynamic error coefficients.

26. **What are the advantages of generalized error series?**

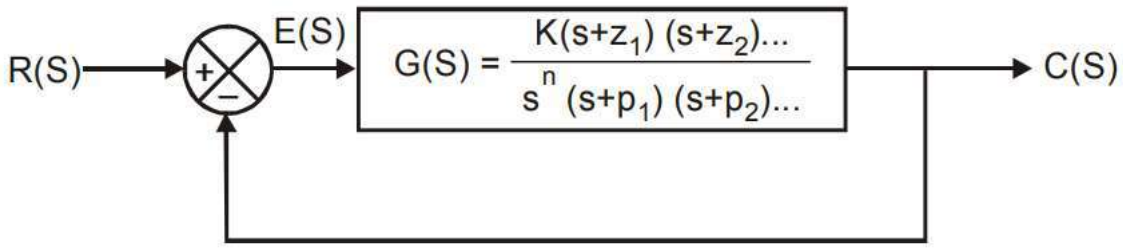
i) Steady state is a function of time.
ii) Steady state can be determined from any type of input.

27. **Give the steady state errors to a various standard input for type-2 system**.

Type 2 system	***Step Input***	***Ramp Input***	***Parabolic***
Steady-State Error Formula	$\frac{1}{1+Kp}$	$\frac{1}{Kv}$	$\frac{1}{Ka}$
Static Error Constant	K_p = infinity	K_v=infinity	$K_a = K$
Error	0	0	$\frac{1}{K}$

28. **What are type 0 and type 1 systems?**

The term of s^n in the denominator of G(s) indicates that there are n integrations in the forward path. According to the value of n, systems can be classified into different types.



Specifically, a system is called Type 0 system if n = 0, Type 1 system if n =1, or Type 2 system if n = 2, and so on. Note that this classification is different from that of the system order

29. **Write the PID controller equation.**

$$u(t) = K_p e(t) + K_i \int_0^t e(t)dt + K_d \frac{de(t)}{dt}$$

30. **How do you find the type of a system?**

The order of denominator in T.F determines the order of the T.F. But type is different. It is the order of the integrator transfer function. The integrator

$T.F$ is $G(s) = 1/s$.

$T(s) = K\,(s+1)/\,(s+2)\,(s+7)$ 2nd order, Type 0

$T(s) = K\,(s+1)/\text{s.}\,(s+2)\,(s+7)$ 3rd order, Type 1

31. **What is the velocity error coefficient?**

The steady-state error of the system for a ramp input is $1 / K_v$ where K_v is the velocity error coefficient. The velocity error coefficient is given by K_v = Lt sG(S) H(S) where limit s = 0

32. **What is the acceleration error coefficient?**

The steady state error of the system for a step input is $1/ K_a$. where K_a is the acceleration error coefficient. The acceleration error coefficient is given by K_a = Lt s^2 G(S) H(S) where limit s = 0

PART-B

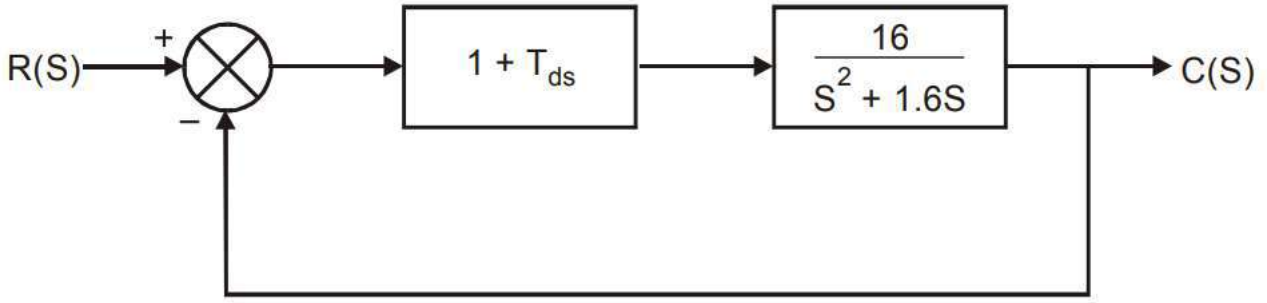
1. Analyze the response of a closed loop first-order system for a unit step input. Plot the response of the system.

2. Summarize the response of the undamped second-order system for unit step input.

3.Obtain the response of the unity feedback system whose open loop transfer function is G(s) = 4/[S(S+5)] and when the input is unit step.

5. Determine K to limit the error of a system for I/P r(t) = 1+8 t+18/2 t^2 to 0.8 having
G(s) H(s) = k/(s+1) (s+4) s^2

6. The following diagram shows unity feedback with derivative control. By using this derivative control, the damping ratio is to be mode 0.5. Determine the value of T_d.



6. Calculate the following parameters for the system whose natural frequency of oscillations is 10 rad/sec and damping ratio is 0.707. i) Delay time ii) Rise time iii) Percentage of peak overshoot iv) Setting time

7.For servo mechanisms with open loop transfer function given below explain what type of input signal gives rise to a constant steady-state error and calculate their values G(S) = 20(S+2)/ s(s+1) (s+3)

8. The loop transfer function can be expressed as a ratio of two polynomials.

UNIT III FREQUENCY RESPONSE AND SYSTEM ANALYSIS

1. What are the frequency domain specifications?
(Or)
Name the parameters that constitute frequency domain specifications.

The frequency domain specifications indicate the performance of the system in frequency domain, and they are Resonant peak (ω_p), Resonant frequency (ω_r), Band width (ω_b), Cut- off rate, Phase margin(γ) & Gain margin (kg).

2. **Define resonant peak and resonant frequency.**

Resonant peak (Mr): The maximum value of the magnitude of closed loop transfer function is called resonant peak. A large resonant peak corresponds to a large overshoot in transient response.

Resonant frequency (ωr): The frequency at which the resonant peak occurs is called resonant frequency. This is related to the frequency of oscillation in the step response and thus, it is indicative of the speed of transient response

3. **What is meant by corner frequency in frequency response analysis?**

The magnitude plot can be approximated by asymptotic straight lines. The frequencies corresponding to the meeting point of asymptotes are called corner frequencies. The slope of the magnitude plot changes at every corner frequency.

4. **Define phase cross-over frequency.**

The phase cross-over frequency is the frequency at which the phase of the open loop transfer function is -180^{o}.

5. **Define the term Gain Margin.**

The gain margin, Kg is defined as the value of gain, to be added to the system to bring the system to the verge of instability. The gain margin is given by the reciprocal of the magnitude of the open loop transfer function at phase cross-over frequency. The phase cross-over frequency is the frequency at which the phase is -180°.

6. **What are all pass systems and non-minimum phase transfer functions?**

All-pass systems: An all-pass system is a system whose frequency magnitude response is constant for all frequencies and the transfer function will have an anti-symmetric pole-zero pattern (i.e. for every pole in the left half of s – plane, there is a zero in the mirror image position concerning imaginary axis.

Non-minimum phase transfer function: A transfer function, that has one or more zeros in the right half s – plane is known as a non-minimum phase transfer function.

7. **What is compensation and what are the types of compensators?**

The compensation is the design procedure in which the system behavior is altered to meet the desired specifications, by introducing an additional device called compensator. The types of compensators are lag compensator, lead compensator, lag-lead compensator.

8. **Discuss the effects of adding a pole to the open loop transfer function of a system.**

The addition of poles to the transfer function has the effect of pulling the root locus to the right, making the system less stable

9. **Why compensators are necessary in a feedback control system?**

In feedback control systems compensation is required in the following situations.

1. When the system is absolutely unstable, then compensation is required to stabilize the system and also to meet the desired performance.
2. When the system is stable, compensation is provided to obtain the desired performance

10. **Name the commonly used electrical compensating networks.**

Lag network - pass filter,
Lead network - high pass filter
Lead-Lag network – Bandpass filter

11. **State the property of a lead compensator.**

The lead compensation increases the bandwidth and improves the speed of response. It also reduces the peak overshoot. If the pole introduced by the compensator is not canceled by a zero in the system, then lead compensation increases the order of the system by one.

When the given system is stable/unstable and requires improvement in transient state response then lead compensation is employed**.**

12. Mention a few applications of the bode plot.

- To determine the stability of OP-AMP and Transistor.
- Stability analysis of control system
- Active filter circuits
- The frequency domain specifications can be easily determined
- The bode plot can be used to analyze both open-loop and closed-loop systems.

13. **What is lag-lead compensation?**

A compensator having the characteristics of a lag-lead network is called a lag-lead compensator. In a lag-lead network when the sinusoidal signal is applied, both phase lag and phase lead occur in the output, but in different frequency regions. Phase lag occurs in the low-frequency region and phase lead occurs in the high-frequency region (i.e.) the phase angle varies from lag to lead as the frequency is increased from zero to infinity.

14. **Define bandwidth.**

The bandwidth is the range of frequencies for which the system gains more than 3 dB. The bandwidth is a measure of the ability of a feedback system to reproduce the input signal, noise rejection characteristics and rise time.

15. **How will you get closed-loop frequency response from open-loop response?**

For design of control systems, any of the three types of plots [Bode, Nyquist, Nichols] can be used to infer closed-loop stability and stability margins (gain and phase margins) from the open-loop frequency response.

16. **Define gain margin and phase margin.**

The gain margin, kg is defined as the reciprocal of the magnitude of the open loop transfer function at phase cross-over frequency.

The phase margin, the rope is the amount of phase lag at the gain cross-over frequency required to bring the system to the verge of instability

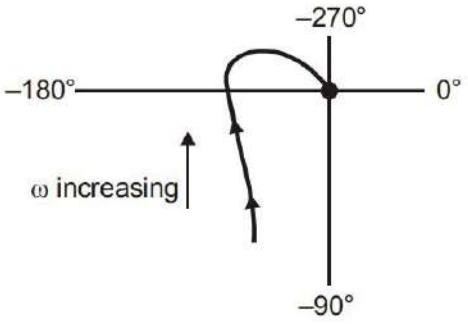
17. **Define Phase lag and phase lead.**

A negative phase angle is called phase lag.

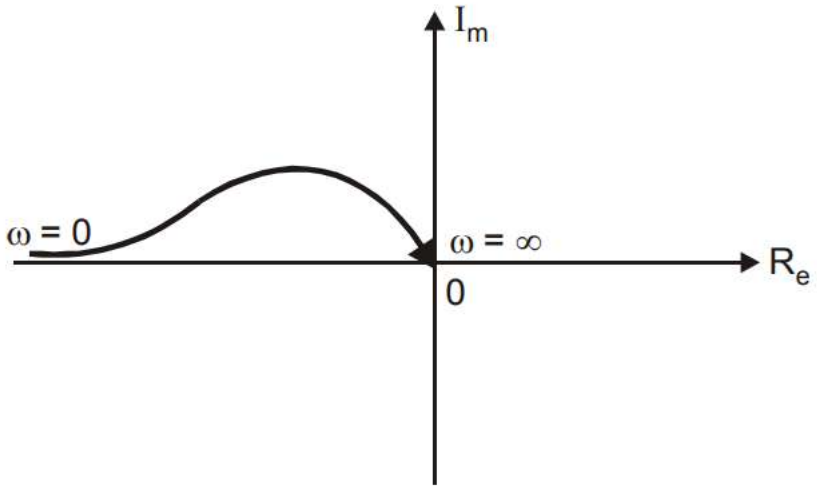
A positive phase angle is called phase lead.

18. **Draw the approximate polar plot for the functions,**

$$G(s) = \frac{10}{s(s+1)(s+2)}$$



19. **Draw the polar plot for a Type 2 third order system.**



Polar plot for type 2, order 3 system

20. Derive the transfer function of a lead compensator network.

$$\text{Transfer function, Glead (s)} = \frac{E_0(s)}{E_i(s)} = \frac{1}{\alpha}\left[\frac{1+\alpha sT}{1+sT}\right]$$

21. **What are the advantages of frequency response analysis?**

1. Design of the system and adjusting the parameters of the system can be easily carried

out.

2. Corrective measurement for noise disturbance generated in the system and parameter variation can be easily determined using frequency analysis.

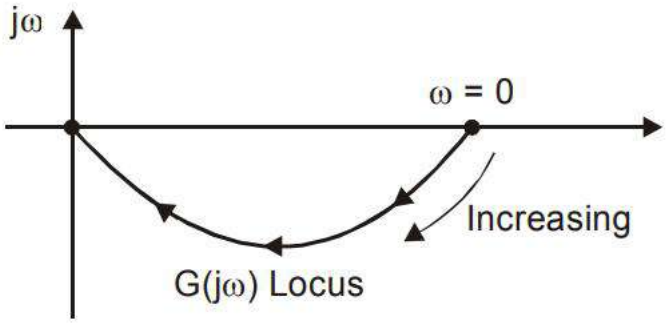
3. Absolute and Relative stability of the closed-loop system can be estimated from the knowledge of the open loop frequency system.

4. Frequency domain analysis can also be carried out for the nonlinear control systems

22. **Define gain cross-over frequency**.

The gain cross-over frequency w_{gc} is the frequency at which the magnitude of the open loop transfer function is unity.

23. Draw the polar plot of G(s) = (1/ 1+sT)



24. What are the main advantages of the Bode plot?

The main advantages are:

i) Multiplication of magnitude can be into addition.

ii) A simple method for sketching an approximate log curve available.

iii) It is based on asymptotic approximation. Such approximation is sufficient if rough.

iv) Information on the frequency response characteristic is needed.

25 What are series compensators?

Connecting compensating circuit diagram error detectors and plants known as series compensator

26. What are the effects of the Lag-Lead compensator?

a) Improves the transient response.

b) Improves the steady-state performance at the expense of slower settling time.

27. What is the need for compensation in control systems?

a) To obtain the desired performance of the system, we use compensating networks. Compensating networks are applied to the system in the form of feed-forward path gain adjustment.

b) Compensate an unstable system to make it stable.

c) A compensating network is used to minimize overshoot.

d) These compensating networks increase the steady-state accuracy of the system. An important point to be noted here is that the increase in the steady state accuracy brings instability to the system.

e) Compensating networks also introduce poles and zeros in the system thereby causing changes in the transfer function of the system. Due to this, the performance specifications of the system change.

28. What is the relation between Φm and α?

$$\sin \phi_m, = \frac{1-\alpha}{1+\alpha}$$

29. What type of compensator suitable for high frequency noisy environment?

Phase lag network allows low frequencies and high frequencies are attenuated.

PART-B

1. Write down the procedure to construct bode plot, polar plot and Nyquist plot

2. For the following open loop transfer function sketch the Bode magnitude and phase plot for G(s) H(s) = 10(s+50)/s(s+5)

3. Given G(s) = $Ke^{-0.2}/s(s+2)(s+8)$. Find K so that the system is stable with (a) gain margin equal to 6 dB and (b) phase margin equal to 45°.

4. The open loop transfer function of a unity feedback system is given G(s) = 1/ $s(1+s)^2$ by Sketch the polar plot and determine the gain s plane margin.

5. Write down the types of compensating network?

6. Write down the procedure to design on lag compensator, lead compensator and lead-lag compensator using bode plot

7. A unity feedback system has an open loop transfer function G(s) = K/s(s+8) . Design a suitable lead compensator is to meet the following specifications.

i) $K_V \geq 100°$ ii) Phase margin ≥ 50°

8. Consider a unit feedback system with the following open loop transfer function G(s) = K/s(s+1)(s+4) .Design a lag compensator to satisfy the following specifications.

i) Damping ratio $\xi = 0.5$ ii) Settling time $t_s = 10$ sec iii) Velocity error constant $K_V \geq 5$ sec^{-1}

UNIT IV CONCEPTS OF STABILITY ANALYSIS

1. Define stability of a system.

A linear time invariant system is said to be stable if the following conditions are satisfied.
(i)When the system is excited by a bounded input, output is also bounded and controllable.

(ii) In the absence of the input, output must tend to zero irrespective of initial conditions.

2. **Define asymptotic stability.**

In the absence of the input, the output tends towards zero (the equilibrium state of the system) irrespective of initial conditions. This stability concept is known as asymptotic stability.

3. What is the limitedly stable system?

For a bounded input signal, if the output has constant amplitude oscillations, then the system may be stable or unstable under some limited constraints. Such a system is called limitedly stable.

4. **What is the relation between stability and coefficient of characteristic polynomial?**

If any one or more of the coefficients of the characteristic's polynomial is negative or zero, then some of the roots lie on the right half of the S plane. Hence the system is unstable. If the coefficients of the characteristic equation are zero and the rest of the coefficients are positive then there is a possibility of the system being stable provided all the roots are lying on the left half of the s-plane.

5. How are the locations of roots of characteristic equations related?

a) If all the roots of the characteristic equations have –ve real parts, the system is bounded Input bounded output stable.
b) If any root of the characteristic equation has a +ve real part the system is unbounded and the impulse response is infinite and the system is unstable.
c) If the characteristic equation has repeated roots on the jω axis the system is marginally stable
d) If the characteristic equation has non-repeated roots on the jω axis the system is limited Stable double roots at the origin is unstable

6. What is the root locus?

The locus of the closed loop poles obtained when the system gain 'K' is varied from -∞ to +∞.(change). The graphical representation in the complex **s**-plane of the possible locations of its closed-loop poles for varying values of a certain system parameter. The points that are part of the root locus satisfy the angle condition.

7. **Comment on the stability of the system, when the roots of characteristic equation are lying on the imaginary axis.**

If the roots of the characteristic equation lie on the imaginary axis then the system is marginally stable system. Here the term marginally stable means the system is in between the conditions of stability and instability.

8. **What are pole and zero of a system?**

The poles of a closed loop system are defined as the roots of the denominator polynomial of the transfer function of that system. It represents the physical dimension of a system The zeros of a closed loop system are defined as the roots of the numerator polynomial of the transfer function of that system. Zeros are the roots of numerator of given transfer function by making numerator is equal to 0

9. **State the advantages –of-Nyquist-plot.**

(i) The Nyquist plot helps in determining the relative stability of the system in addition to the absolute stability of the system.
(ii) It determines the stability of the closed-loop system from the open-loop transfer function without calculating the roots of the characteristic equation

10. **What is meant by relative stability?**

Relative stability is a quantitative measure of how fast the transients die out in the system. It may be measured by the relative settling times of each root or pair of roots. Relative Stability gives the degree of stability or how close it is to instability

11. **Why do closed-loop systems tend to oscillate?**

In a closed loop system it has negative Feedback where the output is always compared with the input and the controller is going to take corrective action based on the difference between errors and it has the tendency to oscillate when the gain in the controller increases.

12. **What is the advantage of using root locus for design?**

To find out the potential closed-loop pole location. It helps to design a good compensator. The Root Locus Plot technique can be applied to determine the dynamic response of the system. This method associates itself with the transient response of the system and is particularly useful in the investigation of the stability characteristics of the system

13. **What is the main objective of the root locus analysis technique?**

The main objective of the root locus plot is to obtain the transient response of the feedback system for various values of open loop gain K and to determine sufficient conditions for the value of 'K' that will make the feedback system unstable.

14. **What is the dominant pole?**

The dominant pole is a pair of complex conjugate poles that decides the transient response of the system. In the higher-order system, the dominant poles are very close to the origin and all other poles of the system are widely separated so they have less effect on the transient response of the system.

15. **What are the effects of adding an open-loop pole to the root locus and the system?**

- Settling time increases
- Range of K reduces.
- Gain Margin enhances relatively, thus stability decreases.
- The system becomes oscillatory changes its nature and shifts towards an imaginary axis.

16. **State the necessary and sufficient condition of the Routh - Hurwitz criterion**

A necessary condition for stability of the system: In this, we have two conditions which are written below:

i) All the coefficients of the characteristic equation should be positive and real.
ii) All the coefficients of the characteristic equation should be non-zero.

17. **State the method of determining the gain K at a point on the root locus.**

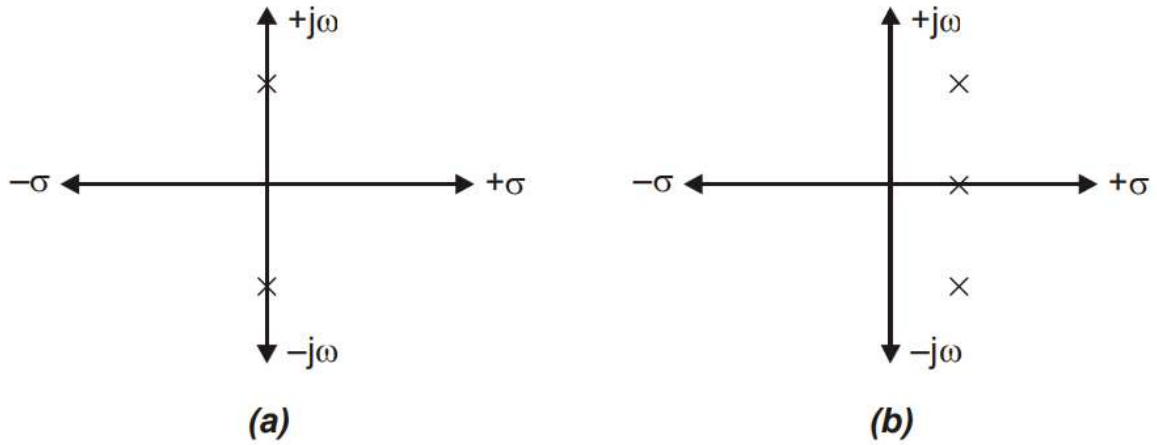
i) Magnitude Criteria: At any point on the root locus, we can apply magnitude criteria as,

|G(s) H(s)| = 1 Using this formula we can calculate the value of K at any desired point.

ii) Using Root Locus Plot: The value of K at any s on the root locus is given by

$$\frac{\text{Product of all of the vector lengths drawn from the poles of } G(s)H(s) \text{ to } s}{\text{Product of all of the vector lengths drawn from the zeros of } G(s)H(s) \text{ to } s}$$

18**. Sketch the time response plot under (a) Roots lying on the imaginary axis (b) Roots lying in R.H.S plane.**

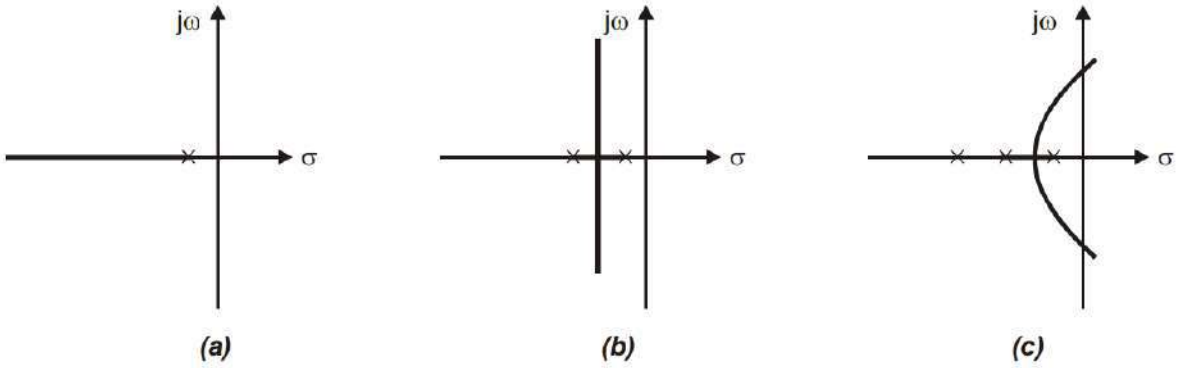


19. What is the correlation between phase margin and damping factor?

$$\Phi_M = 90 - \tan^{-1}\frac{\sqrt{1-2\varsigma^2+\sqrt{1+4\varsigma^4}}}{2\varsigma} = \tan^{-1}\frac{2\varsigma}{\sqrt{2\varsigma^2+\sqrt{1+4\varsigma^4}}}$$

20. What are the effects of addition of open loop poles?

When a pole is added the root locus of the system moves closer to s = jω plane. (Assuming pole is not added far away from origin) hence stability decreases.



Effect of Adding Poles

21. **State the rules for obtaining the breakaway point in root locus**.

To find where the locus breaks away from the axis (or converges on the axis), we note that this always occurs when two (or more) roots intersect. It is a well-known fact, that when a polynomial has multiple roots, not only is the value of the polynomial zero, but its derivative is zero also.

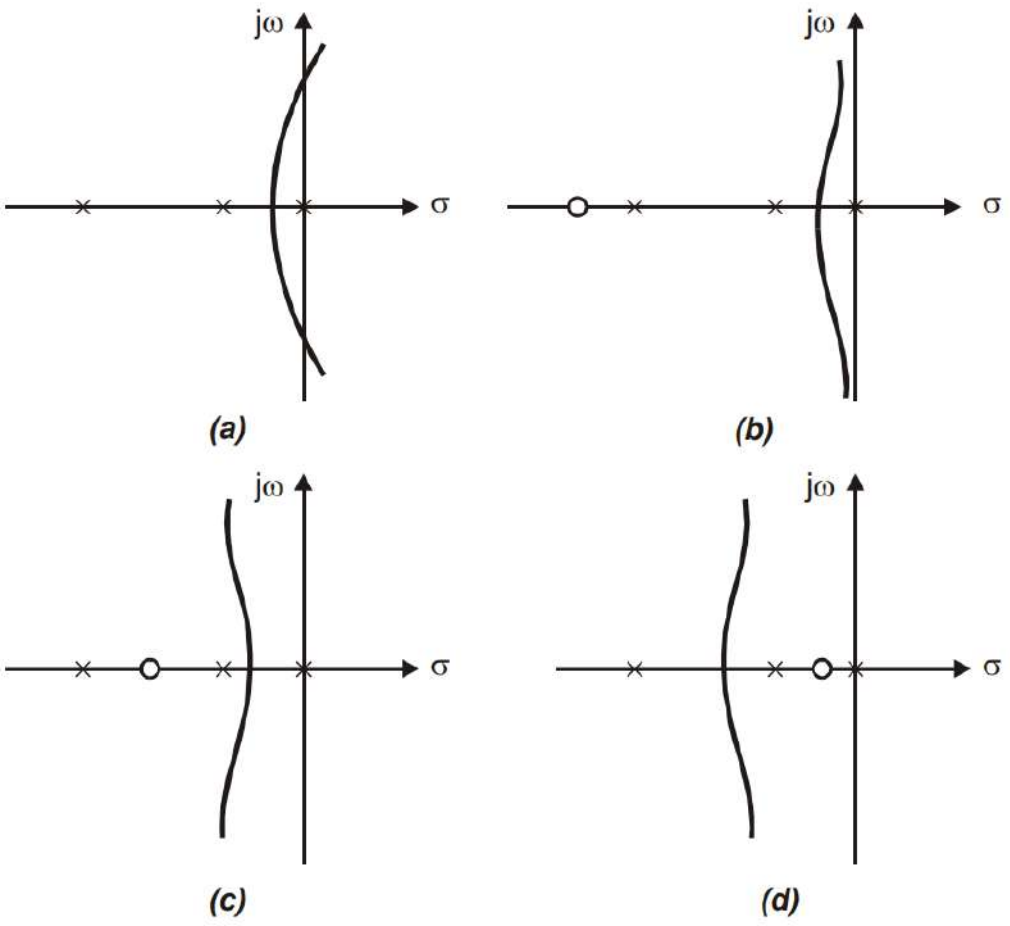
22. **What is centroid?**

The meeting point of asymptotes with the real axis is called the centroid.

$$\text{Centroid} = \text{sum of poles- sum of zeros}/n\text{-}m$$

23. What is effect of adding zeros?

Additional zero pulls the root-locus to the left.

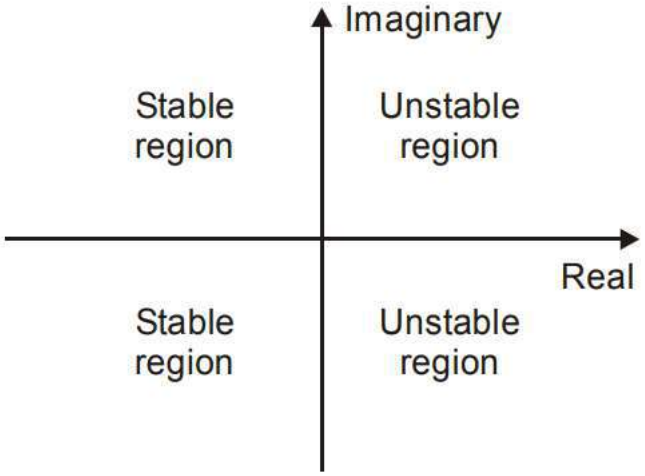


24. What is BIBO stability criterion?

A linear relaxed system is said to have BIBIO stability if every bounded input results in a bounded output.

25. How are the locations of roots of characteristics equation related to stability?

If poles lies in the left part of s- plane then the system is stable, else unstable.



26. What is meant by +20db/dec slope change?

Decade (log scale). One decade is a factor of 10 difference between two numbers (an order of magnitude difference) measured on a logarithmic scale. Along with the octave, it is a logarithmic unit used to describe frequency bands or frequency ratios.

27**. What are root loci?**

The path taken by the roots of the open loop transfer function when the loop gain is varied from 0 to a is called root loci.

28. How will you find root locus on real axis?

To find the root locus on real axis, choose a test point on real axis. If the total number of poles and zeros on the real axis to the right of this rest point is odd number then the rest point lies on the root locus. If it is even then the test point does not lie on the root locus.

29 **What are the asymptotes?**

Asymptotes are straight lines which are parallel to root locus going to infinity and meet the root locus at infinity.

30. **How will you find the angle of asymptotes?**

$$\text{Asymptotes} = \frac{180(2q+1)}{n-m}; \quad q = 0, 1, 2 \ldots\ldots\ldots(n-m)$$

31. How to find the crossing point of root locus in imaginary axis.

Method: i) by Routh Hurwitz criterion
Method: ii) by letting s=jω in the characteristic's equation.

32. What is the characteristic equation?

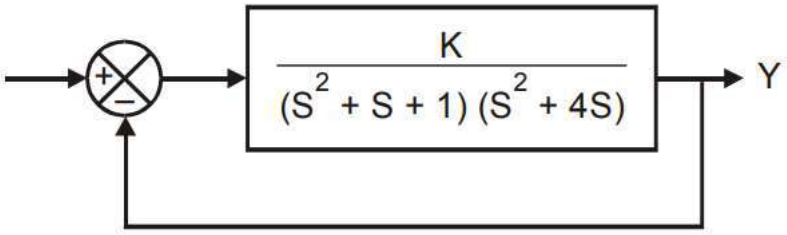
The denominator polynomial C(s)/R(s) is the characteristic equation of the system.

33. What is the necessary condition for stability?

The necessary condition for stability is that all the coefficients of characteristic polynomials are positive.

PART-B

1. A closed-loop control system has the characteristic equation given by $s^3 + 4.5 s^2 + 3.5 s + 1.5 = 0$. Investigate the stability using the Routh-Hurwitz criterion.
2. Determine the stability of a closed loop control system whose characteristic equation is $s^5 + s^4 + 2s^3 + 2 s^2 + 11 s + 10 = 0$.
3. For each of the characteristic equations of the feedback control system given, determine the range of K for stability. Determine the value of K so that the system is marginally stable and the frequency of sustained oscillations. $s^4 + 25s^3 + 15s^2 + 20s + K = 0$
4. Write the procedure to construct the root locus.
5. A unity feedback control system has an open loop transfer function G(s) = K/s(s+4). Draw the root locus and determine the value of K if the damping ratio γ is to be 0.707.
6. The open loop transfer function of a control system is given by G(s) H(s) = K/ s(s+6)(s2+4s+13). Sketch the root locus and determine a) The breakaway points b) The angle of departure from complex poles c) The stability condition
7. Comment on the Nyquist stability of the system whose open loop transfer function G(s) H(s) = 1/s(1+2s) (1+s). Also, find gain and phase margin.
8. Consider the closed loop system shown in Figure to determine the range of K for which the system is stable.



UNIT V CONTROL SYSTEM ANALYSIS USING STATE VARIABLE METHODS

1. **Define state and state variables.**

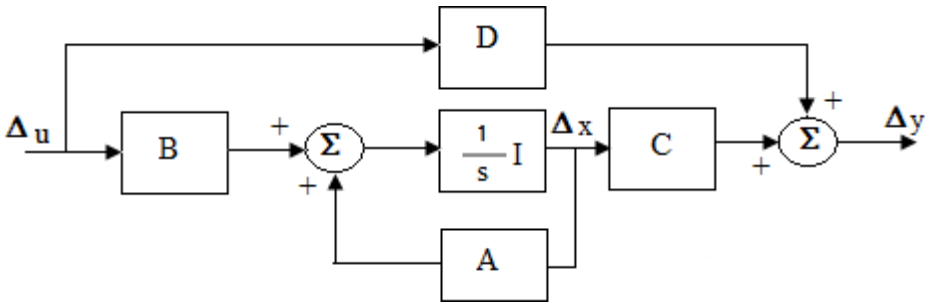
State: The minimum number of initial conditions that must be specified at any initial time t_0 so that the complete behavior of the system for $t \geq 0$ is determined when the input is known**.** The state is the condition of a system at any time instant.

State variable: State variables depend on the dynamic model selected to describe the physical system which can be described by nth-order differential equations. A set of variables that describe the state of the system at any time instant are called state variables.

2. **What is state space?**

Sate space is the state of a system described by a set of all possible variables in which the state vector X(t) can have at time ‘t’ forms the state space of the system.

3. **Draw the block diagram of state space model.**



4. **What are the advantages of the state space approach?**

a) The state space analysis applies to any type of system. They can be used for modeling and analysis of linear and nonlinear systems, time-variant and time-invariant systems, and multi-input multi-output systems.

b) The state space analysis can be performed with initial conditions.

c) The variables used to represent the system can be any variables in the system.

d) Using this analysis, the internal states of the system at any time instant can be predicted

5. Compare the merits and demerits of realizing a given system in state variable and transfer function form.

Merits of transfer function:

1. It is useful for analyzing the effects of the input.
2. Transfer function can be used as a multiplier to obtain the forced response transform from the input transform.
3. transfer function is independent of the input function and the initial conditions

Demerits of transfer function form:

1. Transfer function is defined under zero initial zero conditions.
2. Transfer function is applicable to linear time invariant systems.
3. Transfer function analysis is restricted to single input and output systems.
4. Does not provide information regarding the internal state of the system.

Merits of State Variable form:

1. The state space analysis can be predicted to be performed with initial conditions.
2. The variables used to represent the system can be any variables in the system.
3. Using this analysis the internal states of the system at any time instant.

6. What are the different methods available for computing the State Transition matrix (e^{At})?

a) Using matrix exponential
b) Using Laplace transform
c) Using canonical transformation
d) Using Cayley-Hamilton theorem

7.How the modal matrix is determined?

In linear algebra, the modal matrix is used in the diagonalization process involving eigenvalues and eigenvectors.

8. Define state equation.

In control engineering, a state-space representation is a mathematical model of a physical system as a set of input, output, and state variables related by first-order differential equations.

9. Give the concept of controllability.

Controllability is an important property of a control system, and the controllability property plays a crucial role in many control problems, such as stabilization of unstable systems by feedback, or optimal control.

10. What are the properties of the state transition matrix?

1. $\Phi(0) = I$
2. $\Phi^{-1}(t) = \Phi(-t)$
3. $x(0) = \Phi(-t)\, x(t)$
4. $\Phi(t_2 - t_1)\Phi(t_1 - t_0) = \Phi(t_2 - t_0)$
5. $\Phi(t)^k = \Phi(kt)$

11. Define observability of a system.
In control theory, observability is a measure for how well internal states of a system can be inferred by knowledge of its external outputs.

PART-B

1. Write down the state space representation of n order differential equation and electrical network
2. Determine the LaPlace Transform Method to Solve State Equation
3. Determine the Infinite Series Method for Solving Homogeneous State Equation
4. Determine the transfer matrix for the MIMO system.
5. Determine the controllability and observability of the system
6. Write down the state space representation of controllable canonical form

$Y(s)/\ U(s) = 10(s + 4)/\ s(s + 1)(s + 3)$

7. Obtain the transfer function of the system defined by the following state space model $[\ x_1\ x_2\ x_3\ ] = [\ -2\ 1\ 0, 0\ -3\ 1\ , -3\ -4\ -5\ ][\ x_1\ x_2\ x_3\ ] + [\ 0\ 0\ 1\ ]\ u$ and $y = [0\ 1\ 0][\ x_1\ x_2\ x_3\ ]$
8. Calculate e^{At} If $A = [\ 0\ 1\ , -2\ -3\ ]$
9. Construct a state model for the system characterized by the differential equation $d^3y / dt^3 + 6\ d^2y/\ dt^2 + 11\ dy/\ dt + 6y + u = 0$

10. Construct the state model of the given mechanical system
11. Deduce the digital control design using state feedback with necessary steps
12. The state model of a discrete time system is given by

$X(k+1) = A\,X(k) + B\,U(k)$

$Y(k) = C\,X(k) + D\,U(k)$

Determine its transfer function.

MADHA
Expertise | Empathy | Excellence
ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC3352 DIGITAL SYSTEMS DESIGN

SEMESTER III

REGULATIONS 2021

NOTES

&

QUESTION BANK

EC3352 **DIGITAL SYSTEMS DESIGN** **L T P C**
3 0 2 4

COURSE OBJECTIVES :

- To present the fundamentals of digital circuits and simplification methods
- To practice the design of various combinational digital circuits using logic gates
- To bring out the analysis and design procedures for synchronous and asynchronous Sequential circuits
- To learn integrated circuit families.
- To introduce semiconductor memories and related technology

UNIT I BASIC CONCEPTS **9**

Review of number systems-representation-conversions, Review of Boolean algebra- theorems, sum of product and product of sum simplification, canonical forms min term and max term, Simplification of Boolean expressions-Karnaugh map, completely and incompletely specified functions, Implementation of Boolean expressions using universal gates ,Tabulation methods.

UNIT II COMBINATIONAL LOGIC CIRCUITS **9**

Problem formulation and design of combinational circuits - Code-Converters, Half and Full Adders, Binary Parallel Adder – Carry look ahead Adder, BCD Adder, Magnitude Comparator, Decoder, Encoder, Priority Encoder, Mux/Demux, Case study: Digital trans-receiver / 8 bit Arithmetic and logic unit, Parity Generator/Checker, Seven Segment display decoder

UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS **9**

Latches, Flip flops – SR, JK, T, D, Master/Slave FF, Triggering of FF, Analysis and design of clocked sequential circuits – Design - Moore/Mealy models, state minimization, state assignment,lock - out condition circuit implementation - Counters, Ripple Counters, Ring Counters, Shift registers, Universal Shift Register. Model Development: Designing of rolling display/real time clock

UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS **9**

Stable and Unstable states, output specifications, cycles and races, state reduction, race free assignments, Hazards, Essential Hazards, Fundamental and Pulse mode sequential circuits, Design of Hazard free circuits.

UNIT V LOGIC FAMILIES AND PROGRAMMABLE LOGIC DEVICES **9**

Logic families- Propagation Delay, Fan - In and Fan - Out - Noise Margin - RTL ,TTL,ECL, CMOS - Comparison of Logic families - Implementation of combinational logic/sequential logic design using standard ICs, PROM, PLA and PAL, basic memory, static ROM,PROM,EPROM,EEPROM EAPROM.

45 PERIODS

PRACTICAL EXERCISES : **30 PERIODS**

1. Design of adders and subtractors & code converters.
2. Design of Multiplexers & Demultiplexers.
3. Design of Encoders and Decoders.
4. Design of Magnitude Comparators
5. Design and implementation of counters using flip-flops
6. Design and implementation of shift registers.

COURSE OUTCOMES :

At the end of the course the students will be able to

CO1: Use Boolean algebra and simplification procedures relevant to digital logic.
CO2: Design various combinational digital circuits using logic gates.
CO3:Analyse and design synchronous sequential circuits.
CO4: Analyse and design asynchronous sequential circuits. .
CO5: Build logic gates and use programmable devices

TOTAL:75 PERIODS

TEXTBOOKS :

1. M. Morris Mano and Michael D. Ciletti, 'Digital Design', Pearson, 5th Edition, 2013. (Unit - I - V)

REFERENCES :

1. Charles H. Roth, Jr, 'Fundamentals of Logic Design', Jaico Books, 4th Edition, 2002.
2. William I. Fletcher, "An Engineering Approach to Digital Design", Prentice- Hall of India, 1980.
3. Floyd T.L., "Digital Fundamentals", Charles E. Merril publishing company,1982.
4. John. F. Wakerly, "Digital Design Principles and Practices", Pearson Education, 4 th Edition,2007.

5. Charles H. Roth, Jr, ‘Fundamentals of Logic Design’, Jaico Books, 4th Edition, 2002.
6. William I. Fletcher, "An Engineering Approach to Digital Design", Prentice- Hall of India, 1980.
7. Floyd T.L., "Digital Fundamentals", Charles E. Merril publishing company,1982.
8. John. F. Wakerly, "Digital Design Principles and Practices", Pearson Education, 4 th Edition,2007.

UNIT – I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES

Number System:

• A numeral system (or system of numeration) is a writing system for expressing numbers, that is, a mathematical notation for representing numbers of a given set, using digits or other symbols .The values of each digit is determined by the digit, the position of the digit in the number and the base or radix of the number system.The number system will be of 4 types.

1. Decimal
2. Binary
3. Octal
4. Hexadecimal

Decimal:

Decimal number system has base 10 as it uses 10 digits from 0 to 9..

Binary:

- Uses two digits, 0 and 1.It is also called as base 2 number system
- Each position in a binary number represents a x power of the base (2).
- Example: 2^X
- Last position in a binary number represents an x power of the base (2).
- Example: 2^x , where x =0,1,2,….. from LSB bit .

Octal

- Uses eight digits, 0,1,2,3,4,5,6,7. It is also called as base 8 number system
- Each position in an octal number represents a x power of the base (8). Example: 8^X
- LSB bit position in an octal number represents an x power of the base (8).
- Example: 8^x where x =0,1,2,….. from LSB bit.

Hexadecimal:

- Uses 10 digits and 6 letters, 0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F.
- Letters represents numbers starting from 10. A = 10, B = 11, C = 12, D = 13, E = 14, F = 15. Hexadecimal number system is also called as base 16 number system.
- Each position in a hexadecimal number represents a x power of the base (16). Example 16^x.
- LSB bit position in a hexadecimal number represents an x power of the base (16). Example 16^x , where x =0,1,2,….. from LSB bit

Decimal (10)	Binary (2)	Octal (8)	Hexadecimal (16)
0	0 0 0 0	0	0
1	0 0 0 1	1	1
2	0 0 1 0	2	2
3	0 0 1 1	3	3
4	0 1 0 0	4	4
5	0 1 0 1	5	5
6	0 1 1 0	6	6
7	0 1 1 1	7	7
8	1 0 0 0	10	8
9	1 0 0 1	11	9
10	1 0 1 0	12	A
11	1 0 1 1	13	B
12	1 1 0 0	14	C
13	1 1 0 1	15	D
14	1 1 1 0	16	E
15	1 1 1 1	17	F

Convert the following decimal to binary/ Octal/ Hexadecimal.

i). 267_{10} ii).14768_{10} iii). 34.45_{10}

(i) 267

Binary:

2	267	
2	133	1
2	66	1
2	33	0
2	16	1
2	8	0
2	4	0
2	2	0
	1	

$(267)_{10} = (10001011)_2$

Octal:

8	267	
8	33	3
	4	1

$(267)_{10} = (413)_8$

Hexadecimal:

16	267	
16	16	11
	1	0

$(267)_{10} = 1011 = (10B)_{16}$

ii).14768_{10}

Binary:

2	14768	
2	7384	0
2	3692	0
2	1846	0
2	923	0
2	451	1
2	23	1
2	11	1
2	5	1
2	2	1
	1	

$(14768)_{10} = (1111110000)_2$

Octal:

8	14768	
8	1846	0
8	23	6
	2	7

$(14768)_{10} = (2760)_8$

Hexadecimal:

16	14768	
16	923	0
16	57	B
	3	9

$(14768)_{10} = (39B0)_{16}$

iii). 34.45_{10}

Binary:

2	34	
2	17	0
2	8	1
2	4	0
2	2	0
	1	0

$34_{10} = 100010_2$

$0.45 \times 2 = 0.90$ 0 (LSB)
$0.90 \times 2 = 1.80$ 1
$0.80 \times 2 = 1.60$ 1
$0.60 \times 2 = 1.20$ 1
$0.20 \times 2 = 0.40$ 0 (MSB)

$(0.45)_{10} = (0.01110)_2$
$(34.45)_{10} = (100010.01110)_2$

Octal:

8	34	
	4	2

$34_{10} = 42_8$

$0.45 \times 8 = 3.6$ 3(LSB)
$0.60 \times 8 = 4.8$ 4
$0.80 \times 8 = 6.4$ 6
$0.40 \times 8 = 3.2$ 3
$0.20 \times 8 = 1.6$ 1(MSB)

$(0.45)_{10} = (0.34631)_8$
$(34.45)_{10} = (42.34631)_8$

Hexadecimal:

16	34	
	2	2

$34_{10} = 22_{16}$

$0.45 \times 16 = 7.2$ 7
$0.2 \times 16 = 3.2$ 3
$0.2 \times 16 = 3.2$ 3

$(0.45)_{10} = (0.733)_{16}$
$(34.45)_{10} = (22.733)_{16}$

Convert the Binary number 11100101 to its decimal, octal and hexadecimal equivalent.

Decimal:

$$1 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$$
$$= 128 + 64 + 32 + 0 + 0 + 4 + 0 + 1$$
$$= [229]_{10}$$

Octal: $\underbrace{011}_{3}\ \underbrace{100}_{4}\ \underbrace{101}_{5} = [345]_8$

Hexadecimal $\underbrace{1110}_{E}\ \underbrace{0101}_{5} = [E5]_{16}$

Convert the Octal number 2436 to its decimal, binary and hexadecimal equivalent.

Decimal: $2 \times 8^3 + 4 \times 8^2 + 3 \times 8^1 + 6 \times 8^0$
$$= 1024 + 256 + 24 + 6$$
$$(2436)_8 = [1310]_{10}$$

2 4 3 6

Binary:

010 100 011 110

$$= [10100011110]_2$$

Hexadecimal: 2 4 3 6

010 100 011 110

$= \underbrace{0101}_{5}\ \underbrace{0001}_{1}\ \underbrace{1110}_{E} = [51E]$

Convert the hexadecimal number 28D to its decimal, binary and octal equivalent.

Decimal: 2 8 D

$= 2\ 8\ 13$

$= 2 \times 16^2 + 8 \times 16^1 + 13 \times 16^0$

$= 512 + 128 + 13$

$= [653]_{10}$

Binary: 2 8 D

$= 2\ \ 8\ \ 13$

$= 0010\ 1000\ 1101$

$= [1010001101]_2$

Octal: 2 8 D

$= 2\ 8\ 13$

$= 0010\ 1000\ 1101$

$= \underbrace{001}_{1}\ \underbrace{010}_{2}\ \underbrace{001}_{1}\ \underbrace{101}_{5}$

$= [1215]_8$

Convert FACE into its binary, octal and decimal equivalent.

Hexadecimal to binary:

FACE = F A C E

15 10 12 14

1111 1010 1100 1110

$= (1111101011001110)_2$

(i) Hexadecimal to octal:

FACE = F A C E

15 10 12 14

1111 1010 1100 1110

$\underbrace{001}\ \underbrace{111}\ \underbrace{101}\ \underbrace{011}\ \underbrace{001}\ \underbrace{110}$

1 7 5 3 1 6

$= (17\ 5\ 316)_8$

(ii) Hexadecimal to decimal

FACE = F A C E

1111 1010 1100 1110

$= 1111101011001110_2$

$= 1x2^{15}+1x2^{14}+1x2^{13}+1x2^{12}+1x2^{11}+0x2^{10}+1x2^9+0x2^8+1x2^7+1x2^6+0x2^5+0x2^4+1x2^3 +1x2^2+1x2^1+0x2^0$

$= 64206_{10}$

1's Complement

1's Complement is found by replacing all 1's by 0 and replace all 0 by 1.
Example : 1's complement of binary number 110010 is 001101

2's Complement

To get 2's complement of a binary number, find 1's complement of the number and add 1 to the least significant bit (LSB) of given result.

2’s complement of binary number 110010

1’s complement of 110010 =

Ans : 001110

$$\begin{array}{cccccccc} & & & & & 1 & & \\ 0 & 0 & 1 & 1 & 0 & 1 & & \\ & & & & & 1 & (+) & \\ \hline \mathbf{0} & \mathbf{0} & \mathbf{1} & \mathbf{1} & \mathbf{1} & \mathbf{0} & & \end{array}$$

Steps for 1’s Complement

Subtraction:

Subtraction of Smaller Number from Larger Number:

The steps for 1’s complement subtraction of a smaller number from a larger binary number are as follows:

Step-1: Determine the 1’s complement of the smaller number.

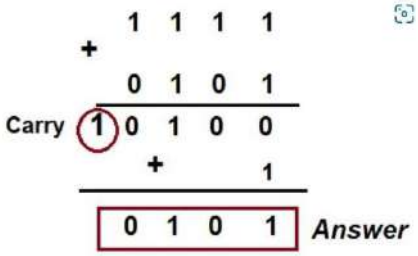
Step-2: Add this to the larger number.

Step-3: Remove the carry and add it to the result. This carry is called end-around-carry.

Example-1: Subtract $(1010)_2$ from $(1111)_2$ using 1’s complement method.

Step-1: Find the 1’s complement of 1010. It will be found by replacing all 0 to 1 and all 1 to 0. In this way, the required 1’s complement will be 0101.

Step-2: In this step, we need to add the vale calculated in step-1 to 1111. This is shown below.



Subtraction of Larger Number from Smaller Number:

The steps involved in 1’s complement subtraction of a larger number from a smaller number are as follows:

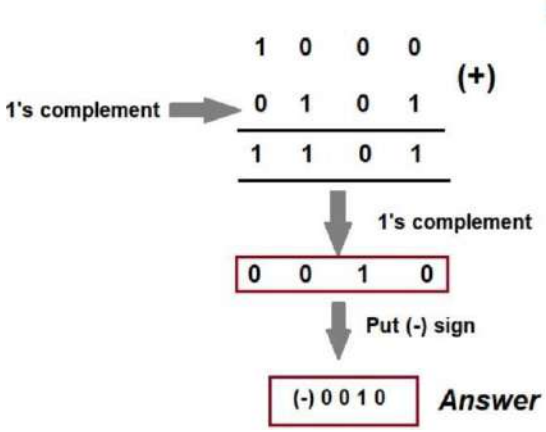
Step-1: Determine the 1’s complement of the larger number.

Step-2: Add this to the smaller number.

Step-3: The answer is the 1’s complement of the true result and opposite in sign. There is no carry.

Example: Subtract $(1010)_2$ from $(1000)_2$ using 1’s complement method.

The 1’s complement of $(1010)_2$ is $(0101)_2$. Now, add this with the smaller number and finally take 1’s complement of the result to get the answer. This is shown below.



Steps for 2's Complement Subtraction:

Subtraction of Smaller Number from Larger Number:

To subtract a smaller number from a larger number using 2's complement subtraction, following steps are to be followed:

Step-1: Determine the 2's complement of the smaller number

Step-2: Add this to the larger number.

Step-3: Omit the carry. Note that, there is always a carry in this case.

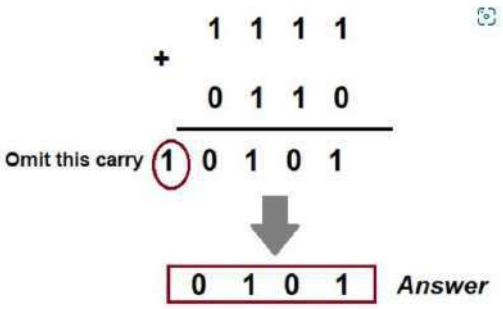
Following example illustrate the above mentioned steps:

Exampe-1: Subtract $(1010)_2$ from $(1111)_2$ using 2's complement method.

Solution:

Step-1: 2's complement of $(1010)_2$ is $(0110)_2$.

Step-2: Add $(0110)_2$ to $(1111)_2$. This is shown below.



Subtraction of Larger Number from Smaller Number:

To subtract a larger number from a smaller number using 2's complement subtraction, following steps are to be followed:

Step-1: Determine the 2's complement of the smaller number

Step-2: Add this to the larger number.

Step-3: There is no carry in this case. The result is in 2's complement form and is negative.

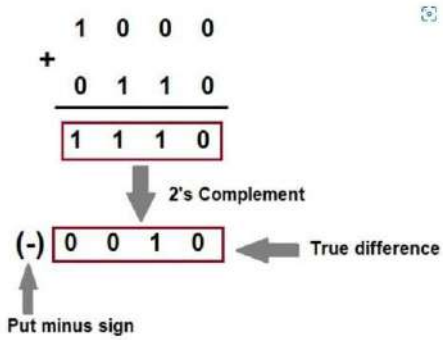
Step-4: To get answer in true form, take 2's complement and change its sign.

Example-2: Subtract $(1010)_2$ from $(1000)_2$ using 2's complement.

Solution:

Step-1: Find the 2's complement of $(1010)_2$. It is $(0110)_2$.

Step-2: Add $(0110)_2$ to $(1000)_2$



9's Complement

For 9's complement , subtract each digit of the given decimal number from 9.

Find 9's complement of 456

9 9 9

4 5 6 (-)

-.....

5 4 3

Ans :543

10's Complement

Add 1 with the **9's complement** of the number to obtain the desired 10's complement

Find 10's Complement of 456

9's complement of 456 = 5 4 3

1(+)

.....-

5 4 4

Ans : 544

Given the two binary numbers X=1010100 and Y= 1000011, perform the subtraction Y-X by using 2's complements.

a) X = 1010100

2's complement of Y = + 0111101

Sum = 10010001

Discard end carry

X -Y = 0010001

b) Y = 1000011

2's complement of X = + 0101100

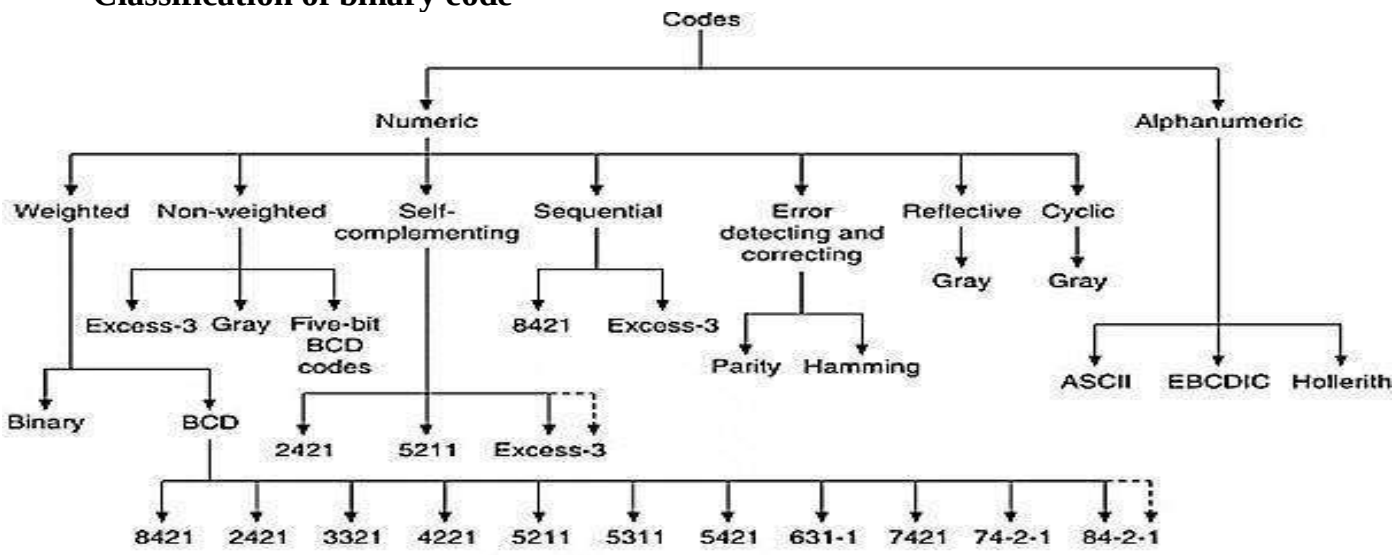
Sum = 1101111

There is no end carry,

Therefore, the answer is Y-X = - (2's complement of 1101111)

= -0010001

Classification of binary code



Weighted codes:

- In weighted codes, each digit is assigned a specific weight according to its position.
- For example, in 8421 BCD code, 1001 the weights of 1, 0, 0, 1 (from left to right) are 8, 4, 2 and 1 respectively.
- The codes 8421 BCD, 2421 BCD, 5211 BCD are all weighted codes

Non-weighted codes:

- The non-weighted codes are not positional weighted.
- In other words, each digit position within the number is not assigned a fixed value (or weight).
- Excess-3 and gray code are non-weighted codes.

Reflective codes:

- A code is reflective when the code is self-complementing.
- In other words, when the code for 9 is the complement of 0, 8 for 1, 7 for 2, 6 for 3 and 5 for 4.
- 2421BCD, 5421BCD and Excess-3 code are reflective codes.

Decimal	Binary 8 4 2 1	Excess - 3	Gray Code
0	0 0 0 0	0 0 1 1	0 0 0 0
1	0 0 0 1	0 1 0 0	0 0 0 1
2	0 0 1 0	0 1 0 1	0 0 1 1
3	0 0 1 1	0 1 1 0	0 0 1 0
4	0 1 0 0	0 1 1 1	0 1 1 0
5	0 1 0 1	1 0 0 0	0 1 1 1
6	0 1 1 0	1 0 0 1	1 0 1 0
7	0 1 1 1	1 0 1 0	0 1 0 0
8	1 0 0 0	1 0 1 1	1 1 0 0
9	1 0 0 1	1 1 0 0	1 1 0 1
10	1 0 1 0	1 1 0 1	1 1 1 1
11	1 0 1 1	1 1 1 0	
12	1 1 0 0	1 1 1 1	
13	1 1 0 1		
14	1 1 1 0		
15	1 1 1 1		

Error detecting and correcting codes:

- Codes which allow error detection and correction are called error detecting and correcting codes.
- Parity code is used to detect error. The two types of parity are even parity (even number of 1) and odd parity (odd number of 1).
- Hamming code is the most commonly used error detecting and correcting code.

Sequential Code:

A code is said to be sequential when each succeeding code is one binary number greater than its preceding code. Example:8421 code, Excess 3 code

Grey Code :

Grey Code is a special case of unit distance code i.e. bit pattern of 2 consecutive number differ in only one pit position. These codes are also called cyclic code.

Alphanumeric Code :

The code which consist of numbers and alphabetic character are called alphanumeric code.
Example:American Standard code for information exchange (ASCII code)
Extended Binary Coded Decimal Information Code (EBCDIC)

Problems in Hamming code

1. Deduce the odd parity hamming code for the data: 1010. Introduce an error in the LSB of the hamming code and deduce the steps to detect the error.

Step 1: Identify number of parity bit

$2^p \geq d+p+1$

Where d = number of data bit

P= number of parity bit

For d=4

Let us assume p=3

$2^3 \geq 4+3+1$

As the condition satisfies , number of parity bit required is 3

Step 2: construct bit location table

Bit Designation	P1	P2	D1	P3	D2	D3	D4
Bit position	1	2	3	4	5	6	7
Bit position number	001	010	011	100	101	110	111
Data Bit			1		0	1	0

P_1 checks bits positions 1, 3, 5 and 7 $=P_1,1,0,0$

For odd parity $P_1=0$

P_2 checks bits positions 2,3, 6 and 7 $=P_2,1,1,0$

For odd parity $P_2=1$

P_3 checks bits positions 4,5, 6 and 7 = P_3, 0,1,0

For odd Parity $P_3=0$

Bit Designation	P1	P2	D1	P3	D2	D3	D4
Bit position	1	2	3	4	5	6	7
Bit position number	001	010	011	100	101	110	111
Data Bit			1		0	1	0
Parity Bit	0	1		0			

Hamming code = 0110010

2. A 12 bit hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8 bit data word that was written into memory if the 12 bit word read out is as

(a) 101110010100 (b) 111111110100.

(a) 101110010100

Step 1:Construct bit location table

Bit Designation	P1	P2	D1	P3	D2	D3	D4	P4	D5	D6	D7	D8
Bit position	1	2	3	4	5	6	7	8	9	10	11	12
Bit position number	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100
Received Code	1	0	1	1	1	0	0	1	0	1	0	0

Step 2: Check for even parity bits

For P1:

P1 checks locations 1, 3, 5, 7, 9 ,11 = 1,1,1,0,0,0

There are three 1s in the group

Hence Parity check for even parity is wrong… .....1 (LSB)

For P2:

P2 checks locations 2,3, 6 ,7 ,10 =0,1,0,0,1

There are two 1s in the group

Hence Parity check for even parity is correct… 0

For P4:

P4 checks locations 4, 5, 6, 7, 12 = 1,1,0,0,0

There are two 1s in the group

Hence Parity check for even parity is correct… 0

For P8:

P8 checks locations 8, 9, 10, 11, 12 = 1,0,1,0,0

There are two1s in the group

Hence Parity check for even parity is correct.....0 (MSB)

The resultant word is 0001

The bit position 1 in the error. The corrected code is 001110010100.

Actual data transmitted :11000100.

(2) Received 12 bit code : 111111110100

Step 1:Construct bit location table

Bit Designation	P1	P2	D1	P3	D2	D3	D4	P4	D5	D6	D7	D8
Bit position	1	2	3	4	5	6	7	8	9	10	11	12
Bit position number	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100
Received Code	1	1	1	1	1	1	1	1	0	1	0	0

Step 2: Check for even parity bits

For P1:

P1 checks locations 1, 3, 5, 7, 9 ,11 = 1,1,1,1,0,0

There are four 1s in the group

Hence Parity check for even parity is correct.....0 (LSB)

For P2:

P2 checks locations 2,3, 6 ,7 ,10 =1,1,1,1,1

There are five 1s in the group

Hence Parity check for even parity is wrong.....1

For P3:

P3 checks locations 4, 5, 6, 7, 12 = 1,1,1,1,0

There are four 1s in the group

Hence Parity check for even parity is correct… 0

For P4:

P4 checks locations 8, 9, 10, 11, 12 = 1,0,1,0,0

There are two1s in the group

Hence Parity check for even parity is correct .....0 (MSB)

The resultant word is 0010

The bit position 2 in the error. The corrected code is **101111110100**

Actual data transmitted :11110100

BCD ADDITION - RULES

Add the two numbers using the rules for binary addition.

If the four bit sum is equal to or less than 9 (1001)2 it is a valid BCD Number.

If the four bit sum is greater than 9 (1001)2 , it is a invalid BCD Number. Add 6 (0110)2 to the four bit sum in order to make a valid BCD number. If a carry results when 6 is added , add the carry to the next four bit group.

Problem 1 : Add 4+5 Using BCD Addition

BCD equivalent of 4 = 0100

BCD equivalent of 5 = 0101

```
    1
    0  1  0  0
+   0  1  0  1
-------------
    1  0  0  1
```

Answer = 1001

Problem 2: Add 4+8 using BCD Addition

BCD equivalent of 4 = 0100

BCD equivalent of 8 = 1000

```
    0  1  0  0
+   1  0  0  0
-------------
    1  1  0  0
```

But 1100 is not a valid BCD Code, because 1100 >9 .

To convert it into a valid BCD Code ,add 0110 to the number

```
       1
    1  1  0  0
    0  1  1  0
-------------
 1  0  0  1  0
```

Answer: 0001 0010

BCD Subtraction

Subtraction of smaller number from larger number

- Find 1's Complement of smaller number
- Add it with the larger number
- Remove the carry and add it to the result
- Add 1010 if end-around carry is 1
- Ignore the intermediate carry

Subtraction of smaller number from larger number

- Find 1's Complement of larger number
- Add it with the smaller number
- Remove the carry and add it to the result. Find I 's Complement of it
- Add 1010 if end-around carry is 1
- Ignore the intermediate carry and provide a negative sign

Subtract 274 from 835 using BCD subtraction

BCD code for 835 =1000 0011 0101

BCD code for 274 =0010 0111 0100

Step1 :1's Complement of 274 =1101 1000 1011

Step 2: Add 1's complement with larger number

						1	1	1	1	1	1		
	1	1	0	1	1	0	0	0	1	0	1	1	
	1	0	0	0	0	0	1	1	0	1	0	1	+
1	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	

Add carry 1 to the result

	0	1	0	1	1	1	0	0	0	0	0	0	
												1	+
	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	

Add 1010 if end around carry is present

				Ignore intermediate Carry 1									
	0	1	0	1	1	1	0	0	0	0	0	1	
	0	0	0	0	1	0	1	0	0	0	0	0	+
	0	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	

Answer = 0101 0110 0001

Excess 3 Addition

Problem : Add 205 and 569 using Excess 3 addition

Excess 3 code of 205 = 0101 0011 1000

Excess 3 code of 569 =1000 1001 1100 (+)

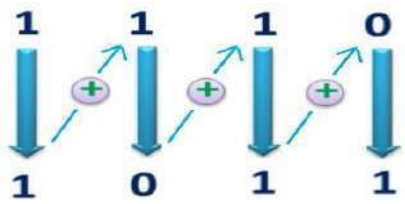
1101 1101 0100

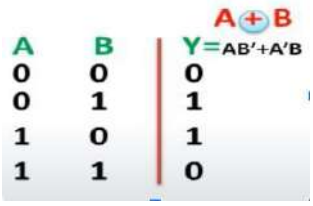
Now add 0011 to the group which produce the carry and subtract 0011 from group which do not produce carry

	1	1	0	1		1	1	0	1		0	1	0	0
-	0	0	1	1	-	0	0	1	1	+	0	0	1	1
	1	0	1	0		1	0	1	0		0	1	1	1

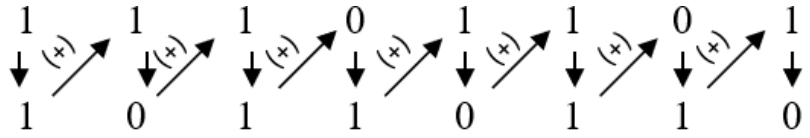
Answer =1010 1010 0111

Convert the gray code 1110 to binary form



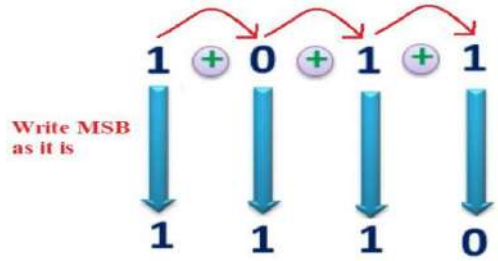


Convert the gray code 11101101 to binary form



$(11101101)_{gray} = (10110110)_2$

Convert the binary number 1011 into gray code



Convert the following Excess 3 numbers into decimal numbers.

a)1011 **b)1001 0011 0111**

a) 1011

\- 0011

1000 = $(8)_{10}$

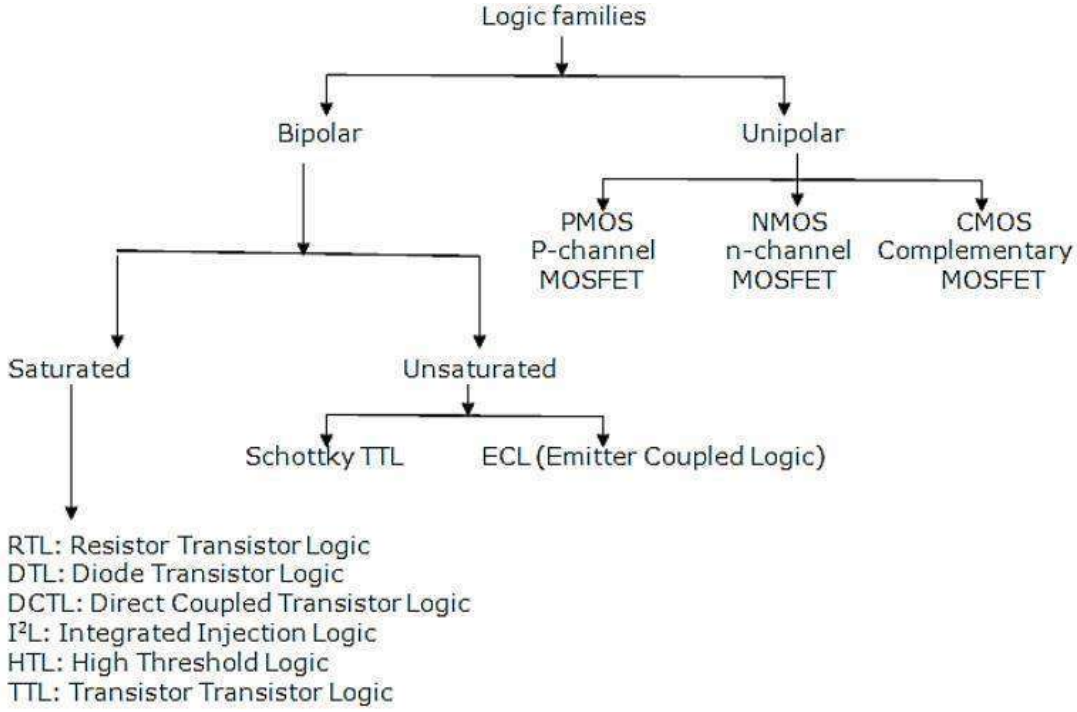
b) 1001 0011 0111

\- 0011 0011 0011

0100 0000 0100 = $(404)_{10}$

DIGITAL LOGIC FAMILIES

A digital logic family is a group of compatible devices with the same logic levels and supply voltages. According to components used in the logic family, digital logic families are classified as shown in the figure. Of the above the most widely used Logic families are TTL, CMOS and ECL, due to their characteristics matching the hardware requirements.



RTL logic families

- In this logic family of ICs, the series of resistors are added to each transistor.
- By reducing the current – hogging effect with resistors, a larger fan-out is achieved. But due to the resistor's presence, the speed of the circuit will be always slow.

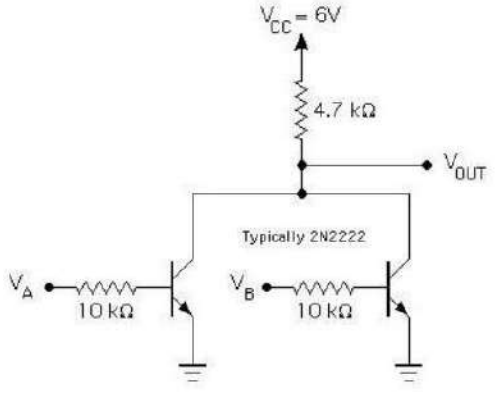


Fig. RTL NOR gate circuit

RTL working:

- When inputs A, B are '0', the transistors Q1 and Q2 are OFF. Thus the node C is not connected to ground and the Vcc will appear at node C s output which is logic '1'.
- When any one inputs either A or B is '1' or if both A and B are '1' Q1 or Q2 or both the transistors will be in saturated mode. Thus the node C will be connected to ground making the output C as 0V or Logic LOW for all the remaining three conditions.

If more number of resistors are included in the logic circuit, then the input resistance gets increased and switching speed will decrease. An alternate approach to increase the switching speed in RTL is to add a capacitor parallel to the resistor in the input of the transistor's base.

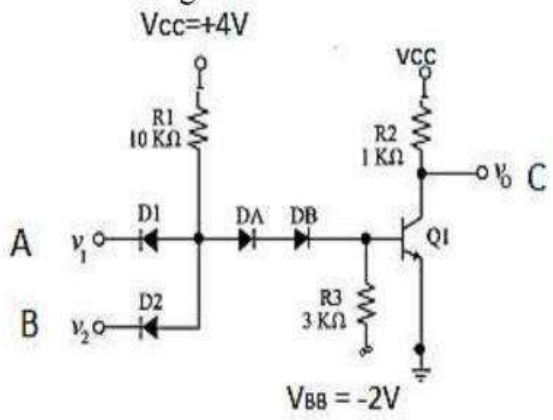
- Another problem is the transistors go to saturation causing longer turn off delay (i.e.,) it takes more time for the output to become 1 to 0. Integrated Injection Logic (IIL) can eliminate all the problems of the RTL circuit

Characteristics of RTL logic circuit:

1. Speed of operation is low. The propagation delay is in the order of 500ns. It cannot operate at speeds above 4MHz.
2. Fan out is 4 or 5 with a switching delay of 50ns and fan in is 4.
3. Poor noise immunity.
4. High average power dissipation due to resistors.
5. The noise margin from zero to the threshold voltage is about 0.5V and from one to the threshold voltage is 0.2V.
6. Sensitive to temperature.

Explain the working of DTL logic families.

The formation of NOT gate using Diode Logic is difficult and requires two voltage levels to represent logic HIGH and LOW. To avoid this, transistor inverter is combined with diodes to form NAND and NOR gates.



A	B	Output =C
0	0	1
0	1	1
1	0	1
1	1	0

The DTL circuit combines the diode AND gate and the bipolar transistor inverter into a NAND gate. The AND function is performed by two diodes with a resistor for pull up and NOT function is formed by the transistor inverter circuit.

- When A=0, B=0, the node X has 0V. This 0V is given as an input to the transistor Q1. The transistor will be in cut off condition only. Node C will have +5V (HIGH).
- Similarly if any one input is 0, or both A and B are 0, then the node X will be grounded. Thus there is no base current. The transistor will be in cut off condition. Therefore the node C will have +5V (HIGH).
- But for the inputs A=1, B=1, A and B are give +5V. Now the node X will have +5V (since both diodes do not conduct). This voltage is given to the transistor's base with a drop by R2.Now the transistor conducts. The output of the NAND gate is LOW. The node C is grounded.

Characteristics of DTL:

- The turnoff delay is larger than turn on delay often by a factor of 2 or 3.The propagation delay is 25ns.
- Fan out of 8 is possible because of high input impedance.
- It has fan-in of 8
- Noise margin is high

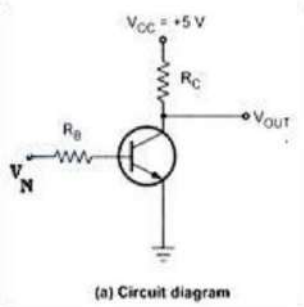
Transistor -Transistor Logic (TTL):

• Transistor Transistor logic, TTL, is named for its dependence on transistor alone for the basic operations. The subfamily circuits along with their characteristics of TTL are discussed below. They are

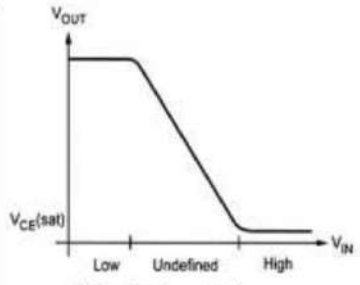
- TTL inverter
- TTL 2-input NAND gate
- TTL 3-input NAND gate
- Totem-pole output
- Open collector output

TTL Inverter

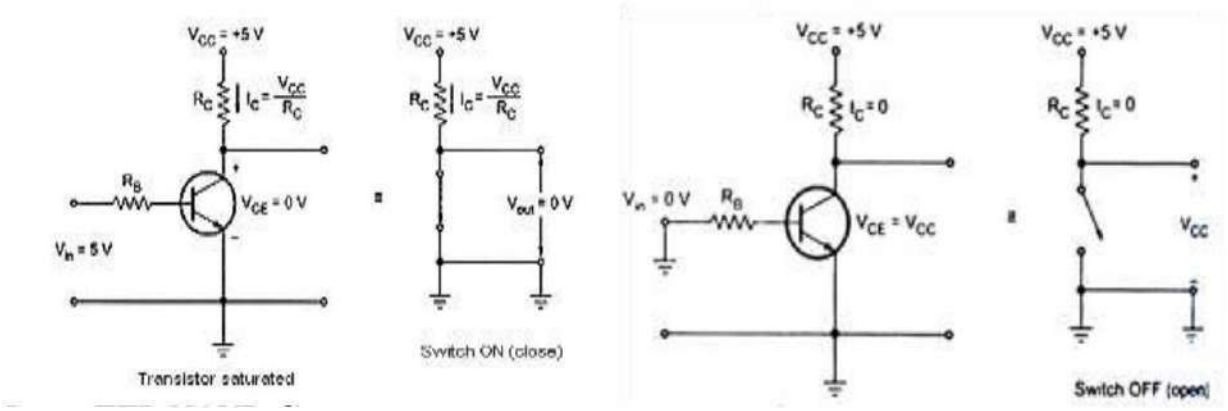
• The operation of transistor inverter for both the input (HIGH and LOW) using switching analogy is shown below.



(a) Circuit diagram

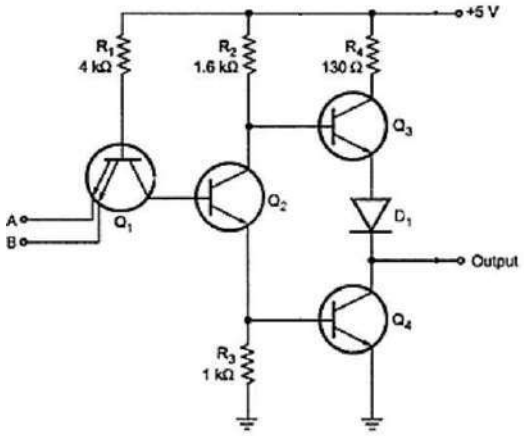


(b) Transfer characteristics

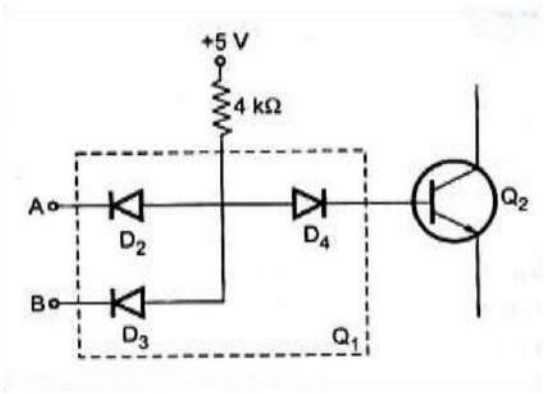


2-Input TTL NAND Gates

- The circuit diagram of 2-input TTL NAND Gate is as shown in figure.
- Its input structure consists of multiple-emitter transistor and output structure consists of totem-pole output.
- Q1 is an NPN transistor having two emitters, one for each input to the gate. we can simplify its analysis by using the diode equivalent of the multiple-emitter transistor Q1.



2-input TTL NAND gate



Diode equivalent for Q_1

The diodes D2 and D3 represents the two E-B junction of Q1 and D4 is the collector-base(CB) junction.

- The input voltages A and B are either LOW (ideally grounded) or HIGH (ideally +5 volts).
- If either A and B or both are low, the corresponding diode conducts and the base of Q1 is pulled to approximately 0.7V. This reduces the base voltage of Q2 to atmost zero. Therefore, Q2 cuts off. With Q2 open, Q4 goes into cut-off and the Q3 Base is pulled HIGH. Since Q3 acts as an emitter follower, the Y output is pulled up to a HIGH voltage.
- On the other hand, when A and B both are HIGH, the emitter diode of Q1 is reverse biased making them off. This causes the collector diode D4 to get in to forward conduction.

This forces Q2 base to go HIGH. In turn, Q4 goes into saturation, producing a low output in all input and output conditions.

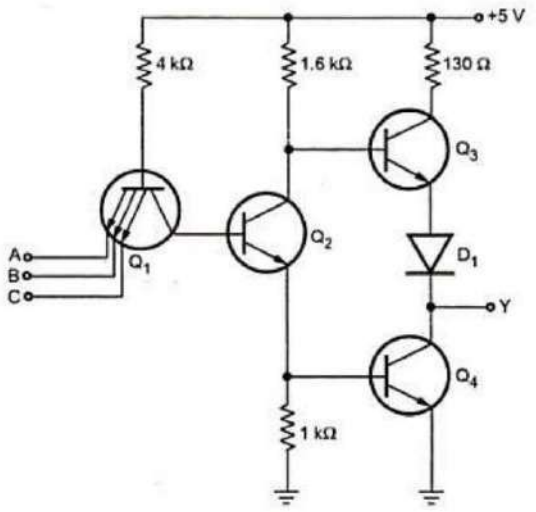
- Without diode D1 in the circuit, Q3 will conduct slightly when the output is low.
- To prevent this, the diode is inserted. Its voltage drops keeps the base-emitter diode of Q3 reverse biased. In this way, only Q4 conducts when the output is low.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth table for 2-input NAND gate

3-Input TTL NAND Gate:

- The three inputs TTL NAND Gate is same as that of two input TTL NAND Gate except that its Q1 (NPN) transistor has three emitters instead of two. Rest of the circuit is same.
- For three input NAND gate if all the inputs are logic 1 then only output is logic 0; otherwise output is logic 1. The operation is similar to the 2-input NAND gate.



Three input TTL NAND gate

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth table of 3 input NAND gate

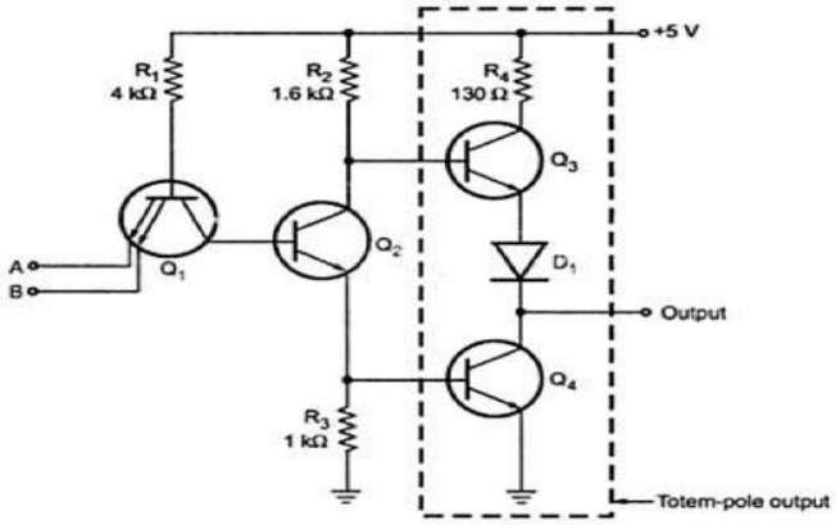
Two input TTL NAND gate with totem-pole ouput:

In the TTL circuit, transistors Q3 and Q4 form a totem-pole. Such a configuration is known as active pull-up or totem pole output.

- The active pull-up formed by Q3 and Q4 has a specific advantage. Totem-pole transistors are used because they produce LOW output impedance.
- Either Q3 acts an emitter follower (HIGH output) or Q4 is saturated (LOW output).
- When Q3 is conducting, the output impedance is approximately 70Ω. When Q4 is

saturated, the output impedance is only 12Ω. Either way, the output impedance is low.

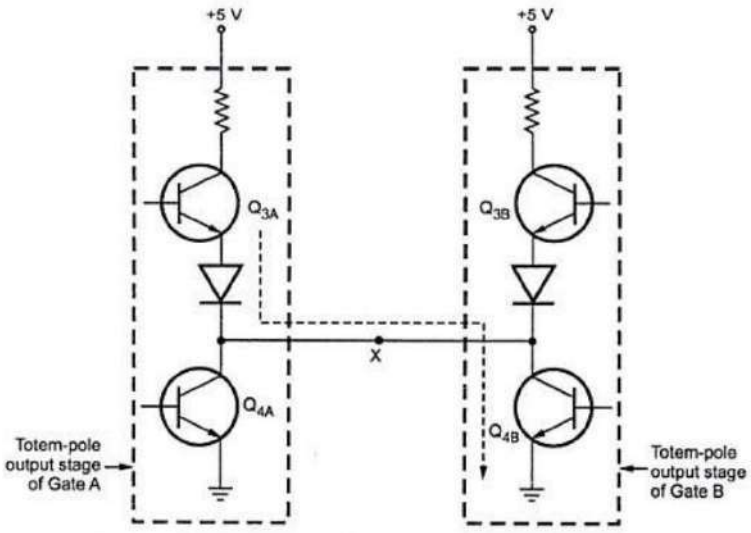
• This means that the output voltage can change quickly from one state to another because any stray output capacitance is rapidly charged or discharged through the low output impedance. Thus the propagation delay is low in totem-pole TTL logic



Two input NAND gate with totem-pole output

TTL with open collector output configuration.

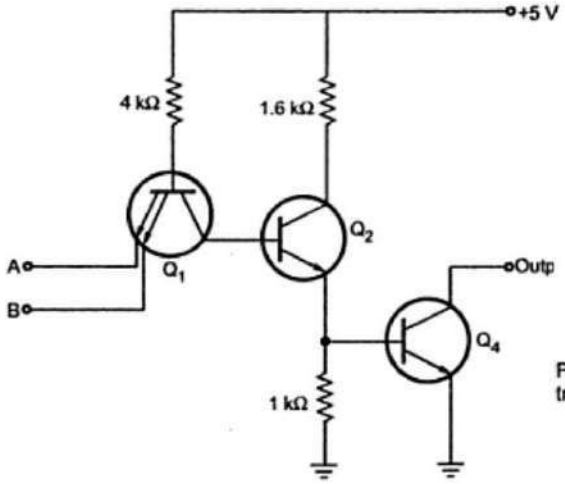
One problem with totem-pole output is that two outputs cannot be tied together, as shown in below figure, where the totem pole outputs of two separate gates are connected together at point X.



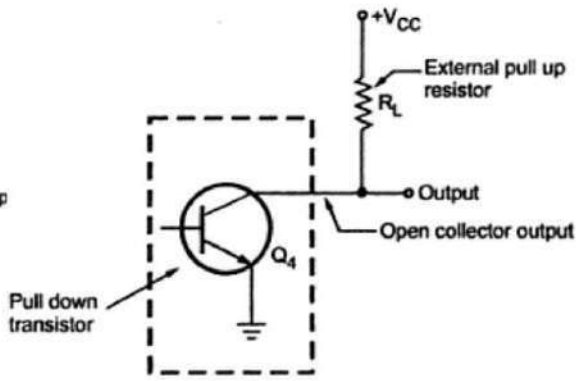
Totem-pole outputs tied together can produce harmful current

When the output of gate A is high (Q_{3A} ON and OFF) and the output of gate B is LOW (Q_{3B} OFF and Q_{4B} ON). In this situation transistor Q_{4B} act as a load for Q_{3A}.

- Since Q_{4B} is a low resistance load, it draws high current around 55mA.
- This current might not damage Q_{3A} or Q_{4B} immediately, but over a period of time it cause overheating and deterioration in performance and eventually device failure.
- Some TTL devices provide another type of output called open collector output.
- The output of two different gates with open collector output can be tied together.This is known as wired logic.
- A 2-input NAND gate with an open-collector output eliminates the pull-up transistor Q3, D1 and R4.
- The output is taken from the open collector terminal of transistor Q4.
- Totem pole o/p tied together can produce harmful current.



Open collector 2-input TTL NAND ga



Open collector output with pull-up resistor

Because the collector of Q4 is open, a gate like this will not work properly until you connect an pull-up resistor.

- When Q4 is OFF output is tied to Vcc through an external pull up resistor. The open collector output of two or more gates can be connected together, as connection is called a wired-AND and represented schematically by the special AND gate symbol.

Compare the Totem pole and open collector outputs.

Sl.No.	Totem Pole	Open Collector
1.	Output stage consists of pull up transistor (Q_4), diode resistor and pull down transistor (Q_5).	Output stage consists of only pull down transistor.
2.	External pull up resistor is not required.	External pull up resistor is not required for proper operation of gate.
3.	Output of two gates cannot be tied together.	Output of two gates can be tied together using Wired AND technique.
4.	Operating speed is high.	Operating speed is low.

CMOS logic circuit configuration and characteristics

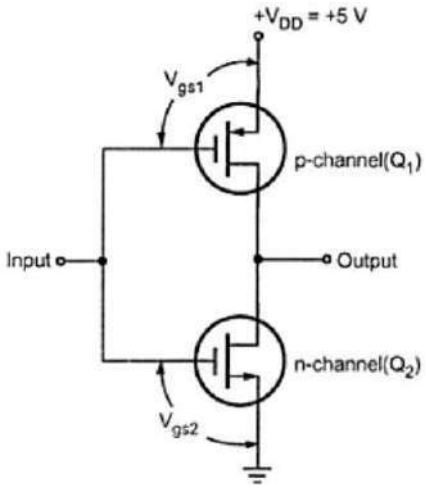
Digital circuit with MOSFETs can be grouped into three categories:

- PMOS - Uses only P-channel enhancement MOSFETs,
- NMOS - Uses only N-channel enhancement MOSFETs, and
- CMOS (Complementary MOS) – Uses both P and N-channel devices.
- PMOS and NMOS digital ICs are economical than CMOS ICs because they have greater packing density than CMOS.
- NMOS has twice the packing density than PMOS. Furthermore, NMOS can operate at about three times faster than their PMOS counterparts.
- This is because NMOS has faster moving current carriers (holes). CMOS has the greatest complexity and lowest packaging density. However, it has advantages of high speed and much lower dissipation. NMOS and CMOS are widely used in the digital ICs, but PMOS are no longer part of new designs.

CMOS circuit contains both NMOS and PMOS devices to speed the switching of capacitive loads. It consumes low power and can operate at high voltages, resulting in improved noise immunity.

CMOS Inverter:

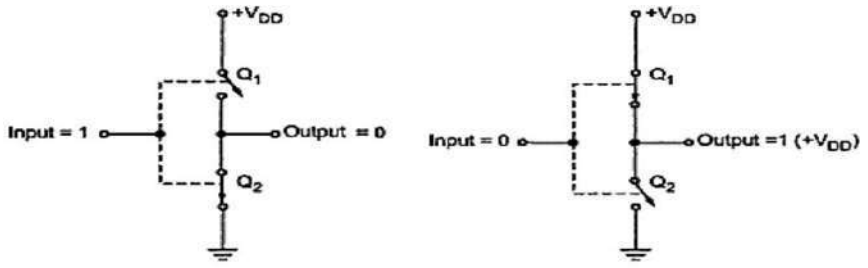
- It consists of two MOSFET's in series in such a way that the p-channel device has its source connected to +VDD and the n-channel device has its source connected to ground.



CMOS inverter circuit

- The gates of the two devices are connected together as the common input and the drains are connected together as the common output. 1. When input is HIGH, the gate of Q1 (p=channel) is at 0 V relative to the source of Q1 i.e. Vgs1 = 0 V. Thus Q1 is OFF. On the other hand, the gate of Q2 (n-channel) as at +VDD relative to its source i.e. Vgs2 = +VDD.

Thus, Q2 is ON. This will produce VOUT = 0 V as in figure a.
When input is LOW, the gate of Q1 (p=channel) is at negative potential relative to its source while Q2 has Vgs = 0 V. Thus Q1 is ON and Q2 is OFF. This produces output voltage approximately +VDD in figure.



(a) Input = 1 **(b) Input = 0**

Operation of CMOS inverter for both input conditions

Truth Table

A	Q1	Q2	Output
0	ON	OFF	1
1	OFF	ON	0

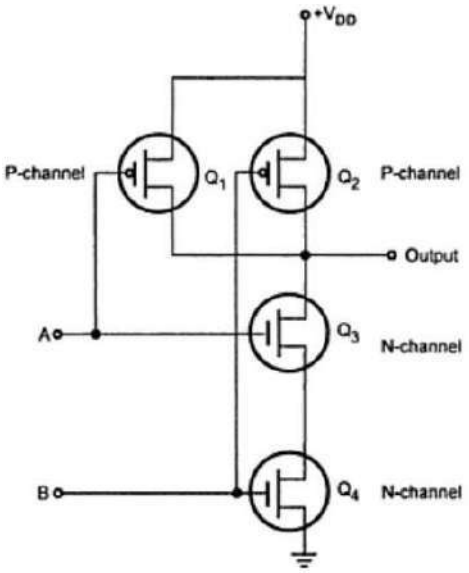
CMOS NAND Gate :

It consists of two p-channel MOSFET's Q1 and Q2, connected in parallel and two n-channel MOSFET's Q3 and Q4 connected in series.

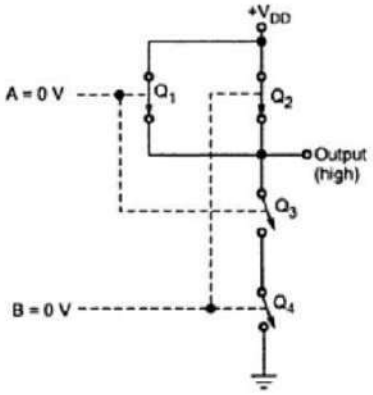
1. When both the inputs are low, the gates of both p-channel MOSFET's are negative with respect to their source, since the sources are connected to +VDD. Thus Q1 and Q2 are both ON. Since the gateto-source voltages of Q3 and Q4 (n-channel MOSFETs) are both 0 V, those MOSFET's are OFF. The output is therefore connected to +VDD (HIGH) through Q1 and Q2 and is disconnected from ground, as shown in fig(b).
2. When A=0 and B=+VDD, Q1 is ON because Vgs1=-VDD and Q4 is ON because Vgs4=+VDD. MOSFET's Q2 and Q3 are OFF because their gate-to-source voltages are 0 V. Since Q1 is ON and Q3 is OFF, the output is connected to +VDD and it is disconnected from ground. Output is HIGH.
3. When A=+VDD and B=0, Q1 is OFF because Vgs1=+VDD and Q4 is OFF because Vgs4=-VDD. MOSFET's Q2 and Q3 are ON because their gate-to-source voltage is +VDD. Since Q2 and Q3 are ON, the output is connected to +VDD and it is disconnected from ground. Output is HIGH.
4. Finally, when both inputs are HIGH, Q1 and Q2 are both OFF and Q3 and Q4 are both ON, therefore the output is connected to ground and is LOW.

Note:

- P-channel MOSFET is ON when its gate voltage is negative with respect to its source
- N-channel MOSFET is ON when its gate voltage is positive with respect to its source.



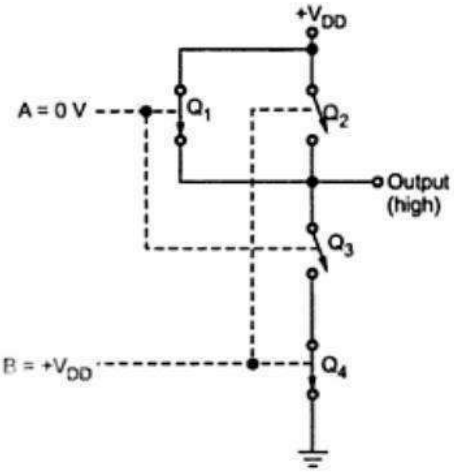
(a) Schematic



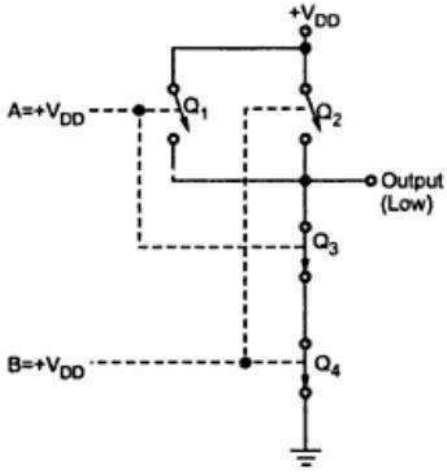
(b) A = B = 0 V
$V_{GS1} = V_{GS2} = -V_{DD}$
$V_{GS3} = V_{GS4} = 0$ V

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Truth table for CMOS NAND gate



(c) A = 0 V, B = $+V_{DD}$
$V_{GS1} = -V_{DD}$
$V_{GS2} = V_{GS3} = 0$ V
$V_{GS4} = +V_{DD}$

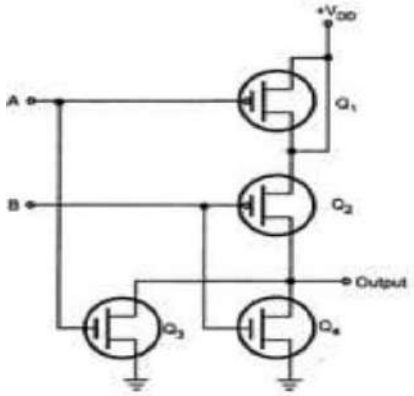


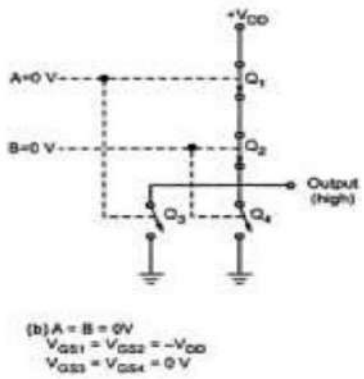
(d) A = B = $+V_{DD}$
$V_{GS1} = V_{GS2} = 0$ V
$V_{GS3} = V_{GS4} = +V_{DD}$

CMOS NAND gate

CMOS NOR Gate:

Below figure shows 2-input CMOS NOR gate. The p-channel MOSFET's Q1 and Q2 are connected in series and n-channel MOSFET's Q3 and Q4 are connected in parallel. Like NAND circuit, this circuit can be analyzed by realizing that a LOW at any input turns ON its corresponding p-channel MOSFET and turns OFF its corresponding n-channel MOSFET, and vice versa for a HIGH input.

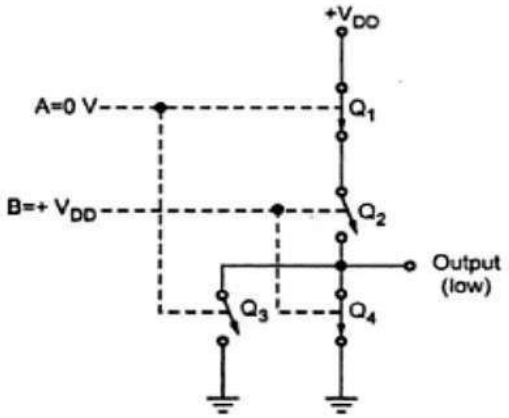


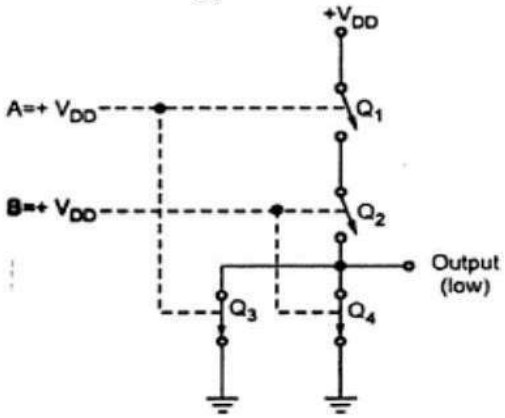


(b) A = B = 0V
$V_{GS1} = V_{GS2} = -V_{DD}$
$V_{GS3} = V_{GS4} = 0$ V

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

Truth table for CMOS NOR gate





(c) A = 0V, B = $+V_{DD}$
$V_{GS1} = -V_{DD}$
$V_{GS2} = V_{GS3} = 0$ V
$V_{GS4} = +V_{DD}$

(d) A = B = $+V_{DD}$
$V_{GS1} = V_{GS2} = 0$ V
$V_{GS3} = V_{GS4} = +V_{DD}$

CMOS NOR gate

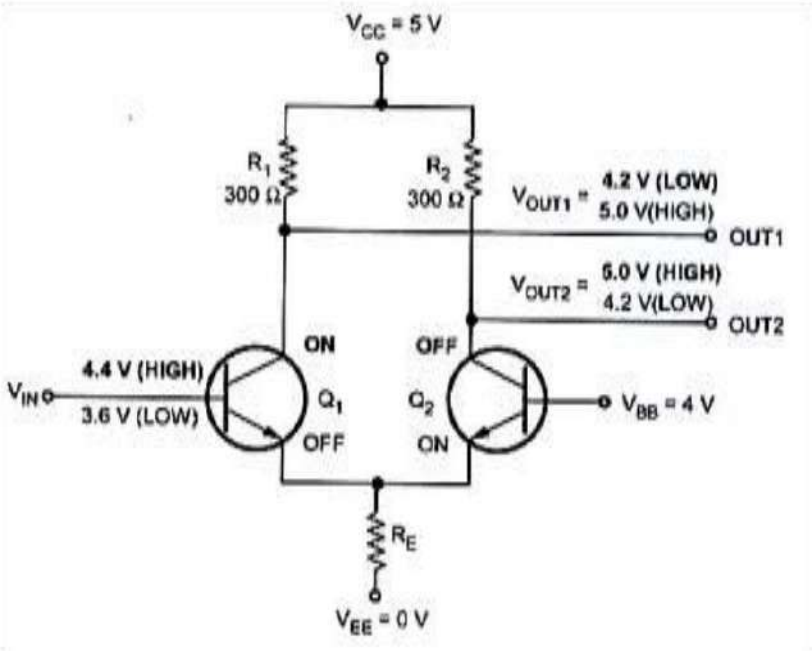
Characteristics of CMOS family:

- Operating Speed: Slower than TTL series. Approximately 25 to 100ns depending on the subfamily of CMOS. It also depends on the power supply voltage.
- Voltage levels and noise margins: The voltage level for CMOS varies according to their subfamilies. Noise margin are calculated as follow. $V_{NH} = V_{OH\,(MIN)} - V_{IH\,(MIN)}$
$V_{NL} = VIL_{\,(MAX)} - V_{OL\,(MAX)}$
- Fan-out: The CMOS inputs have an extremely large resistance ($10^{12}\Omega$) that draws essentially no current from the signal source. Each CMOS input, however, typically present a 5 pF load to ground .This input capacitance limits the number of CMOS inputs that one CMOS output can drive.
- The CMOS output has to charge and discharge the parallel combination of all the input capacitances. This charging and discharging time increases as we increase number of loads.
- Typically, each CMOS load increases the driving circuit's propagation delay by 3ns.

Thus, fan-out for CMOS depends on the permissible maximum propagation delay.
Typically, CMOS outputs are limited to a fan-out of 50 for low-frequency operation

ECL Circuit

The TTL family uses transistors operating in saturation mode due to which their switching speed is limited .Emitter Coupled logic overcomes this problem. It doesnot produce a large voltage swing between low and high levels.
The basic inverter/buffer circuit in ECL family consists of two transistor connected in differential single ended input mode with a common emitter resistance.

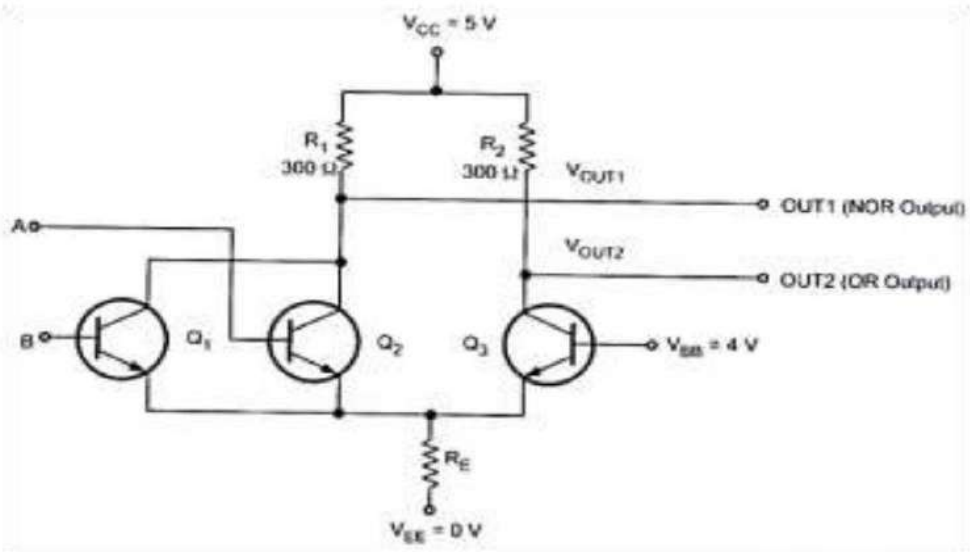


The circuit has two outputs: inverting output (OUT1) and non-inverting output (OUT2). For this circuit, the input LOW and HIGH voltage levels are defined as 3.6 V and 4.4 V, and it produces output LOW and HIGH levels as 4.2 V and 5.0 V.

- When V_{IN} is HIGH (4.4V), transistor Q1 is ON, but not saturated and transistor Q2 is OFF. Thus V_{OUT2} is pulled to 5.0V (HIGH) through R2 and drop across R1 is 0.8 V so that V_{OUT1}.
- When V_{IN} is LOW (3.6V), transistor Q2 is ON, but not saturated and transistor Q1 is OFF. Thus, V_{OUT1} is pulled to 5.0V (HIGH) through R1 and drop across R2 is 0.8 V so that V_{OUT2} is 4.2 V (LOW).

ECL OR/NOR Gate

- The 2-input ECL OR/NOR gate and it logic symbol. There has an additional transistor in parallel with Q1 as compared to ECL inverter.
- If any input is HIGH corresponding transistor is active, and V_{OUT1} is LOW (NOR output).At the same time Q3 is off producing V_{OUT2} HIGH (OR output).



Characteristics of ECL :

- It is the fastest of all logic families
- Transistors are not allowed to go into complete saturation, thus eliminating storage delays.
- Logic levels are chosen close to each others, to prevent transistors from going into saturation.
- Noise margin is reduced, hence difficult to achieve good noise immunity
- Power consumption is more because transistors are not completely saturated
- Switching transients is less because power supply current is more stable than TTL and CMOS

Compare the characteristics of TTL, ECL and CMOS logic families

S.No:	Parameter	CMOS	TTL	ECL
1	Device used	n-channel and p-channel MOSFET	Bipolar junction transistor	Bipolar junction transistor
2	$V_{IH(min)}$	3.5 V	2 V	-1.2 V
3	$V_{Il(max)}$	1.5 V	0.8 V	-1.4 V
4	$V_{OH(min)}$	4.95 V	2.7 V	-0.9 V
5	$V_{OL(max)}$	0.005 V	0.4 V	-1.7 V
6	High level noise margin	V_{NH}=1.45 V	0.4 V	0.3 V
7	Low level noise margin	V_{NL}=1.45 V	0.4 V	0.3 V
8	Noise immunity	Better than TTL	Less than CMOS	More vulnerable to noise
9	Propagation delay	70 ns	10 ns	500 ps
10	Switching speed	Less than TTL	Faster than CMOS	Fastest
11	Power dissipation per gate	0.1 mW	10 mW	25 mW
12	Speed power product	0.7 pJ	100 pJ	0.5 pJ
13	Fan-out	50	10	25
14	Power supply voltage	3-15 V	Fixed 5 V	-4.5 to 5.2 V
15	Power dissipation	Increase with frequency	Increase with frequency	Constant with frequency
16	Application	Portable instrument where battery supply is used.	Laboratory instruments	High speed instruments.

UNIT II COMBINATIONAL CIRCUITS

Combinational logic - representation of logic functions-SOP and POS forms, K-map representations - minimization using K maps - simplification and implementation of combinational logic – multiplexers and de multiplexers - code converters, adders, subtractors, Encoders and Decoders.

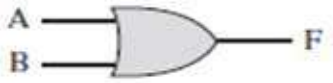
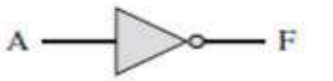
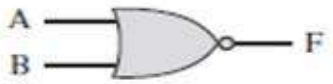
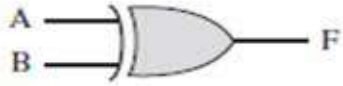
Boolean Algebra:

Boolean Algebra is an algebra, which deals with binary numbers & binary variables. Hence, it is also called as Binary Algebra or logical Algebra. A mathematician, named George Boole had developed this algebra in 1854. The variables used in this algebra are also called as Boolean variables.

The range of voltages corresponding to Logic 'High' is represented with '1' and the range of voltages corresponding to logic 'Low' is represented with '0'.

Types of Basic Logic Gates:

The basic gates, their symbol and their corresponding truth table is given below.

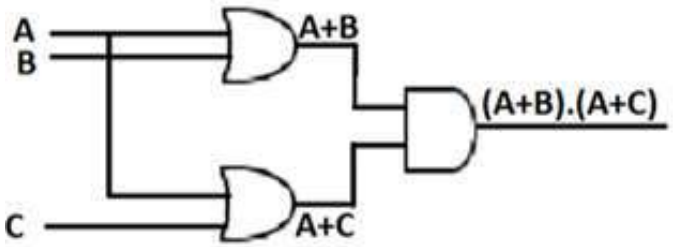
Name	Graphical Symbol	Algebraic Function	Truth Table
AND		$F = A \cdot B$ or $F = AB$	A B | F 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1
OR		$F = A + B$	A B | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1
NOT		$F = \overline{A}$ or $F = A'$	A | F 0 | 1 1 | 0
NAND		$F = \overline{AB}$	A B | F 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0
NOR		$F = \overline{A + B}$	A B | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0
XOR		$F = A \oplus B$	A B | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0

Boolean Expressions:

Give the truth table and draw the logic diagram of the given expressions:

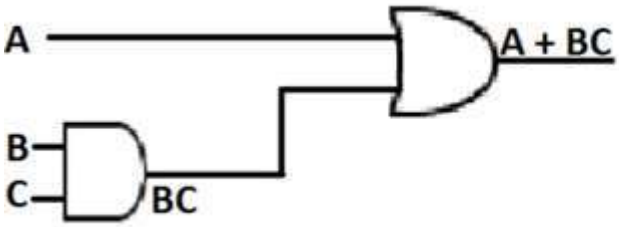
(i) F= (A+B)(A+C) (ii) F=A+BC

$(\boldsymbol{i}).\boldsymbol{F} = (\boldsymbol{A}+\boldsymbol{B})(\boldsymbol{A}+\boldsymbol{C})$



A	B	C	A+B	A+C	(A+B).(A+C)
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	1	1
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1

$(\boldsymbol{ii}).\boldsymbol{F} = \boldsymbol{A} + \boldsymbol{BC}$



A	B	C	BC	A + BC
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Postulates and Basic Laws of Boolean Algebra:

In this section, let us discuss about the Boolean postulates and basic laws that are used in Boolean algebra. These are useful in minimizing Boolean functions.

Boolean Postulates

Consider the binary numbers 0 and 1, Boolean variable xx and its complement x′x′. Either the Boolean variable or complement of it is known as **literal**. The four possible **logical OR** operations among these literals and binary numbers are shown below.

$$x + 0 = x$$

$$x + 1 = 1$$

$$x + x = x$$

$$x + x' = 1$$

Similarly, the four possible **logical AND** operations among those literals and binary numbers are shown below.

$$x.1 = x$$

$$x.0 = 0$$

$$x.x = x$$

$$x.x' = 0$$

These are the simple Boolean postulates. We can verify these postulates easily, by substituting the Boolean variable with '0' or '1'.

Note− The complement of complement of any Boolean variable is equal to the variable itself. i.e., x′x′′=x.

Basic Laws of Boolean Algebra

Following are the three basic laws of Boolean Algebra.

- Commutative law
- Associative law
- Distributive law

Commutative Law

If any logical operation of two Boolean variables give the same result irrespective of the order of those two variables, then that logical operation is said to be **Commutative**. The logical OR & logical AND operations of two Boolean variables x & y are shown below

$$x + y = y + x$$

$$x.y = y.x$$

The symbol '+' indicates logical OR operation. Similarly, the symbol '.' indicates logical AND operation and it is optional to represent. Commutative law obeys for logical OR & logical AND operations.

Associative Law

If a logical operation of any two Boolean variables is performed first and then the same operation is performed with the remaining variable gives the same result, then that logical operation is said to be **Associative**. The logical OR & logical AND operations of three Boolean variables x, y & z are shown below.

$$x + y+z = y+z+x$$

$$x.y.z= z.x.y$$

Associative law obeys for logical OR & logical AND operations.

Distributive Law

If any logical operation can be distributed to all the terms present in the Boolean function, then that logical operation is said to be **Distributive**. The distribution of logical OR & logical AND operations of three Boolean variables x, y & z are shown below.

$$x.y+z = (x.y) + (x.z)$$
$$x + y.z =(x+y).(x+z)$$

Distributive law obeys for logical OR and logical AND operations.

These are the Basic laws of Boolean algebra. We can verify these laws easily, by substituting the Boolean variables with '0' or '1'.

Theorems of Boolean Algebra

The following two theorems are used in Boolean algebra.

- Duality theorem
- DeMorgan's theorem

Duality Theorem

This theorem states that the **dual** of the Boolean function is obtained by interchanging the logical AND operator with logical OR operator and zeros with ones. For every Boolean function, there will be a corresponding Dual function.

Let us make the Boolean equations relationsrelations that we discussed in the section of Boolean postulates and basic laws into two groups. The following table shows these two groups.

Group1	Group2
x + 0 = x	x.1 = x
x + 1 = 1	x.0 = 0
x + x = x	x.x = x
x + x' = 1	x.x' = 0
x + y = y + x	x.y = y.x
x + y+z = x+y+z	x.y.z = x.y.z

x.y+z = x.y + x.z	x + y.z = x+y.x+z

In each row, there are two Boolean equations and they are dual to each other. We can verify all these Boolean equations of Group1 and Group2 by using duality theorem.

DeMorgan's Theorem

This theorem is useful in finding the **complement of Boolean function**. It states that the complement of logical OR of at least two Boolean variables is equal to the logical AND of each complemented variable.

DeMorgan's theorem with 2 Boolean variables x and y can be represented as

$$(x+y)' = x'.y'$$

The dual of the above Boolean function is

$$(x.y)' = x' + y'$$

Therefore, the complement of logical AND of two Boolean variables is equal to the logical OR of each complemented variable. Similarly, we can apply DeMorgan's theorem for more than 2 Boolean variables also.

Simplification of Boolean Functions

Till now, we discussed the postulates, basic laws and theorems of Boolean algebra. Now, let us simplify some Boolean functions.

1. $(x' + y) = xx' + xy$
$= 0 + xy = \boldsymbol{xy} \quad as\ xx' = 0$

2. $x + x'y = x + xy + x'y \qquad as \quad x + xy = x$
$= x + (x + x') \qquad as\ x + x' = 1$
$= \boldsymbol{x + y}$

3. $(x + y)(x + y') = ?$
$= xx + xy' + xy + yy'$
$= x + xy + xy' \qquad as\ xx = x; \qquad as\ yy' = 0;$
$= (1 + y + y') = \boldsymbol{x} \qquad \boldsymbol{as\ (1 + x) = 1}$

4. $xy + x'z + yz$
$= xy + x'z + y(x + x') \qquad as\ x + x' = 1$
$= xy + x'z + xyz + x'yz$
$= xy + xyz + x'z + x'yz$
$= x(1 + z) + x'z(1 + y) \qquad as\ 1 + z = 1\ ; 1 + y = 1$
$= xy + x'z$

5. $x + xy' + x'y$
$= x'y + (1 + y')$
$= x'y + x$ $\quad as\ x + x'y = (x + x').(x + y) = x + y$
$= \boldsymbol{x + y}$

6. $xyz + xy'z + xyz'$

$= xy(z + z') + xy'z$
$= xy + xy'z$
$= x(y + y'z) = \boldsymbol{x(y + z)}$ $\quad as\ y + y'z = (y + y')(y + z) = y + z$

7. $AB + (AC)' + AB'C(AB + C)$
$= AB + A' + C' + AB'CAB + AB'CC$ $\quad as\ (AC)' = A' + C'$
$= AB + A' + C' + 0 + AB'C$ $\quad as\ BB' = 0$
$= AB + A' + C' + AB'$ $\quad as\ C' + AB'C = (C' + AB')(C' + C) = C' + AB'$
$= A(B + B') + A' + C'$
$= A + A' + C'$
$= 1 + C'$
$= \boldsymbol{C'}$

8. $x'y'z' + x'y'z + x'yz' + x'yz + xy'z'$
$= x'y'(z + z') + x'y(z' + z) + xy'z'$
$= x'y' + x'y + xy'z'$
$= x' + xy'z' = \boldsymbol{x' + y'z'}$ $\quad as\ x + x'y = x + y$

9. $(x + y)(x'z' + z)(y' + xz)'$ $\quad as\ demorgam's\ theorem (A + B)' = A'.B'$
$= (x + y)(x' + z)(y''.(xz)')$ $\quad$ as x′ + xz = x′ + z
$= (xx' + xz + yx' + yz)(y.(x' + z'))$
$= (0 + xz + yx' + yz)(yx' + yz')$ $\quad$ as xx′ = 0;

$= 0 + xzyx' + yx'yx' + yx'yz + xzyz' + yz'yx' + yyzz'$ $\quad as\ aa = a;$
$= 0 + 0 + yx' + x'yz + 0 + x'yz' + 0$ $\quad as$
$= yx'(1 + z + z')$
$= x'y$

10. $x'y'z + x'yz + xy'$
$= x'(y + y') + xy'$ $\quad$ as y + y′ = 1
$= x'z + xy'$

Canonical Forms:

Minterms:

- **Boolean Variables are combined by AND operation**

A	B	C	MINTERMS	
0	0	0	$\bar{A}\bar{B}\bar{C}$	m0
0	0	1	$\bar{A}\bar{B}C$	m1
0	1	0	$\bar{A}B\bar{C}$	m2
0	1	1	$\bar{A}BC$	m3
1	0	0	$A\bar{B}\bar{C}$	m4
1	0	1	$A\bar{B}C$	m5
1	1	0	$AB\bar{C}$	m6
1	1	1	ABC	m7

Maxterms:

Boolean Variables are combined by OR operation.

A	B	C	Maxterms	
0	0	0	$A+B+C$	M0
0	0	1	$A+B+\bar{C}$	M1
0	1	0	$A+\bar{B}+C$	M2
0	1	1	$A+\bar{B}+\bar{C}$	M3
1	0	0	$\bar{A}+B+C$	M4
1	0	1	$\bar{A}+B+\bar{C}$	M5
1	1	0	$\bar{A}+\bar{B}+C$	M6
1	1	1	$\bar{A}+\bar{B}+\bar{C}$	M7

SOP(Sum of Products) or Summation of Minterms:

	A	B	C	F	$\bar{F}$
0	0	0	0	0	1
1	0	0	1	1	0
2	0	1	0	0	1
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	1	0
7	1	1	1	1	0

The SoP form is

$F = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + ABC$

$F = \sum_m(1, 4, 6, 7)$

POS(Products of Sum) or Product of Maxterms:

The PoS form for the above tabular column is

$\bar{F} = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$

$F = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$

$F = (A + B + C)(A + \bar{B} + C)(A + \bar{B} + \bar{C})(\bar{A} + B + \bar{C})$

F=$\prod(0, 2, 3, 5)$

Express the following table in PoS and SoP form.

	A	B	C	F	$\bar{F}$
0	0	0	0	1	0
1	0	0	1	1	0
2	0	1	0	0	1
3	0	1	1	1	0
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	1	0
7	1	1	1	1	0

The SoP form is

$F = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + ABC$

$F = \sum_m(0, 1, 3, 4, 6, 7)$

The Pos form is

$\bar{F} = \bar{A}B\bar{C} + A\bar{B}\bar{C}$

$\bar{F} = \overline{\bar{A}B\bar{C} + A\bar{B}\bar{C}}$

$F = \overline{\bar{A}B\bar{C}}\,\overline{A\bar{B}\bar{C}}$

$F = (A + \bar{B} + C)(\bar{A} + B + \bar{C})$

$F = G_M(2, 5)$

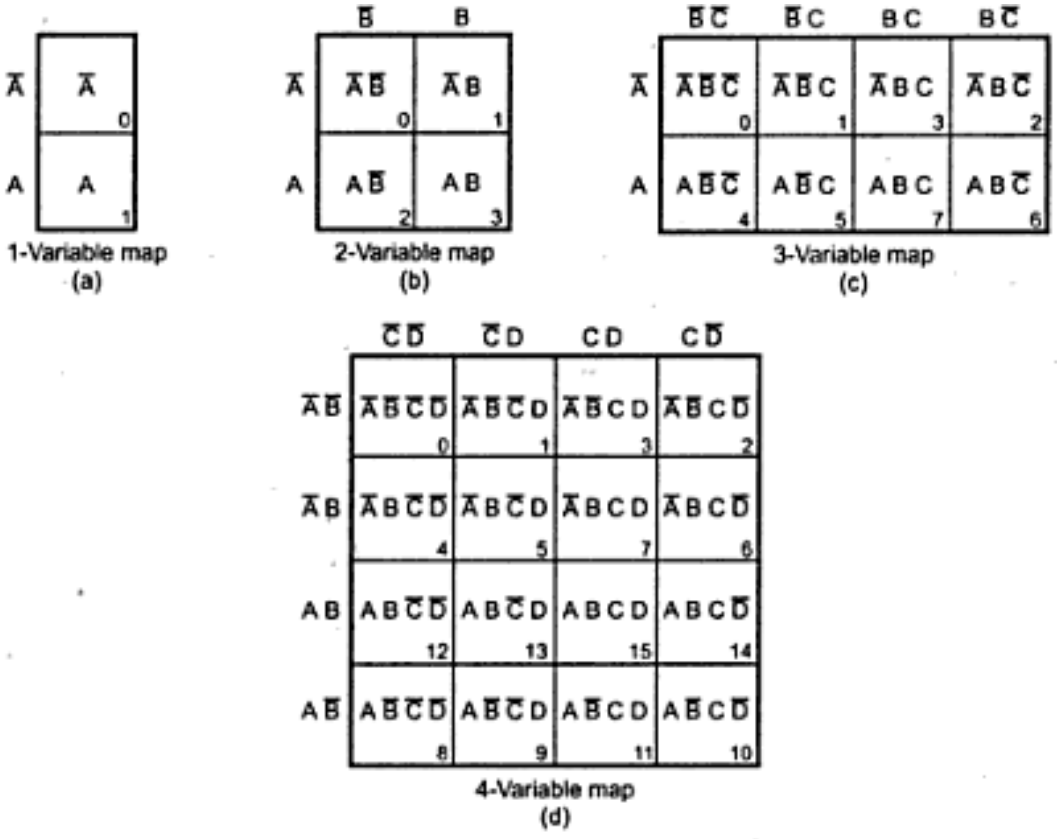
<u>Simplification Methods</u>

The simplification methods are

- Boolean Postulates and Theorems
- K- Maps
- Quine Mccluskey Method

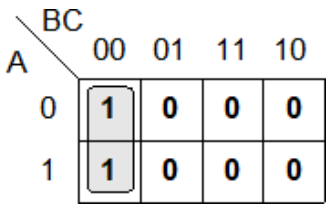
Karnaugh Maps(K Maps):

- Karnaugh maps (K-maps) is a graphical technique to simplify boolean functions of upto six variables.
- An *n*-variable K-map has 2^n cells with each cell corresponding to a row of an *n*-variable truth table.
- K-map cells are arranged such that adjacent cells correspond to truth-table rows that differ in only one bit position (*logical adjacency*).
- Switching functions are mapped (or plotted) by placing the function's value (*0,1,d*) in each cell of the map.



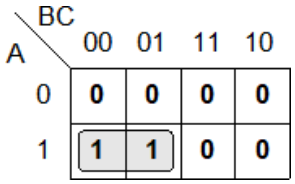
Reduce the given expressions using K – Maps:

$\boldsymbol{a.f = \sum(0,4)}$



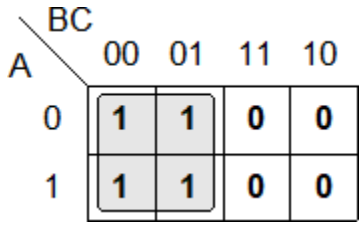
$$f = \bar{B}$$

b. $f = \sum(4, 5)$



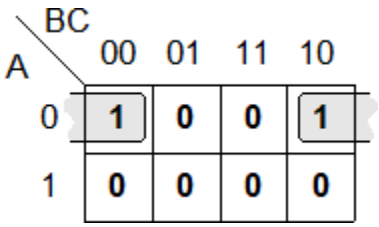
$$f = A\bar{B}$$

c. $f = \sum(0, 1, 4, 5)$

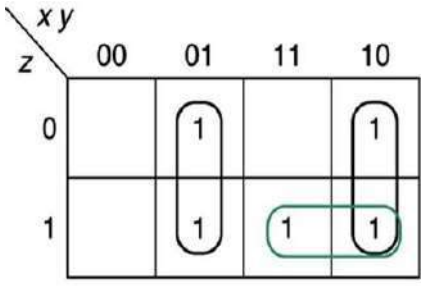


$$f = \bar{B}$$

d. $f = \sum(0, 2,)$



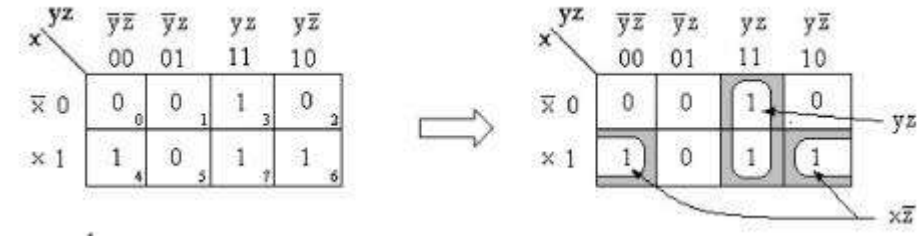
e. $f = \sum(2, 3, 4, 5, 7)$



$x'y + xy' + xz$

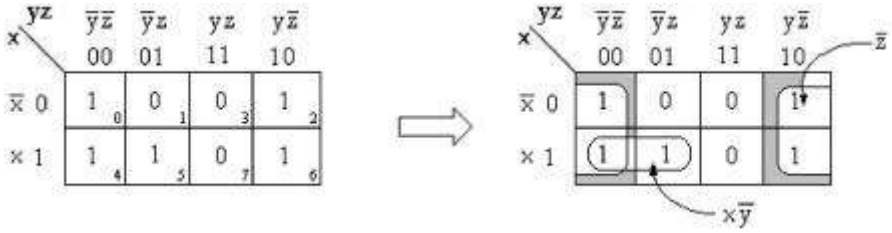
1.Simplify the Boolean expression.

$$F(x, y, z) = \sum(3, 4, 6, 7)$$



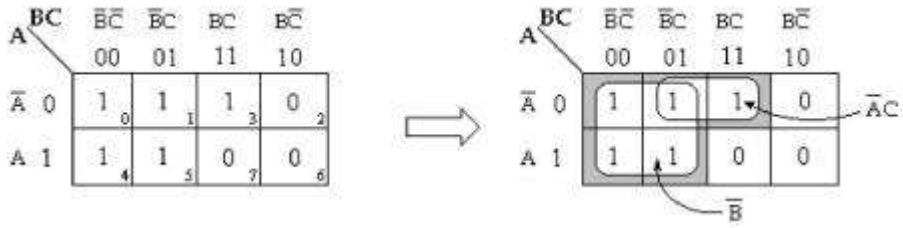
$f = yz + xz'$

2. $(x, y, z) = \sum(0,2,4,5,6)$



F=z'+xy'

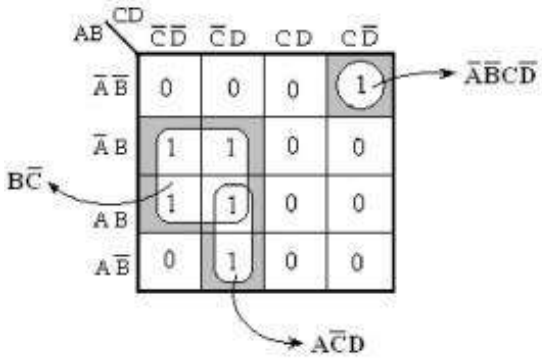
2. AB'C+A'B'C+A'BC+AB'C'+A'B'C'
Sol:
= m5+m1+m3+m4+m0
= ∑ (0,1,3,4,5)



F= A'C+B'

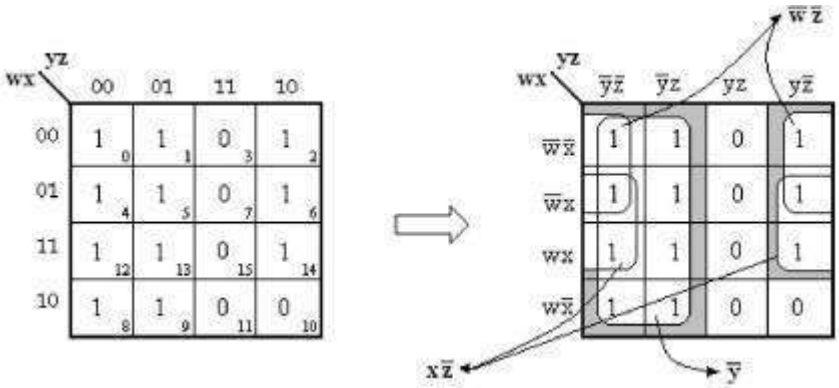
Four Variable Map:

1. Y= A'BC'D'+A'BC'D+ABC'D'+ABC'D+AB'C'D+A'B'CD'



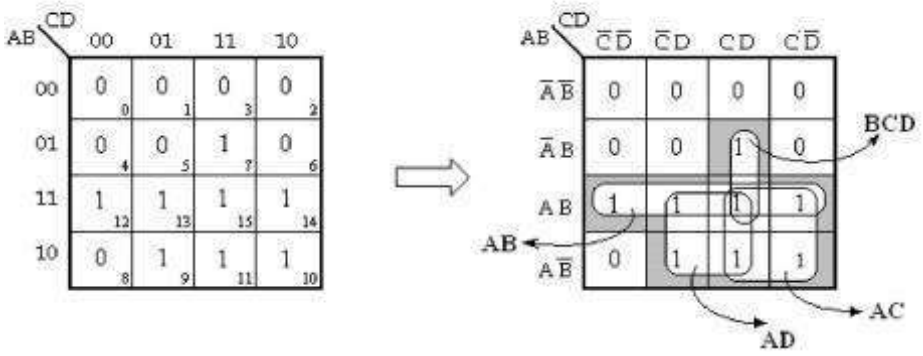
Y= A'B'CD'+AC'D+BC'

2.$f(w,x,y,z) = \sum m(0,1,2,4,5,6,8,912,13,14)$



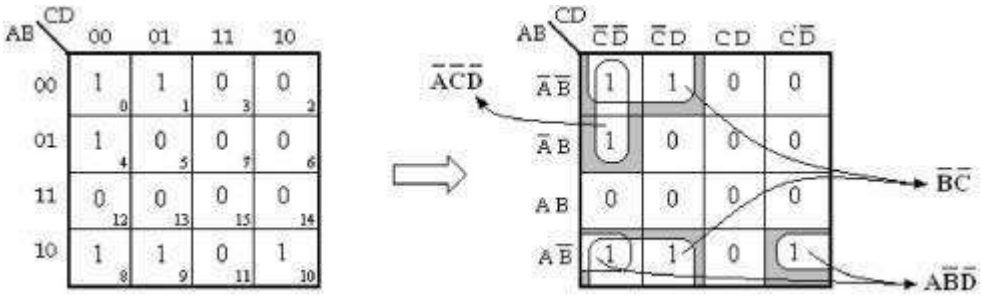
F=y'+w'z'+xz'

3. $Y(A,B,C,D) = \sum m(7,9,10,11,12,13,14,15)$



Y=AB+AC+AD+BCD

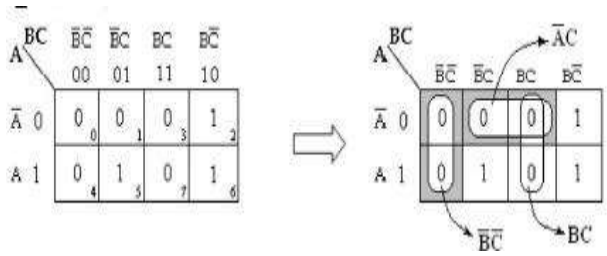
4. $F(A,B,C,D) = \sum m\,(0,1,4,8,9,10)$



F=A'C'D'+AB'D'+B'C'

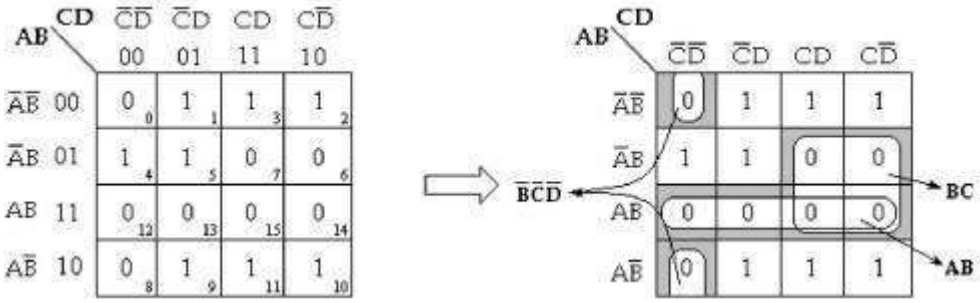
Simplify the expression:

1. **Y= (A+B+C')(A+B'+C')(A'+B'+C')(A'+B+C)(A+B+C)**
   = M1.M3.M7.M4.M0
   = $\prod M(0,1,3,4,7) = \sum m(2,5,6)$



Y=Y''= (B'C'+A'C+BC)'
= (B'C')'.(A'C')'.(BC)'
= (B''+C'').(A+C').(B'+C')
=(B+C)(A+C')(B'+C')

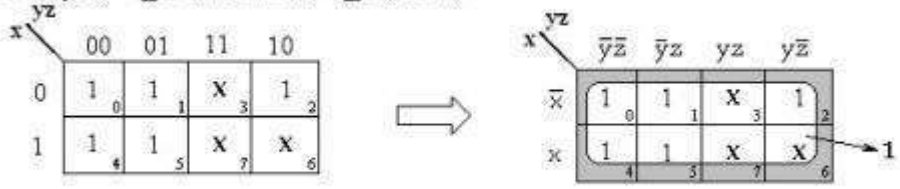
2. **$y = \prod (0, 6, 7, 8, 12, 13, 14, 15)$**



Y'=B'C'D'+AB+BC
Y''= (B'C'D'+AB+BC)'
= (B'C'D')'+(AB)'+(BC)'
=(B''+C''+D'')(A'+B')(B'+C')
= (B+C+D)(A'+B')(b'=C')

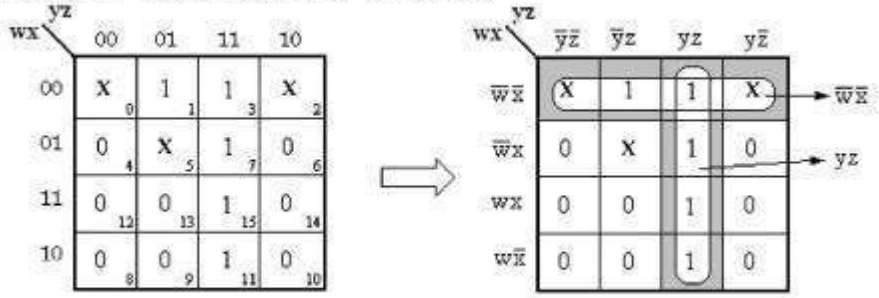
Don't Care Conditions:

1. F (x, y, z) = ∑m (0, 1, 2, 4, 5)+ ∑d (3, 6, 7)



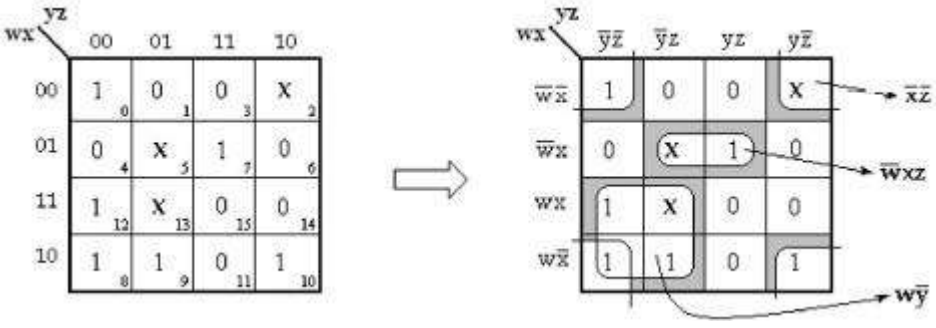
F (x, y, z) = 1

2. F (w, x, y, z) = ∑m (1, 3, 7, 11, 15)+ ∑d (0, 2, 5)



F (w, x, y, z) = w′x′+ yz

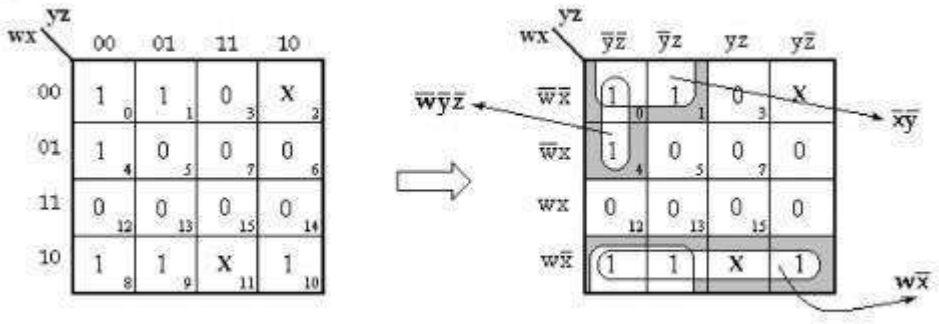
3. F (w, x, y, z) = ∑m (0, 7, 8, 9, 10, 12)+ ∑d (2, 5, 13)



F (w, x, y, z) = w′xz+ wy′+ x′z′.

4. F (w, x, y, z) = ∑m (0, 1, 4, 8, 9, 10)+ ∑d (2, 11)

Soln:



F (w, x, y, z) = wx′+ x′y′+ w′y′z′.

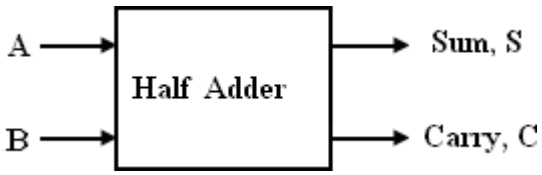
ARITHMETIC CIRCUITS – BASIC BUILDING BLOCKS:

In this section, we will discuss those combinational logic building blocks that can be used to perform addition and subtraction operations on binary numbers. Addition and subtraction are the two most commonly used arithmetic operations, as the other two, namely multiplication and division, are respectively the processes of repeated addition and repeated subtraction.

The basic building blocks that form the basis of all hardware used to perform the arithmetic operations on binary numbers are half-adder, full adder, half-subtractor, full-subtractor.

Half-Adder:

A half-adder is a combinational circuit that can be used to add two binary bits. It has two inputs that represent the two bits to be added and two outputs, with one producing the SUM output and the other producing the CARRY.



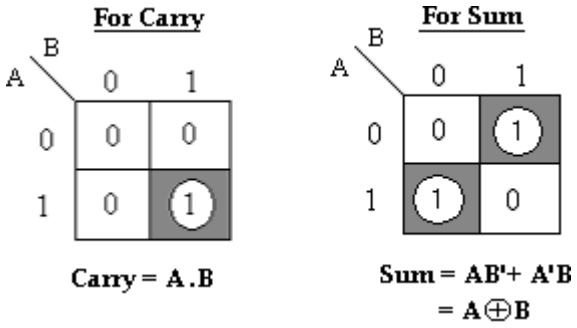
Block schematic of half-adder

The truth table of a half-adder, showing all possible input combinations and the corresponding outputs are shownbelow.

Truth table of half-adder

Inputs		Outputs	
A	**B**	**Carry (C)**	**Sum (S)**
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

K-map simplification for carry and sum:



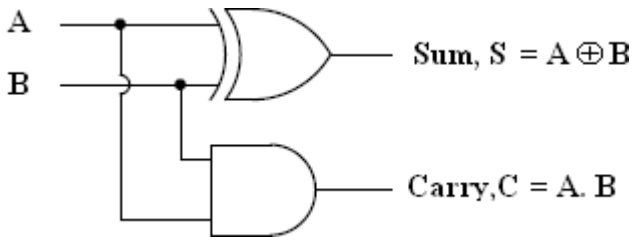
The Boolean expressions for the SUM and CARRY outputs are given by the equations,

Sum, S = A'B+ AB'= A⊕B

Carry, C = A . B

The first one representing the SUM output is that of an EX-OR gate, the second one representing the CARRY output is that of an AND gate.

The logic diagram of the half adder is,

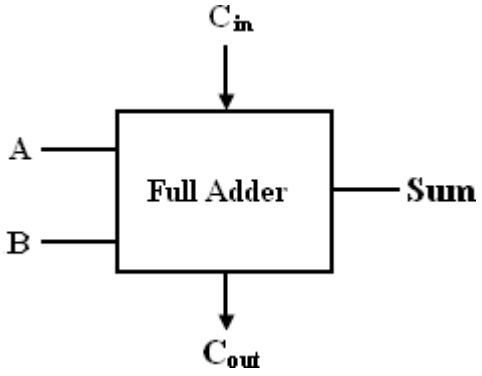


Logic Implementation of Half-adder

Full- Adder

A full adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of 3 inputs and 2 outputs.

Two of the input variables, represent the significant bits to be added. The third input represents the carry from previous lower significant position. The block diagram of full adder is given by,



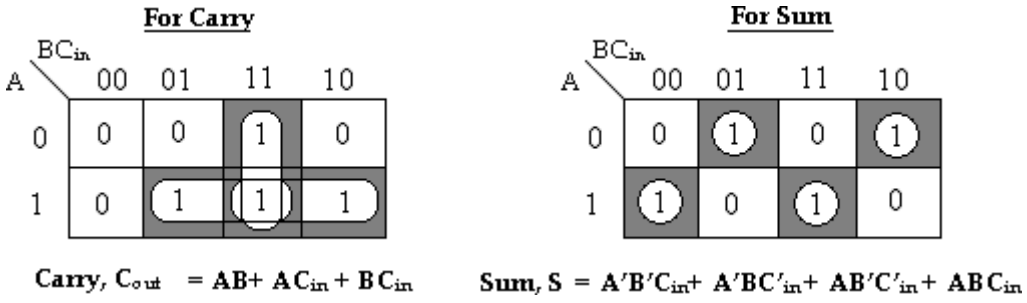
Block schematic of full-adder

The full adder circuit overcomes the limitation of the half-adder, which can be used to add two bits only. As there are three input variables, eight different input combinations are possible. The truth table is shown below,

Truth Table:

Inputs			Outputs	
A	**B**	**Cin**	**Sum (S)**	**Carry (Cout)**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

To derive the simplified Boolean expression from the truth table, the Karnaugh map method is adopted as,

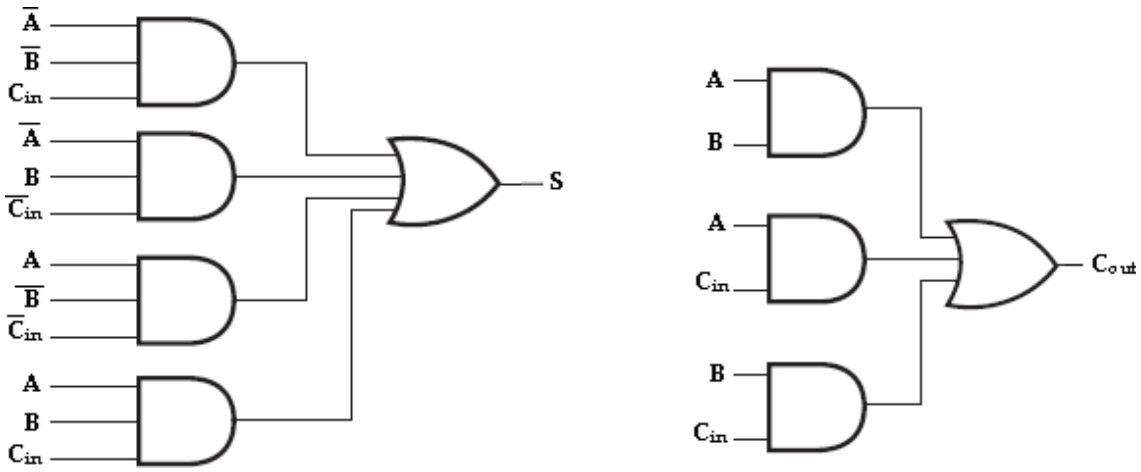


The Boolean expressions for the SUM and CARRY outputs are given by the equations,

Sum, S = A'B'Cin+ A'BC'in + AB'C'in + ABCin

Carry, Cout = AB+ ACin + BCin .

The logic diagram for the above functions is shown as,



Implementation of full-adder in Sum of Products

The logic diagram of the full adder can also be implemented with two half-adders and one OR gate. The S output from the second half adder is the exclusive-OR of Cin and the output of the first half-adder, giving

Sum = Cin ⊕ (A⊕ B) [x⊕y = x'y+ xy']

= Cin ⊕ (A'B+AB')

= C‘in (A‘B+AB‘) +Cin (A‘B+AB‘)‘ [(x‘y+xy‘)‘= (xy+x‘y‘)]

= C‘in (A‘B+AB‘) + Cin (AB+A‘B‘)

= A‘BC‘in + AB‘C‘in + ABCin + A‘B‘Cin

and the carry output is,

Carry, Cout = AB+ Cin (A’B+AB’)

= AB+ A‘BCin+ AB‘Cin

= AB (Cin+1) + A‘BCin+ AB‘Cin [Cin+1= 1]

= ABCin+ AB+ A‘BCin+ AB‘Cin

= AB+ ACin (B+B‘) + A‘BCin

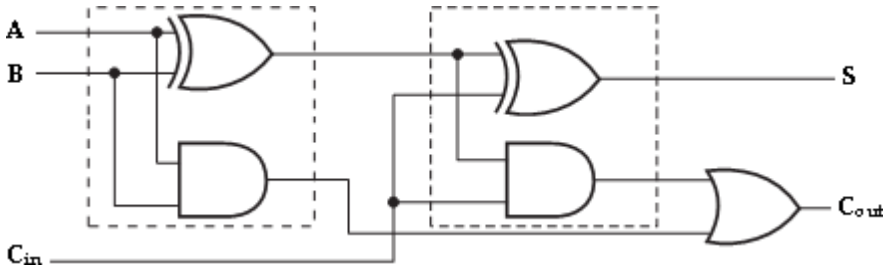
= AB+ ACin+ A‘BCin

= AB (Cin+1) + ACin+ A‘BCin [Cin+1= 1]

= ABCin+ AB+ ACin+ A‘BCin

= AB+ ACin+ BCin (A +A‘)

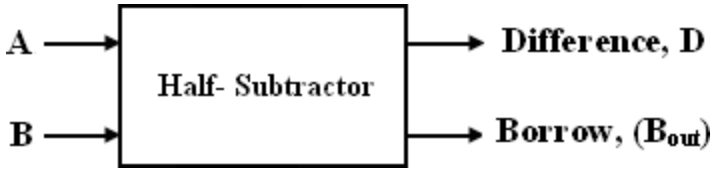
= AB+ ACin+ BCin.



Implementation of full adder with two half-adders and an OR gate

Half -Subtractor:

A *half-subtractor* is a combinational circuit that can be used to subtract one binary digit from another to produce a DIFFERENCE output and a BORROW output. The



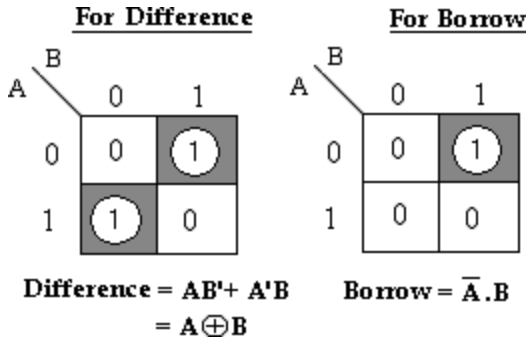
BORROW output here specifies whether a _1' has been borrowed to perform the subtraction.

Block schematic of half-subtractor

The truth table of half-subtractor, showing all possible input combinations and the corresponding outputs are shown below.

Input		Output	
A	**B**	**Difference (D)**	**Borrow (Bout)**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

K-map simplification for half subtractor:

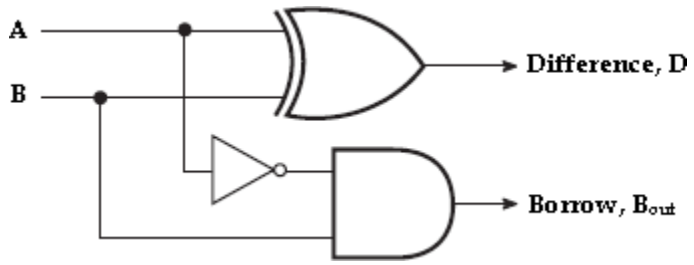


The Boolean expressions for the DIFFERENCE and BORROW outputs are given by the equations,

Difference= A⊕B; Borrow= A'B

The first one representing the DIFFERENCE (**D**)output is that of an exclusive-OR gate, the expression for the BORROW output (**Bout**) is that of an AND gate with input A complemented before it is fed to thegate.

The logic diagram of the half adder is,



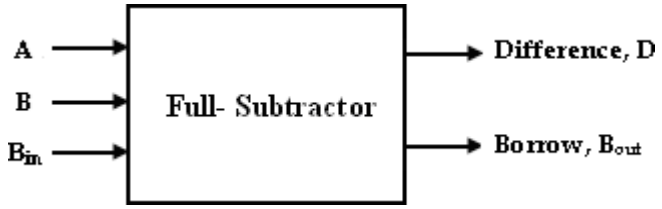
Logic Implementation of Half-Subtractor

Comparing a half-subtractor with a half-adder, we find that the expressions for the SUM and DIFFERENCE outputs are just the same.

Full Subtractor:

A *full subtractor* performs subtraction operation on two bits, a minuend and a subtrahend, and also takes into consideration whether a 1 has already been borrowed by the previous adjacent lower minuend bit or not.

As a result, there are three bits to be handled at the input of a full subtractor, namely the two bits to be subtracted and a borrow bit designated as B_{in}. There are two outputs, namely the DIFFERENCE output D and the BORROW output B_o. The BORROW output bit tells whether the minuend bit needs to borrow a 1 from the next possible higher minuend bit.

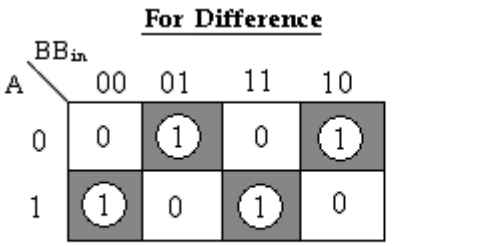


Block schematic of full-Subtractor

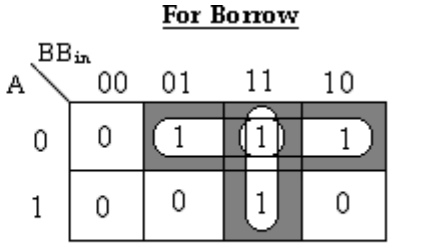
The truth table for full-subtractor is,

Inputs			Outputs	
A	**B**	**Bin**	**Difference(D)**	**Borrow(B_{out})**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1

1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Difference, $D = A'B'B_{in} + A'BB'_{in} + AB'B'_{in} + ABB_{in}$



Borrow, $B_{out} = A'B + A'B_{in} + BB_{in}$

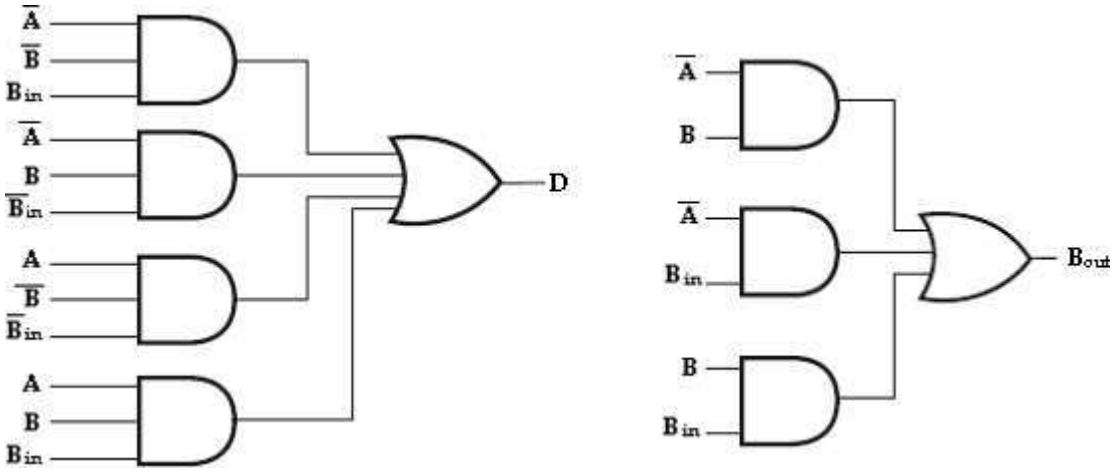
K-map simplification for full-subtractor:

The Boolean expressions for the DIFFERENCE and BORROW outputs are given by the equations,

Difference, D = A'B'Bin+ A'BB'in + AB'B'in +ABBin

Borrow, Bout = A'B+ A'Cin + BBin .

The logic diagram for the above functions is shown as,



Implementation of full - subtractor in Sum of Products

The logic diagram of the full-subtractor can also be implemented with two half-subtractors and one OR gate. The difference,D output from the second half subtractor is

the exclusive-OR of Bin and the output of the first half-subtractor,giving

Difference,D= $B_{in} \oplus (A \oplus B)$ [x ⊓ y = x‘y+xy‘]

$= B_{in} \oplus (A‘B+AB‘)$

$= B‘_{in} (A‘B+AB‘) + B_{in} (A‘B+AB‘)‘$ [(x‘y+xy‘)‘= (xy+x‘y‘)]

$= B‘_{in} (A‘B+AB‘) + B_{in} (AB+A‘B‘)$

$= A‘BB‘_{in} + AB‘B‘_{in} + ABB_{in} + A‘B‘B_{in}$.

and the borrow output is,

Borrow, B_{out} = A’B+ B_{in} (A’B+AB’)’ [(x‘y+xy‘)‘= (xy+x‘y‘)]

$= A‘B+ B_{in} (AB+A‘B‘)$

$= A‘B+ ABB_{in}+ A‘B‘B_{in}$

$= A‘B (B_{in}+1) + ABB_{in}+ A‘B‘B_{in}$ [C_{in}+1= 1]

$= A‘BB_{in}+ A‘B+ ABB_{in}+ A‘B‘B_{in}$

$= A‘B+ BB_{in} (A+A‘)+ A‘B‘B_{in}$ [A+A‘= 1]

$= A‘B+ BB_{in}+ A‘B‘B_{in}$

$= A‘B (B_{in}+1) + BB_{in}+ A‘B‘B_{in}$ [C_{in}+1= 1]

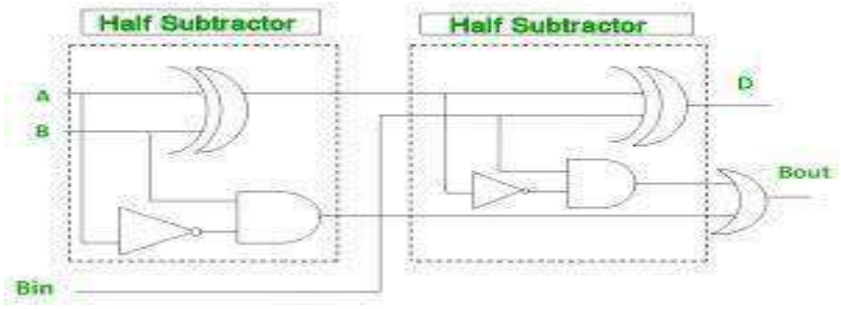
$= A‘BB_{in}+ A‘B+ BB_{in}+ A‘B‘B_{in}$

$= A‘B+ BB_{in}+ A‘B_{in} (B +B‘)$

$= A‘B+ BB_{in}+ A‘B_{in}$.

Therefore,

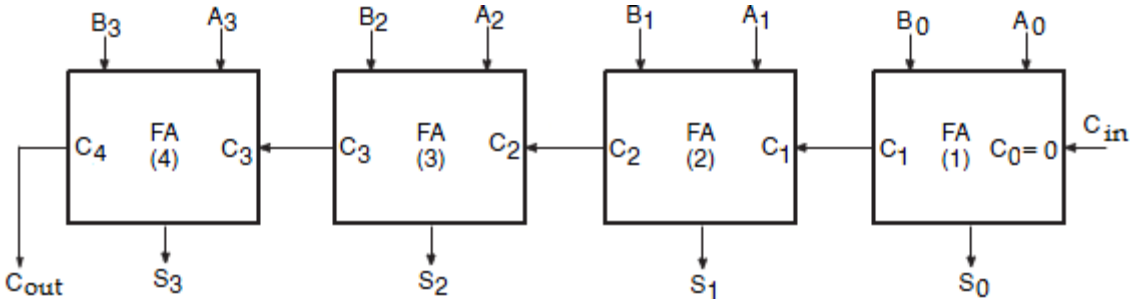
we can implement full-subtractor using two half-subtractors and OR gate as,



Implementation of full-subtractor with two half-subtractors and an OR gate

Binary Adder (Parallel Adder):

The 4-bit binary adder using full adder circuits is capable of adding two 4-bit numbers resulting in a 4-bit sum and a carry output as shown in figure below.



4-bit binary parallel Adder

Since all the bits of augend and addend are fed into the adder circuits simultaneously and the additions in each position are taking place at the same time, this circuit is known as parallel adder.

Let the 4-bit words to be added be represented by,
A3A2A1A0= 1111 and B3B2B1B0= 0011.

Significant place		4	3	2	1
Input carry		1	1	1	0
Augend word A :		1	1	1	1
Addend word B :		0	0	1	1
	1	0	0	1	0 ← Sum
	↑				
	Output Carry				

The bits are added with full adders, starting from the least significant position, to form the sum it and carry bit. The input carry C0 in the least significant position must be 0. The carry output of the lower order stage is connected to the carry input of the next higher order stage. Hence this type of adder is called ripple-carry adder.

In the least significant stage, A0, B0 and C0 (which is 0) are added resulting in sum S0 and carry C1. This carry C1 becomes the carry input to the second stage. Similarly in the second stage, A1, B1 and C1 are added resulting in sum S1 and carry C2, in the third stage, A2, B2 and C2 are added resulting in sum S2 and carry C3, in the third stage, A3, B3 and C3 are added resulting in sum S3 and C4, which is the output carry. Thus the circuit results in a sum (S3S2S1S0) and a carry output (Cout).

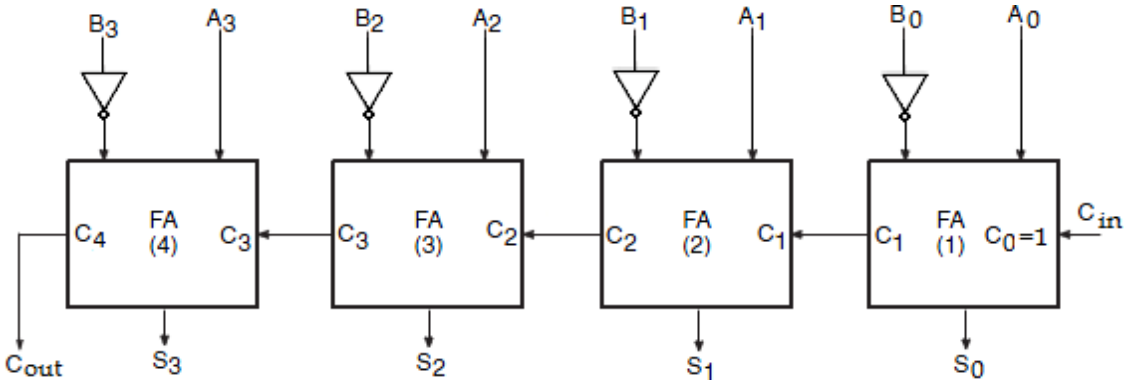
Though the parallel binary adder is said to generate its output immediately after the inputs are applied, its speed of operation is limited by the carry propagation delay through all stages. However, there are several methods to reduce this delay.

One of the methods of speeding up this process is look-ahead carry addition which eliminates the ripple-carry delay.

Binary Subtractor (Parallel Subtractor):

The subtraction of unsigned binary numbers can be done most conveniently by means of complements. The subtraction A-B can be done by taking the 2‘s complement of B and adding it to A. The 2‘s complement can be obtained by taking the 1‘s complement and adding 1 to the least significant pair of bits. The 1‘s complement can be implemented with inverters and a 1 can be added to the sum through the input carry.

The circuit for subtracting A-B consists of an adder with inverters placed between each data input B and the corresponding input of the full adder. The input carry C0 must be equal to 1 when performing subtraction. The operation thus performed becomes A, plus the 1‘s complement of B, plus1. This is equal to A plus the 2‘s complement of B.

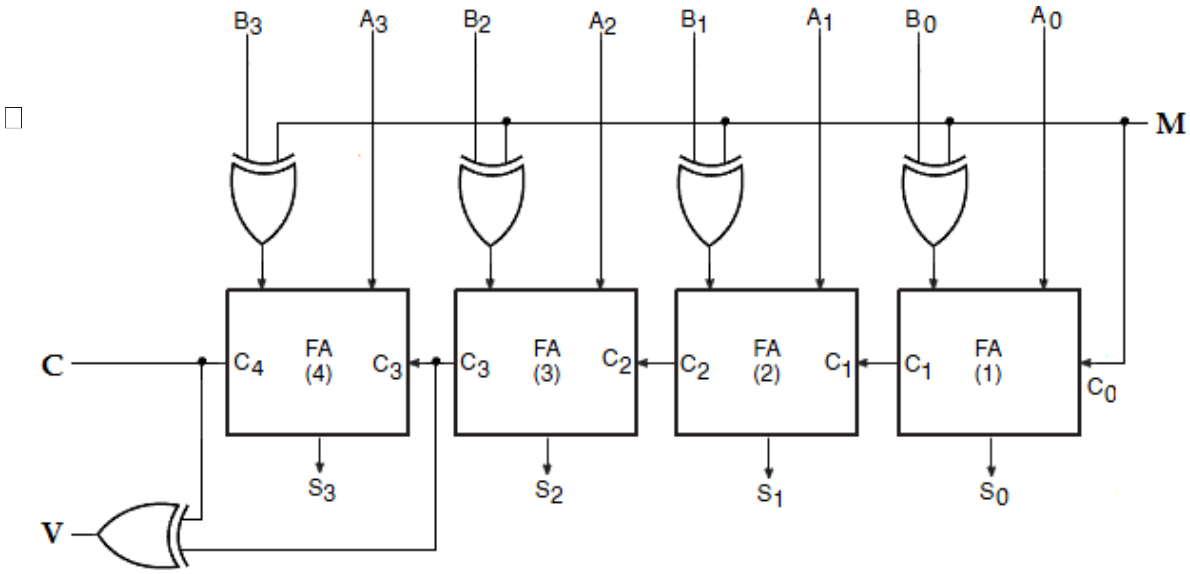


4-bit Parallel Subtractor

Parallel Adder/ Subtractor:

The addition and subtraction operation can be combined into one circuit with one common binary adder. This is done by including an exclusive-OR gate with each full adder. A 4-bit adder Subtractor circuit is shown below.

4-Bit Adder Subtractor



The mode input M controls the operation. When M= 0, the circuit is an adder and when M=1, the circuit becomes a Subtractor. Each exclusive-OR gate receives input M and one of the inputs of B. When M=0, we have B 0= B. The full adders receive the value of B, the input carry is 0, and the circuit performs A plus B. When M=1, we have B 1= B‘ and C0=1. The B inputs are all complemented and a 1 is added through the input carry. The circuit performs the operation A plus the 2‘s complement of B. The exclusive-OR with output V is for detecting an overflow.

Decimal Adder (BCD Adder):

The digital system handles the decimal number in the form of binary coded decimal numbers (BCD). A BCD adder is a circuit that adds two BCD bits and produces a sum digit also inBCD.

Consider the arithmetic addition of two decimal digits in BCD, together with an input carry from a previous stage. Since each input digit does not exceed 9, the output sum cannot be greater than 9+ 9+1 = 19; the 1 is the sum being an input carry. The adder will form the sum in binary and produce a result that ranges from 0 through 19.

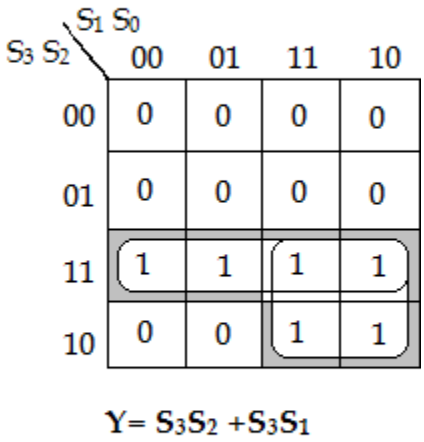
These binary numbers are labeled by symbols K, Z8, Z4, Z2, Z1, K is the carry. The columns under the binary sum list the binary values that appear in the outputs of the 4- bit binary adder. The output sum of the two decimal digits must be represented in BCD.

Binary Sum					BCD Sum					Decimal
K	**Z8**	**Z4**	**Z2**	**Z1**	**C**	**S8**	**S4**	**S2**	**S1**	
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	2
0	0	0	1	1	0	0	0	1	1	3
0	0	1	0	0	0	0	1	0	0	4
0	0	1	0	1	0	0	1	0	1	5
0	0	1	1	0	0	0	1	1	0	6
0	0	1	1	1	0	0	1	1	1	7
0	1	0	0	0	0	1	0	0	0	8
0	1	0	0	1	0	1	0	0	1	9
0	1	0	1	0	1	0	0	0	0	10
0	1	0	1	1	1	0	0	0	1	11
0	1	1	0	0	1	0	0	1	0	12
0	1	1	0	1	1	0	0	1	1	13
0	1	1	1	0	1	0	1	0	0	14
0	1	1	1	1	1	0	1	0	1	15
1	0	0	0	0	1	0	1	1	0	16
1	0	0	0	1	1	0	1	1	1	17
1	0	0	1	0	1	1	0	0	0	18
1	0	0	1	1	1	1	0	0	1	19

In examining the contents of the table, it is apparent that when the binary sum is equal to or less than 1001, the corresponding BCD number is identical, and therefore no conversion is needed. When the binary sum is greater than 9 (1001), we obtain a non-valid BCD representation. The addition of binary 6 (0110) to the binary sum converts it to the correct BCD representation and also produces an output carry as required.

The logic circuit to detect sum greater than 9 can be determined by simplifying the boolean expression of the given truth table.

Inputs				Output
S_3	S_2	S_1	S_0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

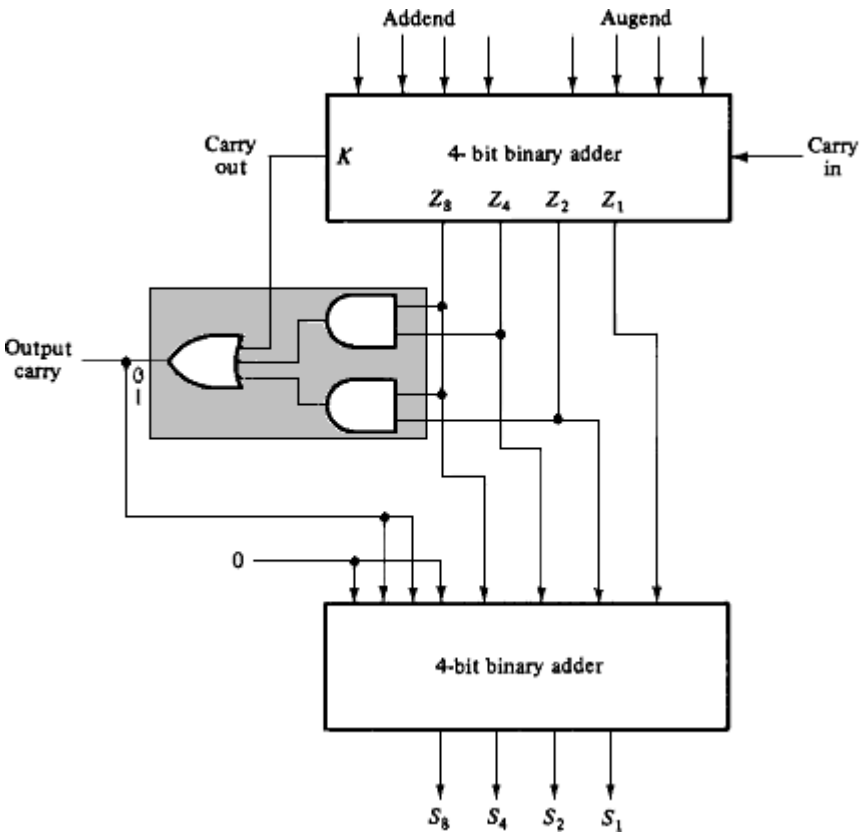


$Y = S_3S_2 + S_3S_1$

To implement BCD adder we require:

- 4-bit binary adder for initialaddition
- Logic circuit to detect sum greater than9 and
- One more 4-bit adder to add 01102 in the sum if the sum is greater than 9 or carry is 1.

The two decimal digits, together with the input carry, are first added in the top4-bit binary adder to provide the binary sum. When the output carry is equal to zero, nothing is added to the binary sum. When it is equal to one, binary 0110 is added to the binary sum through the bottom 4-bit adder. The output carry generated from the bottom adder can be ignored, since it supplies information already available at the output carry terminal. The output carry from one stage must be connected to the input carry of the next higher-order stage.



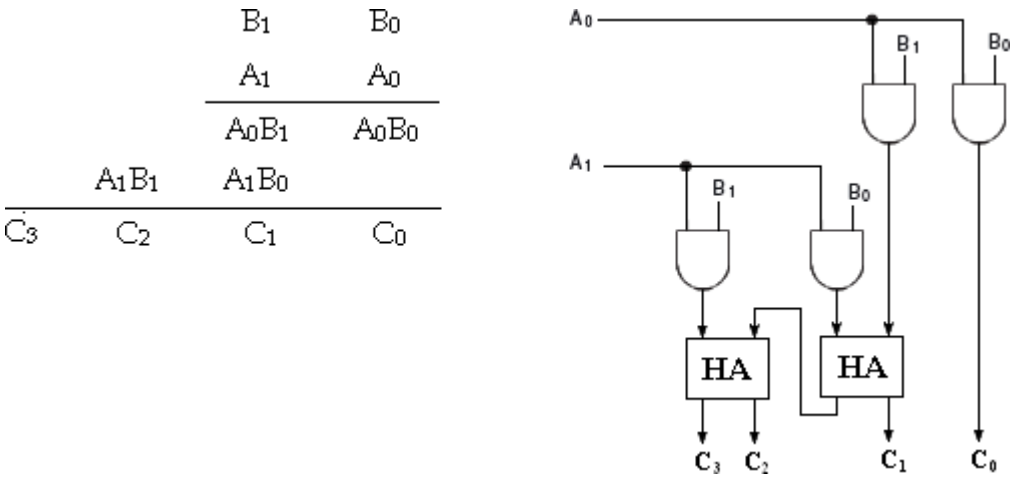
Block diagram of BCD adder

Binary Multiplier:

Multiplication of binary numbers is performed in the same way as in decimal numbers. The multiplicand is multiplied by each bit of the multiplier starting from the least significant bit. Each such multiplication forms a partial product. Such partial products are shifted one position to the left. The final product is obtained from the sum of partial products.

Consider the multiplication of two 2-bit numbers. The multiplicand bits are B_1 and B_0, the multiplier bits are A_1 and A_0, and the product is C_3, C_2, C_1 and C_0. The first partial product is formed by multiplying A_0 by B_1B_0. The multiplication of two bits such as A_0 and B_0 produces a 1 if both bits are 1; otherwise, it produces a 0. This is identical to an AND operation. Therefore the partial product can be implemented with AND gates as shown in the diagram below.

The second partial product is formed by multiplying A_1 by B_1B_0 and shifted one position to the left. The two partial products are added with two half adder (HA) circuits.

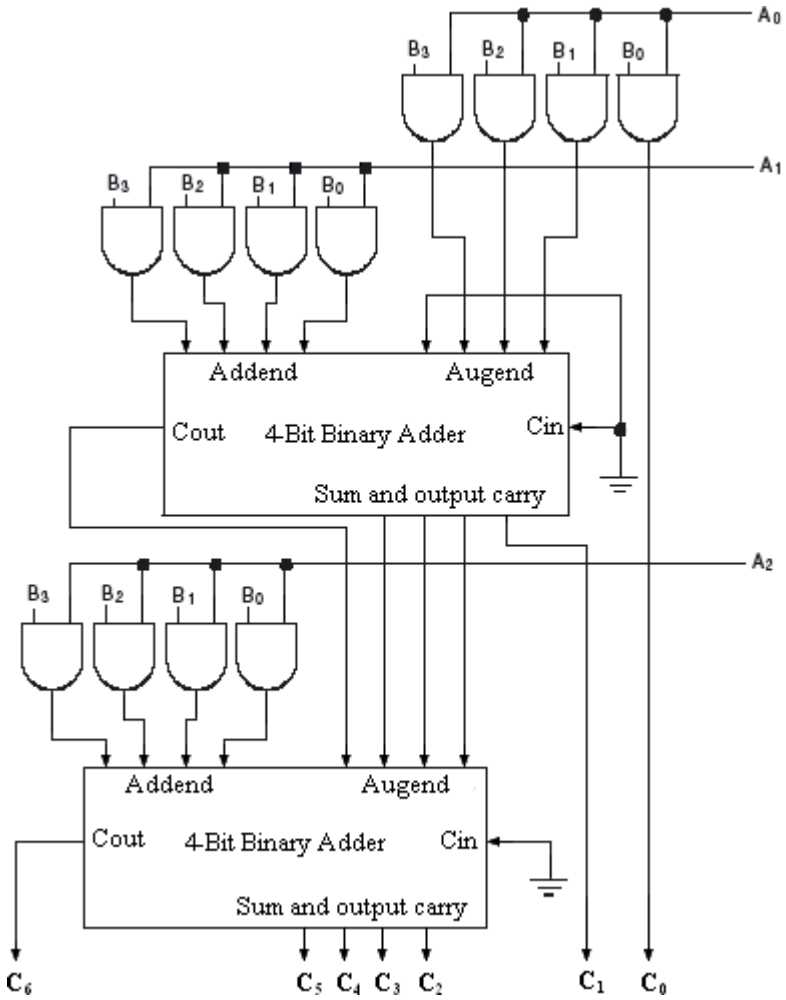


2-bit by 2-bit Binary multiplier

Usually there are more bits in the partial products and it is necessary to use full adders to produce the sum of the partial products. The least significant bit of the product does not have to go through an adder since it is formed by the output of the first AND gate.

A combinational circuit binary multiplier with more bits can be constructed in a similar fashion. A bit of the multiplier is ANDed with each bit of the multiplicand in as many levels as there are bits in the multiplier. The binary output in each level of AND gates are added with the partial product of the previous level to form a new partial product. The last level produces the product. For J multiplier bits and K multiplicand bits we need (J x K) AND gates and (J-1) k-bit adders to produce a product of J+K bits.

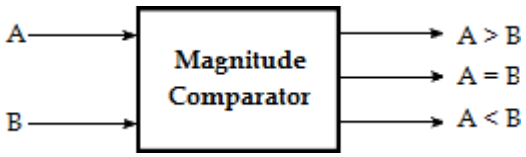
Consider a multiplier circuit that multiplies a binary number of four bits by a number of three bits. Let the multiplicand be represented by B3, B2, B1, B0 and the multiplier by A2, A1, and A0. Since K= 4 and J= 3, we need 12 AND gates and two 4-bit adders to produce a product of seven bits. The logic diagram of the multiplier is shown below.



4-bit by 3-bit Binary multiplier

MAGNITUDE COMPARATOR:

A ***magnitude comparator*** is a combinational circuit that compares two given numbers (A and B) and determines whether one is equal to, less than or greater than the other. The output is in the form of three binary variables representing the conditions A = B, A>B and A<B, if A and B are the two numbers being compared.



Block diagram of magnitude comparator

For comparison of two *n*-bit numbers, the classical method to achieve the Boolean expressions requires a truth table of 2^{2n} entries and becomes too lengthy and cumbersome.

2-bit Magnitude Comparator:

The truth table of 2-bit comparator is given in table below

Truth table:

Inputs				**Outputs**		
A 1	**A_0**	**B_1**	**B_0**	**A>B**	**A=B**	**A<B**
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

K-map Simplification**:**

For A>B

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

$A>B = A_0B_1'B_0' + A_1B_1' + A_1A_0B_0'$

For A=B

A_1A_0 \ B_1B_0	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

$A=B = A_1'A_0'B_1'B_0' + A_1'A_0B_1'B_0 + A_1A_0B_1B_0 + A_1A_0'B_1B_0'$

$= A_1'B_1' (A_0'B_0' + A_0B_0) + A_1B_1 (A_0B_0 + A_0'B_0')$

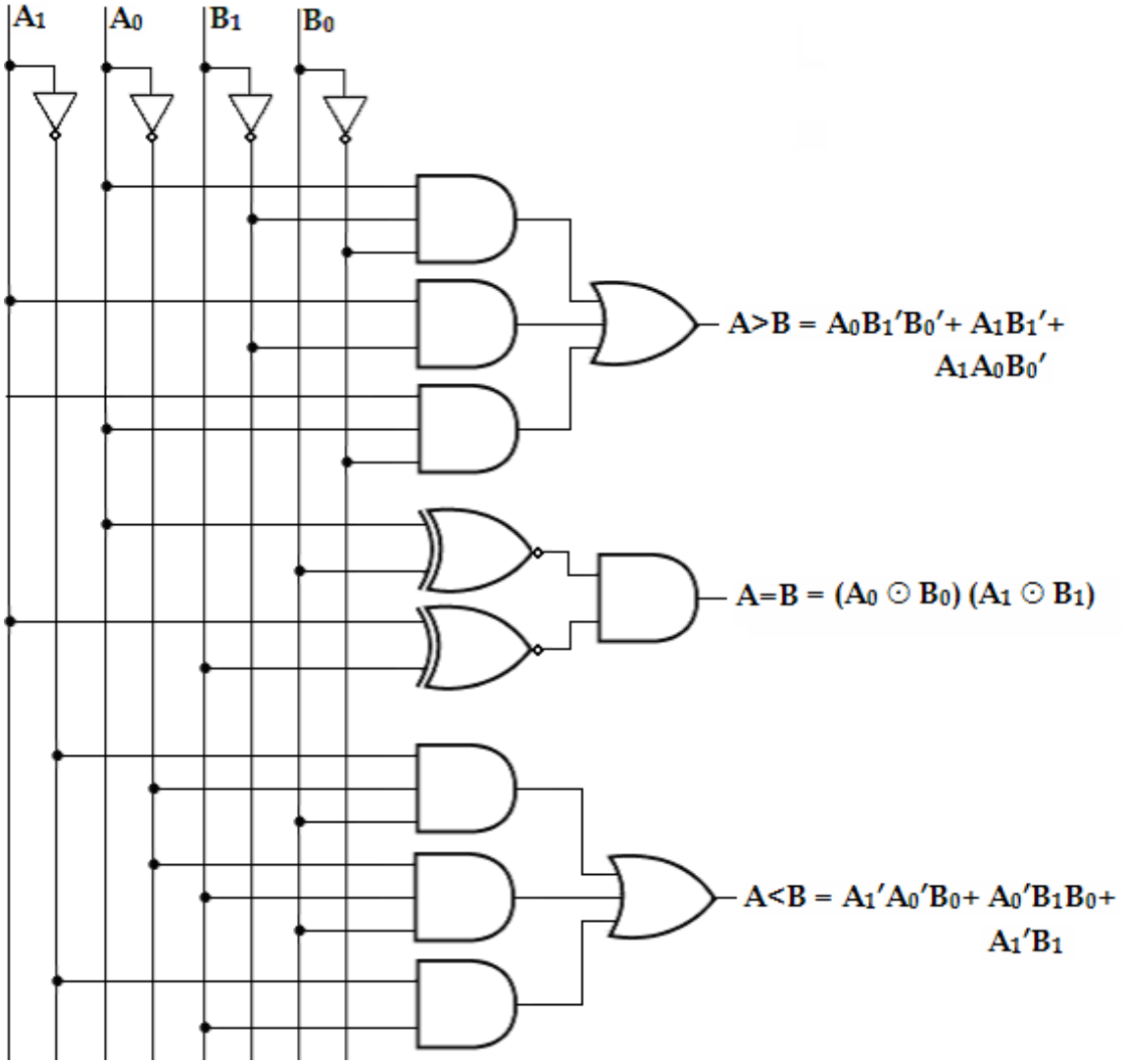
$= (A_0 \odot B_0)(A_1 \odot B_1)$

For A<B

A_1A_0 \ B_1B_0	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	1	0

$A<B = A_1'A_0'B_0 + A_0'B_1B_0 + A_1'B_1$

Logic Diagram:



2-bit Magnitude Comparator

4- bit Magnitude Comparator:

Let us consider the two binary numbers A and B with four digits each. Write the coefficient of the numbers in descending order as,

A= A3A2A1A0

B = B3 B2 B1 B0,

Each subscripted letter represents one of the digits in the number. It is observed from the bit contents of two numbers that A = B when A3 = B3, A2 = B2, A1 = B1 and A0 = B0. When the numbers are binary they possess the value of either 1 or 0, the equality relation of each pair can be expressed logically by the equivalence function as

X*i* = **A*i*B*i*** + **A*i*′B*i*′** for *i* = 1, 2, 3, 4.

Or, **X*i*** = (**A** ⊕ **B**)′. or, **X*i*′** = **A** ⊕ **B**

Or, $\mathbf{X_i = (A_iB_i' + A_i'B_i)'.}$

where,

$X_i = 1$ only if the pair of bits in position i are equal (ie., if both are 1 or both are 0).

To satisfy the equality condition of two numbers A and B, it is necessary that all X_i must be equal to logic 1. This indicates the AND operation of all X_i variables. In other words, we can write the Boolean expression for two equal 4-bit numbers.

$$\mathbf{(A = B) = X_3X_2X_1 X_0.}$$

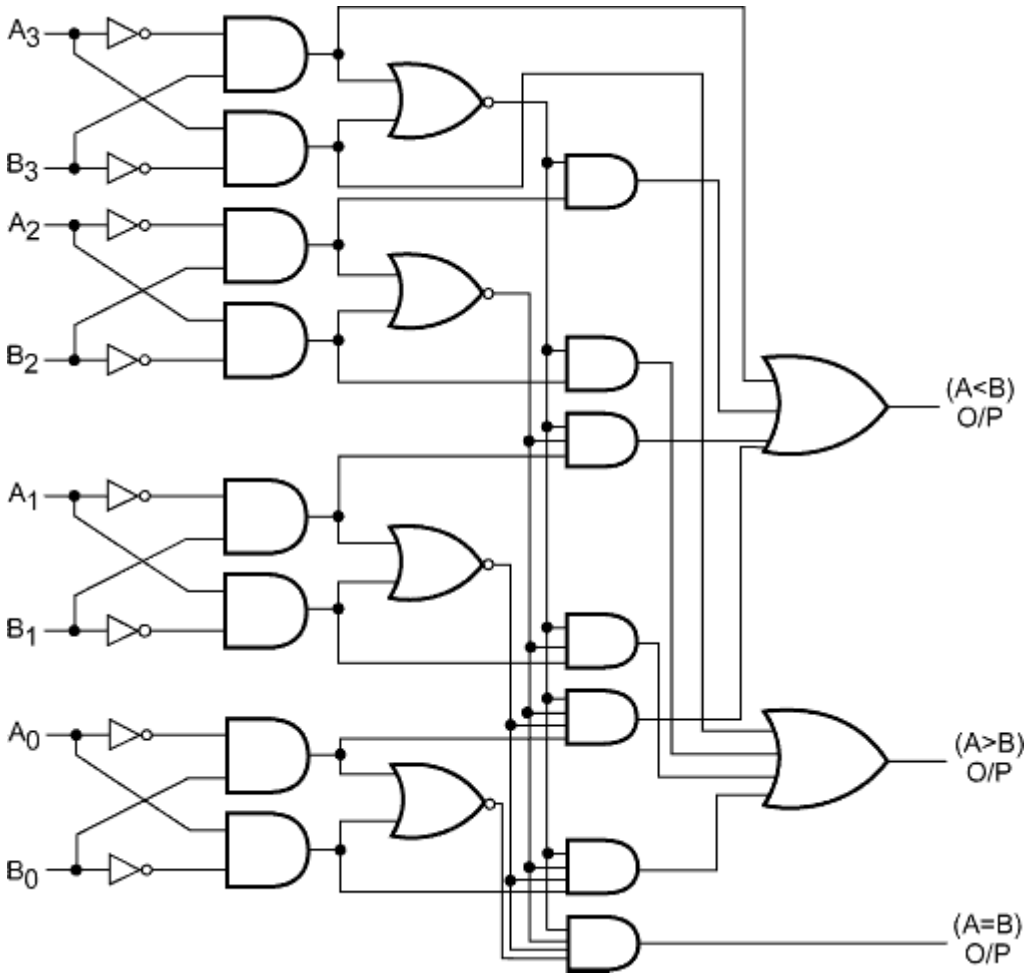
The binary variable (A=B) is equal to 1 only if all pairs of digits of the two numbers are equal.

To determine if A is greater than or less than B, we inspect the relative magnitudes of pairs of significant bits starting from the most significant bit. If the two digits of the most significant position are equal, the next significant pair of digits is compared. The comparison process is continued until a pair of unequal digits is found. It may be concluded that A>B, if the corresponding digit of A is 1 and B is 0. If the corresponding digit of A is 0 and B is 1, we conclude that A<B. Therefore, we can derive the logical expression of such sequential comparison by the following two Boolean functions,

$$\mathbf{(A>B) = A_3B_3' + X_3A_2B_2' + X_3X_2A_1B_1'}$$
$$\mathbf{+X_3X_2X_1A_0B_0' \ (A<B) = A_3'B_3 + X_3A_2'B_2}$$
$$\mathbf{+X_3X_2A_1'B_1 + X_3X_2X_1A_0'B_0}$$

The symbols (A>B) and (A<B) are binary output variables that are equal to 1 when A>B or A<B, respectively.

The gate implementation of the three output variables just derived is simpler than it seems because it involves a certain amount of repetition. The unequal outputs can use the same gates that are needed to generate the equal output. The logic diagram of the 4-bit magnitude comparator is shown below,

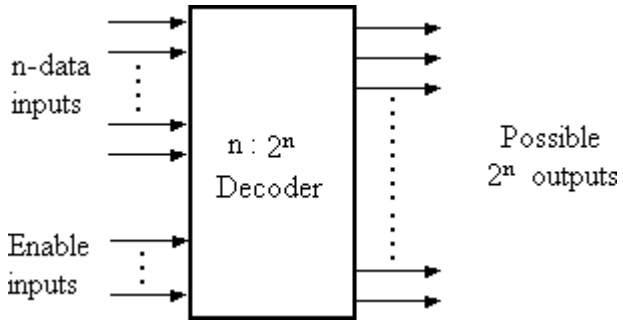


4- bit Magnitude Comparator

The four x outputs are generated with exclusive-NOR circuits and applied to an AND gate to give the binary output variable (A=B). The other two outputs use the x variables to generate the Boolean functions listed above. This is a multilevel implementation and has a regular pattern.

DECODERS:

A decoder is a combinational circuit that converts binary information from _n' input lines to a maximum of _2^n' unique output lines. The general structure of decoder circuit is –

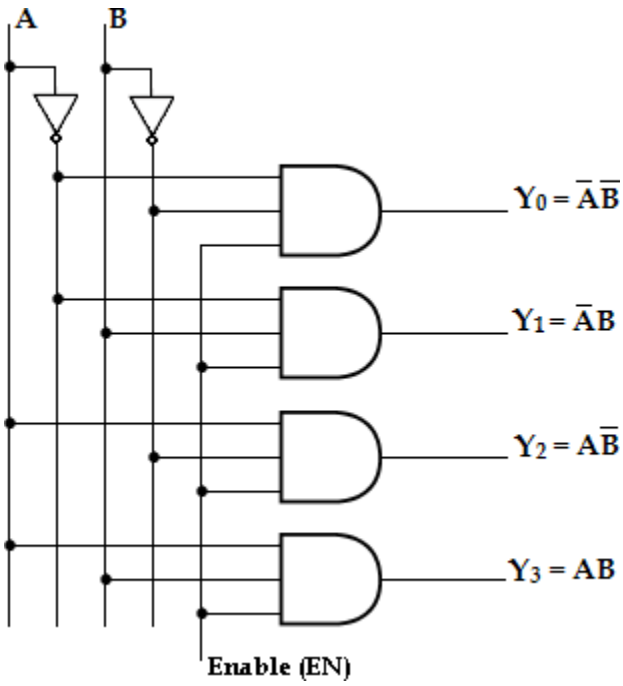


General structure of decoder

The encoded information is presented as n inputs producing 2^n possible outputs. The 2^n output values are from 0 through 2^n-1. A decoder is provided with enable inputs to activate decoded output based on data inputs. When any one enable input is unasserted, all outputs of decoder are disabled.

Binary Decoder (2 to 4 decoder):

A binary decoder has _n' bit binary input and a one activated output out of 2^n outputs. A binary decoder is used when it is necessary to activate exactly one of 2^n outputs based on an n-bit input value.



2- **to-4 Line decoder**

Here the 2 inputs are decoded into 4 outputs, each output representing one of the minterms of the two input variables.

Inputs			Outputs			
Enable	A	B	Y3	Y2	Y1	Y0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

As shown in the truth table, if enable input is 1 (EN= 1) only one of the outputs ($Y0 – Y3$), is active for a given input.
The output $Y0$ is active, ie., $Y0$= 1 when inputs A= B= 0,
$Y1$ is active when inputs, A= 0
and B= 1, $Y2$ is active, when
input A= 1 and B= 0, $Y3$ is
active, when inputs A= B= 1.

3 to 8 Line Decoder:

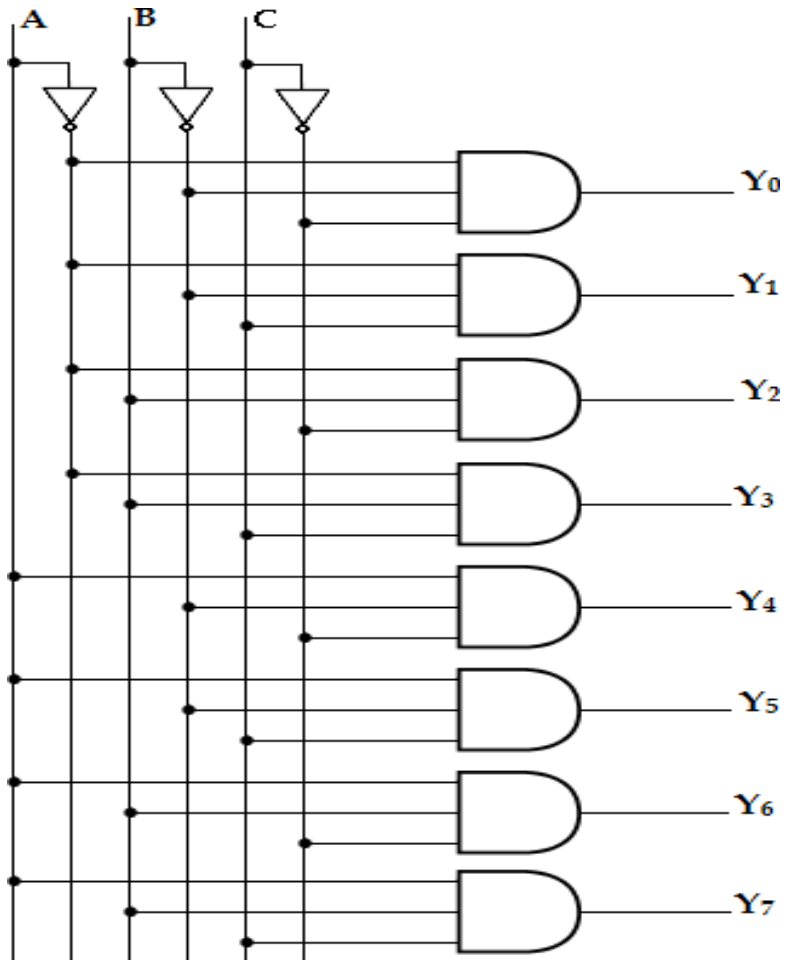
A 3-to-8 line decoder has three inputs (A, B, C) and eight outputs ($Y0$- $Y7$). Based on the 3 inputs one of the eight outputs is selected.

The three inputs are decoded into eight outputs, each output representing one of the minterms of the 3-input variables. This decoder is used for binary-to-octal conversion. The input variables may represent a binary number and the outputs will represent the eight digits in the octal number system. The output variables are mutually exclusive because only one output can be equal to 1 at any one time. The output line whose value is equal to 1 represents the minterm equivalent of the binary number presently available in the input lines.

Inputs			Outputs							
A	B	C	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

3- **to-8 line decoder**

Logic Diagram:

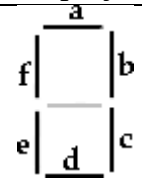
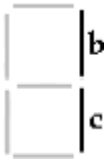
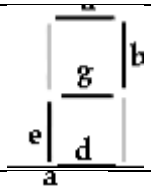
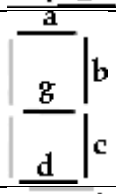
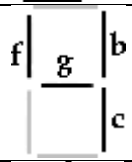
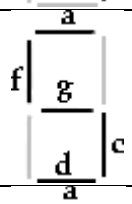
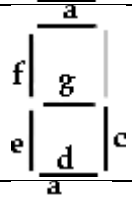
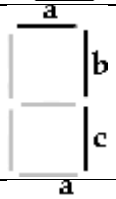
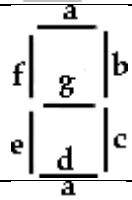
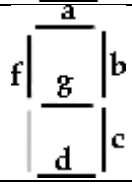


BCD to 7-Segment Display Decoder:A seven-segment display is normally used for displaying any one of the decimal digits, 0 through 9. A BCD-to-seven segment decoder accepts a decimal digit in BCD and generates the corresponding seven-segment code.

Each segment is made up of a material that emits light when current is passed through it. The segments activated during each digit display are tabulated as—

Truth Table:

K-map Simplification:

Digit	Display	Segments Activated
0		a, b, c, d, e, f
1		b, c
2		a, b, d, e, g
3		a, b, c, d, g
4		b, c, f, g
5		a, c, d, f, g
6		a, c, d, e, f, g
7		a, b, c
8		a, b, c, d, e, f, g
9		a,b,c,d,f,g

For (a)

AB \ CD	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	X	X	X	X
10	1	1	X	X

a= A+ C+ BD+ B'D'

For (b)

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	X	X	X	X
10	1	1	X	X

b= B'+ C'D'+ CD

For (c)

AB \ CD	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	X	X	X	X
10	1	1	X	X

c= B+ C'+ D

For (d)

AB \ CD	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	X	X	X	X
10	1	1	X	X

d= B'D'+ CD'+ BC'D+ B'C+ A

For (e)

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	X	X	X	X
10	1	0	X	X

e= B'D'+ CD'

For (f)

AB \ CD	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	X	X	X	X
10	1	1	X	X

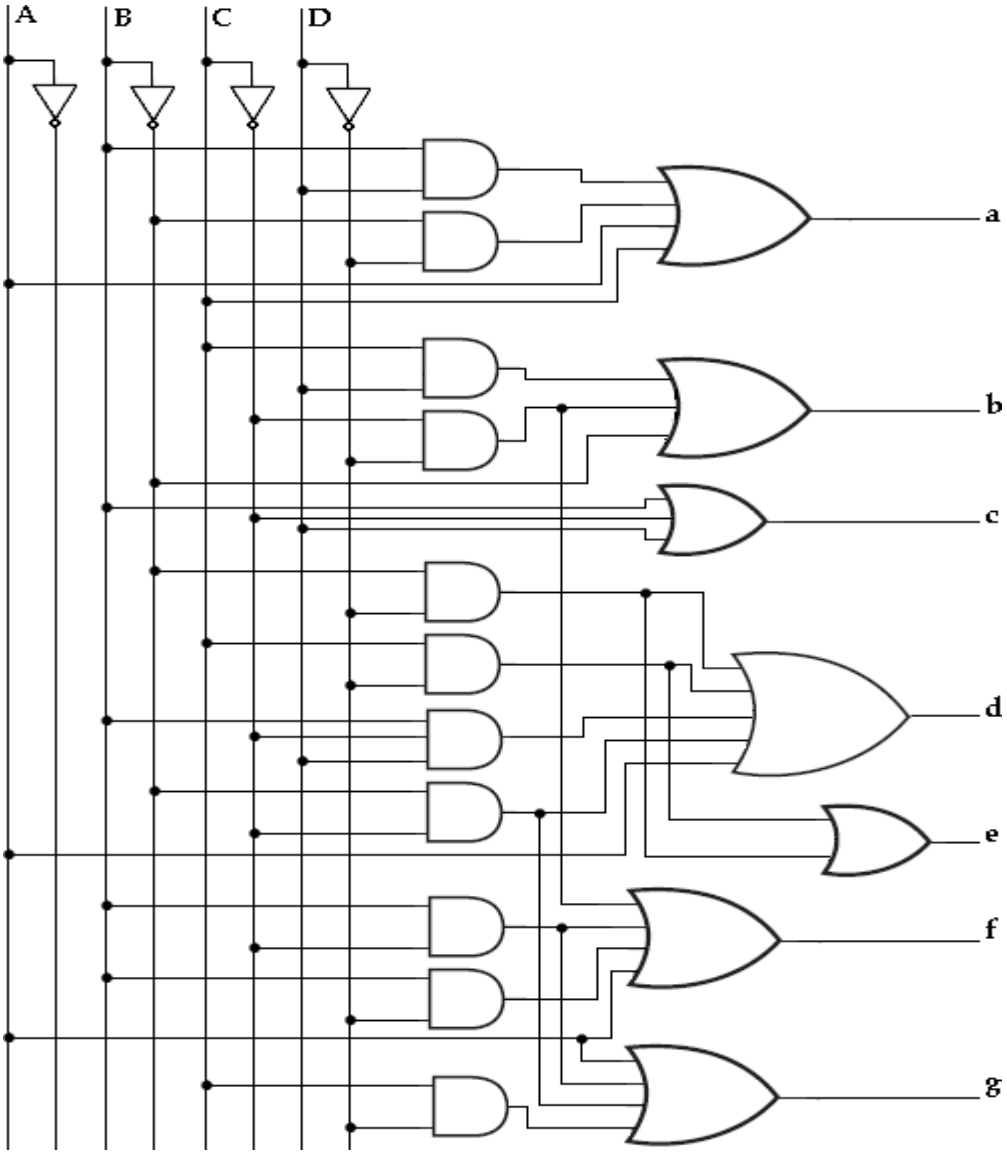
f= A+ C'D'+ BC'+ BD'

For (g)

AB \ CD	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	X	X	X	X
10	1	1	X	X

g= A+ BC'+ B'C+ CD'

Logic Diagram:



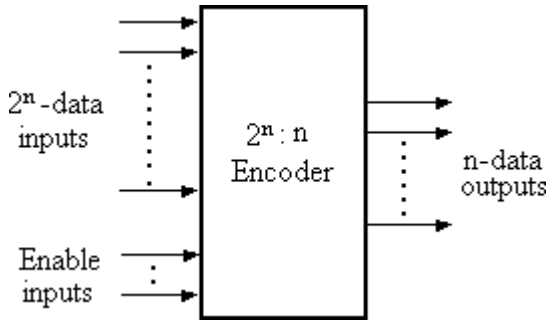
BCD to 7-segment display decoder

Applications of decoders:

1. Decoders are used in counter system.
2. They are used in analog to digital converter.
3. Decoder outputs can be used to drive a display system.

ENCODERS:

An encoder is a digital circuit that performs the inverse operation of a decoder. Hence, the opposite of the decoding process is called encoding. An encoder is a combinational circuit that converts binary information from 2^n input lines to a maximum of _n' unique output lines.
The general structure of encoder circuit is –



General structure of Encoder

It has 2^n input lines, only one which 1 is active at any time and _n' output lines. It encodes one of the active inputs to a coded binary output with _n' bits. In an encoder, the number of outputs is less than the number ofinputs.

Octal-to-Binary Encoder:

It has eight inputs (one for each of the octal digits) and the three outputs that generate the corresponding binary number. It is assumed that only one input has a value of 1 at any given time.

Inputs								Outputs		
D 0	D 1	D 2	D 3	D 4	D 5	D 6	D 7	X	Y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1

0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

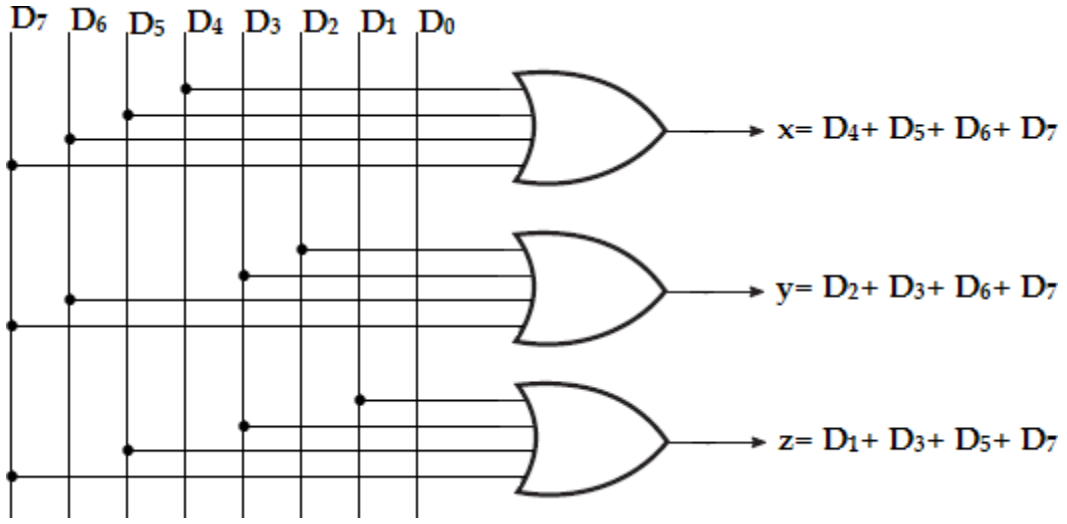
The encoder can be implemented with OR gates whose inputs are determined directly from the truth table. Output z is equal to 1, when the input octal digit is 1 or 3 or 5 or 7. Output y is 1 for octal digits 2, 3, 6, or 7 and the output is 1 for digits 4, 5, 6 or
7. These conditions can be expressed by the following output Boolean functions:

$z = D_1 + D_3 + D_5 + D_7$

$y = D_2 + D_3 + D_6 + D_7$ **$x = D_4 + D_5 + D_6 + D_7$**

The encoder can be implemented with three OR gates. The encoder defined in the below table, has the limitation that only one input can be active at any given time. If two inputs are active simultaneously, the output produces an undefined combination.

For eg., if D_3 and D_6 are 1 simultaneously, the output of the encoder may be 111. This does not represent either D_6 or D_3. To resolve this problem, encoder circuits must establish an input priority to ensure that only one input is encoded. If we establish a higher priority for inputs with higher subscript numbers and if D_3 and D_6 are 1 at the same time, the output will be 110 because D_6 has higher priority than D_3.



Octal-to-Binary Encoder

Another problem in the octal-to-binary encoder is that an output with all 0‘s is generated when all the inputs are 0; this output is same as when D_0 is equal to 1. The discrepancy can be resolved by providing one more output to indicate that atleast one input is equal to 1.

Priority Encoder:

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

In addition to the two outputs x and y, the circuit has a third output, V (valid bit indicator). It is set to 1 when one or more inputs are equal to 1. If all inputs are 0, there is no valid input and V is equal to 0.

The higher the subscript number, higher the priority of the input. Input D3, has the highest priority. So, regardless of the values of the other inputs, when D3 is 1, the output for xy is 11. D2 has the next priority level. The output is 10, if D2= 1 provided D3= 0. The output for D1 is generated only if higher priority inputs are 0, and so on down the priority levels.

Truth table:

Inputs				Outputs		
D 0	**D 1**	**D 2**	**D 3**	**x**	**y**	**V**
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

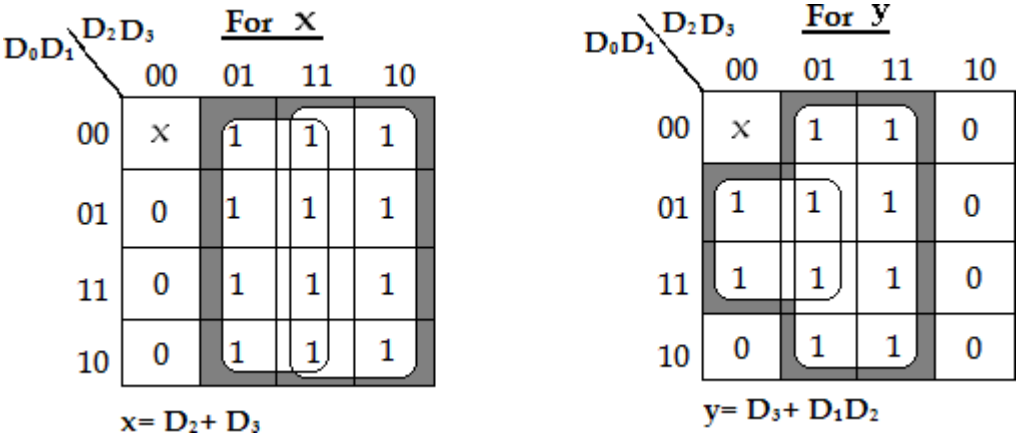
Although the above table has only five rows, when each don‘t care condition is replaced first by 0 and then by 1, we obtain all 16 possible input combinations. For example, the third row in the table with X100 represents minterms 0100 and 1100. The don‘t care condition is replaced by 0 and 1 as shown in the table below.

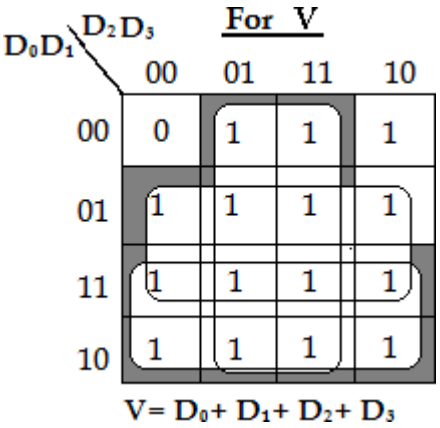
Modified Truth table:

Inputs				Outputs		
D 0	**D 1**	**D 2**	**D 3**	**x**	**y**	**V**
0	0	0	0	x	x	0
1	0	0	0	0	0	1
0 1	1 1	0 0	0 0	0	1	1
0 0 1 1	0 1 0 1	1 1 1 1	0 0 0 0	1	0	1
0 0 0	0 0 1	0 1 0	1 1 1			

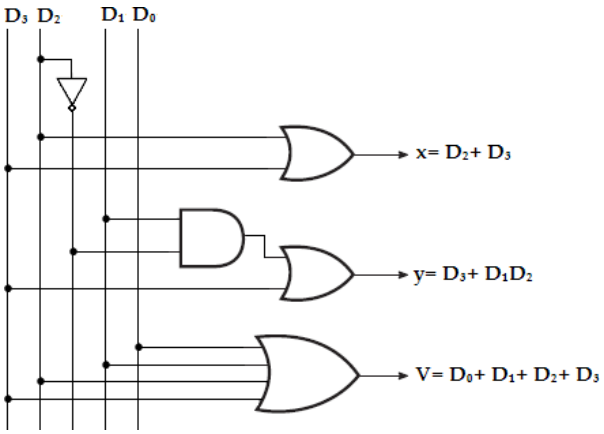
0	1	1	1	1	1	1
1	0	0	1			
1	0	1	1			
1	1	0	1			
1	1	1	1			

K-map Simplification:





The priority encoder is implemented according to the above Boolean functions.

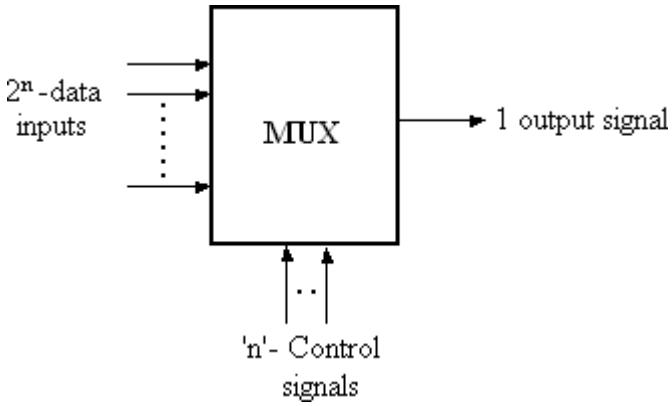


Input Priority Encoder

MULTIPLEXER: (Data Selector)

A ***multiplexer*** or *MUX*, is a combinational circuit with more than one input line, one output line and more than one selection line. A multiplexer selects binary information present from one of many input lines, depending upon the logic status of the selection inputs, and routes it to the output line. Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected. The multiplexer is often labeled as MUX in block diagrams.

A multiplexer is also called a **data selector**, since it selects one of many inputs and steers the binary information to the output line.

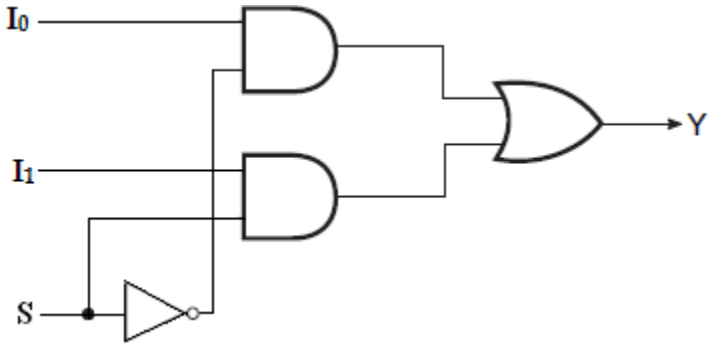


Block diagram of Multiplexer

2-to-1- line Multiplexer:

The circuit has two data input lines, one output line and one selection line, S. When S= 0, the upper AND gate is enabled and I_0 has a path to the output.

When S=1, the lower AND gate is enabled and I_1 has a path to the output.



Logic diagram

The multiplexer acts like an electronic switch that selects one of the two sources.

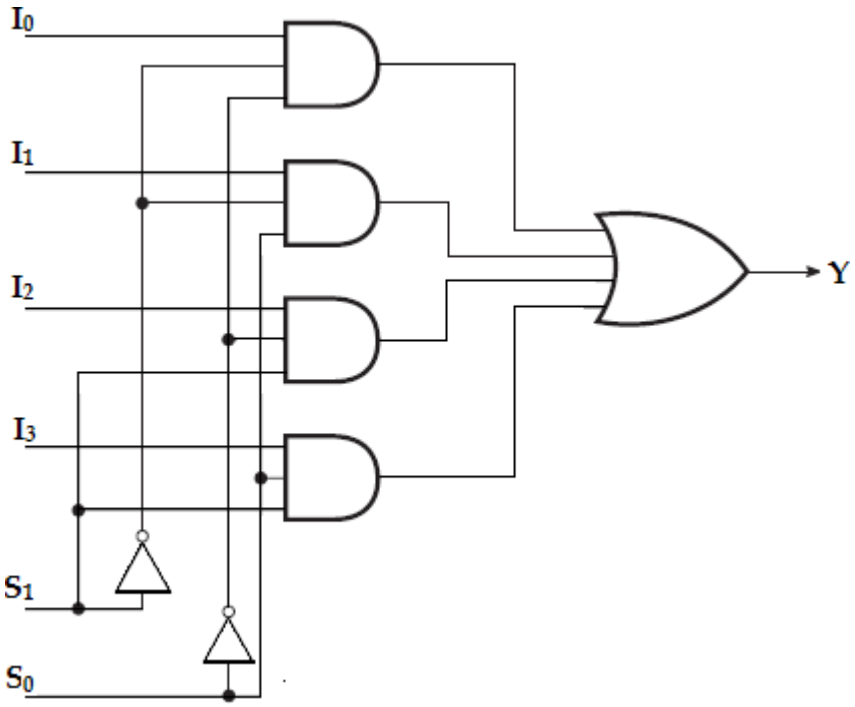
Truth table:

S	Y
0	I_0
1	I_1

4-to-1-line Multiplexer:

A 4-to-1-line multiplexer has four (2^n) input lines, two (n) select lines and one output line. It is the multiplexer consisting of four input channels and information of one of the channels can be selected and transmitted to an output line according to the select inputs combinations. Selection of one of the four input channel is possible by two selection inputs.

Each of the four inputs I_0 through I_3, is applied to one input of AND gate. Selection lines S_1 and S_0 are decoded to select a particular AND gate. The outputs of the AND gate are applied to a single OR gate that provides the 1-line output.



4-to-1-Line Multiplexer

Function table:

S1	S0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

To demonstrate the circuit operation, consider the case when S_1S_0= 10. The AND gate associated with input I_2 has two of its inputs equal to 1 and the third input connected to I_2. The other three AND gates have atleast one input equal to 0, which makes their outputs equal to 0. The OR output is now equal to the value of I_2, providing a path from the selected input to the output.

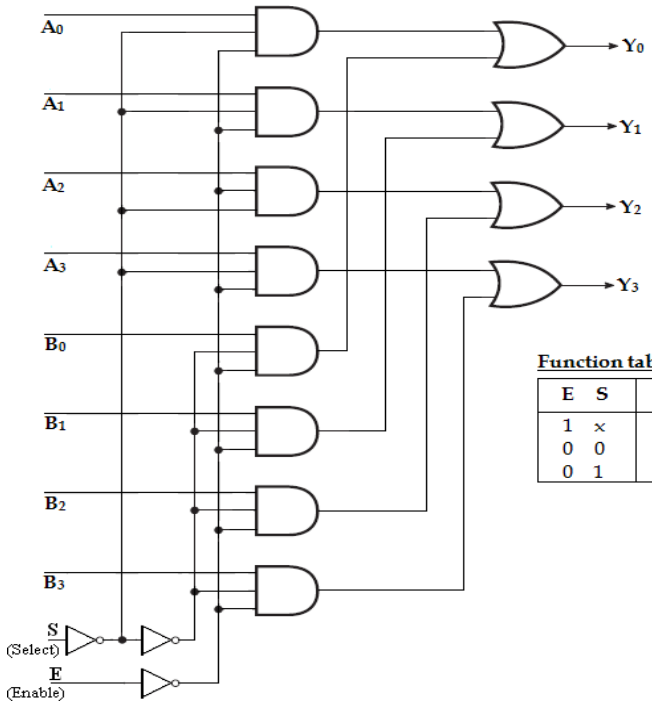
The data output is equal to I_0 only if S_1= 0 and S_0= 0; Y= I_0S_1'S_0'. The data output is equal to I_1 only if S_1= 0 and S_0= 1; Y= I_1S_1'S_0. The data output is equal to I_2 only if S_1= 1 and S_0= 0; Y= $I_2S_1S_0$'. The data output is equal to I_3 only if S_1= 1 and S_0= 1; Y= $I_3S_1S_0$.

When these terms are ORed, the total expression for the data output is,

Y= I_0S_1'S_0'+ I_1S_1'S_0 +$I_2S_1S_0$'+ $I_3S_1S_0$.

As in decoder, multiplexers may have an enable input to control the operation of the unit. When the enable input is in the inactive state, the outputs are disabled, and when it is in the active state, the circuit functions as a normal multiplexer.

Quadruple 2-to-1 Line Multiplexer:



Function table:

E	S	Output Y
1	x	All 0's
0	0	Select A
0	1	Select B

This circuit has four multiplexers, each capable of selecting one of two

input lines. Output Y0 can be selected to come from either A0 or B0. Similarly, output Y1may have the value of A1 or B1, and so on. Input selection line, S selects one of the lines in each of the four multiplexers. The enable input E must be active for normal operation.

Although the circuit contains four 2-to-1-Line multiplexers, it is viewed as a circuit that selects one of two 4-bit sets of data lines. The unit is enabled when E= 0. Then if S= 0, the four A inputs have a path to the four outputs. On the other hand, if S=1, the four B inputs are applied to the outputs. The outputs have all 0's when E= 1, regardless of the value of S.

Application:

The multiplexer is a very useful MSI function and has various ranges of applications in data communication. Signal routing and data communication are the important applications of a multiplexer. It is used for connecting two or more sources to guide to a single destination among computer units and it is useful for constructing a common bus system. One of the general properties of a multiplexer is that Boolean functions can be implemented by this device.

Implementation of Boolean Function using MUX:

Any Boolean or logical expression can be easily implemented using a multiplexer. If a Boolean expression has (n+1) variables, then _n' of these variables can be connected to the select lines of the multiplexer. The remaining single variable along with constants 1 and 0 is used as the input of the multiplexer. For example, if C is the single variable, then the inputs of the multiplexers are C, C', 1 and 0. By this method any logical expression can be implemented.

In general, a Boolean expression of (n+1) variables can be implemented using a multiplexer with 2^n inputs.

1. **Implement the following boolean function using 4: 1 multiplexer, F (A, B, C) = ∑m (1, 3, 5, 6).**

Solution:

Variables, n= 3 (A, B, C) Select lines= n-1 = 2 (**S1, S0**)

2^{n-1} to MUX i.e., 2^2 to 1 = 4 to 1 MUX Input lines= $2^{n-1} = 2^2$ = 4 (**D0, D1, D2, D3**)

Implementation table:

Apply variables A and B to the select lines. The procedures for implementing the function are:

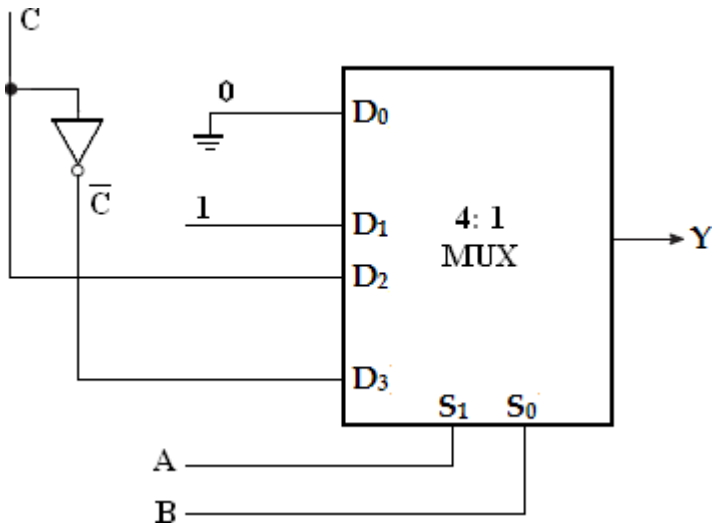
i. List the input of the multiplexer
ii. List under them all the minterms in two rows as shownbelow.

The first half of the minterms is associated with A‘ and the second half with A. The given function is implemented by circling the minterms of the function and applying the following rules to find the values for the inputs of the multiplexer.

1. If both the minterms in the column are not circled, apply 0 to the corresponding input.
2. If both the minterms in the column are circled, apply 1 to the corresponding input.
3. If the bottom minterm is circled and the top is not circled, apply C to the input.
4. If the top minterm is circled and the bottom is not circled, apply C‘ to the input.

	D_0	D_1	D_2	D_3
$\overline{C}$	0	(1)	2	(3)
C	4	(5)	(6)	7
	0	**1**	C	$\overline{C}$

Multiplexer Implementation:



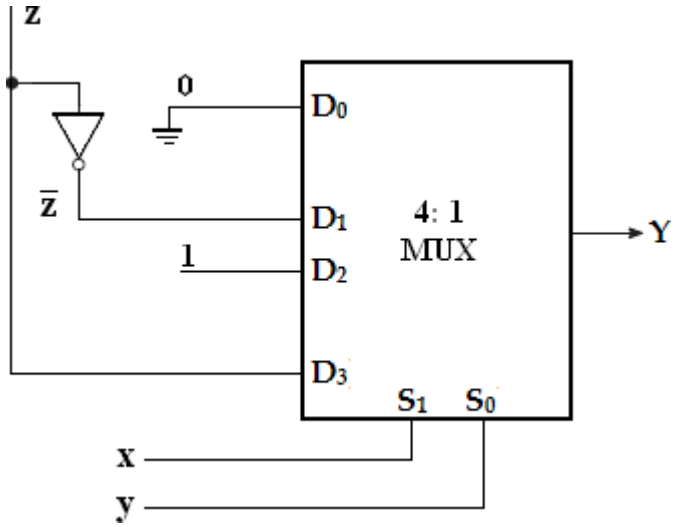
2. F (x, y, z) = ∑m (1, 2, 6, 7)

Solution:

Implementation table:

	D_0	D_1	D_2	D_3
$\bar{z}$	0	(1)	(2)	3
z	4	5	(6)	(7)
	0	$\bar{z}$	**1**	**z**

Multiplexer Implementation:



3. **F (A, B, C) = ∑m (1, 2, 4, 5)**

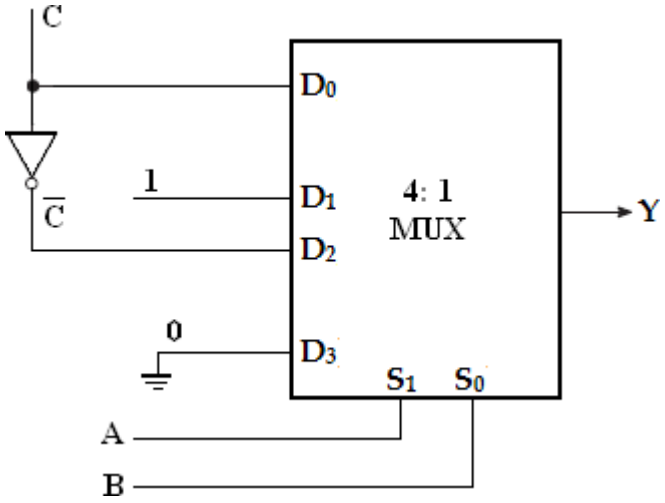
Solution:

Variables, n= 3 (A,
B, C) Select lines=
n-1 = 2 (**S1, S0**)
2^{n-1} to MUX i.e., 2^2 to 1 = 4 to 1
MUX Input lines= $2^{n-1} = 2^2 = 4$
(**D0, D1, D2, D3**)

Implementation table:

	D_0	D_1	D_2	D_3
$\overline{C}$	0	1	2	3
C	4	5	6	7
	C	1	$\overline{C}$	0

Multiplexer Implementation:



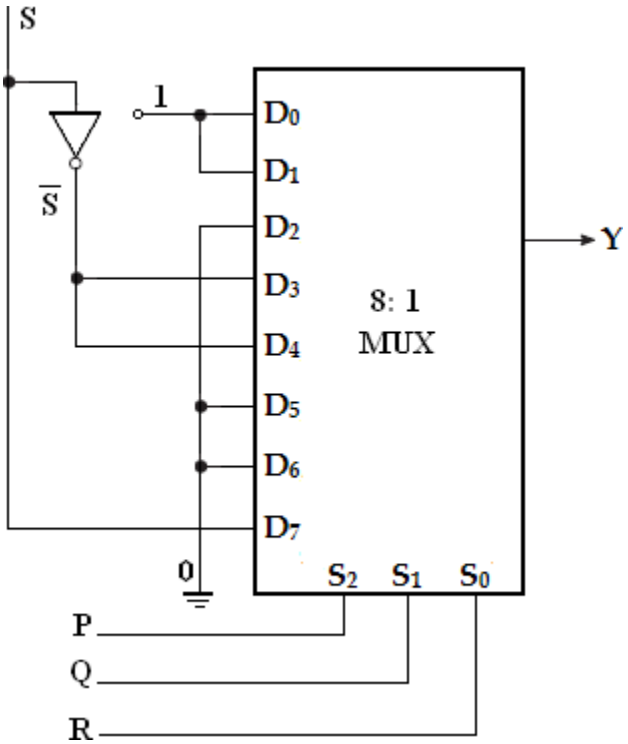
4. F(P, Q, R, S)= ∑m (0, 1, 3, 4, 8, 9, 15)

Solution:

Variables, n= 4 (P, Q, R,
S) Select lines= n-1 = 3
(**S2, S1, S0**)
2^{n-1} to MUX i.e., 2^3 to 1 = 8 to 1 MUX
Input lines= $2^{n-1} = 2^3$ = 8 (**D0, D1, D2, D3, D4, D5, D6, D7**)

Implementation table:

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\overline{S}$	0	1	2	3	4	5	6	7
S	8	9	10	11	12	13	14	15
	1	**1**	**0**	$\overline{S}$	$\overline{S}$	**0**	**0**	**S**



Multiplexer Implementation:

5. **Implement the Boolean function using 8: 1 and also using 4:1 multiplexer F (A, B, C, D) = ∑m (0, 1, 2, 4, 6, 9, 12, 14)**

Solution:

Variables, n= 4 (A, B, C, D) Select lines= n-1 = 3 (**S2, S1, S0**)

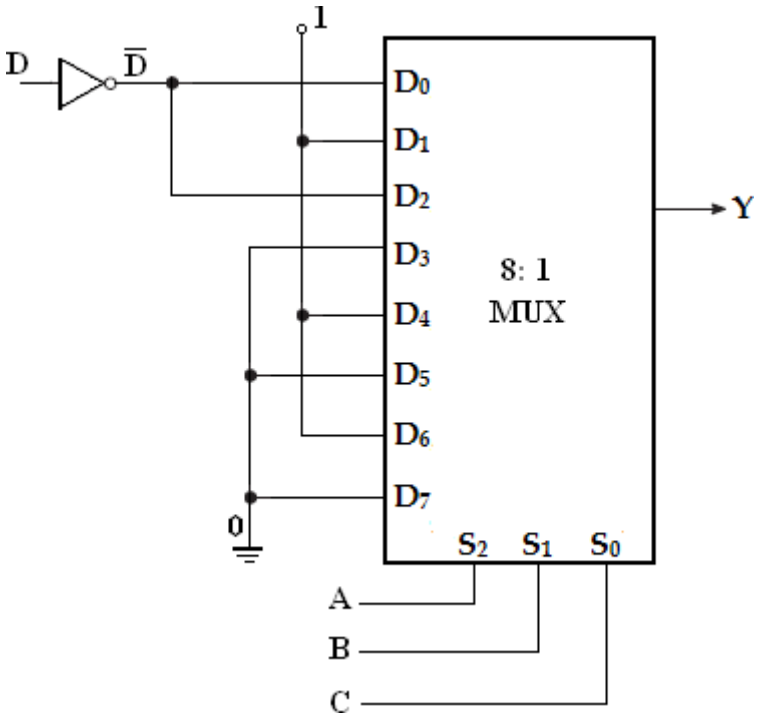
2^{n-1} to MUX i.e., 2^3 to 1 = 8 to 1 MUX

Input lines= $2^{n-1} = 2^3 = 8$ (**D0, D1, D2, D3, D4, D5, D6, D7**)

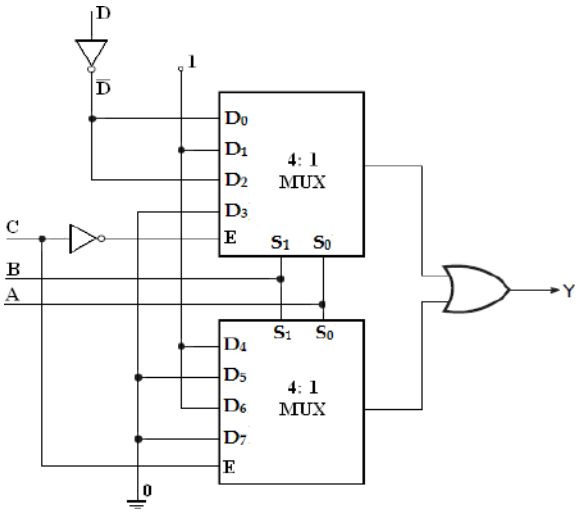
Implementation table:

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\overline{D}$	0	1	2	3	4	5	6	7
D	8	9	10	11	12	13	14	15
	$\overline{D}$	**1**	$\overline{D}$	**0**	**1**	**0**	**1**	**0**

Multiplexer Implementation (Using 8: 1 MUX):



Using 4: 1 MUX:



6. F (A, B, C, D) = ∑m (1, 3, 4, 11, 12, 13, 14, 15)

Solution:

Variables, n= 4 (A, B, C, D) Select lines= n-1 = 3 (**S2, S1, S0**)

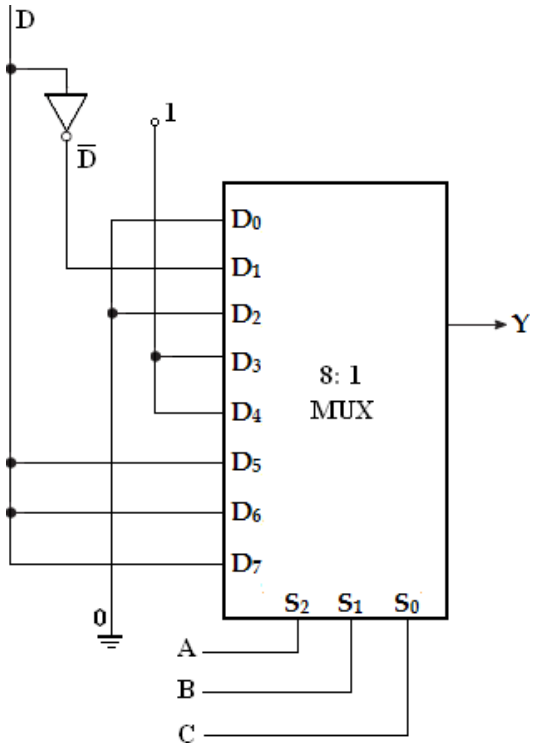
2^{n-1} to MUX i.e., 2^3 to 1 = 8 to 1 MUX

Input lines= $2^{n-1} = 2^3 = 8$ (**D0, D1, D2, D3, D4, D5, D6, D7**)

Implementation table:

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\overline{D}$	0	(1)	2	(3)	(4)	5	6	7
D	8	9	10	(11)	(12)	(13)	(14)	(15)
	0	$\overline{D}$	**0**	**1**	**1**	D	D	D

Multiplexer Implementation:



6. Implement the Boolean function using 8: 1 multiplexer.

F (A, B, C, D) = A'BD' + ACD + B'CD + A'C'D.

Solution:

Convert into standard SOP form,

= A‘BD‘ (C‘+C) + ACD (B‘+B) + B‘CD (A‘+A) + A‘C‘D (B‘+B)

= A‘BC‘D‘ + A‘BCD‘+ AB‘CD + ABCD +A‘B‘CD + AB‘CD +A‘B‘C‘D+ A‘BC‘D

= A‘BC‘D‘ + A‘BCD‘+ AB‘CD + ABCD +A‘B‘CD +A‘B‘C‘D+ A‘BC‘D

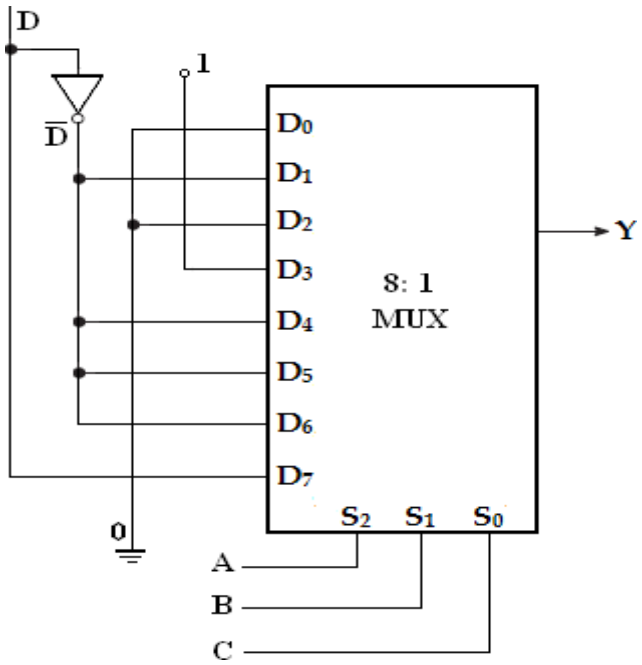
= m4+ m6+ m11+ m15+ m3+ m1+ m5

= ∑m (1, 3, 4, 5, 6, 11, 15)

Implementation table:

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\overline{D}$	0	(1)	2	(3)	(4)	(5)	(6)	7
D	8	9	10	(11)	12	13	14	(15)
	0	$\overline{D}$	**0**	**1**	$\overline{D}$	$\overline{D}$	$\overline{D}$	D

Multiplexer Implementation:



7. Implement the Boolean function using 8: 1 multiplexer.

F (A, B, C, D) = AB'D + A'C'D + B'CD' + AC'D.

Solution:

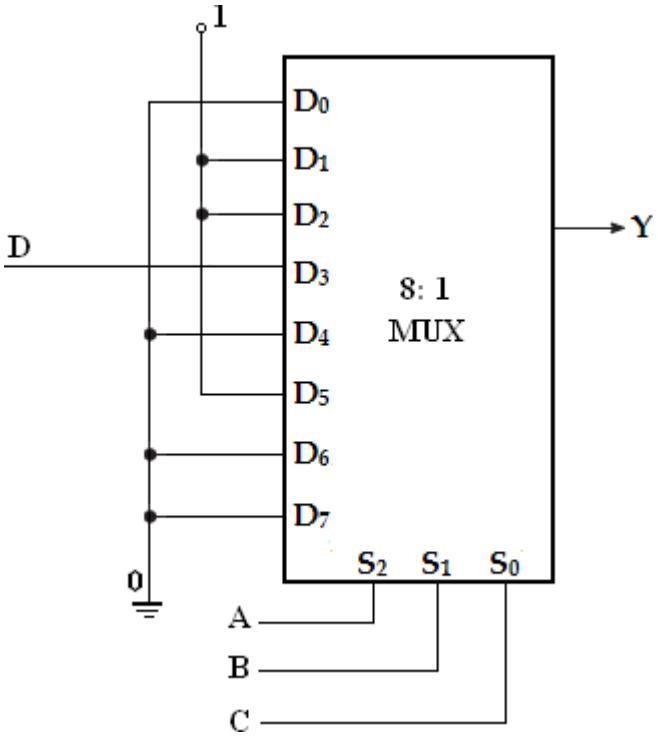
Convert into standard SOP form,

= AB‘D (C‘+C) + A‘C‘D (B‘+B) + B‘CD‘ (A‘+A) + AC‘D (B‘+B)
= AB‘C‘D + AB‘CD+ A‘B‘C‘D + A‘BC‘D +A‘B‘CD‘ + AB‘CD‘
+AB‘C‘D+ ABC‘D
= AB‘C‘D + AB‘CD+ A‘B‘C‘D + A‘BC‘D +A‘B‘CD‘ + AB‘CD‘+ ABC‘D
= m9+ m11+ m1+ m5+ m2+ m10+ m13
= ∑m (1, 2, 5, 9, 10, 11, 13).

Implementation Table:

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\overline{D}$	0	(1)	(2)	3	4	(5)	6	7
D	8	(9)	(10)	(11)	12	(13)	14	15
	0	**1**	**1**	D	**0**	**1**	**0**	**0**

Multiplexer Implementation:



8. Implement the Boolean function using 8: 1 and also using 4:1 multiplexer

F (w, x, y, z) = ∑m (1, 2, 3, 6, 7, 8, 11, 12, 14)

Solution:

Variables, n= 4 (w, x, y,
z) Select lines= n-1 = 3

(**S2, S1, S0**)

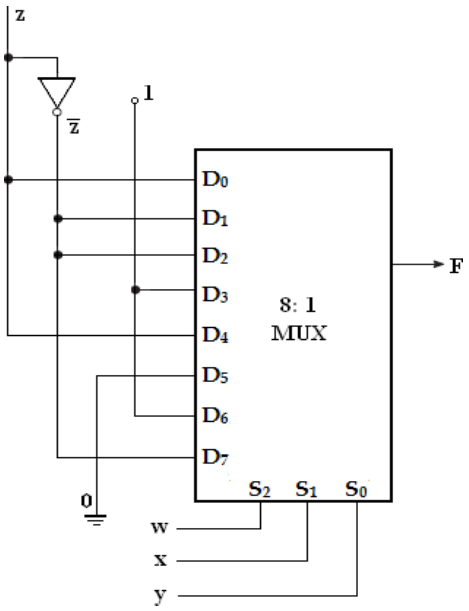
2^{n-1} to MUX i.e., 2^3 to 1 = 8 to 1 MUX

Input lines= $2^{n-1} = 2^3 = 8$ (**D0, D1, D2, D3, D4, D5, D6, D7**)

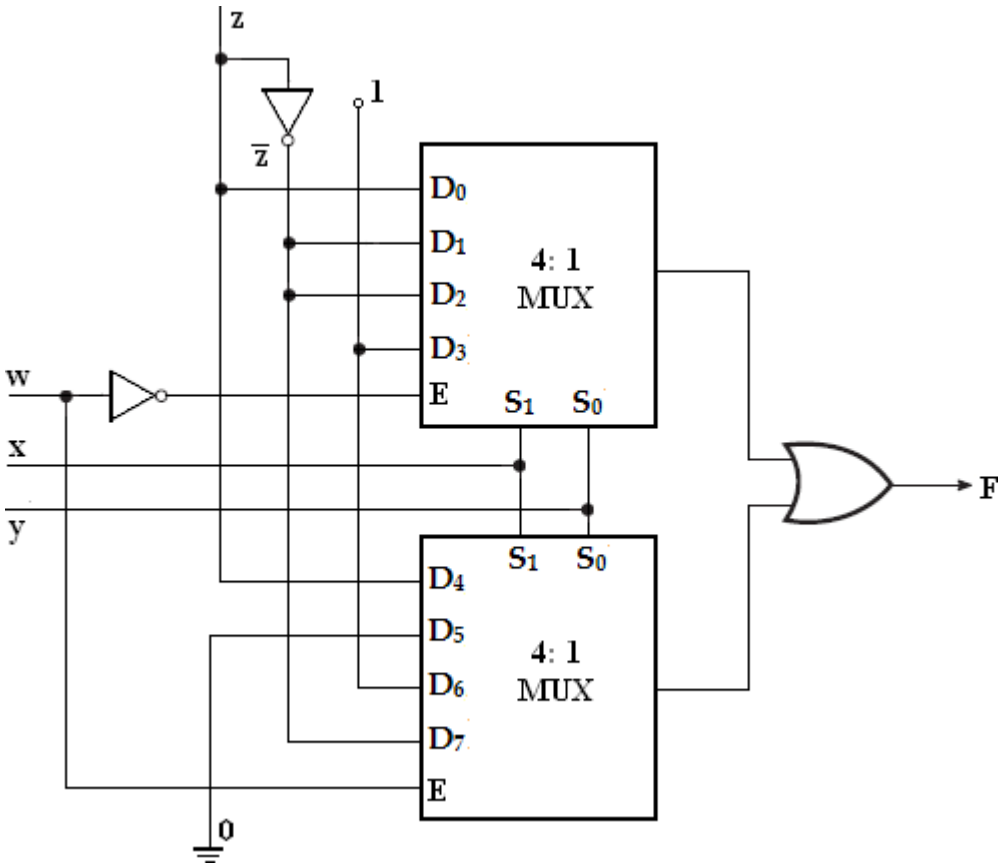
Implementation table:

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{z}$	0	(1)	(2)	(3)	4	5	(6)	(7)
z	(8)	9	10	(11)	(12)	13	(14)	15
	z	$\bar{z}$	$\bar{z}$	**1**	z	**0**	**1**	$\bar{z}$

Multiplexer Implementation (Using 8:1 MUX):



(Using 4:1 MUX):



9. Implement the Boolean function using 8: 1 multiplexer

F (A, B, C, D) = ∏m (0, 3, 5, 8, 9, 10, 12, 14)

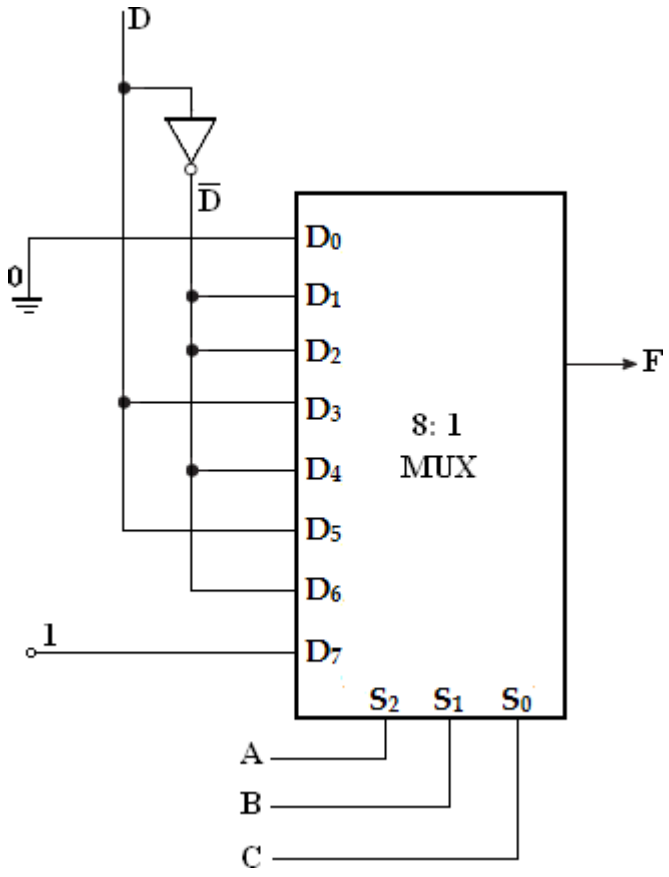
Solution:

Variables, n= 4 (A, B, C, D) Select lines= n-1 = 3 (**S2, S1, S0**)
2^{n-1} to MUX i.e., 2^3 to 1 = 8 to 1 MUX
Input lines= $2^{n-1} = 2^3 = 8$ (**D0, D1, D2, D3, D4, D5, D6, D7**)

Implementation table:

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\overline{D}$	0	(1)	(2)	3	(4)	5	(6)	(7)
D	8	9	10	(11)	12	(13)	14	(15)
	0	$\overline{D}$	$\overline{D}$	D	$\overline{D}$	D	$\overline{D}$	**1**

Multiplexer Implementation:



10. Implement the Boolean function using 8: 1 multiplexer

F (A, B, C, D) = ∑m (0, 2, 6, 10, 11, 12, 13) + d (3, 8, 14)

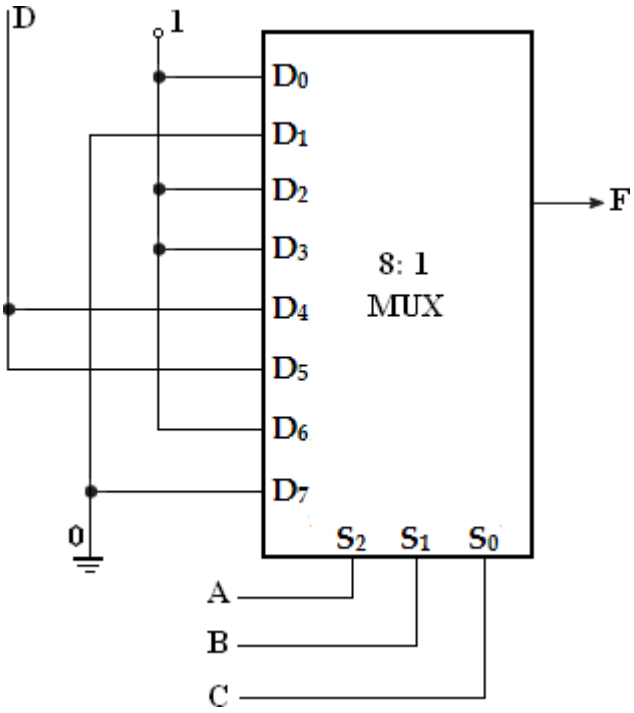
Solution:

Variables, n= 4 (A, B, C, D) Select lines= n-1 = 3 (**S2, S1, S0**)
2^{n-1} to MUX i.e., 2^3 to 1 = 8 to 1 MUX
Input lines= $2^{n-1} = 2^3 = 8$ (**D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7**)

Implementation Table:

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\overline{D}$	(0)	1	(2)	(3)	4	5	(6)	7
D	(8)	9	(10)	(11)	(12)	(13)	(14)	15
	1	**0**	**1**	**1**	**D**	**D**	**1**	**0**

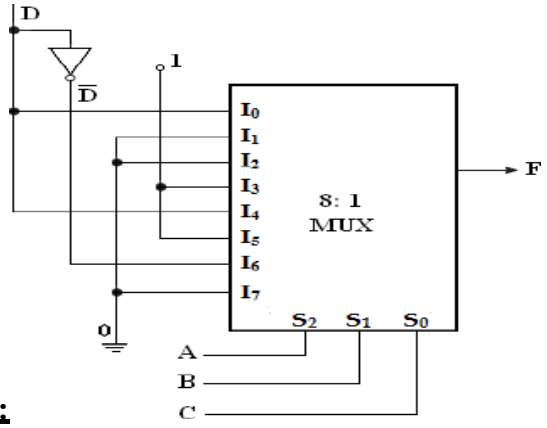
Multiplexer Implementation:



11. An 8×1 multiplexer has inputs A, B and C connected to the selection inputs S2, S1, and S0 respectively. The data inputs I0 to I7 are as follows

$I_1=I_2=I_7=0$; $I_3=I_5=1$; $I_0=I_4=D$ and **$I_6=D'$.**

Determine the Boolean function that the multiplexer implements.



Multiplexer Implementation:

Implementation table:

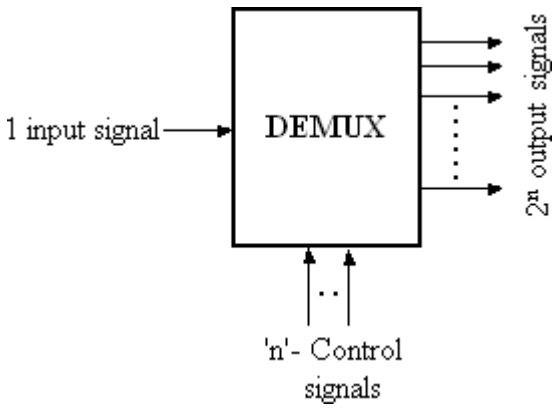
	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\overline{D}$	0	1	2	(3)	4	(5)	(6)	7
D	(8)	9	10	(11)	(12)	(13)	14	15
	D	0	0	1	D	1	$\overline{D}$	0

F (A, B, C, D) = ∑m (3, 5, 6, 8, 11, 12, 13).

DEMULTIPLEXER:

Demultiplex means one into many. Demultiplexing is the process of taking information from one input and transmitting the same over one of several outputs.

A demultiplexer is a combinational logic circuit that receives information on a single input and transmits the same information over one of several (2^n) output lines.

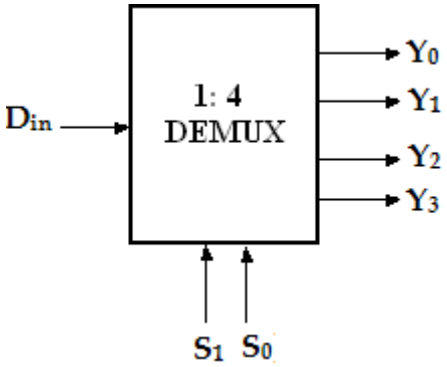


Block diagram of demultiplexer

The block diagram of a demultiplexer which is opposite to a multiplexer in its operation is shown above. The circuit has one input signal, _n' select signals and 2^n output signals. The select inputs determine to which output the data input will be connected. As the serial data is changed to parallel data, i.e., the input caused to appear
on one of the n output lines, the demultiplexer is also called a —***data distributer***‖ or a —***serial-to-parallel converter***‖.

1-to-4 Demultiplexer:

A 1-to-4 demultiplexer has a single input, D_{in}, four outputs (Y_0 to Y_3) and two select inputs (S_1 and S_0).



Logic Symbol

The input variable D_{in} has a path to all four outputs, but the input information is directed to only one of the output lines. The truth table of the 1-to-4 demultiplexer is shown below.

Enable	S1	S0	Din	Y0	Y1	Y2	Y3
0	x	x	x	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	1	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	1

Truth table of 1-to-4 demultiplexer

From the truth table, it is clear that the data input, D_{in} is connected to the output Y_0, when S_1= 0 and S_0= 0 and the data input is connected to output Y_1 when S_1= 0 and S_0= 1. Similarly, the data input is connected to output Y_2 and Y_3 when S_1= 1 and S_0= 0 and when S_1= 1 and S_0= 1, respectively. Also, from the truth table, the expression for outputs can be written as follows,

$Y_0 = S_1'S_0'D_{in}$

$Y_1 = S_1'S_0D_{in}$

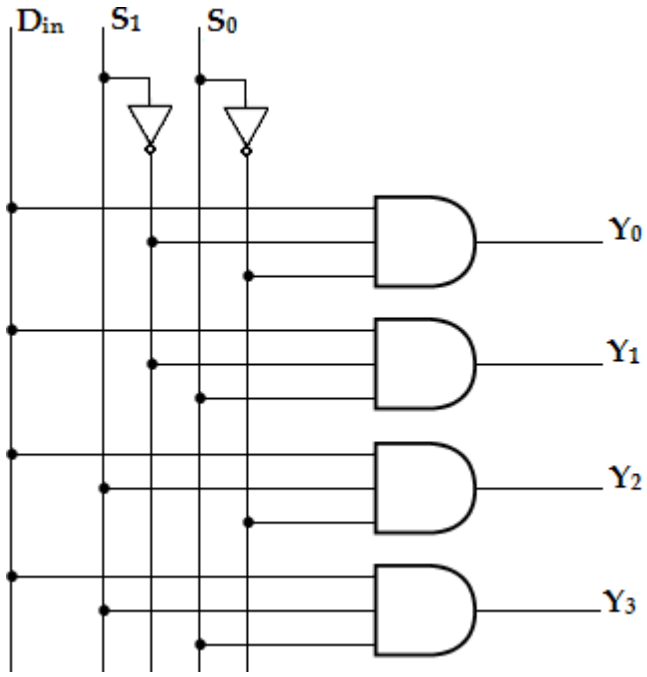
$Y_2 = S_1S_0'D_{in}$

$Y_3 = S_1S_0D_{in}$

Now, using the above expressions, a 1-to-4 demultiplexer can be implemented using four 3-input AND gates and two NOT gates. Here, the input data line D_{in}, is connected to all the AND gates. The two select lines S_1, S_0 enable only one gate at a time and the data that appears on the input line passes through

the selected gate to the associated output line.

Logic diagram of 1-to-4 demultiplexer



1-to-8 Demultiplexer:

A 1-to-8 demultiplexer has a single input, **Din**, eight outputs (**Y0 to Y7**) and three select inputs (**S2, S1 and S0**). It distributes one input line to eight output lines based on the select inputs. The truth table of 1-to-8 demultiplexer is shown below.

Truth table of 1-to-8 demultiplexer

Din	S2	S1	S0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

From the above truth table, it is clear that the data input is connected with one of the eight outputs based on the select inputs. Now from this truth table, the expression for eight outputs can be written as follows:

Y0= ‘S2‘S1‘S0Din

Y1= ‘S2‘S1S0Din

Y2= ‘S2S1‘S0Din

Y3= ‘S2S1S0Din

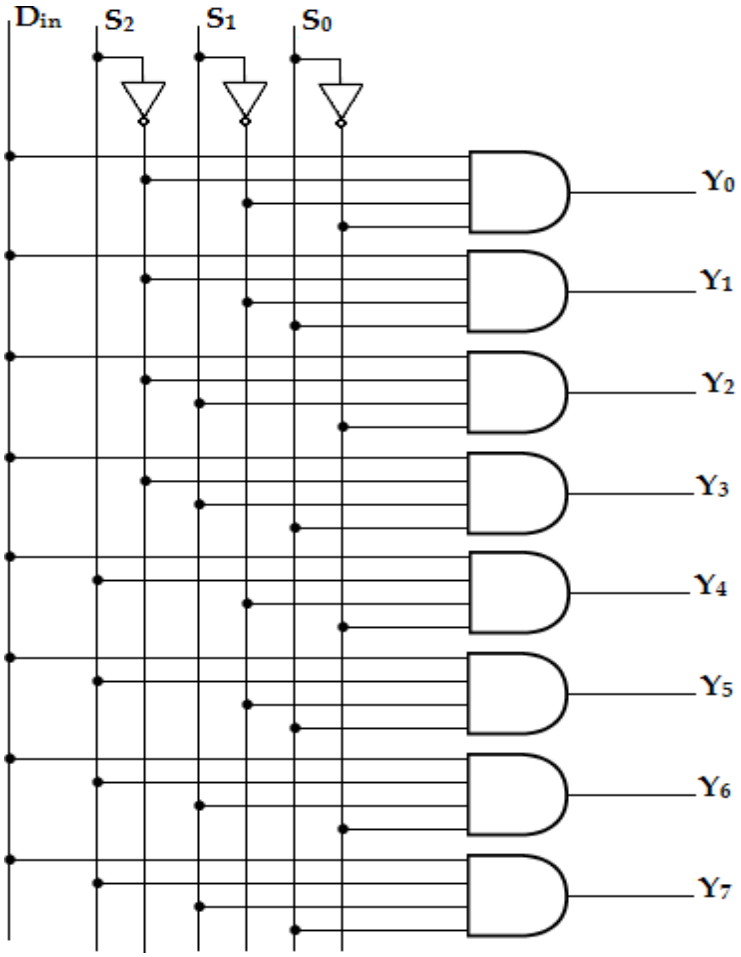
Y4=S2‘S1‘S0Din

Y5= S2 ‘S1 S0Din

Y6= S2 S1‘S0Din

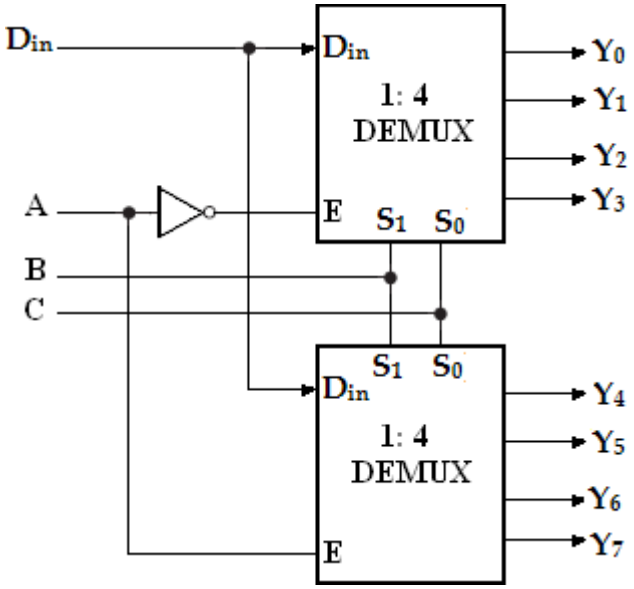
Y7= S2S1S0Din

Now using the above expressions, the logic diagram of a 1-to-8 demultiplexer can be drawn as shown below. Here, the single data line, Din is connected to all the eight AND gates, but only one of the eight AND gates will be enabled by the select input lines. For example, if S2S1S0= 000, then only AND gate-0 will be enabled and thereby the data input, Din will appear at Y0. Similarly, the different combinations of the select inputs, the input Din will appear at the respective output.



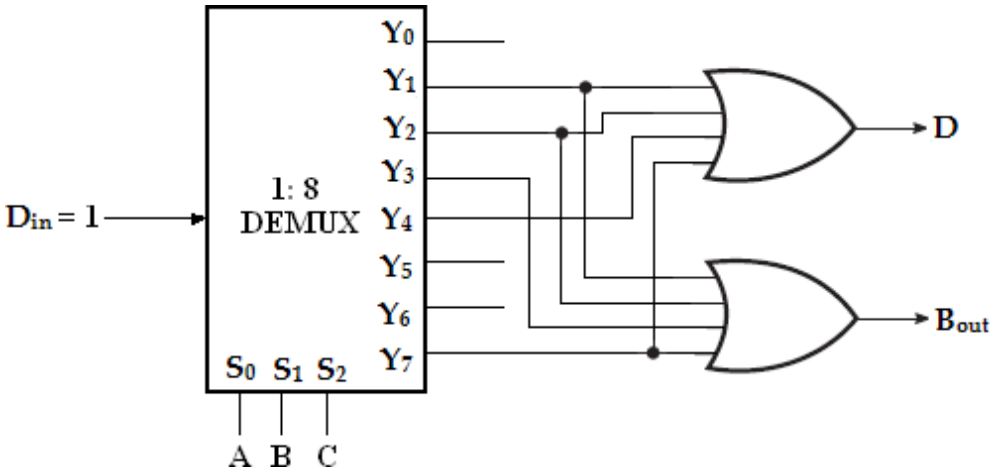
Logic diagram of 1-to-8 demultiplexer

1. Design 1:8 demultiplexer using two 1:4DEMUX.



2. Implement full subtractor using demultiplexer.

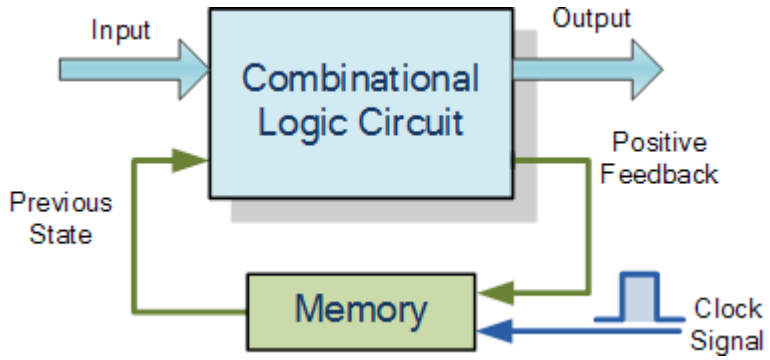
Inputs			Outputs	
A	**B**	**Bin**	**Difference(D)**	**Borrow(B_{out})**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



UNIT – III SYNCHRONOUS SEQUENTIAL CIRCUITS
Sequential logic- SR, JK, D and T flip flops - level triggering and edge triggering - counters - asynchronous and synchronous type - Modulo counters - Shift registers - design of synchronous sequential circuits – Moore and Melay models- Counters, state diagram; state reduction; state assignment.

SEQUENTIAL CIRCUITS

This sequential circuit contains a set of inputs and outputs. The outputs of sequential circuit depends not only on the combination of present inputs but also on the previous outputs. Previous output is nothing but the present state. Therefore, sequential circuits contain combinational circuits along with memory storage elements. Some sequential circuits may not contain combinational circuits, but only memory elements.



Block diagram of Sequential Circuit

The differences between combinational circuits and sequential circuits.

Combinational Circuits	Sequential Circuits
Outputs depend only on present inputs.	Outputs depend on both present inputs and present state.
Feedback path is not present.	Feedback path is present.
Memory elements are not required.	Memory elements are required.
Clock signal is not required.	Clock signal is required.
Easy to design.	Difficult to design.
Eg. Parallel Adder.	Eg. Serial Adder.

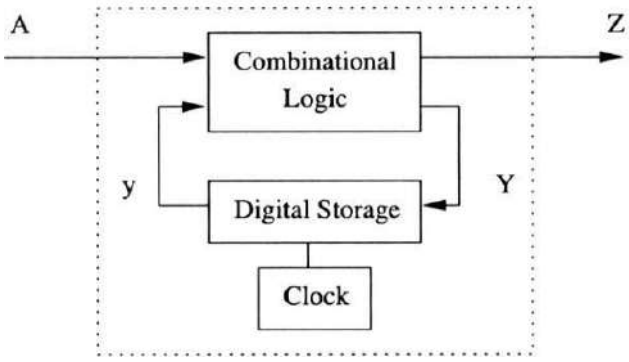
TYPES OF SEQUENTIAL CIRCUITS

The sequential circuits are classified into two types;

- Synchronous sequential circuits
- Asynchronous sequential circuits

Synchronous Circuits

In synchronous circuits, the inputs are pulses with certain restrictions on pulse width and propagation delay. Thus synchronous circuits can be divided into clocked and un-clocked or pulsed sequential circuits.

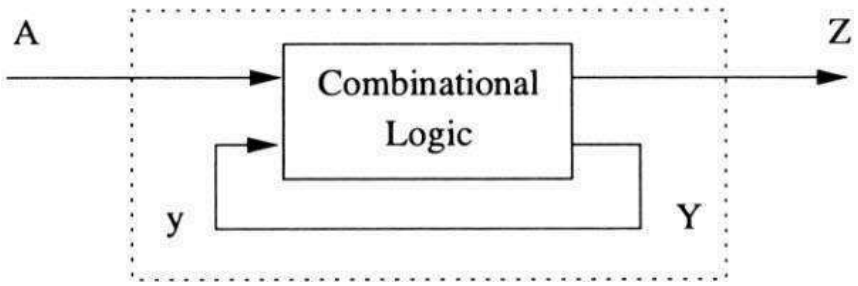


Synchronous Circuit

If all the outputs of a sequential circuit change affect with respect to active transition of clock signal, then that sequential circuit is called as Synchronous sequential circuit. That means, all the outputs of synchronous sequential circuits change affect at the same time. Therefore, the outputs of synchronous sequential circuits are in synchronous with either only positive edges or only negative edges of clock signal.

Asynchronous Circuits

An asynchronous circuit does not have a clock signal to synchronize its internal changes of the state. Hence the state change occurs in direct response to changes that occur in primary input lines. An asynchronous circuit does not require precise timing control from flip-flops.



Asynchronous Circuit

If some or all the outputs of a sequential circuit do not change affect with respect to active transition of clock signal, then that sequential circuit is called as Asynchronous sequential circuit. That means, all the outputs of asynchronous sequential circuits do not change affect at the same time. Therefore, most of the outputs of asynchronous sequential circuits are not in synchronous with either only positive edges or only negative edges of clock signal.

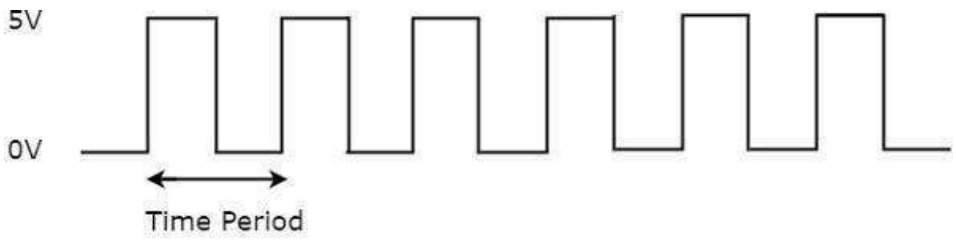
The differences between Synchronous and Asynchronous sequential circuits.

Synchronous Circuits	Asynchronous Circuits
Memory elements are clocked Flip Flops / Latches.	Memory elements are either un-clocked Latches or time delay elements.
The change in input signals can affect memory element upon activation of clock signal.	The change in input signals can affect memory element at any instant of time.
The maximum operating speed of clock depends on time delays involved.	Because of absence of clock, asynchronous circuits can operate faster than synchronous circuits.
Easier to design.	More difficult to design.

CLOCK SIGNAL AND TRIGGERING

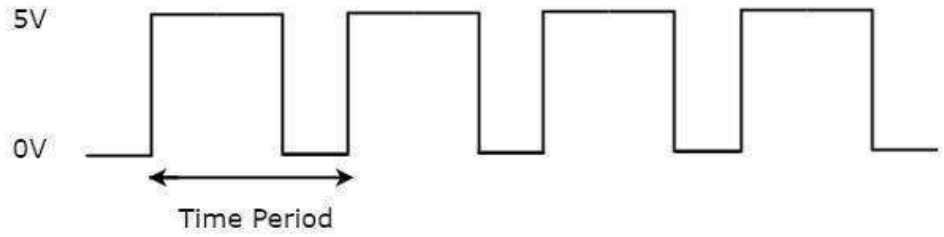
Clock signal

Clock signal is a periodic signal and its ON time and OFF time need not be the same. We can represent the clock signal as a **square wave**, when both its ON time and OFF time are same. This clock signal is shown in the following figure.



The above figure, square wave is considered as clock signal. This signal stays at logic High 5V for some time and stays at logic Low 0V for equal amount of time. This pattern repeats with some time period. In this case, the **time period** will be equal to either twice of ON time or twice of OFF time.

We can represent the clock signal as **train of pulses**, when ON time and OFF time are not same. This clock signal is shown in the following figure.



In the above figure, train of pulses is considered as clock signal. This signal stays at logic High 5V for some time and stays at logic Low 0V for some other time. This pattern repeats with some time period. In this case, the **time period** will be equal to sum of ON time and OFF time.

Types of Triggering

Following are the two possible types of triggering that are used in sequential circuits.

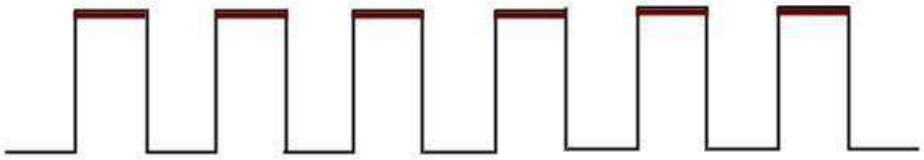
- Level triggering
- Edge triggering

Level triggering

There are two levels, namely logic High and logic Low in clock signal. Following are the two **types of level triggering**.

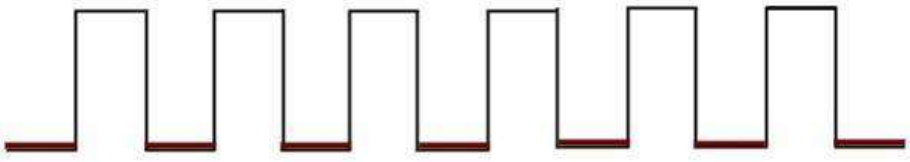
- Positive level triggering
- Negative level triggering

If the sequential circuit is operated with the clock signal when it is in **Logic High**, then that type of triggering is known as **Positive level triggering**. It is highlighted in below figure.



Positive Level Triggering

If the sequential circuit is operated with the clock signal when it is in **Logic Low**, then that type of triggering is known as **Negative level triggering**. It is highlighted in the following figure.



Negative Level Triggering

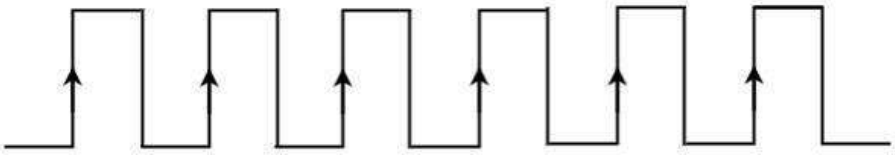
Edge triggering

There are two types of transitions that occur in clock signal. That means, the clock signal transitions either from Logic Low to Logic High or Logic High to Logic Low.

There are the two **types of edge triggering** based on the transitions of clock signal.

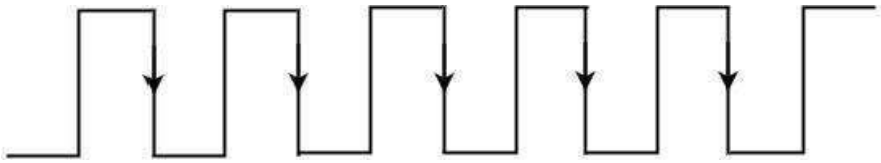
- Positive edge triggering
- Negative edge triggering

If the sequential circuit is operated with the clock signal that is transitioning from Logic Low to Logic High, then that type of triggering is known as **Positive edge triggering**. It is also called as rising edge triggering. It is shown in the following figure.



Positive edge triggering

If the sequential circuit is operated with the clock signal that is transitioning from Logic High to Logic Low, then that type of triggering is known as **Negative edge triggering**. It is also called as falling edge triggering. It is shown in the following figure.



Negative edge triggering

LATCHES & FLIP-FLOPS

Latches and Flip-Flops are the basic building blocks of the most sequential circuits. Latches are used for a sequential device that checks all of its inputs continuously and changes its outputs accordingly at any time independent of clocking signal. Enable signal is provided with the latch. When enable signal is active output changes occur as the input changes. But when enable signal is not activated input changes do not affect the output.

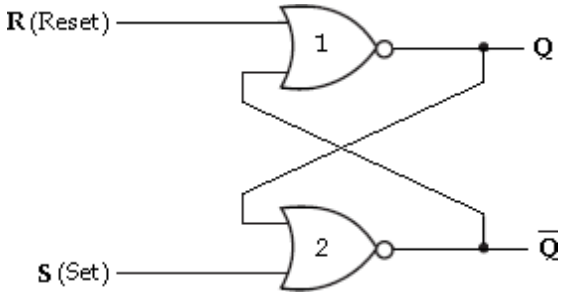
Flip-Flop is used for a sequential device that normally samples its inputs and changes its outputs only at times determined by clocking signal.

SR Latch

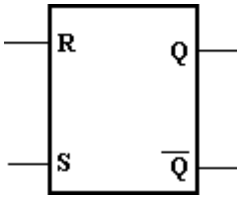
The simplest type of latch is the set-reset (SR) latch. It can be constructed from either two NOR gates or two NAND gates.

SR latch using NOR gates:

The two NOR gates are cross-coupled so that the output of NOR gate 1 is connected to one of the inputs of NOR gate 2 and vice versa. The latch has two outputs Q and Q' and two inputs, set and reset.



SR Latch using NOR gates



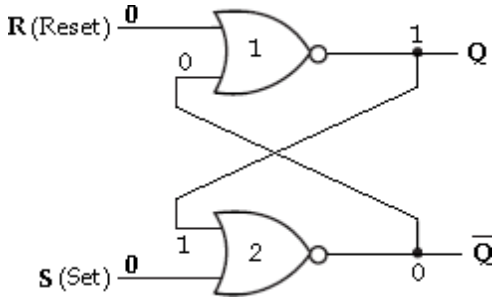
Logic Symbol

Before going to analyse the SR latch, we recall that a logic 1 at any input of a NOR gate forces its output to a logic 0. Let us understand the operation of this circuit for various input/ output possibilities.

Case 1: S = 0 and R = 0

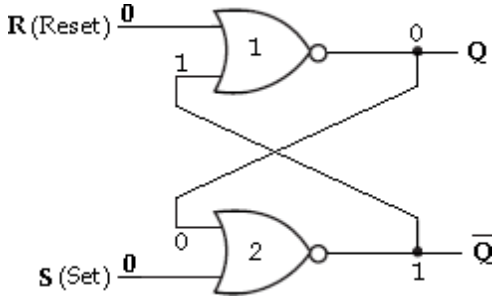
Initially, Q= 1 and Q'= 0

Let us assume that initially Q=1 and Q'=0. With Q'=0, both inputs to NOR gate-1 are at logic 0. So, its output, Q is at logic 1. With Q=1, one input of NOR gate-2 is at logic 1. Hence its output, Q' is at logic 0. This shows that when S and R both are low, the output does not change.



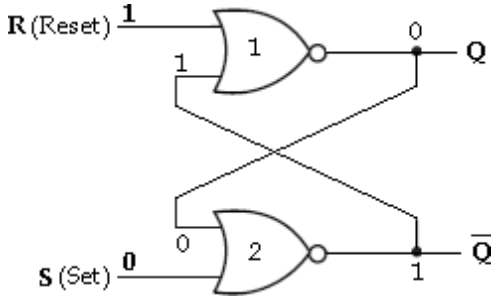
Initially, Q= 0 and Q'= 1

With Q'=1, one input of NOR gate 1 is at logic 1, hence its output, Q is at logic 0. With Q=0, both inputs to NOR gate-2 are at logic 0. So, its output Q' is at logic 1. In this case also there is no change in the output state.



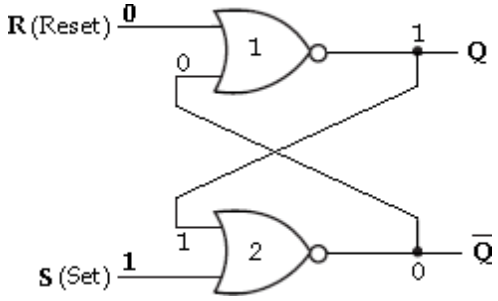
Case 2: S= 0 and R= 1

In this case, R input of the NOR gate-1 is at logic 1, hence its output, Q is at logic 0. Both inputs to NOR gate-2 are now at logic 0. So that its output, Q' is at logic 1.



Case 3: S= 1 and R= 0

In this case, S input of the NOR gate-2 is at logic 1, hence its output, Q is at logic 0. Both inputs to NOR gate-1 are now at logic 0. So that its output, Q is at logic 1.



Case 4: S= 1 and R= 1

When R and S both are at logic 1, they force the outputs of both NOR gates to the low state, i.e., (Q=0 and Q'=0). So, we call this an indeterminate or prohibited state, and represent this condition in the truth table as an asterisk (*). This condition also violates the basic definition of a latch that requires Q to be complement of Q'. Thus in normal operation this

condition must be avoided by making sure that 1's are not applied to both the inputs simultaneously.

We can summarize the operation of SR latch as follows:

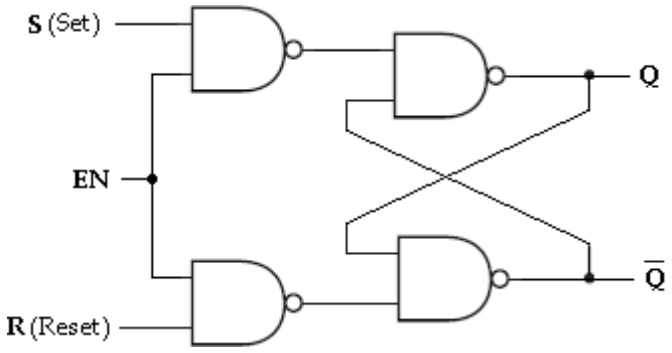
• When S= 0 and R= 0, the output, Qn+1 remains in its present state, Qn.
• When S= 0 and R= 1, the latch is reset to 0.
• When S= 1 and R= 0, the latch is set to 1.
• When S= 1 and R= 1, the output of both gates will produce 0. i.e., **Qn+1= Qn+1'= 0.**

S	R	Q_n	Q_{n+1}	State
0	0	0	0	No Change (NC)
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	x	Indeterminate *
1	1	1	x	
x	x	0	0	No Change (NC)
x	x	1	1	

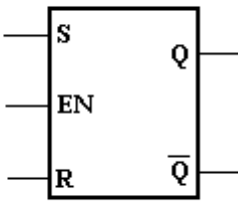
Truth Table of SR latch using NOR gates

Gated SR Latch

In the SR latch, the output changes occur immediately after the input changes i.e, the latch is sensitive to its S and R inputs all the time. A latch that is sensitive to the inputs only when an enable input is active. Such a latch with enable input is known as gated SR latch. The circuit behaves like SR latch when EN= 1. It retains its previous state when EN= 0.



SR Latch with enable input using NAND gates

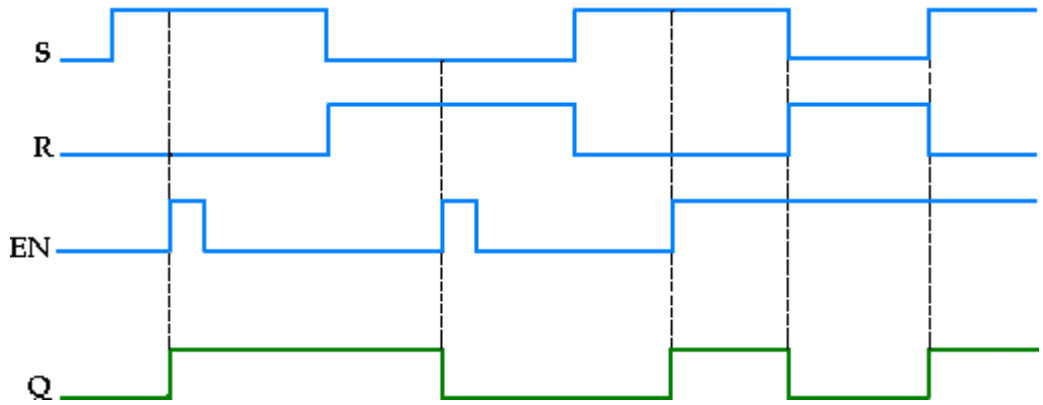


Logic Symbol

The truth table of gated SR latch is show below.

EN	S	R	Qn	Qn+1	State
1	0	0	0	0	No Change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	x	Indeterminate *
1	1	1	1	x	
0	x	x	0	0	No Change (NC)
0	x	x	1	1	

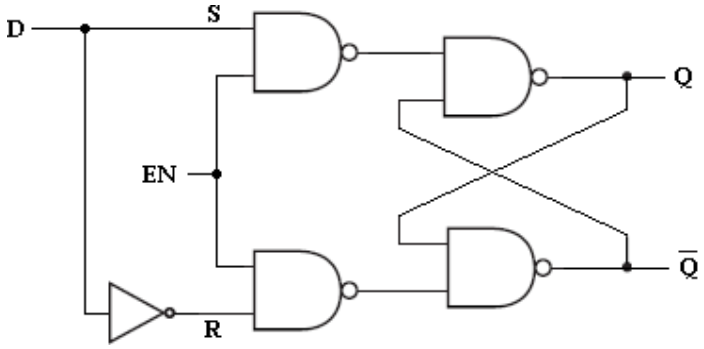
When S is HIGH and R is LOW, a HIGH on the EN input sets the latch. When S is LOW and R is HIGH, a HIGH on the EN input resets the latch.



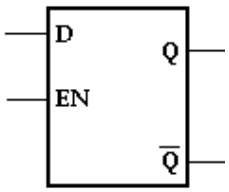
Input and Output waveforms of SR latch

D Latch

In SR latch, when both inputs are same (00 or 11), the output either does not change or it is invalid. In many practical applications, these input conditions are not required. These input conditions can be avoided by making them complement of each other. This modified SR latch is known as **D latch.**



D Latch



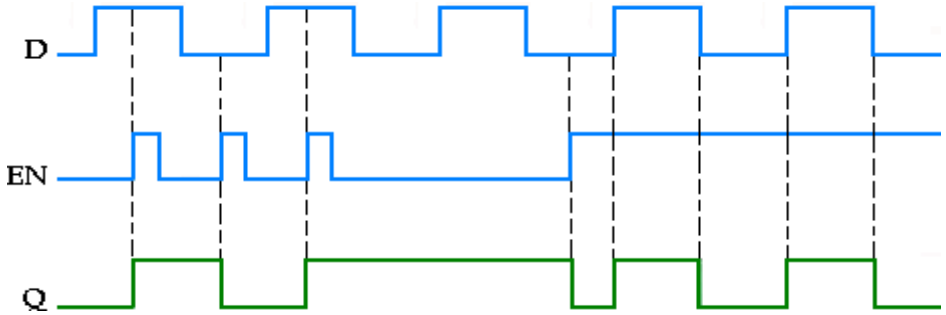
Logic Symbol

As shown in the figure, D input goes directly to the S input, and its complement is applied to the R input. Therefore, only two input conditions exists, either S=0 and R=1 or S=1 and R=0. The truth table for D latch is shown below.

EN	D	Qn	Qn+1	State
1	0	x	0	Reset
1	1	x	1	Set
0	x	x	Qn	No Change (NC)

As shown in the truth table, the Q output follows the D input. For this reason, D latch is called ***transparent latch***.

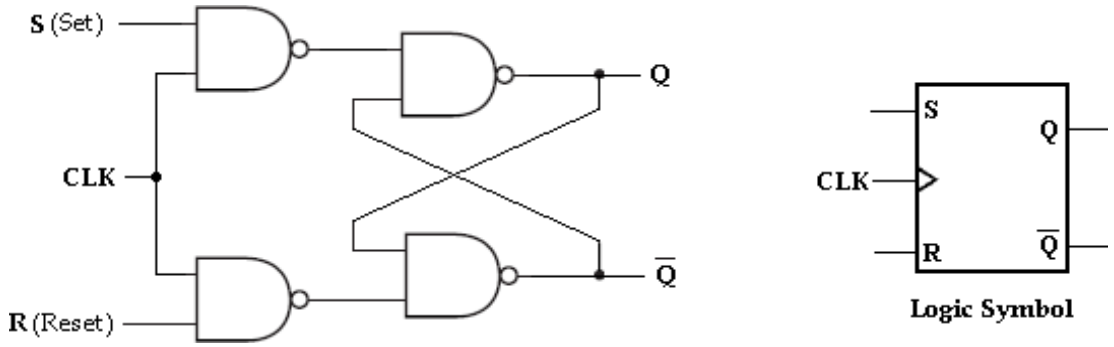
When D is HIGH and EN is HIGH. Q goes HIGH. When D is LOW and EN is HIGH, Q goes LOW. When EN is LOW, the state of the latch is not affected by the D input.



Input and output waveforms of D latch

S-R Flip-Flop

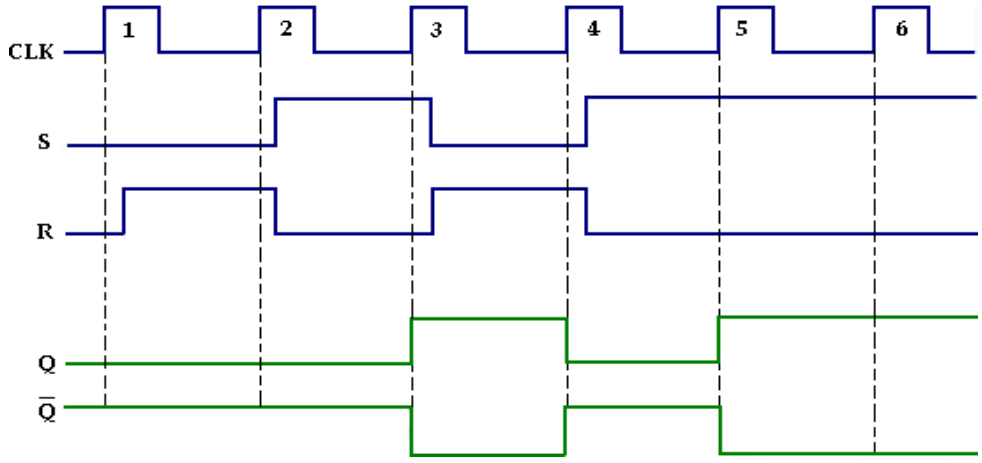
The S and R inputs of the S-R Flip-Flop are called ***synchronous*** inputs because data on these inputs are transferred to the Flip-Flop's output only on the triggering edge of the clock pulse. The circuit is similar to SR latch except enable signal is replaced by clock pulse (CLK). On the positive edge of the clock pulse, the circuit responds to the S and R inputs.



When S is HIGH and R is LOW, the Q output goes HIGH on the triggering edge of the clock pulse, and the Flip-Flop is SET. When S is LOW and R is HIGH, the Q output goes LOW on the triggering edge of the clock pulse, and the Flip-Flop is RESET. When both S and R are LOW, the output does not change from its prior state. An invalid condition exists when both S and R are HIGH.

CLK	S	R	Qn	Qn+1	State
1	0	0	0	0	No Change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	x	Indeterminate *
1	1	1	1	x	
0	x	x	0	0	No Change (NC)
0	x	x	1	1	

Truth table for SR Flip-Flop



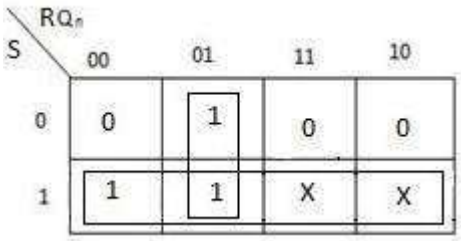
Input and output waveforms of SR Flip-Flop

Characteristic table and Characteristic equation

Characteristic table

Qn	S	R	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	X
1	1	1	X

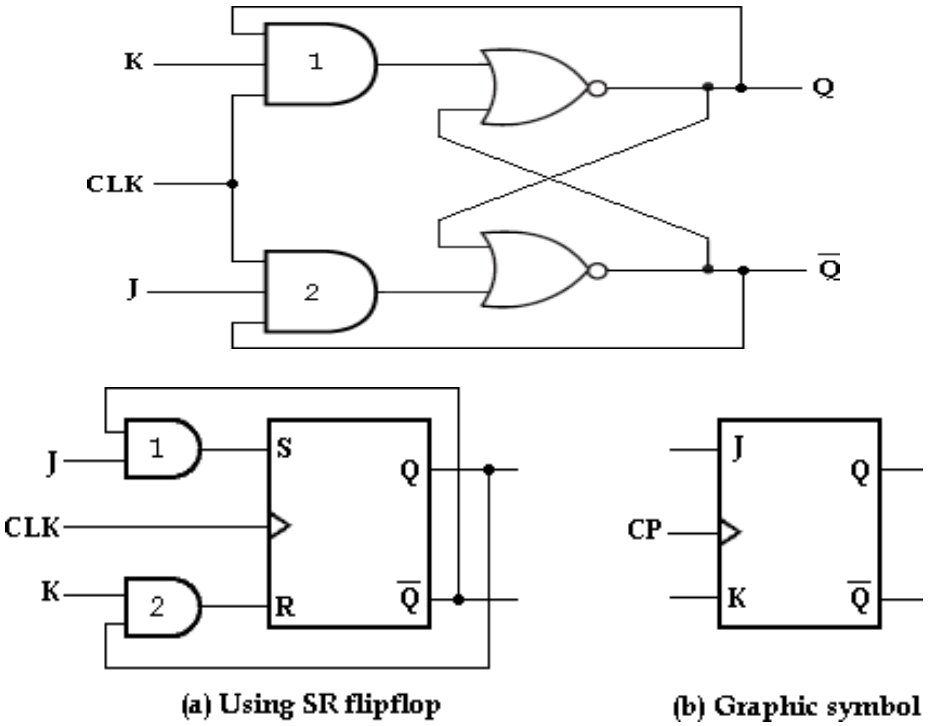
K-Map simplification



Characteristic Equation is **Qn+1 = S + R'Qn**

J-K Flip-Flop

JK means Jack Kilby, Texas Instrument (TI) Engineer, who invented IC in 1958. JK Flip-Flop has two inputs J(set) and K(reset). A JK Flip-Flop can be obtained from the clocked SR Flip-Flop by augmenting two AND gates as shown below.



(a) Using SR flipflop (b) Graphic symbol

The data input J and the output Q' are applied o the first AND gate and its output (JQ') is applied to the S input of SR Flip-Flop. Similarly, the data input K and the output Q are applied to the second AND gate and its output (KQ) is applied to the R input of SR Flip-Flop.

Case1: J= K= 0

When J=K= 0, both AND gates are disabled. Therefore clock pulse have no effect, hence the Flip-Flop output is same as the previous output.

Case2: J= 0, K= 1

When J= 0 and K= 1, AND gate-1 is disabled i.e., S= 0 and R= 1. This condition will reset the Flip-Flop to 0.

Case3: J= 1, K= 0

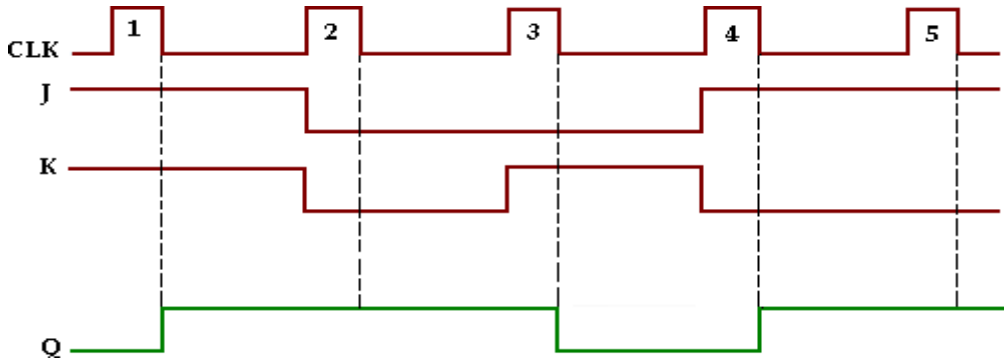
When J= 1 and K= 0, AND gate-2 is disabled i.e., S= 1 and R= 0. Therefore the Flip-Flop will set on the application of a clock pulse.

Case4: J= K= 1

When J=K= 1, it is possible to set or reset the Flip-Flop. If Q is High, AND gate-2 passes on a reset pulse to the next clock. When Q is low, AND gate-1 passes on a set pulse to the next clock. Either way, Q changes to the complement of the last state i.e., toggle. Toggle means to switch to the opposite state.

The truth table of JK Flip-Flop is given below.

CLK	Inputs		Output	State
	J	K	Q_{n+1}	
1	0	0	Q_n	No Change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	Q_n'	Toggle



Input and output waveforms of JK Flip-Flop

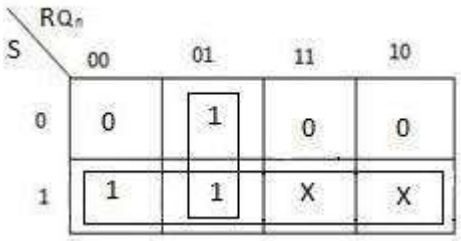
Characteristic table and Characteristic equation:

The characteristic table for JK Flip-Flop is shown in the table below. From the table, K-map for the next state transition (Qn+1) can be drawn and the simplified logic expression which represents the characteristic equation of JK Flip-Flop can be found.

Characteristic table

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

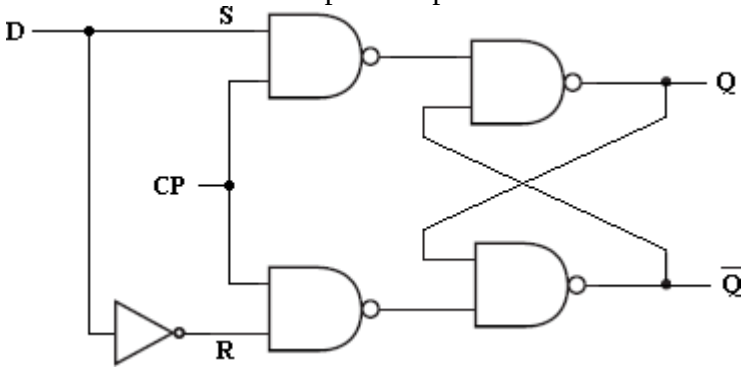
K-map simplification



Characteristic equation is **Qn+1= JQn'+ K'Q.**

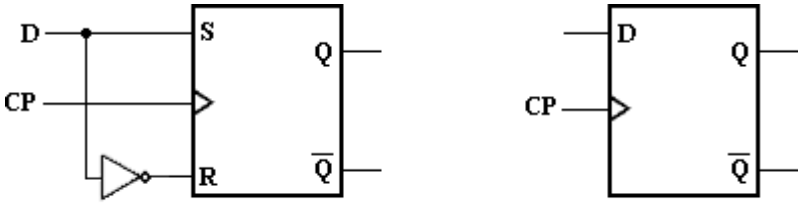
D Flip-Flop

Like in D latch, in D Flip-Flop the basic SR Flip-Flop is used with complemented inputs. The D Flip-Flop is similar to D-latch except clock pulse is used instead of enable input.



D Flip-Flop

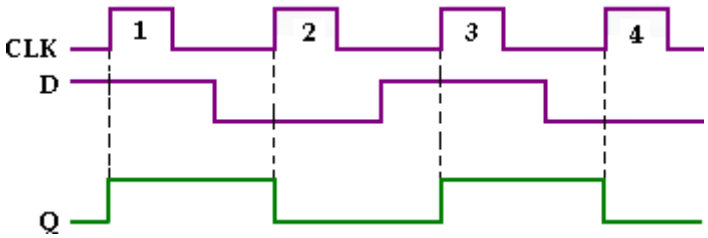
To eliminate the undesirable condition of the indeterminate state in the RS Flip- Flop is to ensure that inputs S and R are never equal to 1 at the same time. This is done by D Flip-Flop. The D (***delay***) Flip-Flop has one input called delay input and clock pulse input. The D Flip-Flop using SR Flip-Flop is shown below.



(a) Using SR flipflop **(b) Graphic symbol**

The truth table of D Flip-Flop is given below.

Clock	D	Qn+1	State
1	0	0	Reset
1	1	1	Set
0	x	Qn	No Change



Input and output waveforms of clocked D Flip-Flop

Looking at the truth table for D Flip-Flop we can realize that Qn+1 function follows the D input at the positive going edges of the clock pulses.

Characteristic table and Characteristic equation:

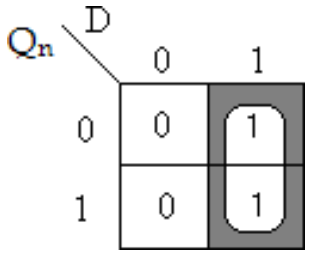
The characteristic table for D Flip-Flop shows that the next state of the Flip- Flop is independent of the present state since Qn+1 is equal to D. This means that an input pulse will transfer the value of input D into the output of the Flip-Flop independent of the value of the output before the pulse was applied.

The characteristic equation is derived from K-map.

Characteristic table

Qn	D	Qn+1
0	0	0
0	1	1
1	0	0
1	1	1

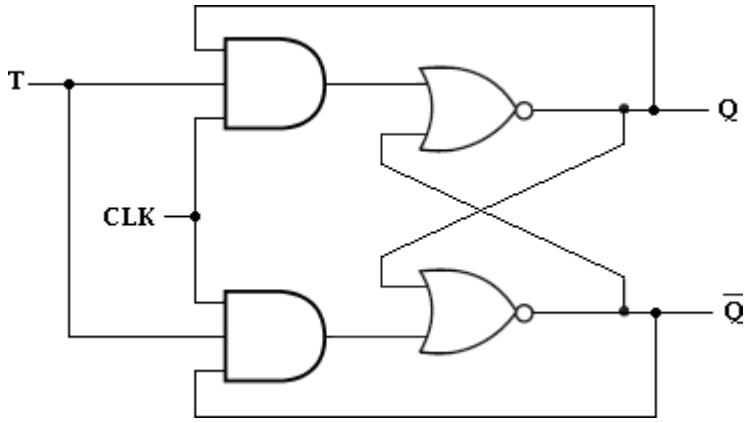
K-Map simplification



Characteristic equation: **Qn+1= D.**

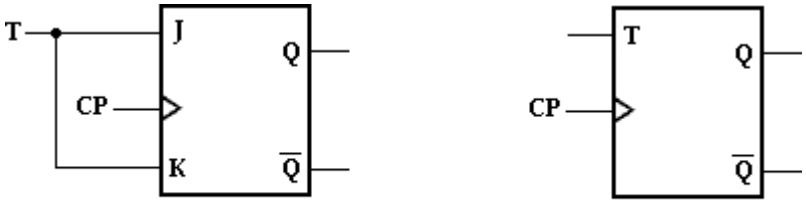
T Flip-Flop

The T (***Toggle***) Flip-Flop is a modification of the JK Flip-Flop. It is obtained from JK Flip-Flop by connecting both inputs J and K together, i.e., single input. Regardless of the present state, the Flip-Flop complements its output when the clock pulse occurs while input T= 1.



T Flip-Flop

When T= 0, $Q_{n+1}= Q_n$, ie., the next state is the same as the present state and no change occurs. When T= 1, $Q_{n+1}= Q_n'$,ie., the next state is the complement of the present state.



(a) Using JK flipflop **(b) Graphic symbol**

The truth table of T Flip-Flop is given below.

T	Qn+1	State
0	Qn	No Change
1	Qn'	Toggle

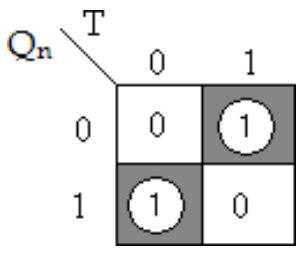
Characteristic table and Characteristic equation:

The characteristic table for T Flip-Flop is shown below and characteristic equation is derived using K-map.

Characteristic table

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

K-map Simplification:

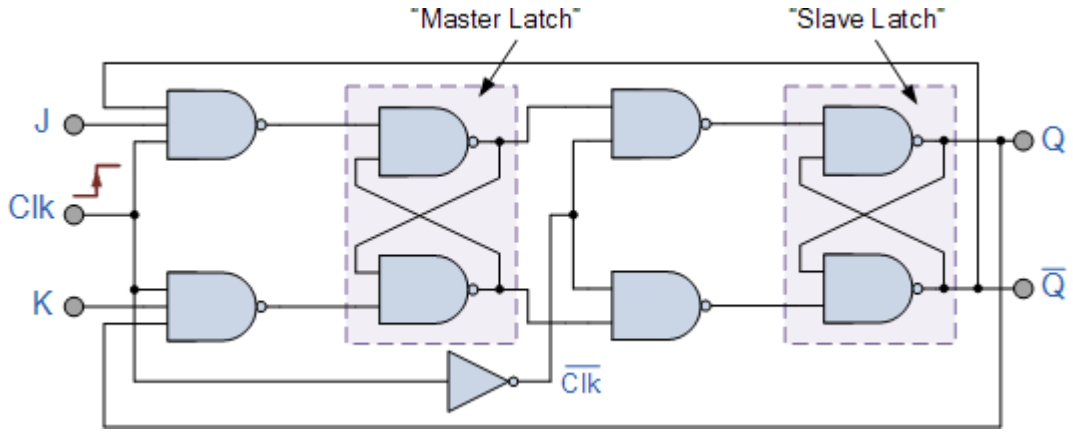


Characteristic equation: **$Q_{n+1}= TQ_n'+ T'Q_n$.**

MASTER-SLAVE JK FLIP-FLOP

The **Master-Slave Flip-Flop** is basically two gated SR flip-flops connected together in a series configuration with the slave having an inverted clock pulse. The outputs from Q and Q from the "Slave" flip-flop are fed back to the inputs of the "Master" with the outputs of the "Master" flip flop being connected to the two inputs of the "Slave" flip flop. This feedback configuration from the slave's output to the master's input gives the characteristic toggle of the JK flip flop as shown below.

The Master-Slave JK Flip Flop



The input signals J and K are connected to the gated "master" SR flip flop which "locks" the input condition while the clock (Clk) input is "HIGH" at logic level "1". As the clock input of the "slave" flip flop is the inverse (complement) of the "master" clock input, the "slave" SR flip flop does not toggle. The outputs from the "master" flip flop are only "seen" by the gated "slave" flip flop when the clock input goes "LOW" to logic level "0".

When the clock is "LOW", the outputs from the "master" flip flop are latched and any additional changes to its inputs are ignored. The gated "slave" flip flop now responds to the state of its inputs passed over by the "master" section.

Then on the "Low-to-High" transition of the clock pulse the inputs of the "master" flip flop are fed through to the gated inputs of the "slave" flip flop and on the "High-to-Low" transition the same inputs are reflected on the output of the "slave" making this type of flip flop edge or pulse-triggered.

Then, the circuit accepts input data when the clock signal is "HIGH", and passes the data to the output on the falling-edge of the clock signal. In other words, the **Master-Slave JK Flip flop** is a "Synchronous" device as it only passes data with the timing of the clock signal.

APPLICATION TABLE (OR) EXCITATION TABLE:

The ***characteristic table*** is useful for **analysis** and for defining the operation of the Flip-Flop. It specifies the next state (Q_{n+1}) when the inputs and present state are known. The ***excitation or application table*** is useful for **design** process. It is used to find the Flip-Flop input conditions that will cause the required transition, when the present state (Q_n) and the next state (Q_{n+1}) are known.

Flip-flop specifies the next state when the input and the present state are known. During the design of sequential circuits, the required transition form present state to next state and to find the FF input conditions that will cause the required transition. For this reason we need a table that lists the required input combinations for a given change of state. Such a table is called a flip-flop excitation table.

The excitation table for SR-FF, JK-FF D-FF and T-FF:

The excitation table can be constructed from the information available in the truth table. In the diagram shown below, the first table shows the truth table, from which the excitation table is derived.

SR Flip-Flop

S	R	Present state Q_n	Next state Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

Invalid states

Truth table of SR flip flop

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Excitation table of SR flip flop

JK Flip-Flop

J	K	Present state Q_n	Next state Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth table of JK flip flop

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Excitation table of JK flip flop

D Flip-Flop

D	Present state Q_n	Next state Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Truth table of D flip flop

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation table of D flip flop

T Flip-Flop

T	Present state Q_n	Next state Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Truth table of T flip flop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table of T flip flop

REALIZATION OF ONE FLIP-FLOP USING OTHER FLIP-FLOP

It is possible to convert one Flip-Flop into another Flip-Flop with some additional gates or simply doing some extra connection. The realization of one Flip-Flop using other Flip-Flops is implemented by the use of characteristic tables and excitation tables.

Procedure:

- Write the truth table/characteristic table for the required flip-flop.
- Write the excitation table for given flip-flop.
- Determine the expression for the given flip-flop inputs by using Kmap.
- Draw the flip-flop conversion logic diagram to obtain the required flip-flop by using the above obtained expression.

1. Conversion of JK Flip-Flop to SR Flip-Flop

Step 1: Write the Truth Table of the Desired Flip-Flop.
Here SR flip-flop is to be designed using JK flip-flop. Thus one needs to write the **truth table for SR flip-flop.**

Inputs		Outputs	
S	R	Present State, Q_n	Next State, Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	invalid	
1	1	invalid	

Step 2: Obtain the Excitation Table for the given Flip-Flop from its Truth Table. Excitation tables provide the details regarding the inputs which must be provided to the flip-flop to obtain a definite next state (Q_{n+1}) from the known current state (Q_n).

Truth Table for JK Flip-Flop

Inputs		Outputs	
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation Table for JK Flip-Flop

Outputs		Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

From the truth table of JK flip-flop one can see that Q_{n+1} will become 0 from $Q_n = 0$ for both (i) J = K = 0 and (ii) J = 0 and K =1 (blue entries in first and third rows of the truth table). This means that to obtain the next state, Q_{n+1} as 0 from the current state $Q_n = 0$, J must be made zero while K can be either 0 or 1.

This is indicated by the first row of the excitation table (blue entries in the first row of excitation table) where the value of K is expressed as 'X' indicating don't care condition. Similarly to obtain the next state as 1 from the current state 0, one has to have J equal to 1 while K can be either 0 or 1 (indicated by green entries of the truth table).

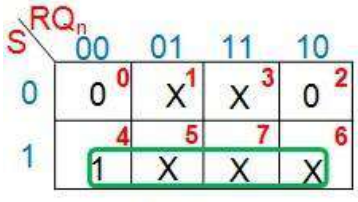
This leads to the second row of excitation table (green entries) to be filled with values $Q_n = 0$, $Q_{n+1} = 1$, J = 1 and K = X. On the same grounds, the entire excitation table needs to be filled (entries in pink and dark red colors).

Step 3: Append the Excitation Table of the given Flip-Flop to the Truth Table of the Desired Flip-Flop Appropriately to obtain Conversion Table. Here the conversion table is obtained by filling-up the values of the J and K inputs for the given Q_n and Q_{n+1}, by referring to the excitation table.

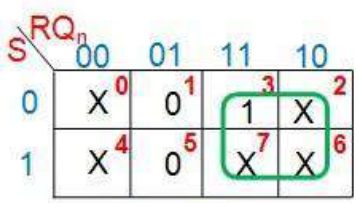
Conversion Table

S	R	Q_n	Q_{n+1}	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	invalid		X	X
1	1	invalid		X	X

Step 4: Simplify the Expressions for the Inputs of the given Flip-Flop. In this case, one needs to arrive at the logical expressions for the inputs J and K in terms of S, R, and Q_n using **K-map simplification** techniques.

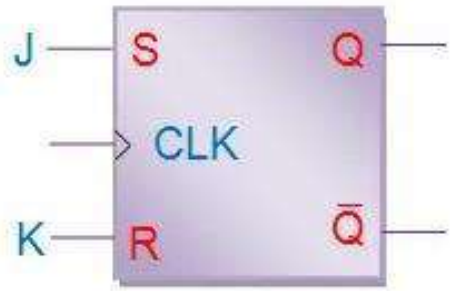


J = S



K = R

Step 5: Design the Necessary Circuit and make the Connections accordingly. Here neither additional circuit nor new connections are necessary.



Logic diagram of JK Flip-Flop using SR Flip-Flop

2. Conversion of JK Flip Flop to D Flip Flop

The conversion from a JK flip flop to a D flip flop is shown below.

1. Truth Table for D Flip-Flop

Input	Outputs	
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

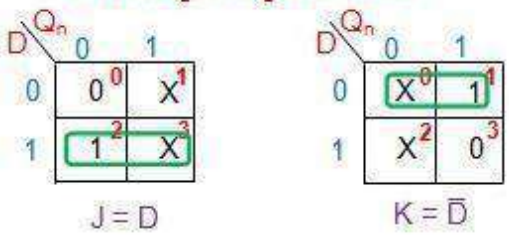
2. Excitation Table for JK Flip-Flop

Outputs		Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

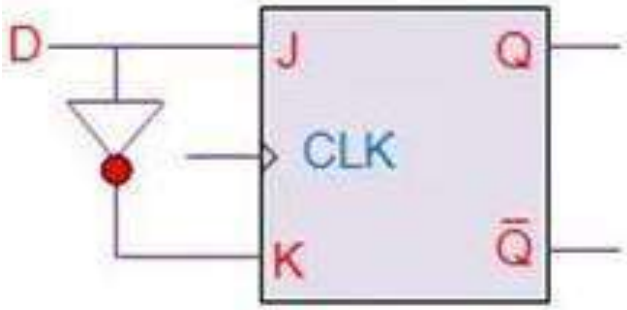
3. Conversion Table

D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

4. K-map Simplification



5. Circuit Design



3. Conversion of JK Flip Flop to T Flip Flop

The conversion from a JK flip flop to a T flip flop is shown below.

1. Truth Table for T Flip-Flop

Input	Outputs	
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

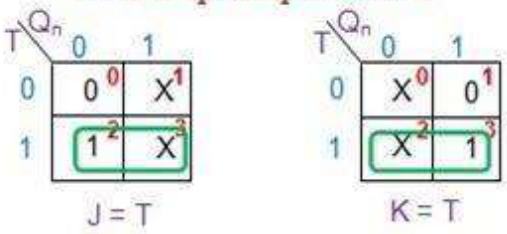
2. Excitation Table for JK Flip-Flop

Outputs		Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

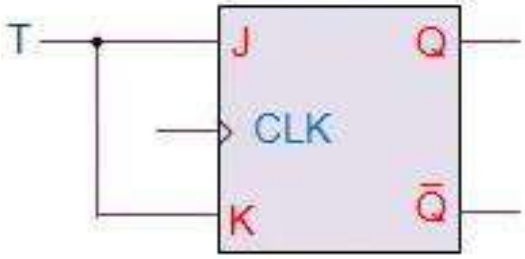
3. Conversion Table

T	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

4. K-map Simplification



5. Circuit Design



4. Conversion of SR Flip Flop to JK Flip Flop

The conversion from a SR flip flop to a JK flip flop is shown below.

1. Truth Table for JK flip-flop

Inputs		Outputs	
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

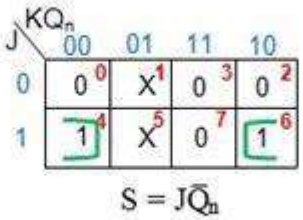
2. Excitation Table for SR flip-flop

Outputs		Inputs	
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

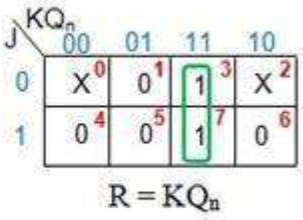
3. Conversion Table

J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

4. K-map Simplification

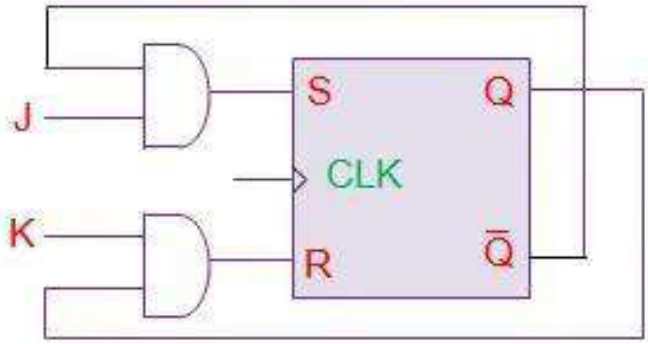


$S = J\bar{Q}_n$



$R = KQ_n$

5. Circuit Design



5. Conversion of SR Flip Flop to D Flip Flop

The conversion from a SR flip flop to a D flip flop is shown below.

1. Truth Table for D Flip Flop

Input	Outputs	
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

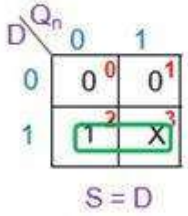
2. Excitation Table for SR Flip Flop

Outputs		Inputs	
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

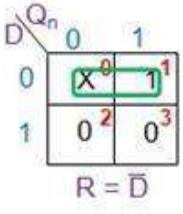
3. Conversion Table

D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

4. K-map Simplification

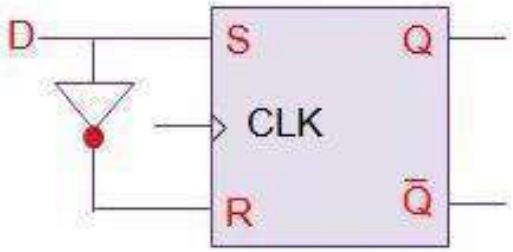


S = D



$R = \bar{D}$

5. Circuit Design



6. Conversion of SR Flip Flop to T Flip Flop

The conversion from a SR flip flop to a T flip flop is shown below.

1. Truth Table for T flip-flop

Input	Outputs	
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

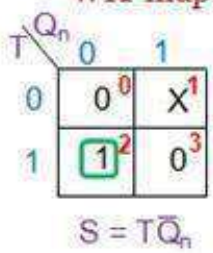
2. Excitation Table for SR flip-flop

Outputs		Inputs	
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

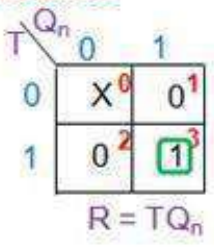
3. Conversion Table

T	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

4. K-map Simplification

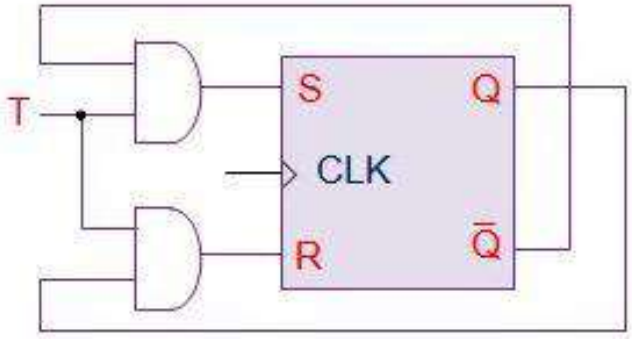


$S = T\bar{Q}_n$



$R = TQ_n$

5. Circuit Design



7. Conversion of D Flip Flop to JK Flip Flop

The conversion from a D flip flop to a JK flip flop is shown below.

1. Truth Table for JK flip-flop

Inputs		Outputs	
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

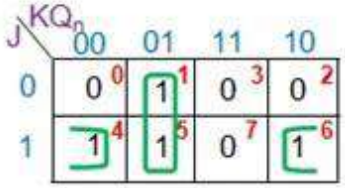
2. Excitation Table for D flip-flop

Outputs		Input
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

3. Conversion Table

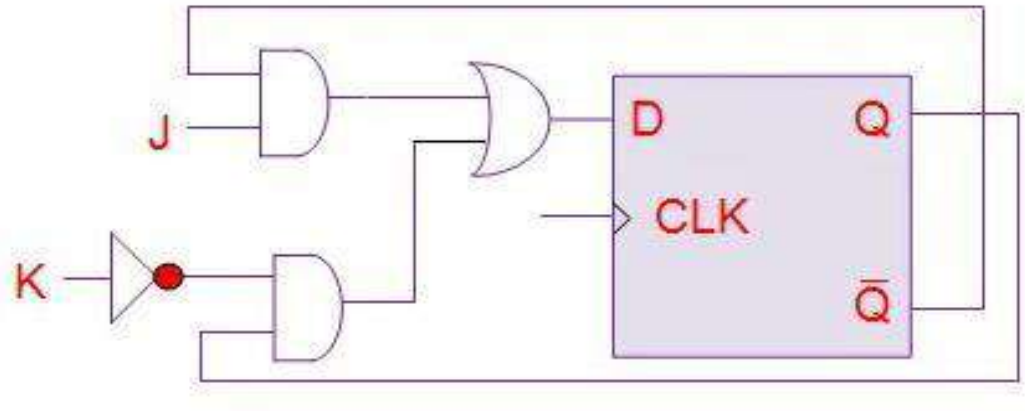
J	K	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

4. K-map Simplification



$$D = J\bar{Q}_n + \bar{K}Q_n$$

5. Circuit Design



8. Conversion of D Flip Flop to SR Flip Flop

The conversion from a D flip flop to a SR flip flop is shown below.

1. Truth Table for SR flip-flop

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	invalid	
1	1	invalid	

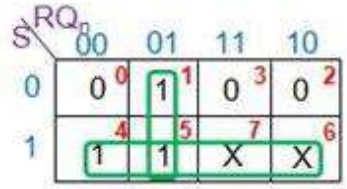
2. Excitation Table for D flip-flop

Outputs		Input
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

3. Conversion Table

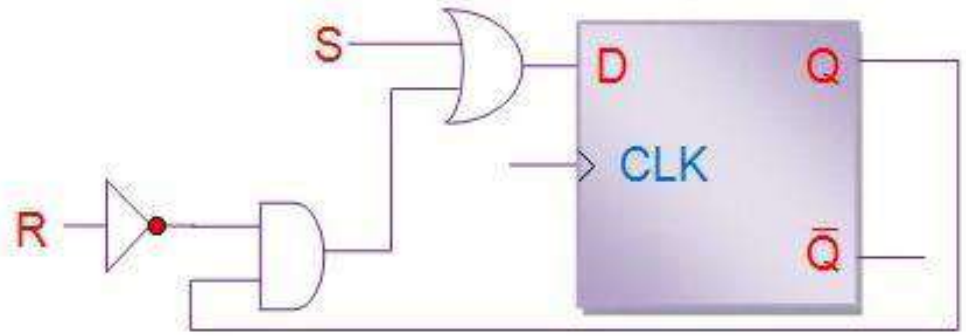
S	R	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	invalid		X
1	1	invalid		X

4. K-map Simplification



$D = S + \bar{R}Q_n$

5. Circuit Design



9. Conversion of D Flip Flop to T Flip Flop

The conversion from a D flip flop to a T flip flop is shown below.

1. Truth Table for T Flip Flop

Input	Outputs	
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

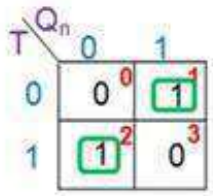
2. Excitation Table for D Flip Flop

Outputs		Input
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

3. Conversion Table

T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

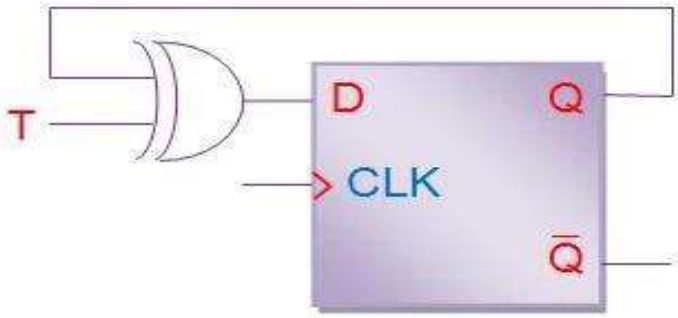
4. K-map Simplification



$D = T\bar{Q}_n + \bar{T}Q_n$

$= T \oplus Q_n$

5. Circuit Design



10. Conversion of T Flip Flop to JK Flip Flop

The conversion from a T flip flop to a JK flip flop is shown below.

1. Truth Table for JK Flip Flop

Inputs		Outputs	
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

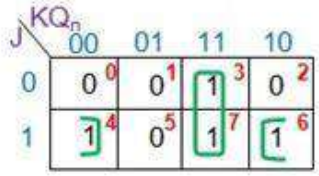
2. Excitation Table for T Flip Flop

Outputs		Input
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

3. Conversion Table

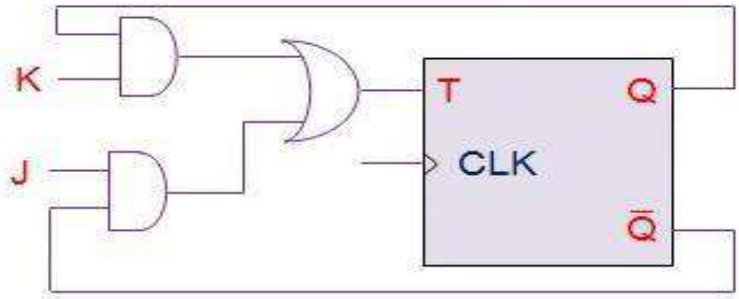
J	K	Q_n	Q_{n+1}	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

4. K-map Simplification



$T = J\bar{Q}_n + KQ_n$

5. Circuit Design



11. Conversion of T Flip Flop to SR Flip Flop

The conversion from a T flip flop to a SR flip flop is shown below.

1. Truth Table for SR Flip Flop

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	invalid	
1	1	invalid	

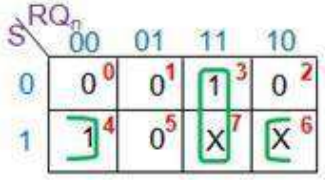
2. Excitation Table for T Flip Flop

Outputs		Input
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

3. Conversion Table

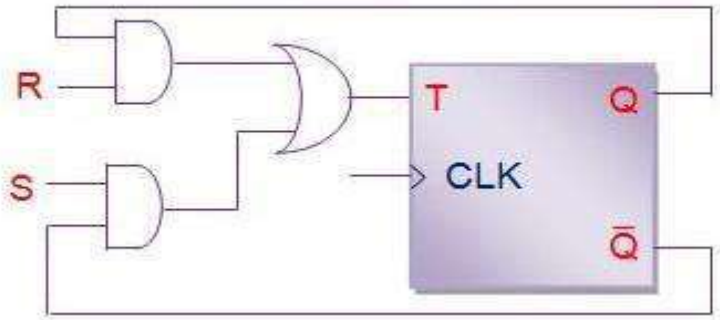
S	R	Q_n	Q_{n+1}	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	invalid		X
1	1	invalid		X

4. K-map Simplification



$T = S\bar{Q}_n + RQ_n$

5. Circuit Design



12. Conversion of T Flip Flop to D Flip Flop

The conversion from a T flip flop to a D flip flop is shown below.

1. Truth Table for D Flip Flop

Input	Outputs	
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

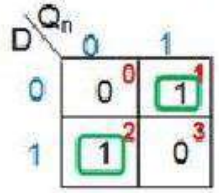
2. Excitation Table for T Flip Flop

Outputs		Input
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

3. Conversion Table

D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

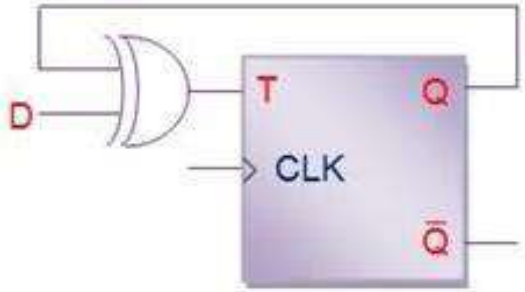
4. K-map Simplification



$D = D\bar{Q}_n + \bar{D}Q_n$

$= D \oplus Q_n$

5. Circuit Design



CLASSIFICATION OF SYNCHRONOUS SEQUENTIAL CIRCUIT

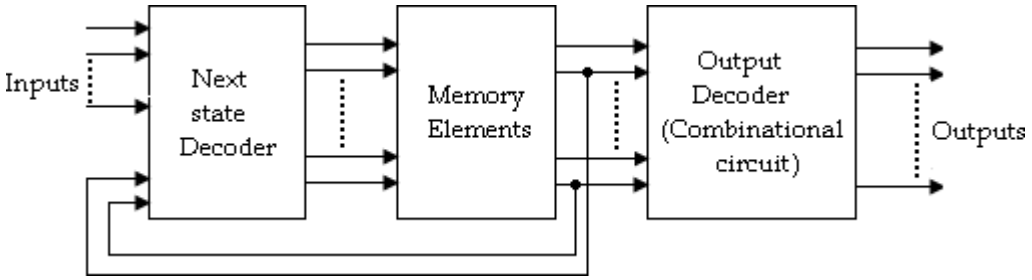
In synchronous or clocked sequential circuits, clocked Flip-Flops are used as memory elements, which change their individual states in synchronism with the periodic clock signal. Therefore, the change in states of Flip-Flop and change in state of the entire circuits occur at the transition of the clock signal.

The synchronous or clocked sequential networks are represented by two models.

- **Moore model:** The output depends only on the present state of the Flip-Flops.
- **Mealy model:** The output depends on both the present state of the Flip-Flops and on the inputs.

Moore model

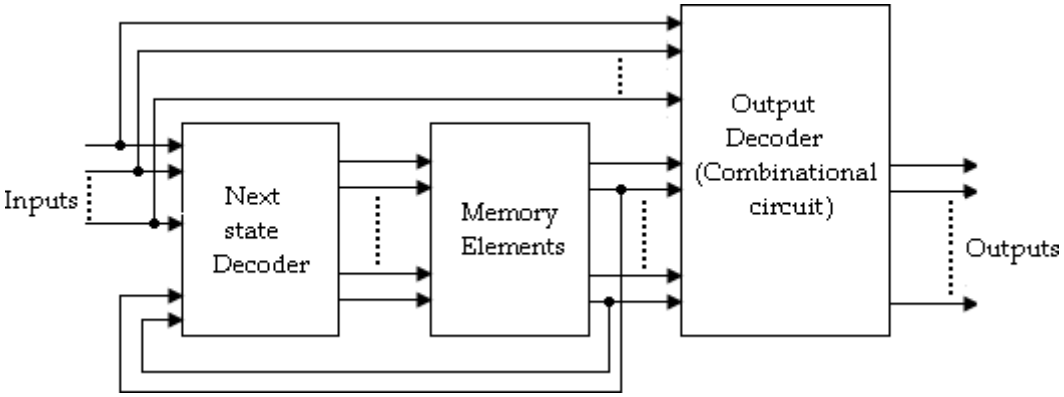
In the Moore model, the outputs are a function of the present state of the Flip- Flops only. The output depends only on present state of Flip-Flops, it appears only after the clock pulse is applied, i.e., it varies in synchronism with the clock input.



Block diagram of Moore model

Mealy model

In the Mealy model, the outputs are functions of both the present state of the Flip-Flops and inputs.



Difference between Moore and Mealy model

S. No	Moore model	Mealy model
1	Its outputs are a function of present state only.	Its outputs are a function of present state as well as present input.
2	Input changes does not affect the output.	Input changes may affect the output of the circuit.
3	It requires more number of states for implementing same function.	It requires less number of states for implementing same function.
4	In Moore machines, more logic is required to decode the outputs resulting in more circuit delays. They generally react one clock cycle later.	Mealy machines react faster to inputs. They generally react in the same clock cycle.

ANALYSIS OF SYNCHRONOUS SEQUENTIAL CIRCUIT

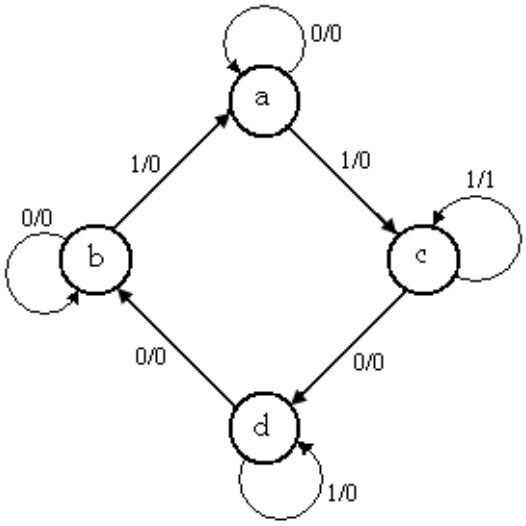
The behavior of a sequential circuit is determined from the inputs, outputs and the state of its Flip-Flops. The outputs and the next state are both a function of the inputs and the present state. The analysis of a sequential circuit consists of obtaining a table or diagram from the time sequence of inputs, outputs and internal states.

Before going to see the analysis and design examples, we first understand the state diagram, state table.

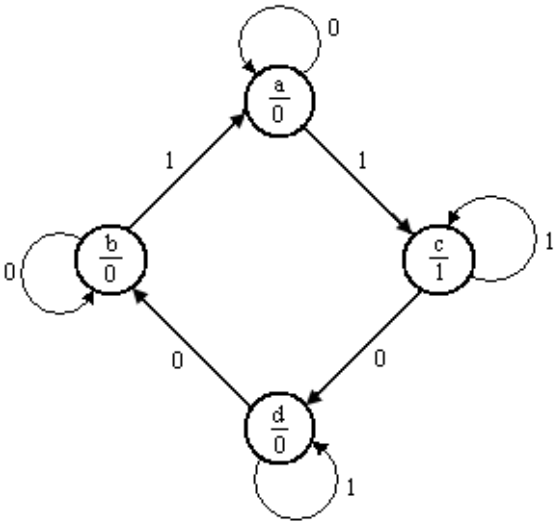
State Diagram

State diagram is a pictorial representation of a behavior of a sequential circuit.

- In the state diagram, a state is represented by a circle and the transition between states is indicated by directed lines connecting the circles.
- A directed line connecting a circle with circle with itself indicates that next state is same as present state.
- The binary number inside each circle identifies the state represented by the circle.
- The directed lines are labeled with two binary numbers separated by a symbol '/'. The input value that causes the state transition is labeled first and the output value during the present state is labeled after the symbol '/'.
- In case of **Moore circuit**, the directed lines are labeled with only one binary number representing the state of the input that causes the state transition. The output state is indicated within the circle, below the present state because output state depends only on present state and not on the input.



State diagram for Mealy circuit



State diagram for Moore circuit

State Table

State table represents relationship between input, output and Flip-Flop states.

- It consists of three sections labeled present state, next state and output.
- The present state designates the state of Flip-Flops before the occurrence of a clock pulse, and the output section gives the values of the output variables during the present state.
- Both the next state and output sections have two columns representing two possible input conditions: X= 0 and X=1.

Present state	Next State		Output	
	X= 0	X= 1	X= 0	X= 1
AB	AB	AB	Y	Y
a	a	c	0	0
b	b	a	0	0

c	d	c	0	1
d	b	d	0	0

- In case of Moore circuit, the output section has only one column since output does not depend on input.

Present state	Next state		Output
	X= 0	X= 1	Y
AB	AB	AB	
a	a	c	0
b	b	a	0
c	d	c	1
d	b	d	0

State Equation

It is an algebraic expression that specifies the condition for a Flip-Flop state transition. The Flip-Flops may be of any type and the logic diagram may or may not include combinational circuit gates.

ANALYSIS PROCEDURE

The synchronous sequential circuit analysis is summarizes as given below:

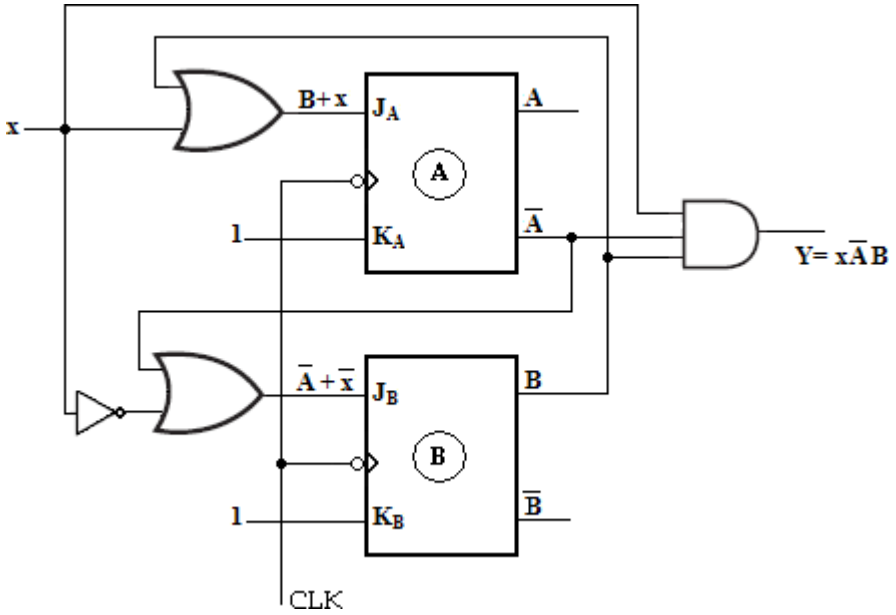
1. Assign a state variable to each Flip-Flop in the synchronous sequential circuit.
2. Write the excitation input functions for each Flip-Flop and also write the Moore/ Mealy output equations.
3. Substitute the excitation input functions into the bistable equations for the Flip-Flops to obtain the next state output equations.
4. Obtain the state table and reduced form of the state table.
5. Draw the state diagram by using the second form of the state table. Analysis of Mealy Model.

Solved Examples:

1. A sequential circuit has two JK Flip-Flops A and B, one input (x) and one output (y) the Flip-Flop input functions are, JA= B + x JB= A'+ x' KA= 1 KB= 1 and the circuit output function, Y= xA'B.

a) Draw the logic diagram of the Mealy circuit,
b) Tabulate the state table,
c) Draw the state diagram.

Soln:



State table:

To obtain the next-state values of a sequential circuit with JK Flip-Flops, use the JK Flip-Flop characteristics table.

Characteristic equation of JK Flip-flop $Q_{n+1}= JQn'+ K'Qn$

For A Flip-flop $A(t+1)=J_AA'+K_A'A$

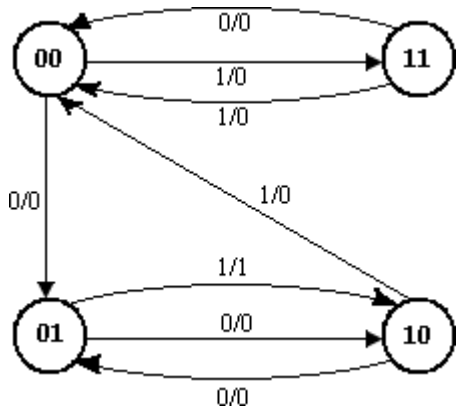
For B Flip-flop $B(t+1)=J_BB'+K_B'B$

Present state		Input	Flip-Flop Inputs				Next state		Output
A	B	x	$J_A= B+ x$	$K_A= 1$	$J_B= A'+ x'$	$K_B= 1$	A(t+1)	B(t+1)	Y= xA'B
0	0	0	0	1	1	1	0	1	0
0	0	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	0	0
0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	1	1	0	1	0
1	0	1	1	1	0	1	0	0	0
1	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	1	0	0	0

Present state		Next state				Output	
		x= 0		x= 1		x= 0	x= 1
A	B	A(t+1)	B(t+1)	A(t+1)	B(t+1)	y	y
0	0	0	1	1	1	0	0
0	1	1	0	1	0	0	1
1	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0

Second form of state table

State Diagram:



2. A sequential circuit with two 'D' Flip-Flops A and B, one input (x) and one output (y). The Flip-Flop input functions are:

$D_A = Ax + Bx$

$D_B = A'x$

and the circuit output function is,

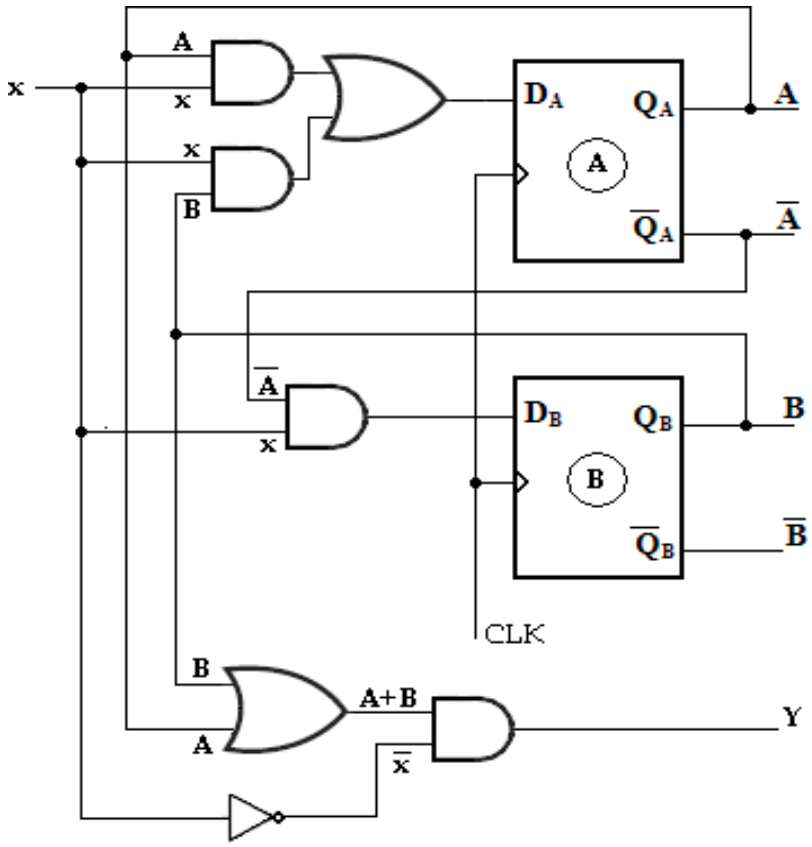
$Y = (A + B)\,x'$.

(a) Draw the logic diagram of the circuit,

(b) Tabulate the state table,

(c) Draw the state diagram.

Soln:



Characteristic equation of D flip-flop Qn+1= D

A(t+1)=DA **B(t+1)=DB**

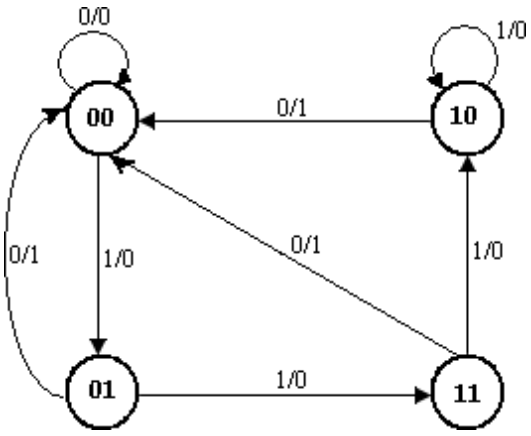
State Table:

Present state		Input	Flip-Flop Inputs		Next state		Output
A	**B**	**x**	**D_A= Ax+Bx**	**D_B= A'x**	**A(t+1)**	**B(t+1)**	**Y= (A+B)x'**
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	0	0	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	1	1	0	1	0	0
1	1	0	0	0	0	0	1
1	1	1	1	0	1	0	0

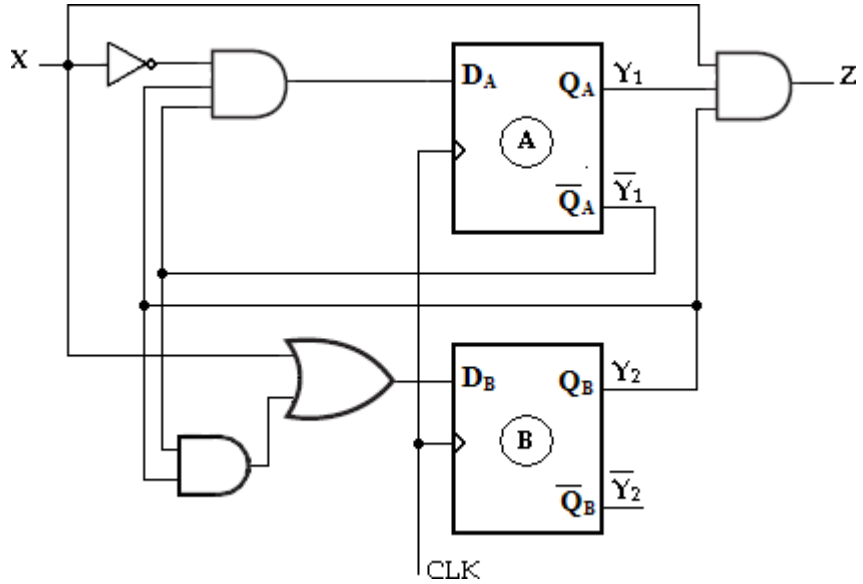
Present state		Next state				Output	
		x= 0		x= 1		x= 0	x= 1
A	**B**	**A**	**B**	**A**	**B**	**Y**	**Y**
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

Second form of state table

State Diagram:



3. Analyze the synchronous Mealy machine and obtain its state diagram.



Soln:

The given synchronous Mealy machine consists of two D Flip-Flops, one input and one output.

The Flip-Flop input functions are,

$D_A = Y_1'Y_2X'$

$D_B = X + Y_1'Y_2$

The circuit output function is, $Z = Y_1Y_2X$

Characteristic equation of D flip-flop is $Q_{n+1} = D$

$Y_1(t+1) = D_A$ $\quad$ $Y2(t+1) = D_B$

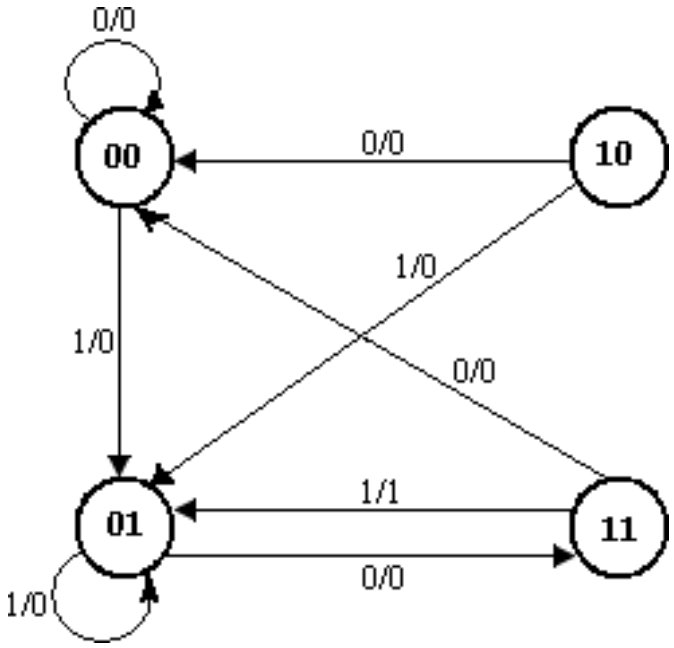
State Table:

Present state		Input	Flip-Flop Inputs		Next state		Output
Y_1	Y_2	X	$D_A = Y_1'Y_2X'$	$D_B = X + Y_1'Y_2$	$Y_1(t+1)$	$Y_2(t+1)$	$Z = Y_1Y_2X$
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	1	1	1	1	0
0	1	1	0	1	0	1	0
1	0	0	0	0	0	0	0
1	0	1	0	1	0	1	0
1	1	0	0	0	0	0	0
1	1	1	0	1	0	1	1

Present state		Next state				Output	
		X= 0		X= 1		X= 0	X= 1
Y_1	Y_2	Y_1	Y_2	Y_1	Y_2	Z	Z
0	0	0	0	0	1	0	0
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	0
1	1	0	0	0	1	0	1

Second form of state table

State Diagram:



4. A sequential circuit has two JK Flop-Flops A and B, two inputs x and y and one output z. The Flip-Flop input equation and circuit output equations are

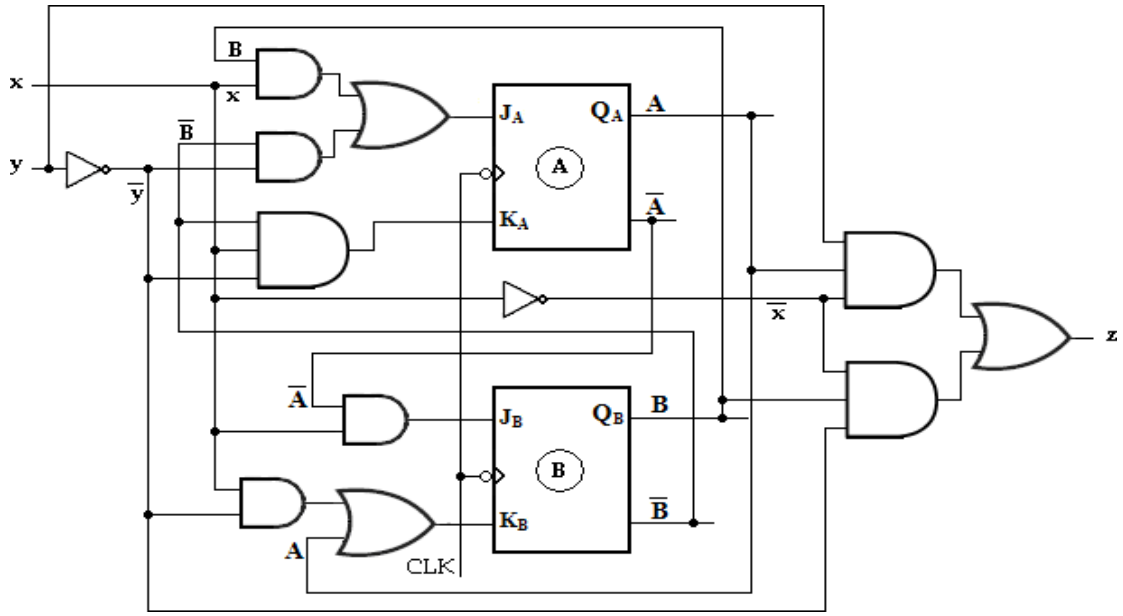
J_A = Bx + B' y' K_A = B' xy' J_B = A' x K_B = A+ xy' z = Ax' y' + Bx' y'

(a) Draw the logic diagram of the circuit

(b) Tabulate the state table.

(c) Derive the state equation.

Soln:
Logic Diagram:



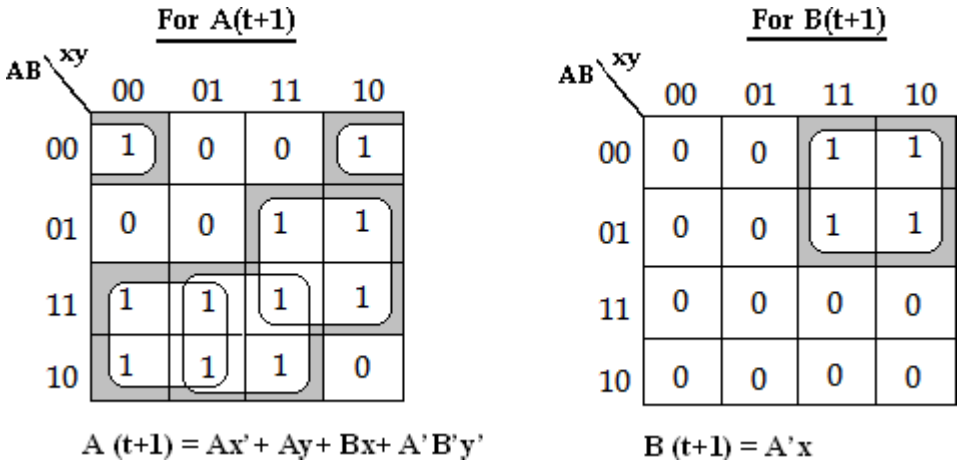
State Table:

To obtain the next-state values of a sequential circuit with JK Flip-Flop, use the JK Flip-Flop characteristic table,

Characteristic equation of JK Flip-flop **Qn+1= JQn'+ K'Qn**
A(t+1)=J_AA'+K_A'A **B(t+1)=J_BB'+K_B'B**

Present State		Input		Flip-Flop Inputs				Next state		Output
A	B	x	y	J_A= Bx+B'y'	K_A= B'xy'	J_B=A'x	K_B= A+xy'	A(t+1)	B(t+1)	Z
0	0	0	0	1	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	1	1	1	1	1	0
0	0	1	1	0	0	1	0	0	1	0
0	1	0	0	0	0	0	0	0	0	1
0	1	0	1	0	0	0	0	0	0	0
0	1	1	0	1	0	1	1	1	1	0
0	1	1	1	1	0	1	0	1	1	0
1	0	0	0	1	0	0	1	1	0	1
1	0	0	1	0	0	0	1	1	0	0
1	0	1	0	1	1	0	1	0	0	0
1	0	1	1	0	0	0	1	1	0	0
1	1	0	0	0	0	0	1	1	0	1
1	1	0	1	0	0	0	1	1	0	0
1	1	1	0	1	0	0	1	1	0	0
1	1	1	1	1	0	0	1	1	0	0

State Equation:



$A(t+1) = Ax' + Ay + Bx + A'B'y'$ $\quad B(t+1) = A'x$

5. A sequential circuit has two JK Flip-Flop A and B. The Flip-Flop input functions are:

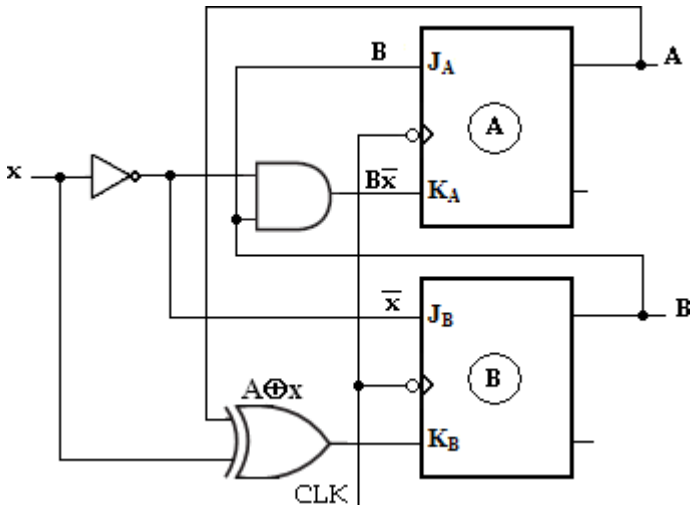
$J_A = B$ $\quad J_B = x'$

$K_A = Bx'$ $\quad K_B = A \oplus x.$

(a) Draw the logic diagram of the circuit,
(b) Tabulate the state table,
(c) Draw the state diagram.

Soln:

Logic diagram:



The output function is not given in the problem. The output of the Flip-Flops may be considered as the output of the circuit.

State Table:

To obtain the next-state values of a sequential circuit with JK Flip-Flop, use the JK Flip-Flop characteristic table.

Characteristic equation of JK Flip-flop **Qn+1= JQn'+ K'Qn**

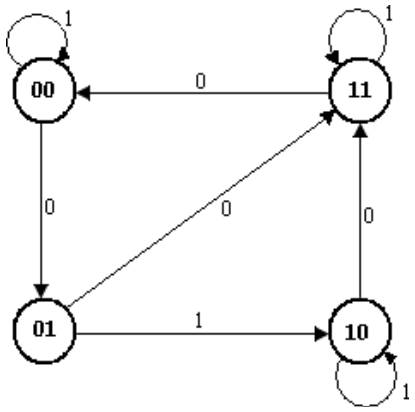
$A(t+1)=J_AA'+K_A'A$ $B(t+1)=J_BB'+K_B'B$

Present state		Input	Flip-Flop Inputs				Next state	
A	**B**	**x**	**J_A= B**	**K_A= Bx'**	**J_B= x'**	**K_B= A x**	**A(t+1)**	**B(t+1)**
0	0	0	0	0	1	0	0	1
0	0	1	0	0	0	1	0	0
0	1	0	1	1	1	0	1	1
0	1	1	1	0	0	1	1	0
1	0	0	0	0	1	1	1	1
1	0	1	0	0	0	0	1	0
1	1	0	1	1	1	1	0	0
1	1	1	1	0	0	0	1	1

Present state		Next state			
		X= 0		X= 1	
A	**B**	**A**	**B**	**A**	**B**
0	0	0	1	0	0
0	1	1	1	1	0
1	0	1	1	1	0
1	1	0	0	1	1

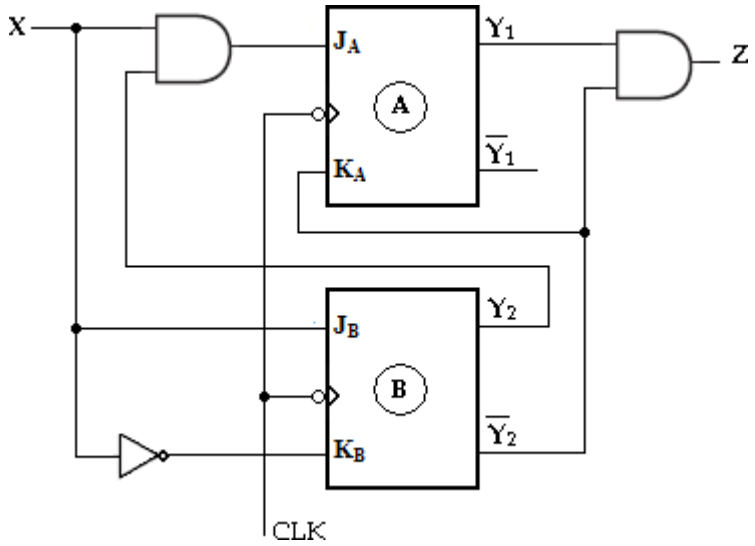
Second form of State table

State Diagram:



Analysis of Moore Model

6. Analyze the synchronous Moore circuit and obtain its state diagram.



Soln:

Using the assigned variable Y1 and Y2 for the two JK Flip-Flops, we can write the four excitation input equations and the Moore output equation as follows:

$J_A = Y_2X$; $K_A = Y_2'$

$J_B = X$; $K_B = X'$ and output function, $Z = Y_1Y_2'$

State Table:

Characteristic equation of JK Flip-flop $Q_{n+1} = JQ_n' + K'Q_n$

$Y_1(t+1) = J_AY_1' + K_A'Y_1$ $Y_2(t+1) = J_BY_2' + K_B'Y_2$

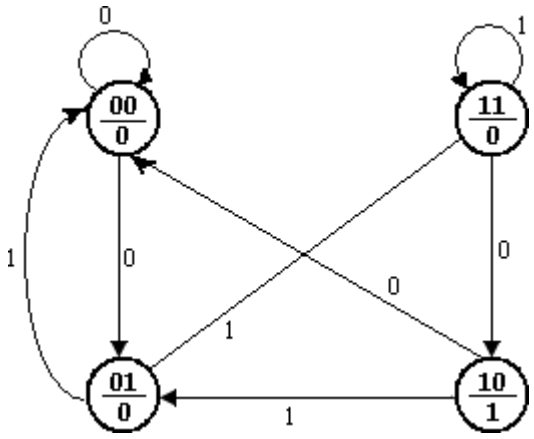
Present state		Input	Flip-Flop Inputs				Next state		Output
Y_1	Y	X	$J_A = Y_2X$	$K_A = Y_2'$	$J_B = X$	$K_B = X'$	$Y_1(t+1)$	$Y_2(t+1)$	$Z = Y_1Y_2'$
0	0	0	0	1	0	1	0	0	0
0	0	1	0	1	1	0	0	1	0
0	1	0	0	0	0	1	0	0	0
0	1	1	1	0	1	0	1	1	0
1	0	0	0	1	0	1	0	0	1
1	0	1	0	1	1	0	0	1	1
1	1	0	0	0	0	1	1	0	0
1	1	1	1	0	1	0	1	1	0

Present state		Next state				Output
		X= 0		X= 1		Y
Y_1	Y_2	Y_1	Y_2	Y_1	Y_2	
0	0	0	0	0	1	0
0	1	0	0	1	1	0
1	0	0	0	0	1	1
1	1	1	0	1	1	0

Second form of State table

State Diagram:

Here the output depends on the present state only and is independent of the input. The two values inside each circle separated by a slash are for the present state and output.



7. A sequential circuit has two T Flip-Flop A and B. The Flip-Flop input functions are:

T_A= Bx

T_B= x y= AB

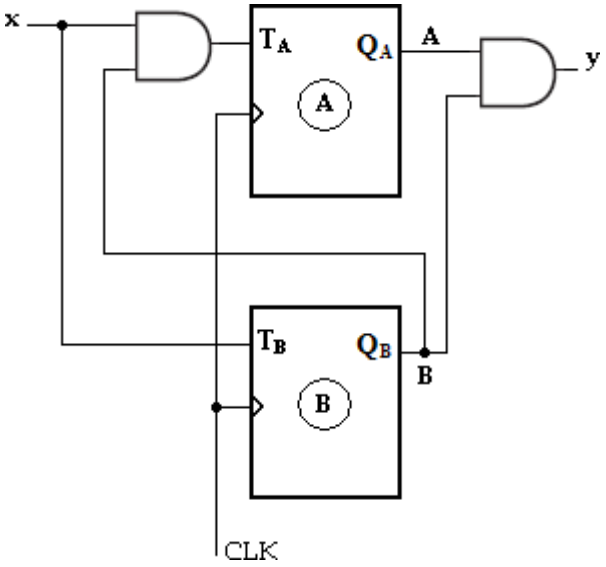
(a) Draw the logic diagram of the circuit,

(b) Tabulate the state table,

(c) Draw the state diagram.

Soln:

Logic diagram:



State Table

Characteristic equation: **Qn+1= TQn'+ T'Qn.**

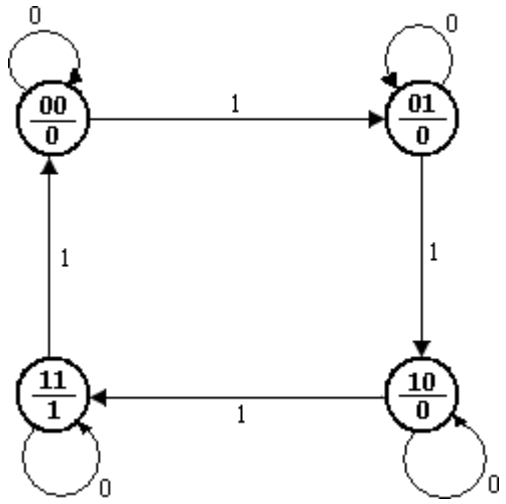
A (t+1)= T_AA'+T_A'A B (t+1)= T_BB'+T_B'B

Present state		Input	Flip-Flop Inputs		Next state		Output
A	**B**	**x**	**T_A= Bx**	**T_B= x**	**A (t+1)**	**B (t+1)**	**y= AB**
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	0	0	1	0
0	1	1	1	1	1	0	0
1	0	0	0	0	1	0	0
1	0	1	0	1	1	1	0
1	1	0	0	0	1	1	1
1	1	1	1	1	0	0	1

Present state		Next state				Output	
		x= 0		x= 1		x= 0	x= 1
A	**B**	**A**	**B**	**A**	**B**	**y**	**y**
0	0	0	0	0	1	0	0
0	1	0	1	1	0	0	0
1	0	1	0	1	1	0	0
1	1	1	1	0	0	1	1

Second form of state table

State Diagram:



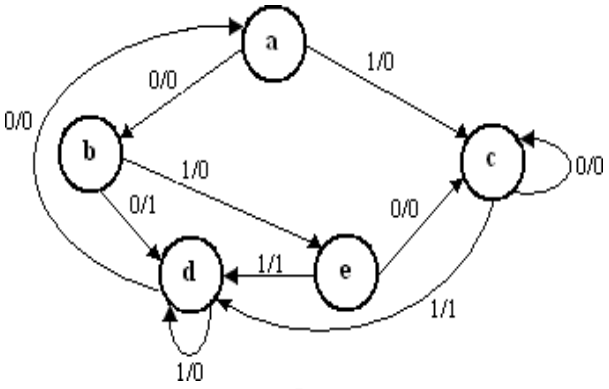
STATE REDUCTION/ MINIMIZATION

The state reduction is used to avoid the redundant states in the sequential circuits. The reduction in redundant states reduces the number of required Flip- Flops and logic gates, reducing the cost of the final circuit.

The two states are said to be redundant or equivalent, if every possible set of inputs generate exactly same output and same next state. When two states are equivalent, one of them can be removed without altering the input-output relationship.

Since 'n' Flip-Flops produced 2^n state, a reduction in the number of states may result in a reduction in the number of Flip-Flops.

The need for state reduction or state minimization is explained with one example.



State diagram

Step 1: Determine the state table for given state diagram

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
A	b	c	0	0
B	d	e	1	0
C	c	d	0	1
D	a	d	0	0
E	c	d	0	1

State table

Step 2: Find equivalent states

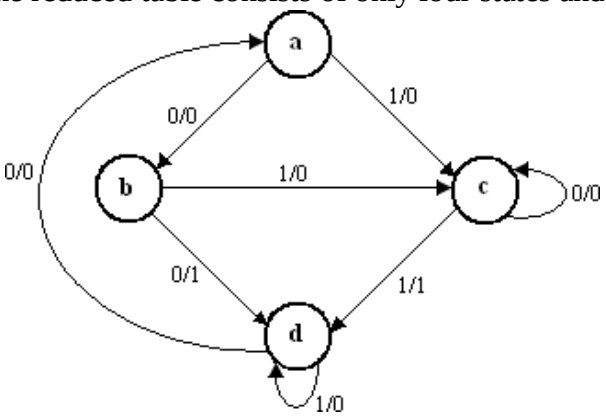
From the above state table **c** and **e** generate exactly same next state and same output for every possible set of inputs. The state **c** and **e** go to next states **c** and **d** and have outputs 0 and 1 for x=0 and x=1 respectively. Therefore state **e** can be removed and replaced by **c**.

The final reduced state table is shown below.

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
A	b	c	0	0
b	d	c	1	0
c	c	d	0	1
D	a	d	0	0

Reduced state table

The state diagram for the reduced table consists of only four states and is shown below.



Reduced state diagram

More Solved Problems:

1. Reduce the number of states in the following state table and tabulate the reduced state table.

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

Soln:

From the above state table **e** and **g** generate exactly same next state and same output for every possible set of inputs. The state **e** and **g** go to next states **a** and **f** and have outputs 0 and 1 for x = 0 and x = 1 respectively. Therefore state g can be removed and replaced by e.

The reduced state table-1 is shown below.

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	**e**	f	0	1

Reduced state table-1

Now states d and f are equivalent. Both states go to the same next state (e, f) and have same output (0, 1). Therefore one state can be removed; **f** is replaced by **d.**

The final reduced state table-2 is shown below.

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
a	a	b	0	0
b	c	d	0	0
c	a	**d**	0	0
d	e	**d**	0	1
e	a	**d**	0	1

Reduced state table-2

Thus 7 states are reduced into 5 states.

2. Determine a minimal state table equivalent furnished below

Present state	Next state	
	X= 0	X= 1
1	1, 0	1, 0
2	1, 1	6, 1
3	4, 0	5, 0
4	1, 1	7, 0
5	2, 0	3, 0
6	4, 0	5, 0
7	2, 0	3, 0

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
1	1	1	0	0
2	1	6	1	1
3	4	5	0	0
4	1	7	1	0
5	2	3	0	0
6	4	5	0	0
7	2	3	0	0

From the above state table, **5** and **7** generate exactly same next state and same output for every possible set of inputs. The state **5** and **7** go to next states **2** and **3** and have outputs 0 and 0 for x=0 and x=1 respectively. Therefore state **7** can be removed and replaced by **5**.

Similarly, **3** and **6** generate exactly same next state and same output for every possible set of inputs. The state **3** and **6** go to next states **4** and **5** and have outputs 0 and 0 for x=0 and x=1 respectively. Therefore state **6** can be removed and replaced by **3**.
The final reduced state table is shown below.

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
1	1	1	0	0
2	1	3	1	1
3	4	5	0	0
4	1	5	1	0
5	2	3	0	0

Reduced state table

Thus 7 states are reduced into 5 states.

3. Minimize the following state table.

Present state	Next state	
	X= 0	X= 1
A	D, 0	C, 1
B	E, 1	A, 1
C	H, 1	D, 1
D	D, 0	C, 1
E	B, 0	G, 1
F	H, 1	D, 1
G	A, 0	F, 1
H	C, 0	A, 1
I	G, 1	H,1

Soln:

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
A	D	C	0	1
B	E	A	1	1
C	H	D	1	1
D	D	C	0	1
E	B	G	0	1
F	H	D	1	1
G	A	F	0	1
H	C	A	0	1
I	G	H	1	1

From the above state table, **A** and **D** generate exactly same next state and same output for every possible set of inputs. The state **A** and **D** go to next states **D** and **C** and have outputs 0 and 1 for x=0 and x=1 respectively. Therefore state **D** can be removed and replaced by **A**. Similarly, **C** and **F** generate exactly same next state and same output for every possible set of inputs. The state **C** and **F** go to next states **H** and **D** and have outputs 1 and 1 for x=0 and x=1 respectively. Therefore state **F** can be removed and replaced by **C**.

The reduced state table-1 is shown below.

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
A	A	C	0	1
B	E	A	1	1
C	H	A	1	1
E	B	G	0	1
G	A	C	0	1
H	C	A	0	1
I	G	H	1	1

Reduced state table-1

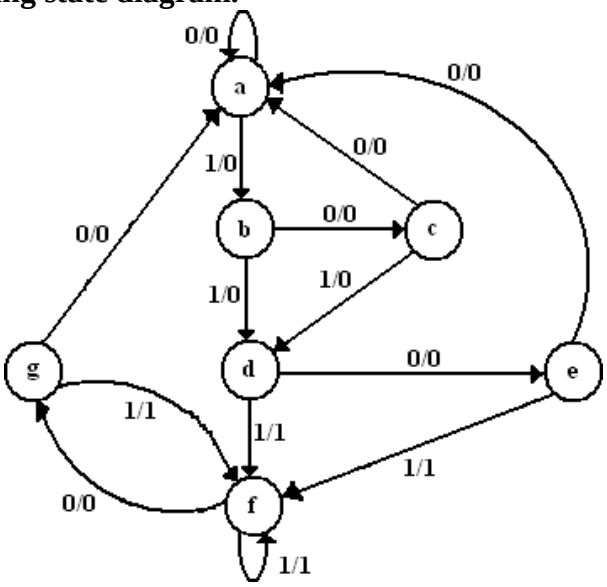
From the above reduced state table-1, **A** and **G** generate exactly same next state and same output for every possible set of inputs. The state **A** and **G** go to next states **A** and **C** and have outputs 0 and 1 for x=0 and x=1 respectively. Therefore state **G** can be removed and replaced by **A**. The final reduced state table-2 is shown below.

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
A	A	C	0	1
B	E	A	1	1
C	H	A	1	1
E	B	A	0	1
H	C	A	0	1
I	A	H	1	1

Reduced state table-2

Thus 9 states are reduced into 6 states.

4. Reduce the following state diagram.



Soln:

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
A	A	b	0	0
B	C	d	0	0
C	A	d	0	0
D	E	f	0	1
E	A	f	0	1
F	G	f	0	1
G	A	f	0	1

State table

From the above state table **e** and **g** generate exactly same next state and same output for every possible set of inputs. The state **e** and **g** go to next states **a** and **f** and have outputs 0 and 1 for x=0 and x=1 respectively. Therefore state **g** can be removed and replaced by **e**. The reduced state table-1 is shown below.

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
A	a	b	0	0
B	c	d	0	0
C	a	d	0	0
D	e	f	0	1
E	a	f	0	1
F	**e**	f	0	1

Reduced state table-1

Now states d and f are equivalent. Both states go to the same next state (e, f) and have same output (0, 1). Therefore one state can be removed; **f** is replaced by **d.**

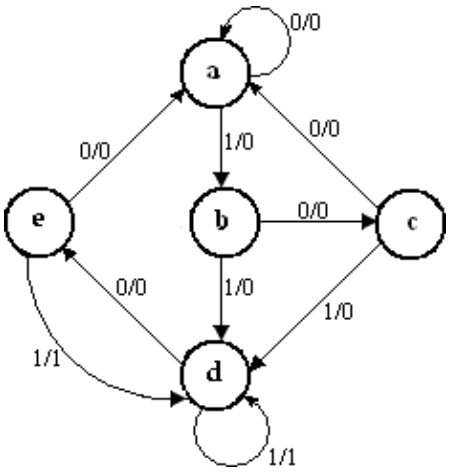
The final reduced state table-2 is shown below.

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
A	a	b	0	0
B	c	d	0	0
C	a	**d**	0	0
D	e	**d**	0	1
E	a	**d**	0	1

Reduced state table-2

Thus 7 states are reduced into 5 states.

The state diagram for the reduced state table-2 is,



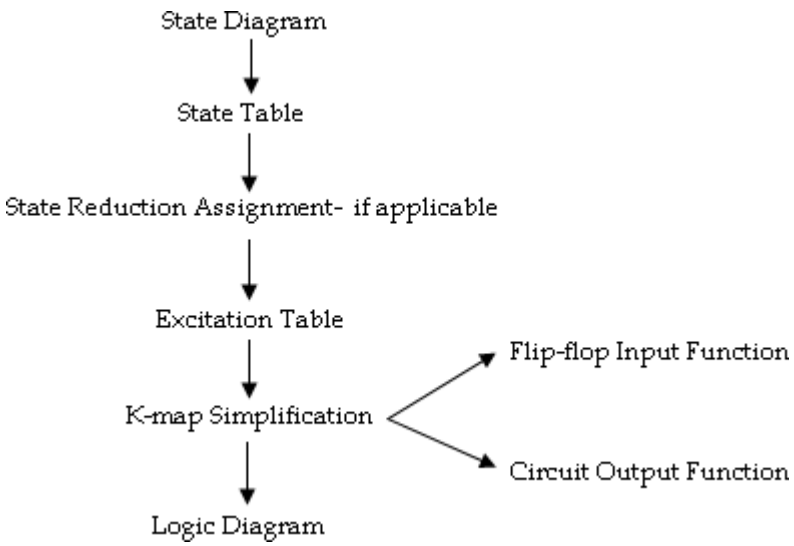
Reduced state diagram

DESIGN OF SYNCHRONOUS SEQUENTIAL CIRCUITS

A synchronous sequential circuit is made up of number of Flip-Flops and combinational gates. The design of circuit consists of choosing the Flip-Flops and then finding a combinational gate structure together with the Flip-Flops. The number of Flip-Flops is determined from the number of states needed in the circuit. The combinational circuit is derived from the state table.

Design procedure:

1. The given problem is determined with a state diagram.
2. From the state diagram, obtain the state table.
3. The number of states may be reduced by state reduction methods (if applicable).
4. Assign binary values to each state (Binary Assignment) if the state table contains letter symbols.
5. Determine the number of Flip-Flops and assign a letter symbol (A, B, C,…) to each.
6. Choose the type of Flip-Flop (SR, JK, D, T) to be used.
7. From the state table, circuit excitation and output tables.
8. Using K-map or any other simplification method, derive the circuit output functions and the Flip-Flop input functions.
9. Draw the logic diagram.



The type of Flip-Flop to be used may be included in the design specifications or may depend what is available to the designer. Many digital systems are constructed with JK Flip-Flops because they are the most versatile available. The selection of inputs is given as follows.

Flip-Flop	Application
JK	General Applications
D	Applications requiring transfer of data (Ex: Shift Registers)
T	Application involving complementation (Ex: Binary Counters)

Excitation Tables:

Before going to the design examples for the clocked synchronous sequential circuits we revise Flip-Flop excitation tables.

SR Flip-flop

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D Flip-flop

Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	0
1	1	1

JK flip-flop

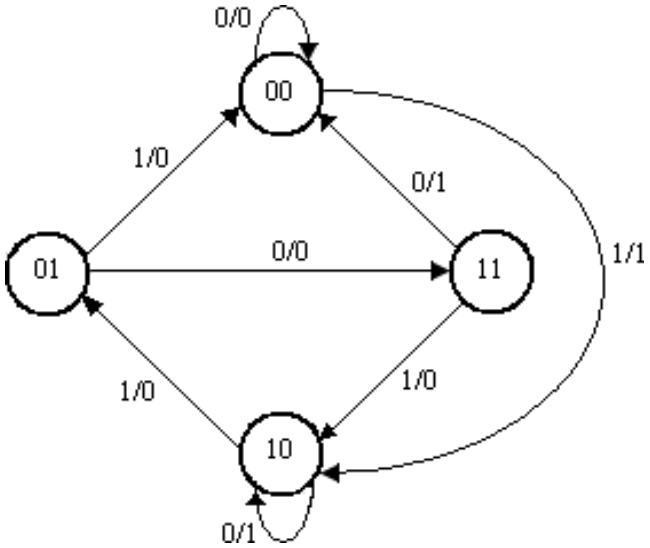
Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

T flip-flop

Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	1
1	1	0

Solved more Example Problems

1. **A sequential circuit has one input and one output. The state diagram is shown below. Design the sequential circuit with a) D-Flip-Flops, b) T Flip-Flops, c) RS Flip-Flops and d) JK Flip-Flops.**



Soln:

State Table:

The state table for the state diagram is,

Present state		Next state		Output	
		X= 0	X= 1	X= 0	X= 1
A	B	AB	AB	Y	Y
0	0	00	10	0	1
0	1	11	00	0	0
1	0	10	01	1	0
1	1	00	10	1	0

State reduction:

As seen from the state table there is no equivalent states. Therefore, no reduction in the state diagram.

The state table shows that circuit goes through four states, therefore we require 2 Flip-Flops (number of states= 2^m, where m= number of Flip-Flops). Since two Flip-Flops are required first is denoted as A and second is denoted as B.

i) Design using D Flip-Flops

Excitation table:

Using the excitation table for T Flip-Flop, we can determine the excitation table for the given circuit as,

Present State	Next State	Input
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation table for D Flip-Flop

Present state		Input	Next state		Flip-Flop Inputs		Output
A	B	X	A	B	D_A	D_B	Y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1
0	1	0	1	1	1	1	0
0	1	1	0	0	0	0	0
1	0	0	1	0	1	0	1
1	0	1	0	1	0	1	0
1	1	0	0	0	0	0	1
1	1	1	1	0	1	0	0

Circuit excitation table

K-map Simplification:

For Flip-flop A

A \ BX	00	01	11	10
0	0	1	0	1
1	1	0	1	0

For Flip-flop B

A \ BX	00	01	11	10
0	0	0	0	1
1	0	1	0	0

For Output

A \ BX	00	01	11	10
0	0	1	0	0
1	1	0	0	1

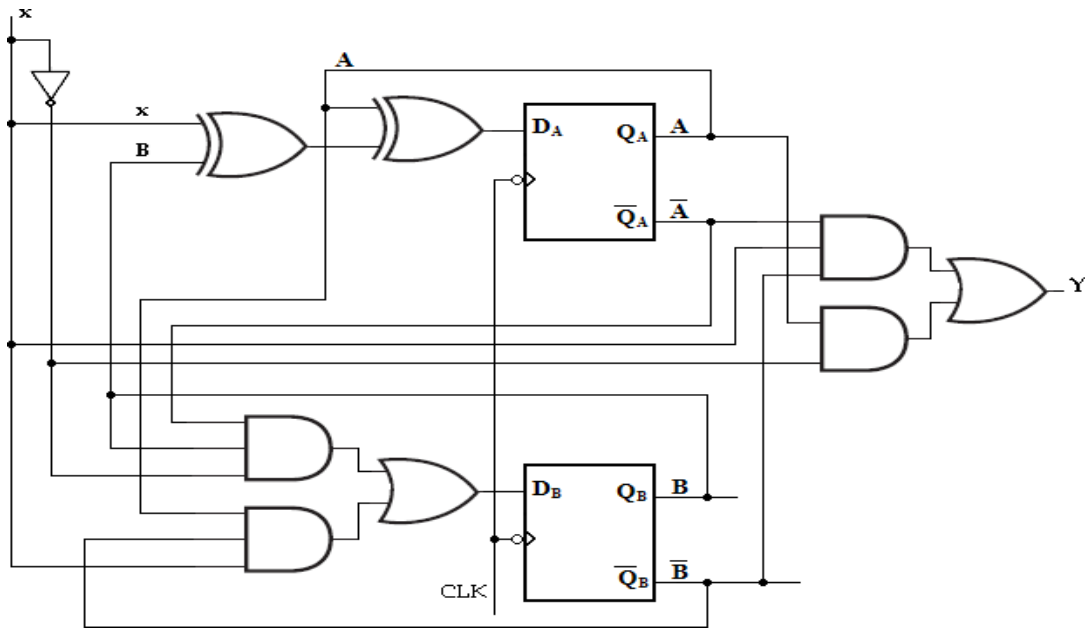
$D_A = A'B'X + A'BX' + ABX + AB'X'$

$= A \oplus (B \oplus x)$

$D_B = A'BX' + AB'X$

$Y = A'B'X + AX'$

With these Flip-Flop input functions and circuit output function we can draw the logic diagram as follows.



Logic diagram of given sequential circuit using D Flip-Flop

ii) Design using T Flip-Flops:

Using the excitation table for T Flip-Flop, we can determine the excitation table for the given circuit as,

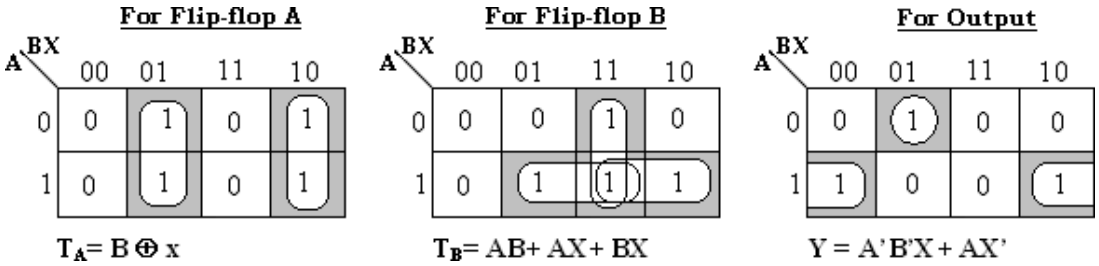
Present State	Next State	Input
Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table for T Flip-Flop

Present state		Input	Next state		Flip-Flop Inputs		Output
A	B	X	A	B	T_A	T_B	Y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1
0	1	0	1	1	1	0	0
0	1	1	0	0	0	1	0
1	0	0	1	0	0	0	1
1	0	1	0	1	1	1	0
1	1	0	0	0	1	1	1
1	1	1	1	0	0	1	0

Circuit excitation table

K-map Simplification:



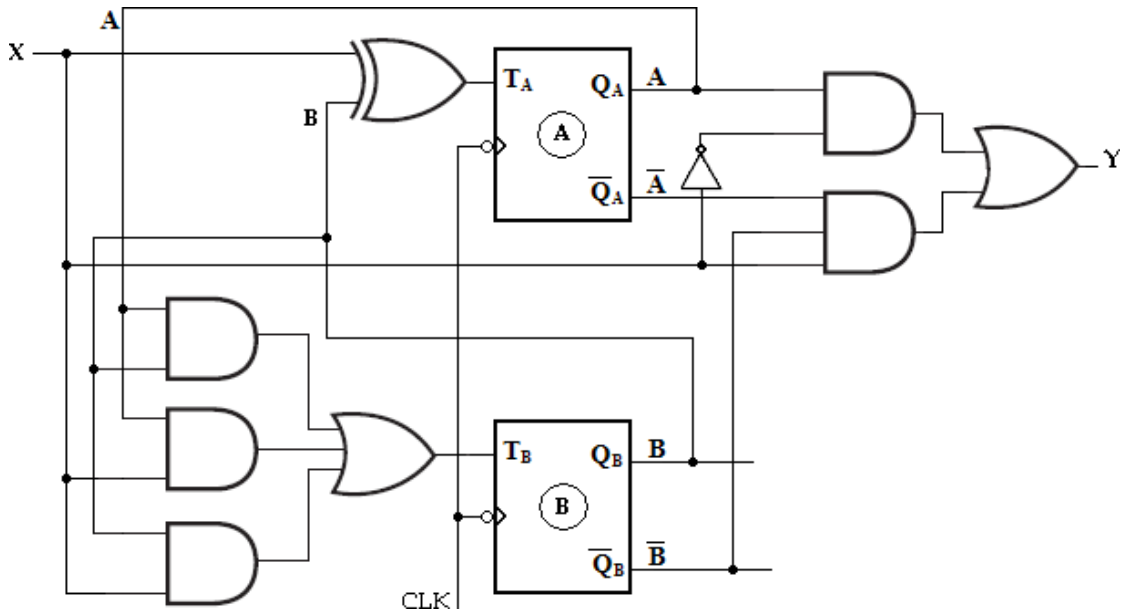
Therefore, input functions for,

$T_A = B \oplus x$ and

$T_B = AB + AX + BX$

Circuit output function, **$Y = XA'B' + X'A$**

With these Flip-Flop input functions and circuit output function we can draw the logic diagram as follows.



Logic diagram of given sequential circuit using T Flip-Flop

iii) Design using SR Flip-Flops:

Using the excitation table for RS Flip-Flop, we can determine the excitation table for the given circuit as,

Present State	Next State	Inputs	
Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Excitation table for SR Flip-Flop

Present state		Input	Next state		Flip-Flop Inputs				Output
A	B	X	A	B	S_A	R_A	S_B	R_B	Y
0	0	0	0	0	0	x	0	x	0
0	0	1	1	0	1	0	0	x	1
0	1	0	1	1	1	0	x	0	0
0	1	1	0	0	0	x	0	1	0
1	0	0	1	0	x	0	0	x	1
1	0	1	0	1	0	1	1	0	0
1	1	0	0	0	0	1	0	1	1
1	1	1	1	0	x	0	0	1	0

Circuit excitation table

K-map Simplification:

For Flip-flop A

For S_A

A \ BX	00	01	11	10
0	0	(1)	0	(1)
1	x	0	x	0

$S_A = A'B'X + A'BX'$

$= A' (B \oplus X)$

For R_A

A \ BX	00	01	11	10
0	x	0	x	0
1	0	(1)	0	(1)

$R_A = ABX' + AB'X'$

For Output

A \ BX	00	01	11	10
0	0	(1)	0	0
1	1	0	0	(1)

$Y = A'B'X + AX'$

For Flip-flop B

For S_B

A \ BX	00	01	11	10
0	0	0	0	x
1	0	(1)	0	0

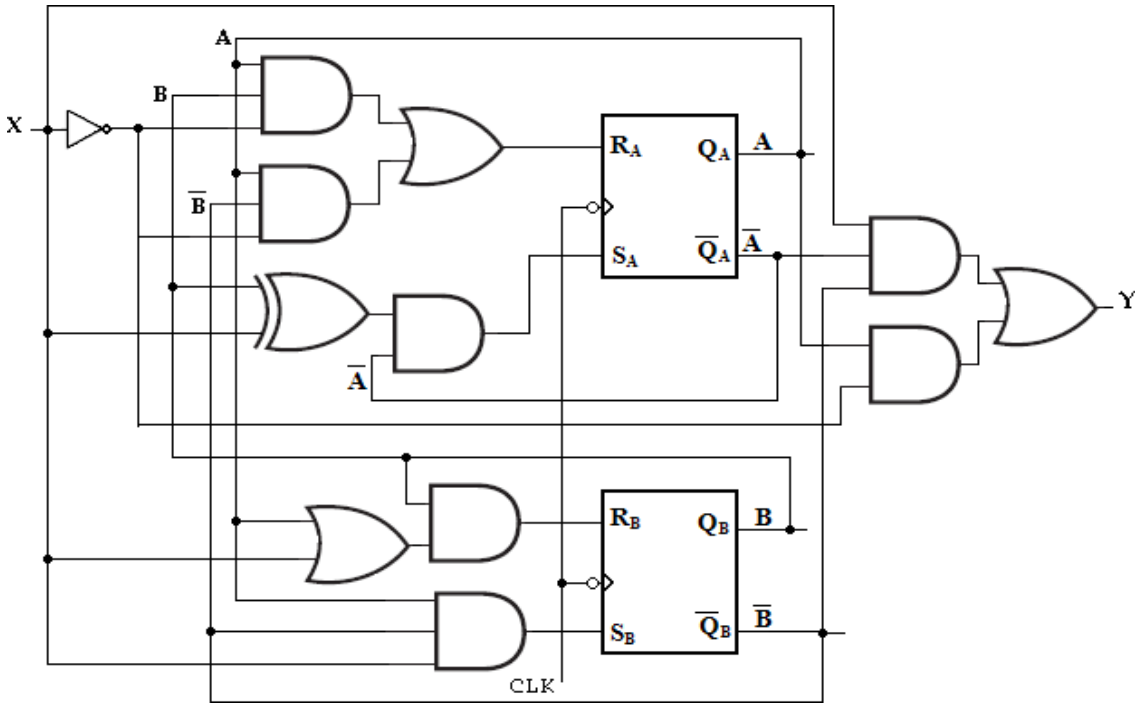
$S_B = AB'X$

For R_B

A \ BX	00	01	11	10
0	x	x	1	0
1	x	0	(1)	1

$R_B = AB + BX$

With these Flip-Flop input functions and circuit output function we can draw the logic diagram as follows.



iii) Design using JK Flip-Flops:

Using the excitation table for JK Flip-Flop, we can determine the excitation table for the given circuit as,

Present State	Next State	Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Excitation table for JK Flip-Flop

Present state		Input	Next state		Flip-Flop Inputs				Output
A	B	X	A	B	J_A	K_A	J_B	K_B	Y
0	0	0	0	0	0	x	0	x	0
0	0	1	1	0	1	x	0	x	1
0	1	0	1	1	1	x	x	0	0
0	1	1	0	0	0	x	x	1	0
1	0	0	1	0	x	0	0	x	1
1	0	1	0	1	x	1	1	x	0
1	1	0	0	0	x	1	x	1	1
1	1	1	1	0	x	0	x	1	0

Circuit excitation table

K-map Simplification:

For Flip-flop A

For J_A

A \ BX	00	01	11	10
0	0	1	0	1
1	x	x	x	x

$J_A = BX' + B'X$
$= B \oplus X$

For K_A

A \ BX	00	01	11	10
0	x	x	x	x
1	0	1	0	1

$K_A = BX' + B'X$
$= B \oplus X$

For Output

A \ BX	00	01	11	10
0	0	1	0	0
1	1	0	0	1

$Y = A'B'X + AX'$

For Flip-flop B

For J_B

A \ BX	00	01	11	10
0	0	0	x	x
1	0	1	x	x

$J_B = AX$

For K_B

A \ BX	00	01	11	10
0	x	x	1	0
1	x	x	1	1

$K_B = A + X$

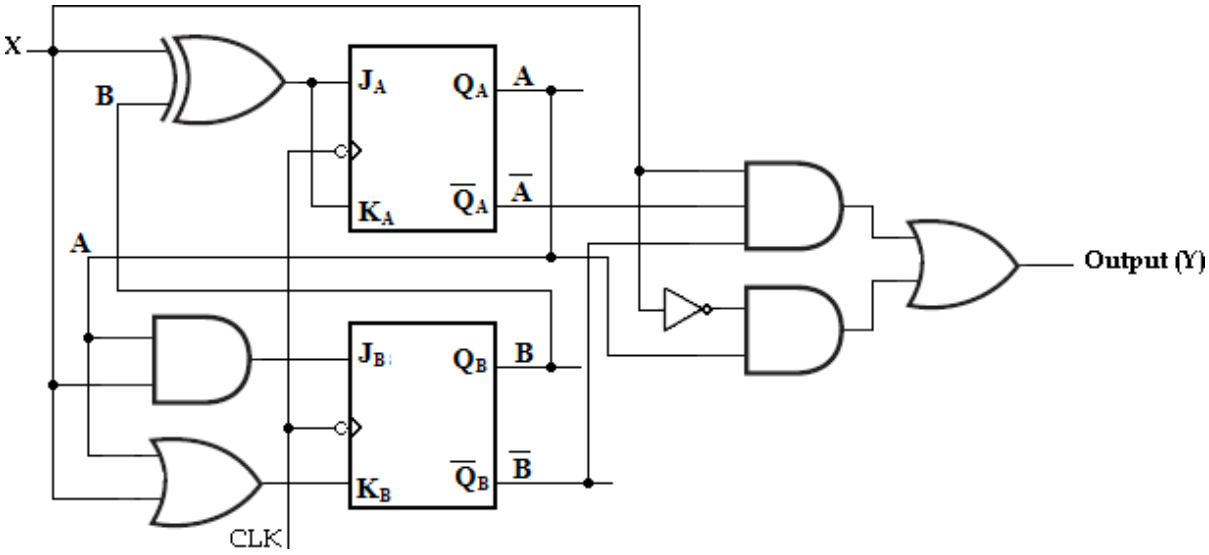
The input functions for,

$J_A = BX' + B'X$ **$J_B = AX$**
$= B \oplus X$

$K_A = BX' + B'X$ **$K_B = A + X$**
$= B \oplus X$

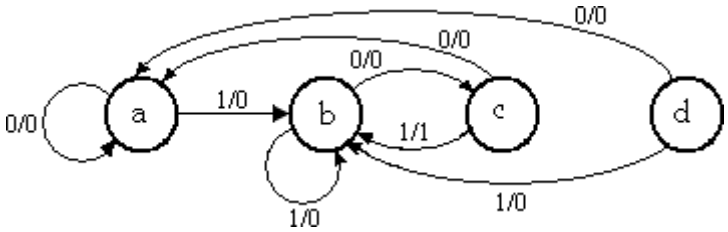
Circuit output function, **$Y = AX' + A'B'X$**

With these Flip-Flop input functions and circuit output function we can draw the logic diagram as follows.



Logic diagram of given sequential circuit using JK Flip-Flop

2. **Design a clocked sequential machine using JK Flip-Flops for the state diagram shown in the figure. Use state reduction if possible. Make proper state assignment.**



Soln:

State Table:

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
a	a	b	0	0
b	c	b	0	0
c	a	b	0	1
d	a	b	0	0

From the above state table **a** and **d** generate exactly same next state and same output for every possible set of inputs. The state **a** and **d** go to next states **a** and **b** and have outputs 0 and 0 for x=0 and x=1 respectively. Therefore state **d** can be removed and replaced by **a**. The final reduced state table is shown below.

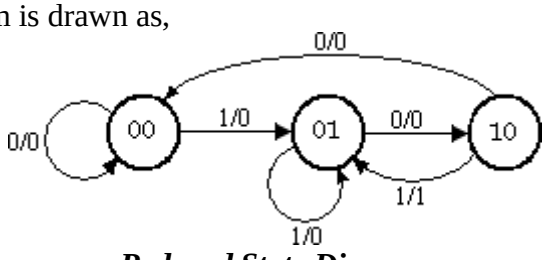
Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
a	a	b	0	0
b	c	b	0	0
c	a	b	0	1

Reduced State table

Binary Assignment:

Now each state is assigned with binary values. Since there are three states, number of Flip-Flops required is two and 2 binary numbers are assigned to the states. a= 00; b= 0; and c= 10

The reduced state diagram is drawn as,



Reduced State Diagram

Excitation Table:

Present State	Next State	Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Excitation table for JK Flip-Flop

Input	Present state		Next state		Flip-Flop Inputs				Output
X	A	B	A	B	J_A	K_A	J_B	K_B	Y
0	0	0	0	0	0	x	0	x	0
1	0	0	0	1	0	x	1	x	0
0	0	1	1	0	1	x	x	1	0
1	0	1	0	1	0	x	x	0	0
0	1	0	0	0	x	1	0	x	0
1	1	0	0	1	x	1	1	x	1
0	1	1	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x

K-map Simplification:

For Flip-flop A

For J_A

A \ BX	00	01	11	10
0	0	1	x	x
1	0	0	x	x

$J_A = X'B$

For K_A

A \ BX	00	01	11	10
0	x	x	x	1
1	x	x	x	1

$K_A = 1$

For Output

A \ BX	00	01	11	10
0	0	0	x	0
1	0	0	x	1

$Y = XA$

For Flip-flop B

For J_B

A \ BX	00	01	11	10
0	0	x	x	0
1	1	x	x	1

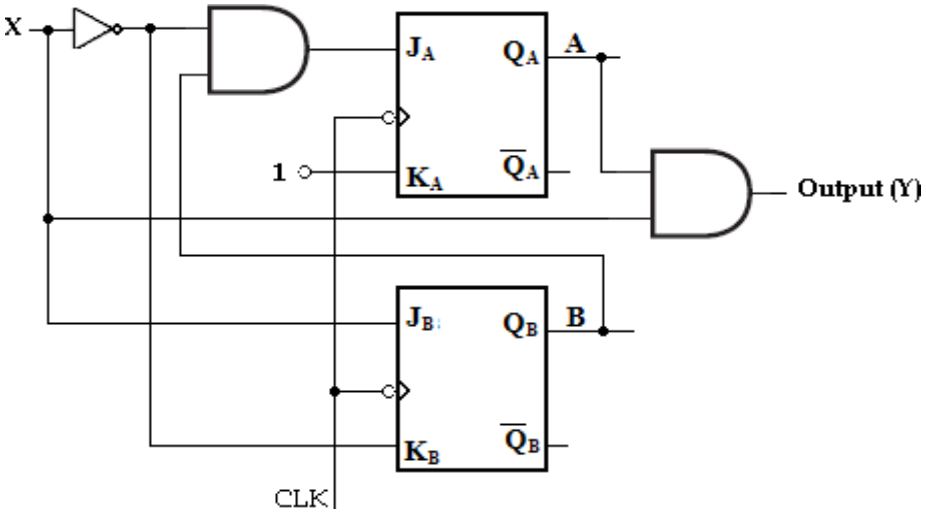
$J_B = X$

For K_B

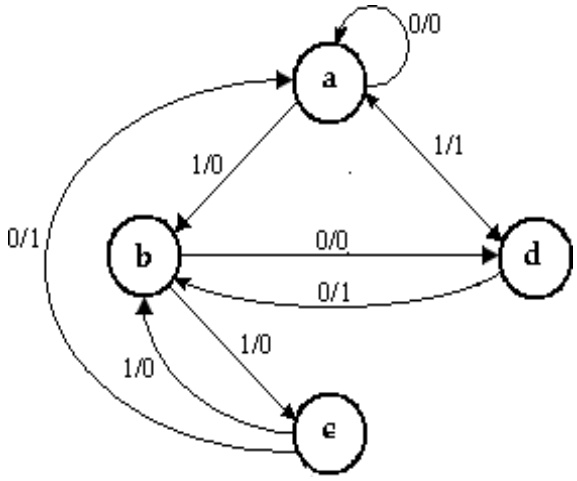
A \ BX	00	01	11	10
0	x	1	x	x
1	x	0	x	x

$K_B = X'$

With these Flip-Flop input functions and circuit output function we can draw the logic diagram as follows.



3. **Design a clocked sequential machine using T Flip-Flops for the following state diagram. Use state reduction if possible. Also use binary state assignment.**



Soln:

State Table:

State table for the given state diagram is,

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
a	a	b	0	0
b	d	c	0	0
c	a	b	1	0
d	b	a	1	1

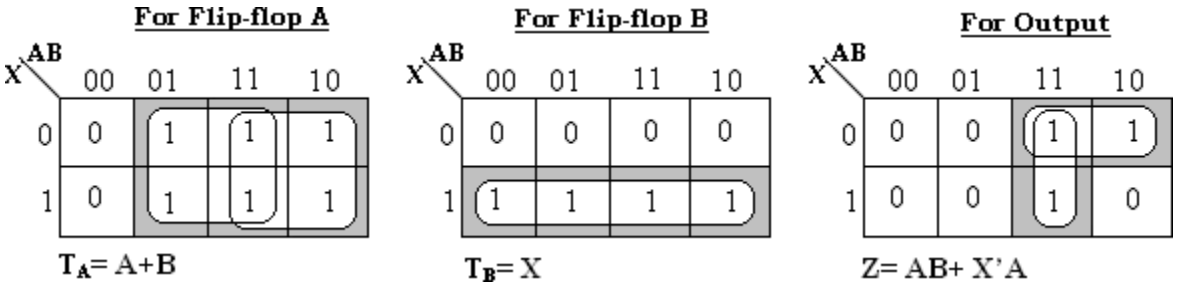
Even though a and c are having same next states for input X=0 and X=1, as the outputs are not same state reduction is not possible.

State Assignment:

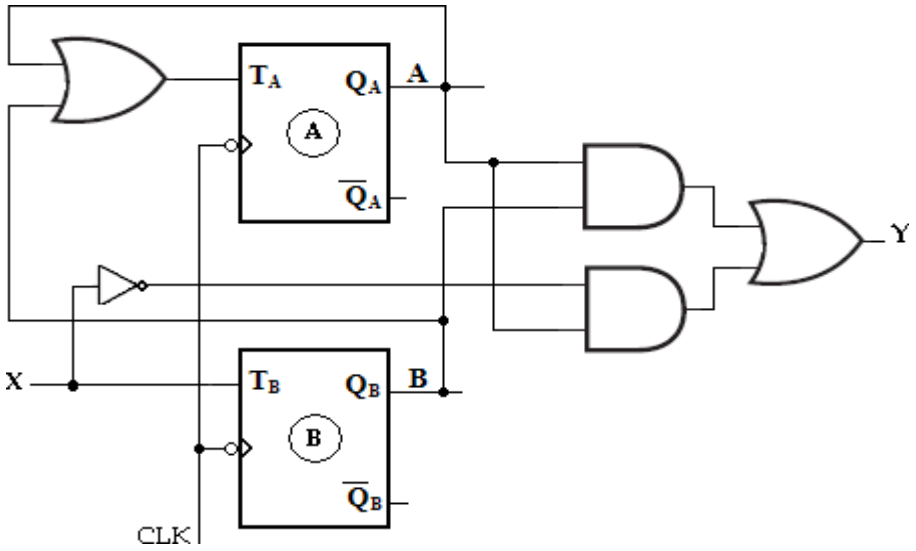
Use straight binary assignments as a= 00, b= 01, c= 10 and d= 11, the transition table is,

Input	Present state		Next state		Flip-Flop Inputs		Output
X	A	B	A	B	T_A	T_B	Y
0	0	0	0	0	0	0	0
0	0	1	1	1	1	0	0
0	1	0	0	0	1	0	1
0	1	1	0	1	1	0	1
1	0	0	0	1	0	1	0
1	0	1	1	0	1	1	0
1	1	0	0	1	1	1	0
1	1	1	0	0	1	1	1

K-map simplification:



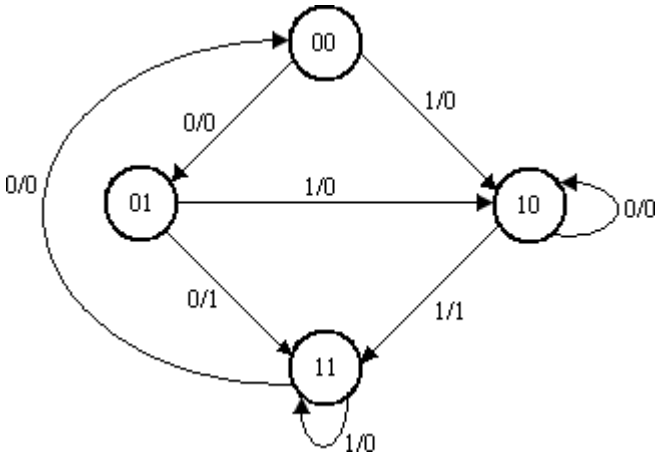
Logic Diagram:



STATE ASSIGNMENT

In sequential circuits, the behavior of the circuit is defined in terms of its inputs, present states, next states and outputs. To generate desired next state at particular present state and inputs, it is necessary to have specific Flip-Flop inputs. These Flip- Flop inputs are described by a set of Boolean functions called Flip-Flop input functions.

To determine the Flip-Flop functions, it is necessary to represent states in the state diagram using binary values instead of alphabets. This procedure is known as ***state assignment***.



Reduced state diagram with binary states

Rules for state assignments

There are two basic rules for making state assignments.

Rule 1: States having the **same** NEXT STATES for a given input condition should have assignments which can be grouped into logically adjacent cells in a K-map.

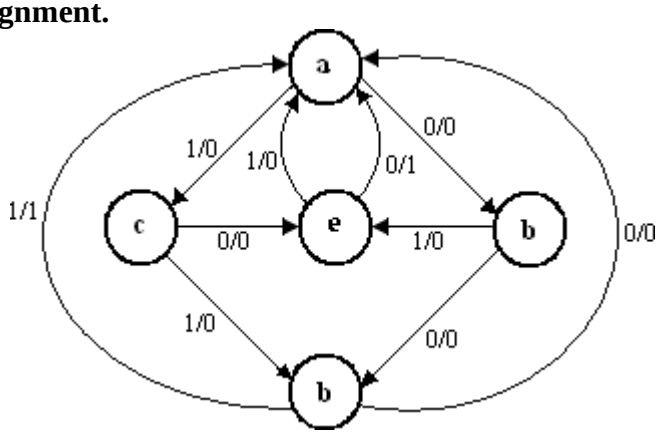
Rule 2: States that are the NEXT STATES of a single state should have assignment which can be grouped into logically adjacent cells in a K-map.

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
00	01	10	0	0
01	11	10	1	0
10	10	11	0	1
11	00	11	0	0

State table with assignment states

State Assignment Problem:

1. **Design a sequential circuit for a state diagram shown below. Use state assignment rules for assigning states and compare the required combinational circuit with random state assignment.**



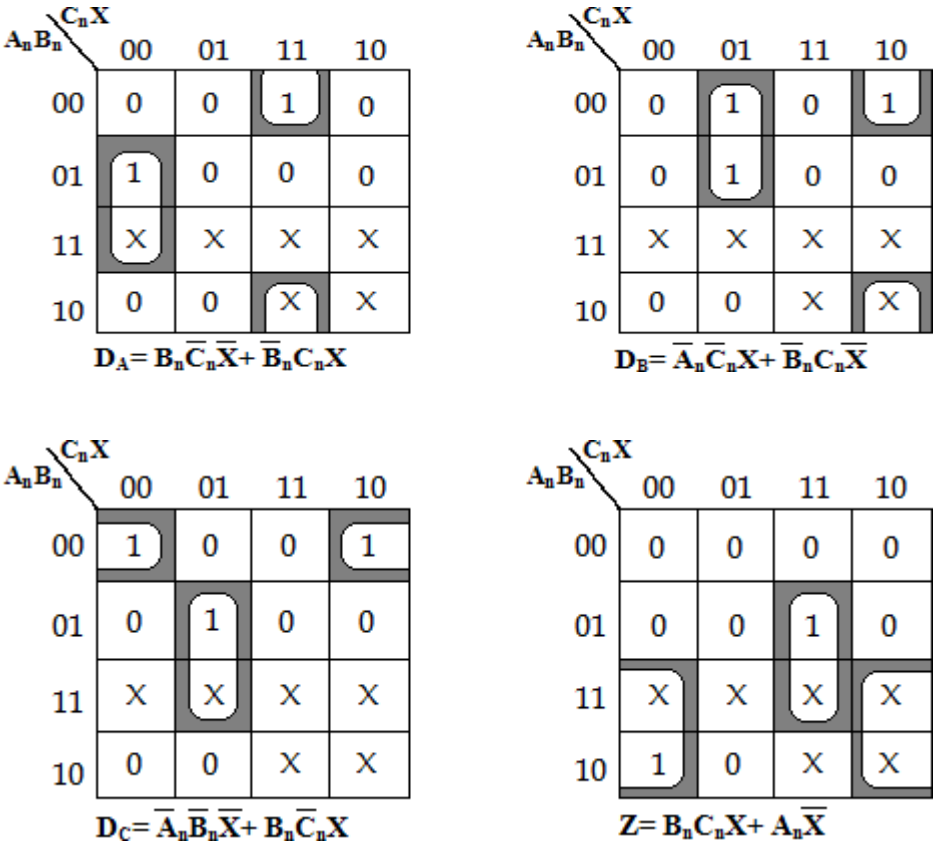
Using random state assignment we assign,

a= 000, b= 001, c= 010, d= 011 and e= 100.

The excitation table with these assignments is given as,

Present state			Input	Next state			Output
A_n	B_n	C_n	X	A_{n+1}	B_{n+1}	C_{n+1}	Z
0	0	0	0	0	0	1	0
0	0	0	1	0	1	0	0
0	0	1	0	0	1	1	0
0	0	1	1	1	0	0	0
0	1	0	0	1	0	0	0
0	1	0	1	0	1	1	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	1
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

K-map Simplification:

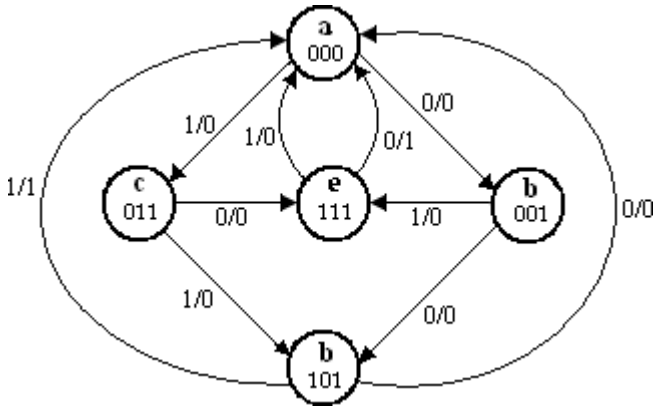


The random assignments require:

7 three input AND functions
1 two input AND function
4 two input OR functions

12 gates with 31 inputs

Now, we will apply the state assignment rules and compare the results.



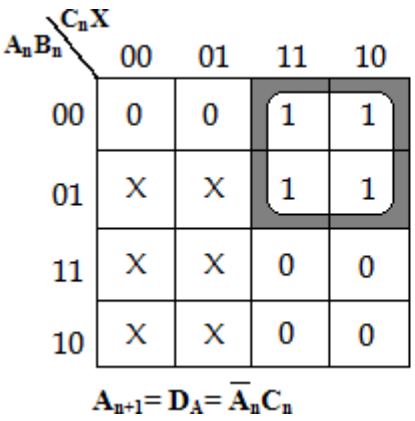
State diagram after applying Rules 1 and 2

Rule 1 says that: e and d must be adjacent, and b and c must be adjacent.
Rule 2 says that: e and d must be adjacent, and b and c must be adjacent.

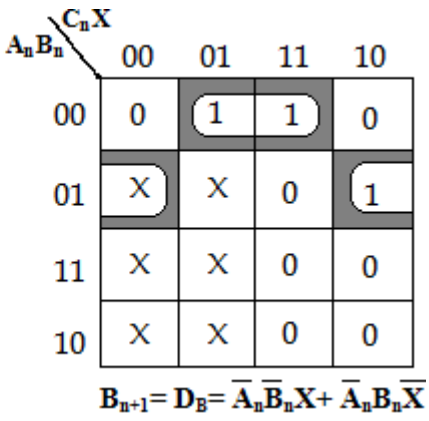
Applying Rule 1, Rule 2 to the state diagram we get the state assignment as,

Present state			Input	Next state			Output
A_n	B_n	C_n	X	A_{n+1}	B_{n+1}	C_{n+1}	Z
0	0	0	0	0	0	1	0
0	0	0	1	0	1	1	0
0	0	1	0	1	0	1	0
0	0	1	1	1	1	1	0
0	1	0	0	x	x	x	x
0	1	0	1	x	x	x	x
0	1	1	0	1	1	1	0
0	1	1	1	1	0	1	0
1	0	0	0	x	x	x	x
1	0	0	1	x	x	x	x
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	0	0	0	1
1	1	1	1	0	0	0	0

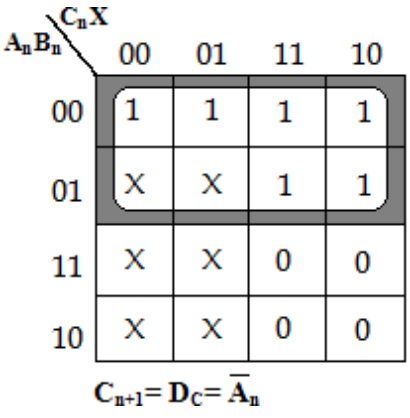
K-map Simplification:



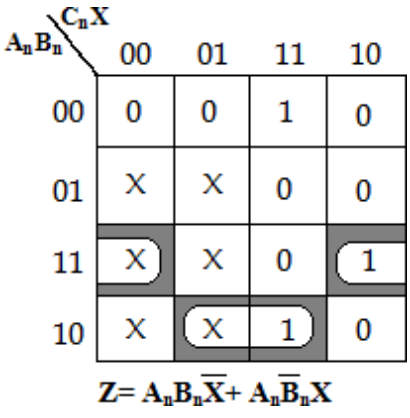
$A_{n+1} = D_A = \overline{A}_n C_n$



$B_{n+1} = D_B = \overline{A}_n \overline{B}_n X + \overline{A}_n B_n \overline{X}$



$C_{n+1} = D_C = \overline{A}_n$



$Z = A_n B_n \overline{X} + A_n \overline{B}_n X$

The state assignments using Rule 1 and 2 require:

4 three input AND functions

1 two input AND function

2 two input OR functions

---

7 gates with 18 inputs

Thus by simply applying Rules 1 and 2 good results have been achieved.

SYNCHRONOUS COUNTERS

Flip-Flops can be connected together to perform counting operations. Such a group of Flip- Flops is a **counter**. The number of Flip-Flops used and the way in which they are connected determine the number of states (called the modulus) and also the specific sequence of states that the counter goes through during each complete cycle.

Counters are classified into two broad categories according to the way they are clocked:

- Asynchronous counters,
- Synchronous counters.

In asynchronous (ripple) counters, the first Flip-Flop is clocked by the external clock pulse and then each successive Flip-Flop is clocked by the output of the preceding Flip-Flop.

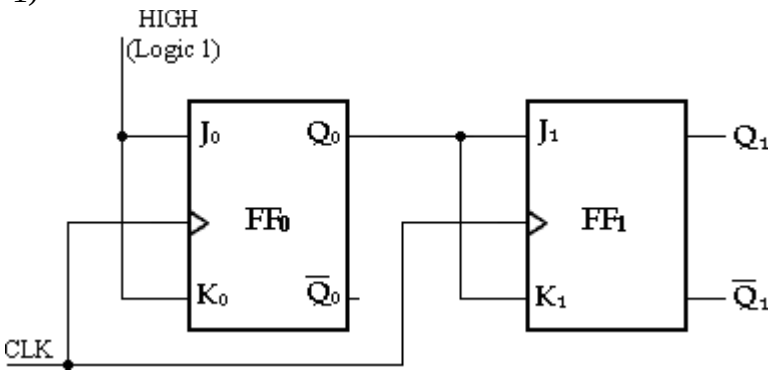
In synchronous counters, the clock input is connected to all of the Flip-Flops so that they are clocked simultaneously. Within each of these two categories, counters are classified primarily by the type of sequence, the number of states, or the number of Flip-Flops in the counter.

The term 'synchronous' refers to events that have a fixed time relationship with each other. In synchronous counter, the clock pulses are applied to all Flip-Flops simultaneously. Hence there is minimum propagation delay.

S.No	Asynchronous (ripple) counter	Synchronous counter
1	All the Flip-Flops are not clocked simultaneously.	All the Flip-Flops are clocked simultaneously.
2	The delay times of all Flip-Flops are added. Therefore there is considerable propagation delay.	There is minimum propagation delay.
3	Speed of operation is low	Speed of operation is high.
4	Logic circuit is very simple even for more number of states.	Design involves complex logic circuit as number of state increases
5	Minimum numbers of logic devices are needed.	The number of logic devices is more than ripple counters.
6	Cheaper than synchronous counters.	Costlier than ripple counters.

2-Bit Synchronous Binary Counter

In this counter the clock signal is connected in parallel to clock inputs of both the Flip-Flops (FF_0 and FF_1). The output of FF_0 is connected to J_1 and K_1 inputs of the second Flip-Flop (FF_1).



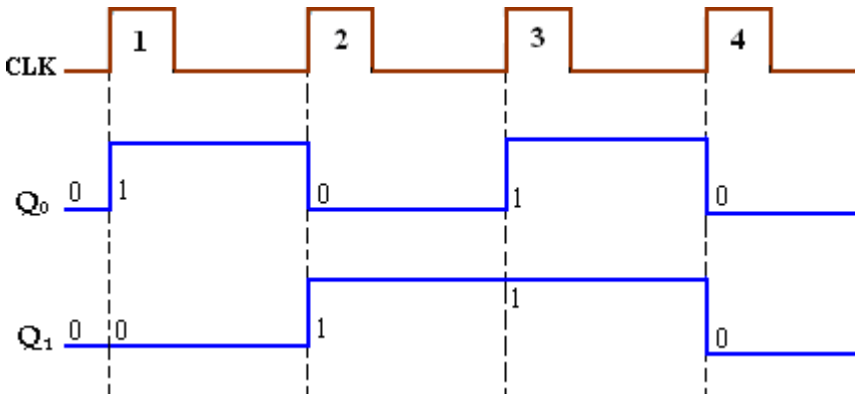
2-Bit Synchronous Binary Counter

Assume that the counter is initially in the binary 0 state: i.e., both Flip-Flops are RESET. When the positive edge of the first clock pulse is applied, FF_0 will toggle because $J_0 = k_0 = 1$, whereas FF_1 output will remain 0 because $J_1 = k_1 = 0$. After the first clock pulse $Q_0=1$ and $Q_1=0$.

When the leading edge of CLK2 occurs, FF_0 will toggle and Q_0 will go LOW. Since FF_1 has a HIGH ($Q_0 = 1$) on its J_1 and K_1 inputs at the triggering edge of this clock pulse, the Flip-Flop toggles and Q_1 goes HIGH. Thus, after CLK2, $Q_0 = 0$ and $Q_1 = 1$.

When the leading edge of CLK3 occurs, FF_0 again toggles to the SET state ($Q_0 = 1$), and FF_1 remains SET ($Q_1 = 1$) because its J_1 and K_1 inputs are both LOW ($Q_0 = 0$). After this triggering edge, $Q_0 = 1$ and $Q_1 = 1$.

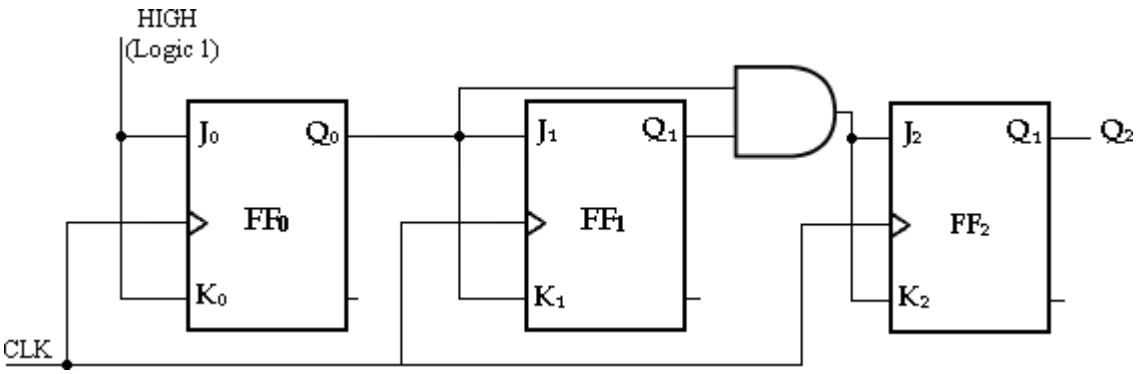
Finally, at the leading edge of CLK4, Q_0 and Q_1 go LOW because they both have a toggle condition on their J_1 and K_1 inputs. The counter has now recycled to its original state, $Q_0 = Q_1 = 0$.



Timing diagram

3-Bit Synchronous Binary Counter

A 3 bit synchronous binary counter is constructed with three JK Flip-Flops and an AND gate. The output of FF_0 (Q_0) changes on each clock pulse as the counter progresses from its original state to its final state and then back to its original state. To produce this operation, FF_0 must be held in the toggle mode by constant HIGH, on its J_0 and K_0 inputs.

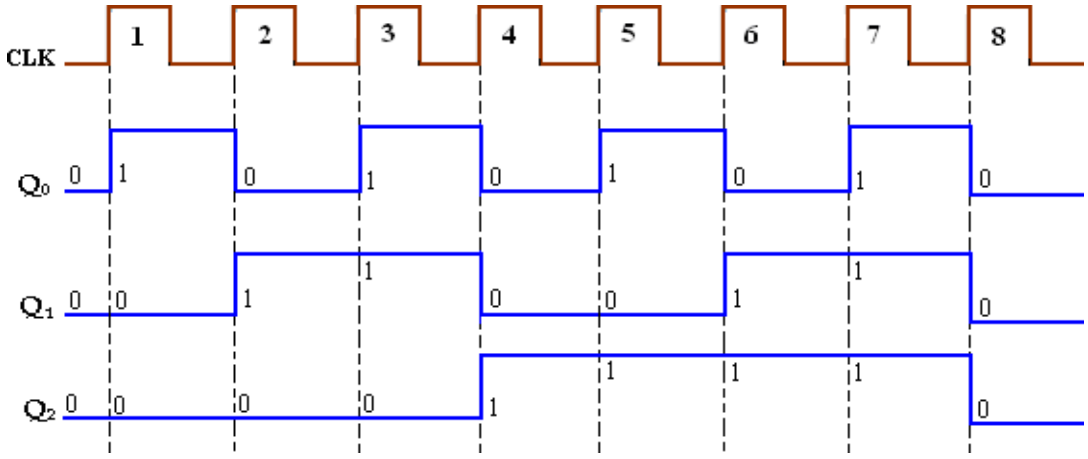


3-Bit Synchronous Binary Counter

The output of FF1 (Q1) goes to the opposite state following each time Q0= 1. This change occurs at CLK2, CLK4, CLK6, and CLK8. The CLK8 pulse causes the counter to recycle. To produce this operation, Q0 is connected to the J1 and K1 inputs of FF1. When Q0= 1 and a clock pulse occurs, FF1 is in the toggle mode and therefore changes state. When Q0= 0, FF1 is in the no-change mode and remains in its present state.

The output of FF2 (Q2) changes state both times; it is preceded by the unique condition in which both Q0 and Q1 are HIGH. This condition is detected by the AND gate and applied to the J2 and K2 inputs of FF3. Whenever both outputs Q0= Q1= 1, the output of the AND gate makes the J2= K2= 1 and FF2 toggles on the following clock pulse. Otherwise, the J2 and K2 inputs of FF2 are held LOW by the AND gate output, FF2 does not change state.

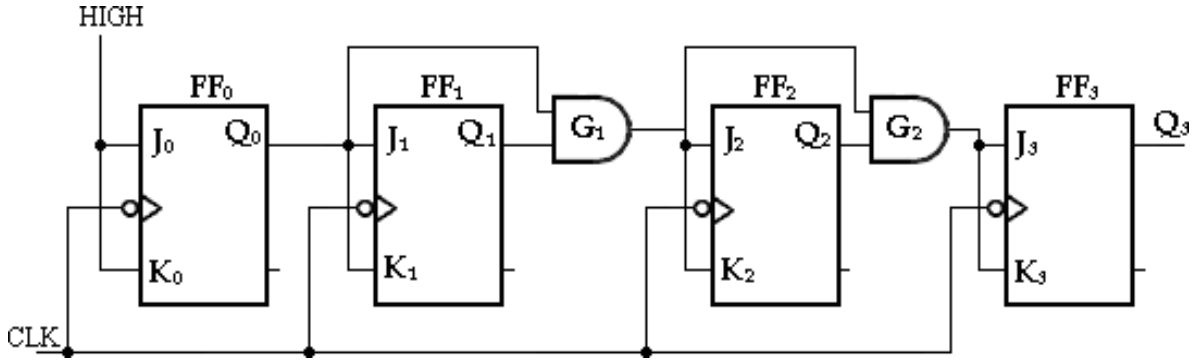
CLOCK Pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0



Timing diagram

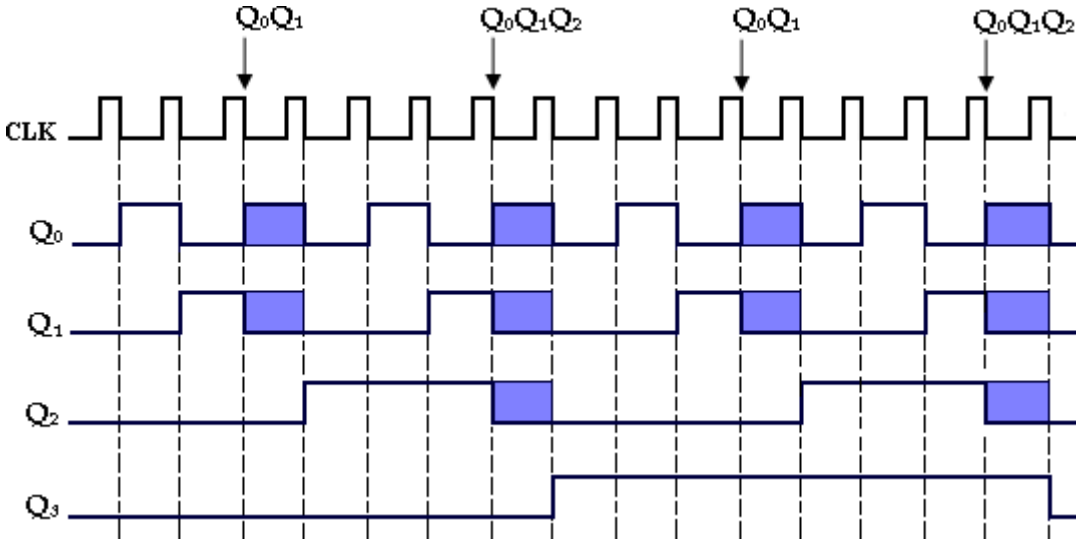
4-Bit Synchronous Binary Counter

This particular counter is implemented with negative edge-triggered Flip- Flops. The reasoning behind the J and K input control for the first three Flip- Flops is the same as previously discussed for the 3-bit counter. For the fourth stage, the Flip- Flop has to change the state when $Q_0 = Q_1 = Q_2 = 1$. This condition is decoded by AND gate G_3.



4-Bit Synchronous Binary Counter

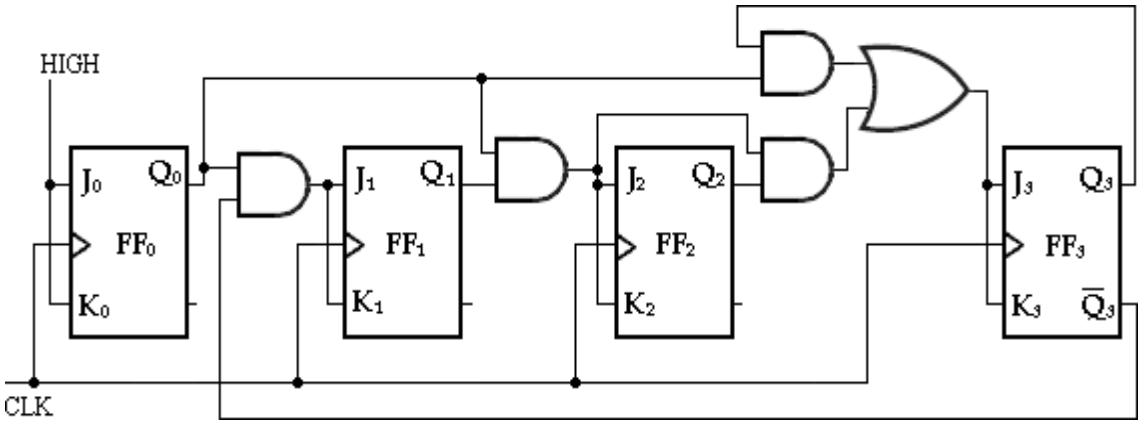
Therefore, when $Q_0 = Q_1 = Q_2 = 1$, Flip-Flop FF3 toggles and for all other times it is in a no-change condition. Points where the AND gate outputs are HIGH are indicated by the shaded areas.



Timing diagram

4-Bit Synchronous Decade Counter: (BCD Counter):

BCD decade counter has a sequence from 0000 to 1001 (9). After 1001 state it must recycle back to 0000 state. This counter requires four Flip-Flops and AND/OR logic as shown below.



4-Bit Synchronous Decade Counter

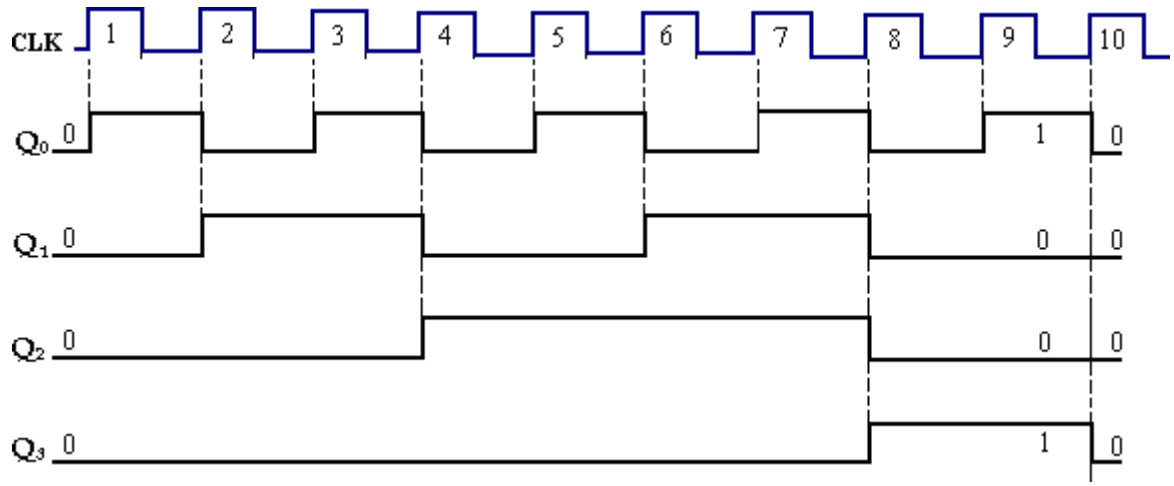
CLOCK Pulse	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10(recycles)	0	0	0	0

First, notice that FF0 (Q0) toggles on each clock pulse, so the logic equation for its J0 and K0 input is**J0= K0= 1.** This equation is implemented by connecting J0 and K0 to a constant HIGH level.

Next, notice from table, that FF1 (Q1) changes on the next clock pulse each time Q0 = 1 and Q3 = 0, so the logic equation for the J1 and K1 inputs is **J1= K1= Q0Q3'.** This equation is implemented by ANDing Q0 and Q3 and connecting the gate output to the J1 and K1 inputs of FFl.

Flip-Flop 2 (Q2) changes on the next clock pulse each time both Q0 = Q1 = 1. This requires an input logic equation as follows: **J2= K2= Q0Q1.** This equation is implemented by ANDing Q0 and Q1 and connecting the gate output to the J2 and K2 inputs of FF3.

Finally, FF3 (Q3) changes to the opposite state on the next clock pulse each time Q0 = 1, Q1 = 1, and Q2 = 1 (state 7), or when Q0 = 1 and Q1 = 1 (state 9). The equation for this is as follows: **J3= K3= Q0Q1Q2+ Q0Q3.** This function is implemented with the AND/OR logic connected to the J3 and K3 inputs of FF3.



Timing diagram

Synchronous UP/DOWN Counter

An up/down counter is a bidirectional counter, capable of progressing in either direction through a certain sequence. A 3-bit binary counter that advances upward through its sequence (0, 1, 2, 3, 4, 5, 6, 7) and then can be reversed so that it goes through the sequence in the opposite direction (7, 6, 5, 4, 3, 2, 1,0) is an illustration of up/down sequential operation.

The complete up/down sequence for a 3-bit binary counter is shown in table below. The arrows indicate the state-to-state movement of the counter for both its UP and its DOWN modes of operation. An examination of Q0 for both the up and down sequences shows that FF0 toggles on each clock pulse. Thus, the J0 and K0 inputs of FF0 are, **J0= K0= 1.**

CLOCK PULSE	UP	Q_2	Q_1	Q_0	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

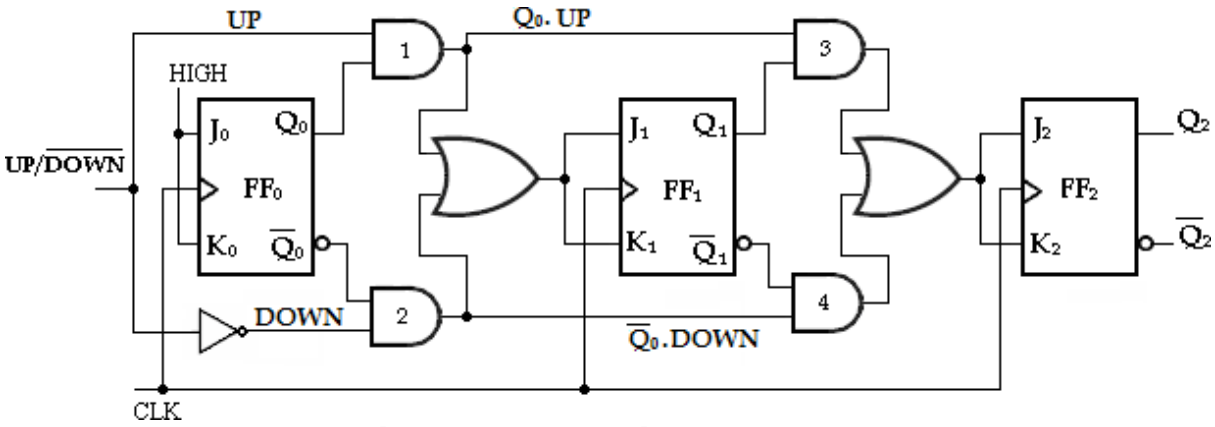
To form a synchronous UP/DOWN counter, the control input (UP/DOWN) is used to allow either the normal output or the inverted output of one Flip-Flop to the J and K inputs of the next Flip-Flop. When UP/DOWN= 1, the MOD 8 counter will count from 000 to 111 and UP/DOWN= 0, it will count from 111 to 000.

When UP/DOWN= 1, it will enable AND gates 1 and 3 and disable AND gates 2 and **4.** This allows the Q0 and Q1 outputs through the AND gates to the J and K inputs of the following Flip-Flops, so the counter counts up as pulses are applied.

When UP/DOWN= 0, the reverse action takes place.

J1= K1= (Q0.UP)+ (Q0'.DOWN)

J2= K2= (Q0. Q1.UP)+ (Q0'.Q1'.DOWN)



3-bit UP/DOWN Synchronous Counter

MODULUS-N-COUNTERS

The counter with 'n' Flip-Flops has maximum MOD number 2^n. Find the number of Flip-Flops (n) required for the desired MOD number (N) using the equation,

$$\mathbf{2^n \geq N}$$

(i) For example, a 3 bit binary counter is a **MOD 8 counter**. The basic counter can be modified to produce MOD numbers less than 2^n by allowing the counter to skin those are normally part of counting sequence.

n= 3

N= 8

$2^n = 2^3 = 8 = N$

(ii) MOD 5 Counter:

$2^n = N$

$2^n = 5$

$2^2 = 4$ less than N.

$2^3 = 8 > N$ (5)

Therefore, 3 Flip-Flops are required.

(iii) MOD 10 Counter:

$2^n = N = 10$

$2^3 = 8$ less than N.

$2^4 = 16 > N$ (10).

To construct any MOD-N counter, the following methods can be used.

1. Find the number of Flip-Flops (n) required for the desired MOD number (N) using the equation,

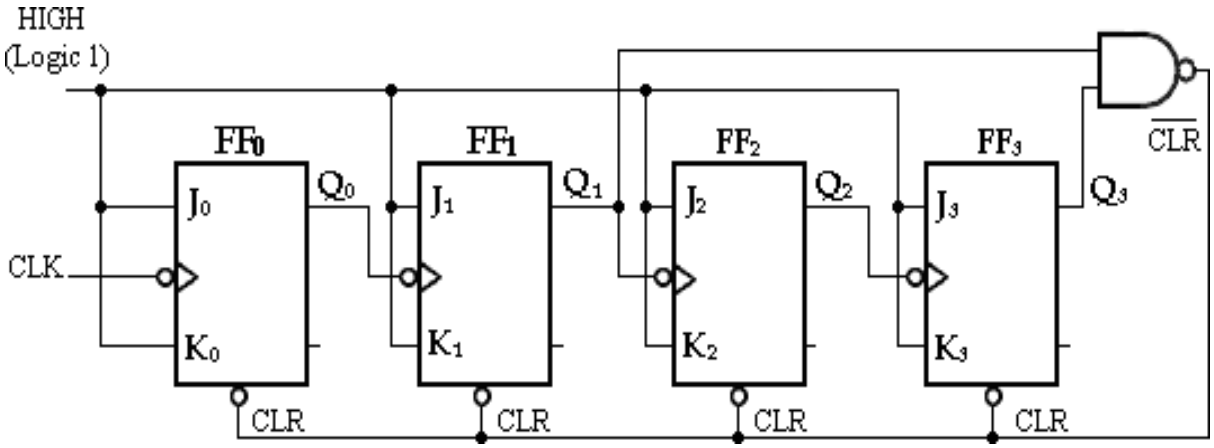
$$\mathbf{2^n \geq N.}$$

2. Connect all the Flip-Flops as a required counter.
3. Find the binary number for N.
4. Connect all Flip-Flop outputs for which Q= 1 when the count is N, as inputsto NAND gate.
5. Connect the NAND gate output to the CLR input of each Flip-Flop.

When the counter reaches N^{th} state, the output of the NAND gate goes LOW, resetting all Flip-Flops to 0. Therefore the counter counts from 0 through N-1.

For example, MOD-10 counter reaches state 10 (1010). i.e., $Q_3Q_2Q_1Q_0$= 1 0 1 0. The outputs Q_3 and Q_1 are connected to the NAND gate and the output of the NAND gate goes LOW and resetting all Flip-Flops to zero. Therefore MOD-10 counter counts from 0000 to 1001. And then recycles to the zero value.

The MOD-10 counter circuit is shown below.



MOD-10 (Decade) Counter

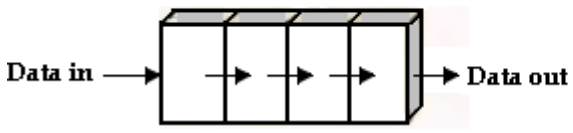
SHIFT REGISTERS

A register is simply a group of Flip-Flops that can be used to store a binary number. There must be one Flip-Flop for each bit in the binary number. For instance, a register used to store an 8-bit binary number must have 8 Flip-Flops. The Flip-Flops must be connected such that the binary number can be entered (shifted) into the register and possibly shifted out. A group of Flip-Flops connected to provide either or both of these functions is called a ***shift register***.

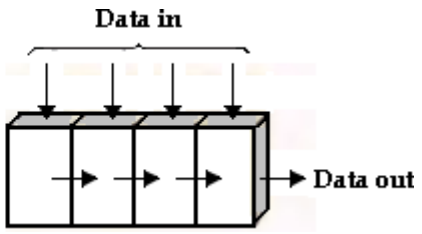
The bits in a binary number (data) can be removed from one place to another in either of two ways. The first method involves shifting the data one bit at a time in a serial fashion, beginning with either the most significant bit (MSB) or the least significant bit (LSB). This technique is referred to as *serial shifting*. The second method involves shifting all the data bits simultaneously and is referred to as *parallel shifting*.

There are two ways to shift into a register (serial or parallel) and similarly two ways to shift the data out of the register. This leads to the construction of four basic register types:

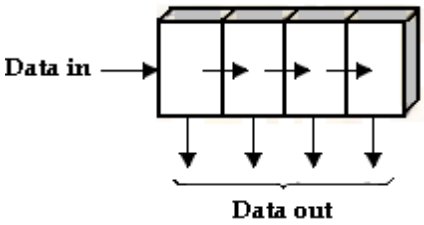
i. **Serial in- serial out,**
ii. **Serial in- parallel out,**
iii. **Parallel in- serial out,**
iv. **Parallel in- parallel out.**



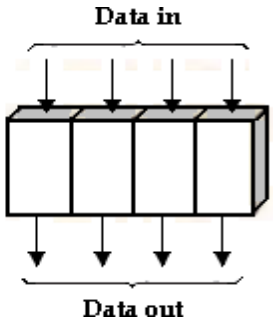
(i) Serial in- serial out



(iii) Parallel in- serial out



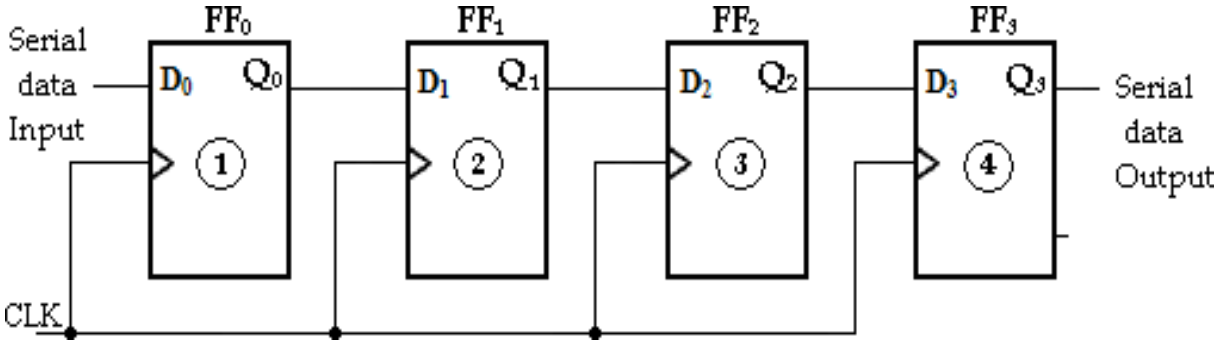
(ii) Serial in- parallel out



(iv) Parallel in- parallel out

(i) Serial-In Serial-Out Shift Register:

The serial in/serial out shift register accepts data serially, i.e., one bit at a time on a single line. It produces the stored information on its output also in serial form.



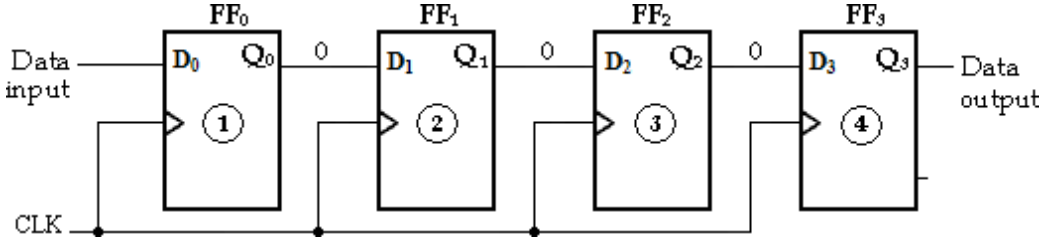
Serial-In Serial-Out Shift Register

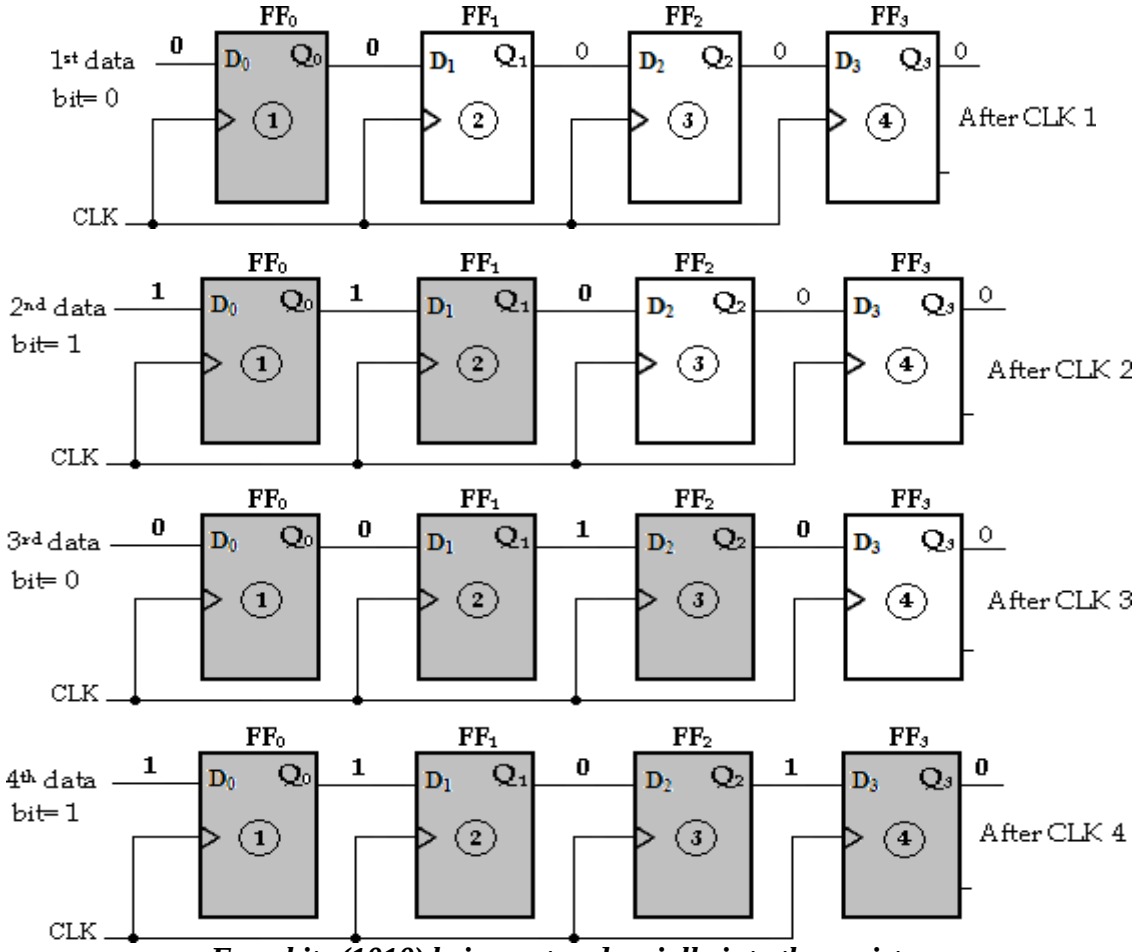
The entry of the four bits **1010** into the register is illustrated below, beginning with the right-most bit. The register is initially clear. The 0 is put onto the data input line, making D=0 for FF0. When the first clock pulse is applied, FF0 is reset, thus storing the 0.

Next the second bit, which is a 1, is applied to the data input, making D=1 for FF0 and D=0 for FF1 because the D input of FF1 is connected to the Q0 output. When the second clock pulse occurs, the 1 on the data input is shifted into FF0, causing FF0 to set; and the 0 that was in FF0 is shifted into FFl.

The third bit, a 0, is now put onto the data-input line, and a clock pulse is applied. The 0 is entered into FF0, the 1 stored in FF0 is shifted into FFl, and the 0 stored in FF1 is shifted into FF2.

The last bit, a 1, is now applied to the data input, and a clock pulse is applied. This time the 1 is entered into FF0, the 0 stored in FF0 is shifted into FFl, the 1 stored in FF1 is shifted into FF2, and the 0 stored in FF2 is shifted into FF3. This completes the serial entry of the four bits into the shift register, where they can be stored for any length of time as long as the Flip-Flops have dc power.

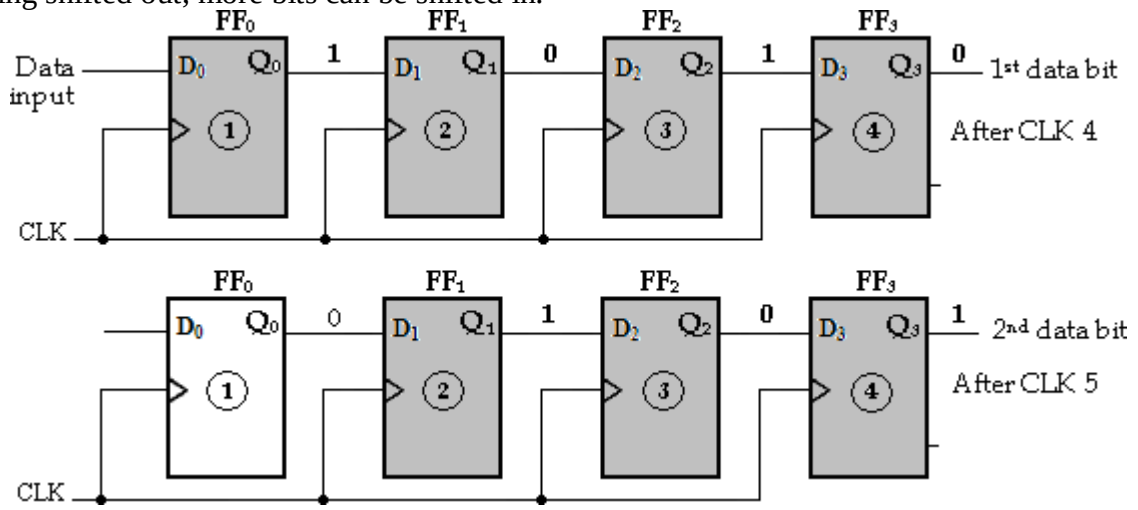


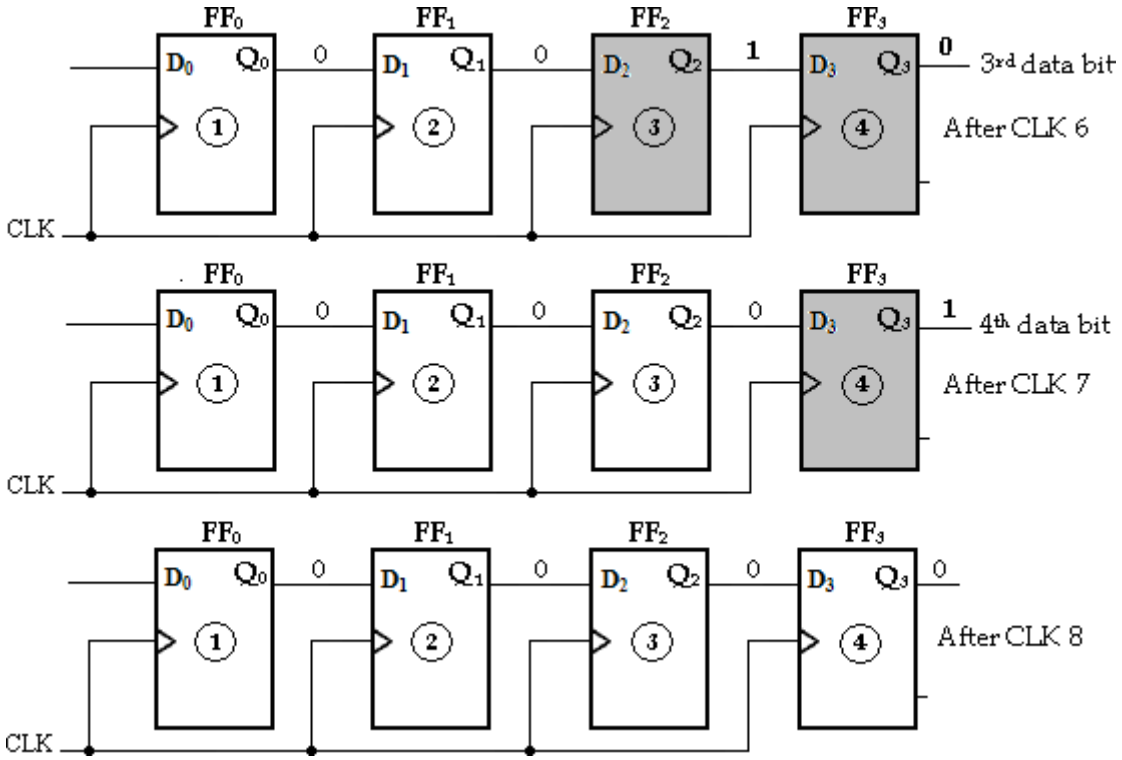


Four bits (1010) being entered serially into the register

To get the data out of the register, the bits must be shifted out serially and taken off the Q3 output. After CLK4, the right-most bit, 0, appears on the Q3 output.

When clock pulse CLK5 is applied, the second bit appears on the Q3 output. Clock pulse CLK6 shifts the third bit to the output, and CLK7 shifts the fourth bit to the output. While the original four bits are being shifted out, more bits can be shifted in. All zeros are shown being shifted out, more bits can be shifted in.

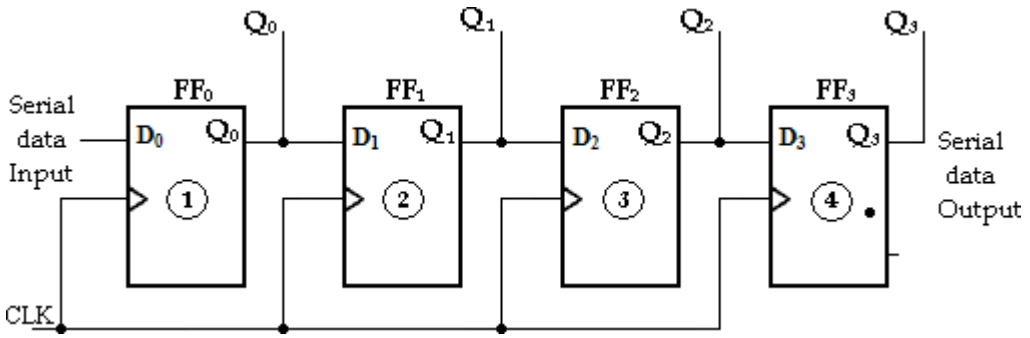




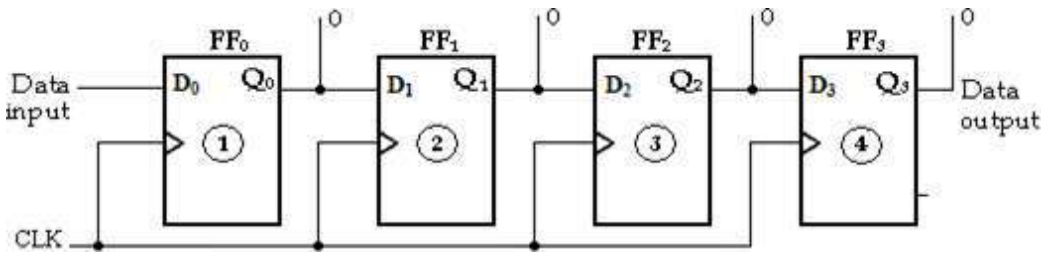
Four bits (1010) being entered serially-shifted out of the register and replaced by all zeros

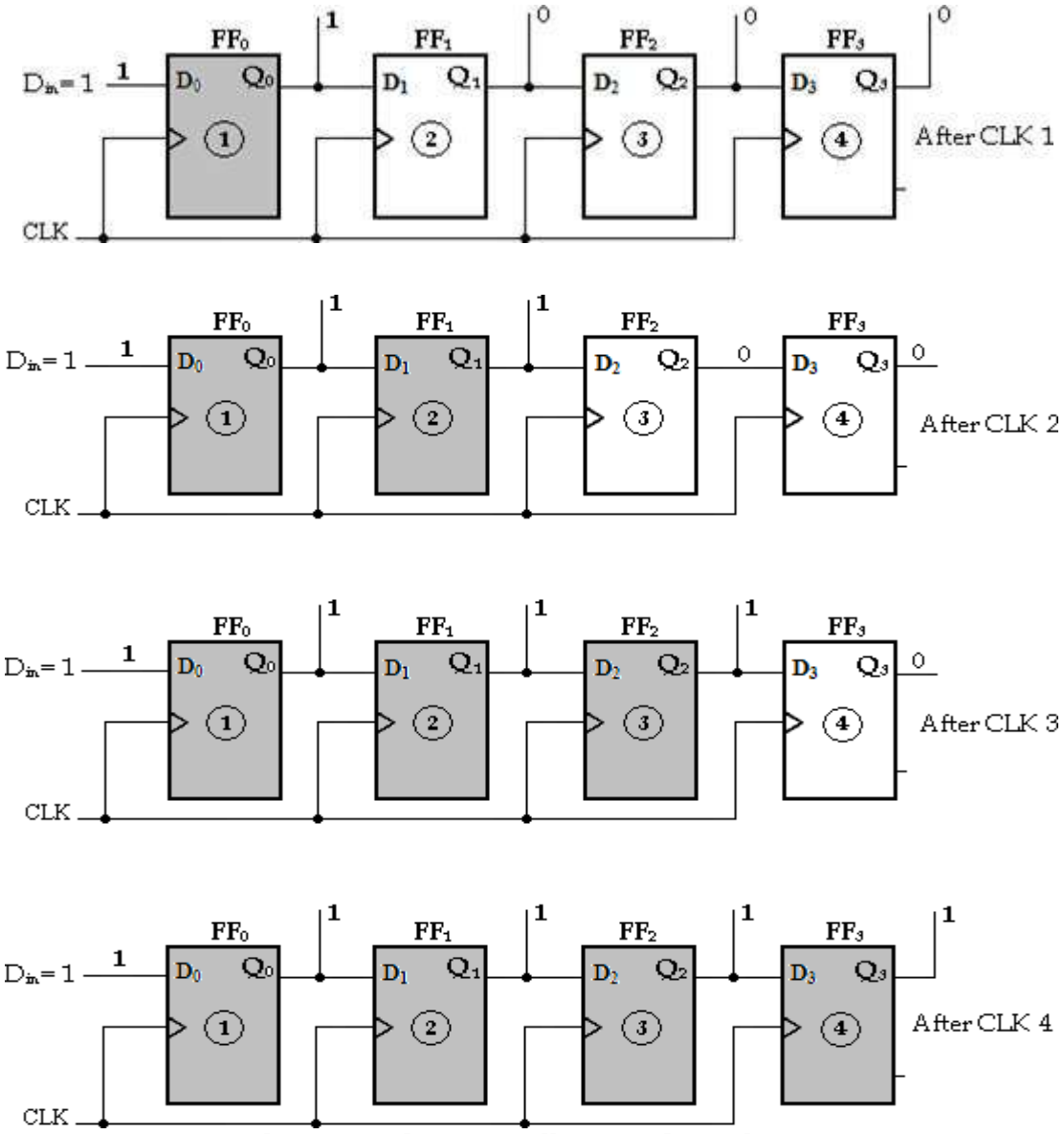
(ii) Serial-In Parallel-Out Shift Register:

In this shift register, data bits are entered into the register in the same as serial- in serial-out shift register. But the output is taken in parallel. Once the data are stored, each bit appears on its respective output line and all bits are available simultaneously instead of on a bit-by-bit.



Serial-In parallel-Out Shift Register



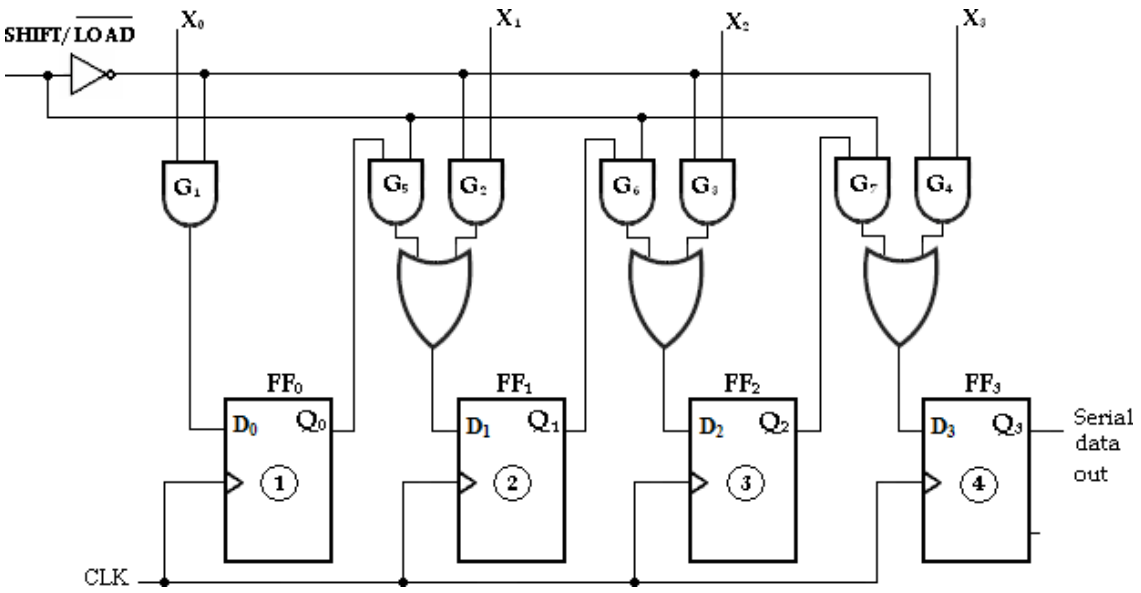


Four bits (1111) being serially entered into the register

(iii) Parallel-In Serial-Out Shift Register:

In this type, the bits are entered in parallel i.e., simultaneously into their respective stages on parallel lines. A 4-bit parallel-in serial-out shift register is illustrated below. There are four data input lines, X0, X1, X2 and X3 for entering data in parallel into the register. SHIFT/ LOAD input is the control input, which allows four bits of data to **load** in parallel into the register.

When SHIFT/LOAD is LOW, gates G1, G2, G3 and G4 are enabled, allowing each data bit to be applied to the D input of its respective Flip-Flop. When a clock pulse is applied, the Flip-Flops with D = 1 will **set** and those with D = 0 will **reset,** thereby storing all four bits simultaneously.

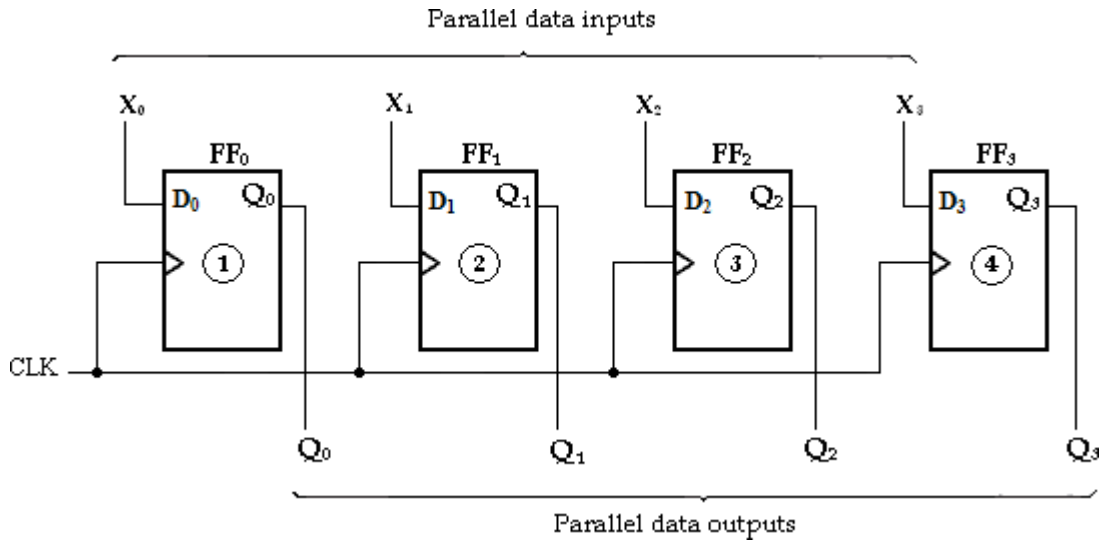


Parallel-In Serial-Out Shift Register

When SHIFT/LOAD is HIGH, gates G1, G2, G3 and G4 are disabled and gates G5, G6 and G7 are enabled, allowing the data bits to shift right from one stage to the next. The OR gates allow either the normal shifting operation or the parallel data- entry operation, depending on which AND gates are enabled by the level on the SHIFT/LOAD input.

(iv) Parallel-In Parallel-Out Shift Register:

In this type, there is simultaneous entry of all data bits and the bits appear on parallel outputs simultaneously.



Parallel-In Parallel-Out Shift Register

UNIVERSAL SHIFT REGISTERS

If the register has shift and parallel load capabilities, then it is called a shift register with parallel load or ***universal shift register***. Shift register can be used for converting serial data to parallel data, and vice-versa. If a parallel load capability is added to a shift register, the data entered in parallel can be taken out in serial fashion by shifting the data stored in the register.

The functions of universal shift register are:

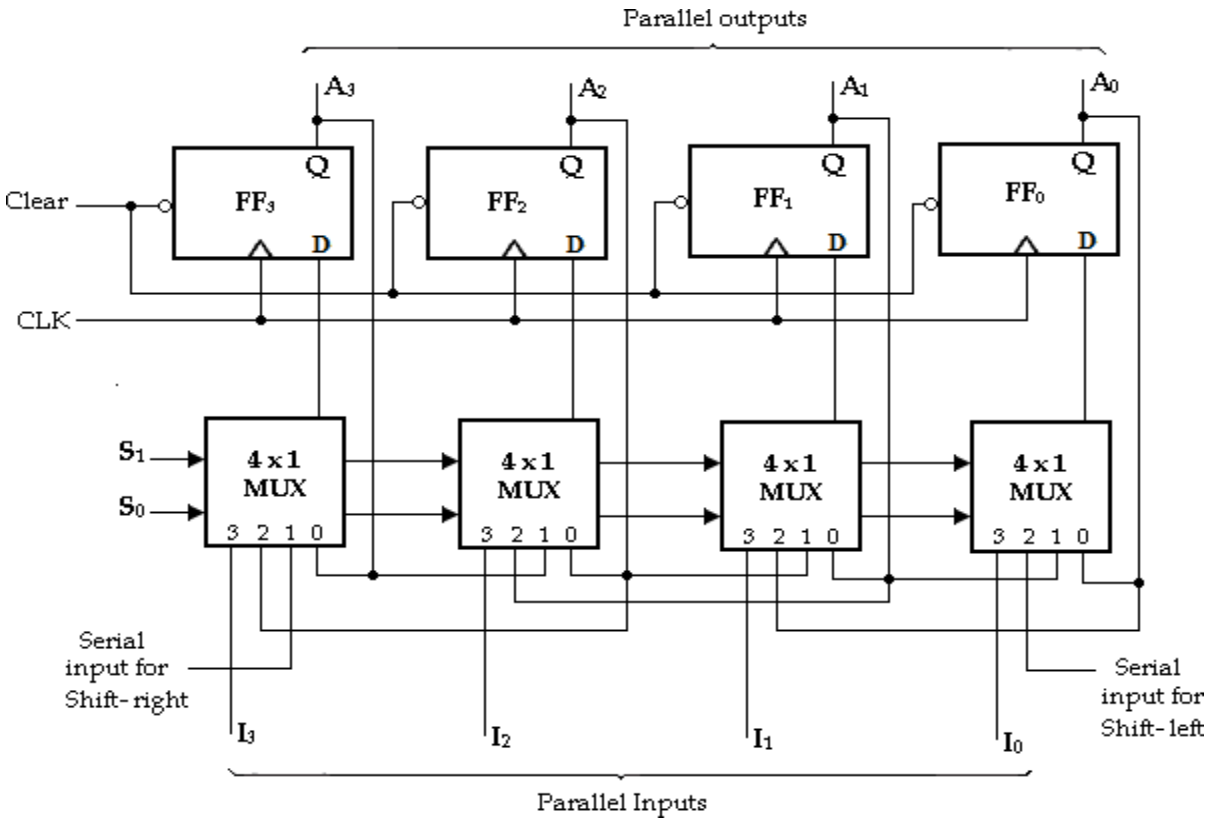
- A clear control to clear the register to 0.

- A clock input to synchronize the operations.
- A shift-right control to enable the shift right operation and the serial input and output lines associated with the shift right.
- A shift-left control to enable the shift left operation and the serial input and output lines associated with the shift left.
- A parallel-load control to enable a parallel transfer and the n input lines associated with the parallel transfer.
- 'n' parallel output lines.
- A control line that leaves the information in the register unchanged even though the clock pulses re continuously applied.

It consists of four D-Flip-Flops and four 4 input multiplexers (MUX). S0 and S1 are the two selection inputs connected to all the four multiplexers. These two selection inputs are used to select one of the four inputs of each multiplexer.

The input 0 in each MUX is selected when S1S0= 00 and input 1 is selected when S1S0= 01. Similarly inputs 2 and 3 are selected when S1S0= 10 and S1S0= 11 respectively. The inputs S1 and S0 control the mode of the operation of the register.

4-Bit Universal Shift Register



When S1S0= 00, the present value of the register is applied to the D-inputs of the Flip-Flops. This is done by connecting the output of each Flip-Flop to the 0 input of the respective multiplexer. The next clock pulse transfers into each Flip-Flop, the binary value is held previously, and hence no change of state occurs.

When S1S0= 01, terminal 1 of the multiplexer inputs has a path to the D inputs of the Flip-Flops. This causes a shift-right operation with the lefter serial input transferred into Flip-Flop FF3.

When S_1S_0= 10, a shift-left operation results with the right serial input going into Flip-Flop FF_1.

Finally when S_1S_0= 11, the binary information on the parallel input lines (I_1, I_2, I_3 and I_4) are transferred into the register simultaneously during the next clock pulse.

The function table of bi-directional shift register with parallel inputs and parallel outputs is shown below.

Mode Control		Operation
S1	**S0**	
0	0	No change
0	1	Shift-right
1	0	Shift-left
1	1	Parallel load

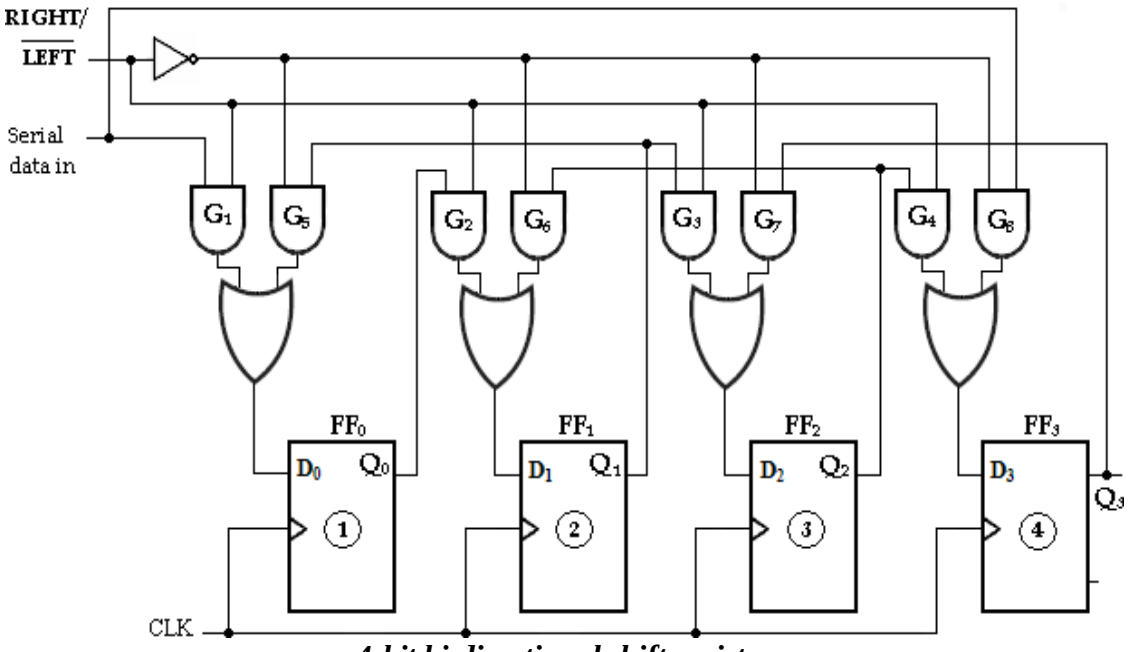
BI-DIRECTION SHIFT REGISTERS

A bidirectional shift register is one in which the data can be shifted either left or right. It can be implemented by using gating logic that enables the transfer of a data bit from one stage to the next stage to the right or to the left depending on the level of a control line.

A 4-bit bidirectional shift register is shown below. A HIGH on the RIGHT/LEFT control input allows data bits inside the register to be shifted to the right, and a LOW enables data bits inside the register to be shifted to the left.

When the RIGHT/LEFT control input is **HIGH**, gates G_1, G_2, G_3 and G_4 are enabled, and the state of the Q output of each Flip-Flop is passed through to the D input of the following Flip-Flop. When a clock pulse occurs, the data bits are shifted one place to the right.

When the RIGHT/LEFT control input is **LOW**, gates G_5, G_6, G_7 and G_8 are enabled, and the Q output of each Flip-Flop is passed through to the D input of the preceding Flip-Flop. When a clock pulse occurs, the data bits are then shifted one place to the left.



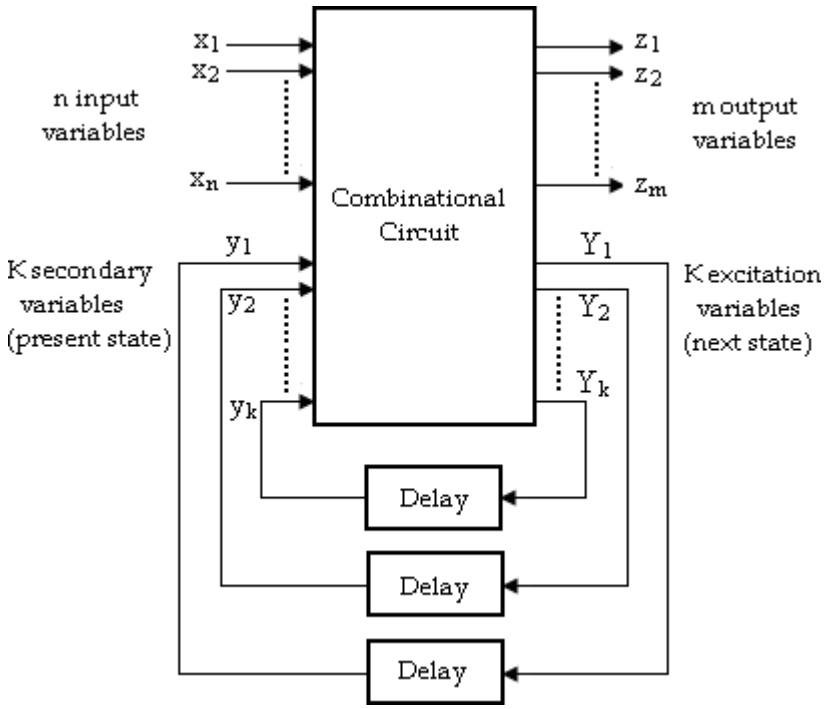
4-bit bi-directional shift register

UNIT – IV ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABLE LOGIC DEVICES

Asynchronous sequential logic circuits-Transition stability, flow stability-race conditions, hazards & errors in digital circuits; analysis of asynchronous sequential logic circuits-Introduction to Programmability Logic Devices: PROM – PLA –PAL, CPLD-FPGA.

ASYNCHRONOUS SEQUENTIAL CIRCUITS

Asynchronous sequential circuits do not use clock pulses. The memory elements in asynchronous sequential circuits are either unclocked flip-flops (Latches) or time-delay elements.



Block diagram of Asynchronous sequential circuits

The block diagram of asynchronous sequential circuit is shown above. It consists of a combinational circuit and delay elements connected to form feedback loops. There are 'n' input variables, 'm' output variables, and 'k' internal states.

The delay elements provide short term memory for the sequential circuit. The present-state and next-state variables in asynchronous sequential circuits are called secondary variables and excitation variables, respectively.

When an input variable changes in value, the 'y' secondary variable does not change instantaneously. It takes a certain amount of time for the signal to propagate from the input terminals through the combinational circuit to the 'Y' excitation variables where the new values are generated for the next state. These values propagate through the delay elements and become the new present state for the secondary variables.

In steady-state condition, excitation and secondary variables are same, but during transition they are different. To ensure proper operation, it is necessary for asynchronous sequential circuits to attain a stable state before the input is changed to a new value. Because of unequal delays in wires and combinational circuits, it is impossible to have two or more input variable change at exactly same instant.

Therefore, simultaneous changes of two or more input variables are avoided. Only one input variable is allowed to change at any one time and the time between input changes is

kept longer than the time it takes the circuit to reach stable state.

Types:

According to how input variables are to be considered, there are two types;

- Fundamental mode circuit
- Pulse mode circuit.

Fundamental mode circuit assumes that:

- The input variables change only when the circuit is stable. Only one.
- Input variable can change at a given time.
- Inputs are levels (0, 1) and not pulses.

Pulse mode circuit assumes that:

- The input variables are pulses (True, False) instead of levels.
- The width of the pulses is long enough for the circuit to respond to the input.
- The pulse width must not be so long that it is still present after the new state is reached.

Analysis of Fundamental Mode Circuits

The analysis of asynchronous sequential circuits consists of obtaining a table or a diagram that describes the sequence of internal states and outputs as a function of changes in the input variables.

Analysis procedure

The procedure for obtaining a transition table from the given circuit diagram is as follows.

1. Determine all feedback loops in the circuit.
2. Designate the output of each feedback loop with variable Y1 and its corresponding inputs $y_1, y_2, \ldots y_k$, where k is the number of feedback loops in the circuit.
3. Derive the Boolean functions of all Y's as a function of the external inputs and the y's.
4. Plot each Y function in a map, using y variables for the rows and the external inputs for the columns.
5. Combine all the maps into one table showing the value of $Y= Y_1, Y_2, \ldots Y_k$ inside each square.
6. Circle all stable states where Y=y. The resulting map is the transition table.

<u>Solved Example Problems</u>

1. An asynchronous sequential circuit is described by the following excitation and output function,

$$Y= x_1x_2+ (x_1+x_2) y$$

$$Z= Y$$

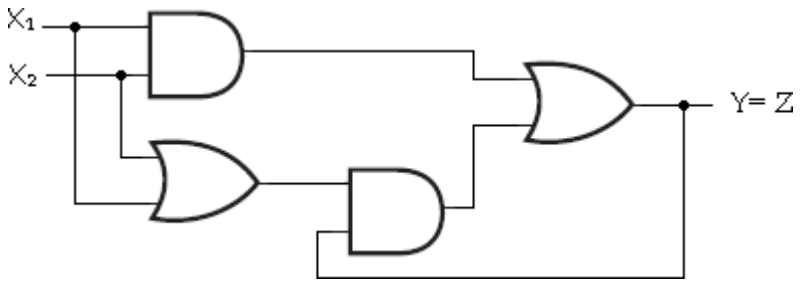
a) Draw the logic diagram of the circuit.

b) Derive the transition table, flow table and output map.

c) Describe the behavior of the circuit.

Soln:

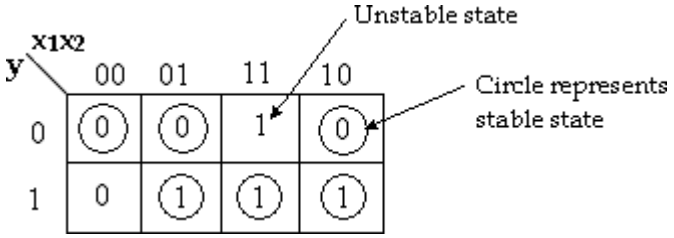
i) The logic diagram is shown as,



Logic diagram

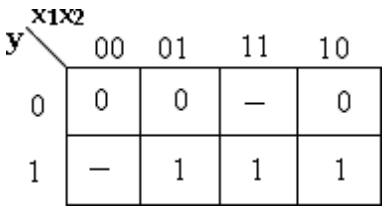
ii) Transition Table

y	x1	x2	x1x2	(x1+x2)y	Y= x1x2+ (x1+x2)y	Z= Y
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	1	0	1	1	1
1	1	0	0	1	1	1
1	1	1	1	1	1	1



Output map:

Output is mapped for all stable states. For unstable states output is mapped unspecified.



Flow table:

Assign a= 0; b= 1

y \ x1x2	00	01	11	10
0	(a)	(a)	b	(a)
1	a	(b)	(b)	(b)

iii) The circuit gives carry output of the full adder circuit.

2. Design an asynchronous sequential circuit that has two internal states and one output. The excitation and output function describing the circuit are as follows:

Y1= x1x2+ x1y2+ x2y1

Y2= x2+ x1y1y2+ x1y1

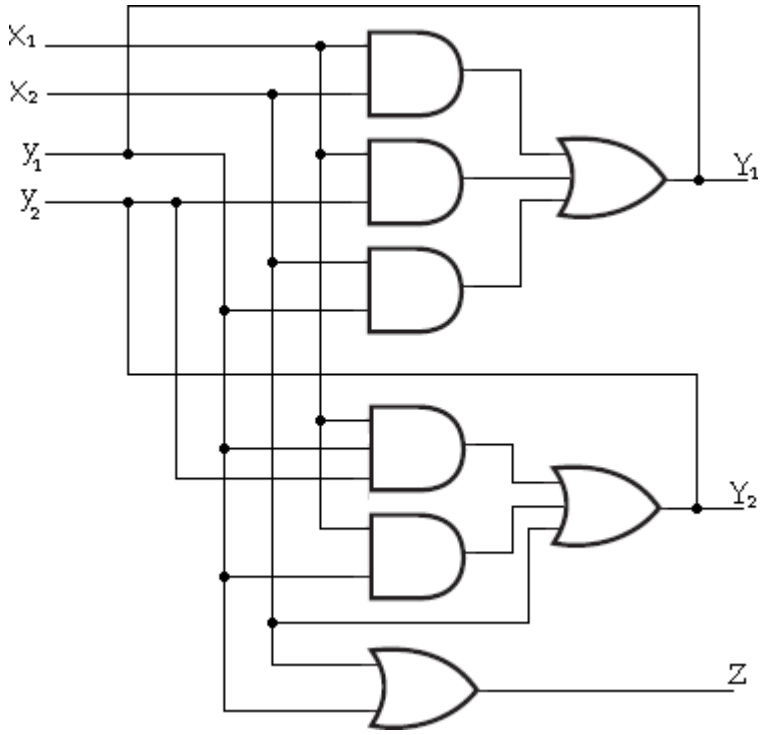
Z= x2+ y1.

a) Draw the logic diagram of the circuit.

b) Derive the transition table, output map and flow table.

Soln:

i) The logic diagram is shown as,



Logic Diagram

ii) **Transition table and Output map**

y_1	y_2	x_1	x_2	x_1x_2	x_1y_2	x_2y_1	$x_1y_1y_2$	x_1y_1	Y_1	Y_2	$Z= x_2+ y_1$
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	1	1
0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	1	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	1	0	0	1	1	1
1	0	1	0	0	0	0	0	1	0	1	1
1	1	0	0	0	0	0	0	0	0	0	1
1	1	0	1	0	0	1	0	0	1	1	1
1	1	1	0	0	1	0	1	1	1	1	1

Map for Y_1

y_1y_2 \ x_1x_2	00	01	11	10
00	0	0	1	0
01	0	0	1	1
11	0	1	1	1
10	0	1	1	0

Map for Y_2

y_1y_2 \ x_1x_2	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	0	1	1	1
10	0	1	1	1

Map for Y_1Y_2

y_1y_2 \ x_1x_2	00	01	11	10
00	(00)	01	11	(00)
01	00	(01)	11	10
11	00	(11)	(11)	(11)
10	00	11	11	01

Transition table

y_1y_2 \ x_1x_2	00	01	11	10
00	0	–	–	0
01	–	1	–	–
11	–	1	1	1
10	–	–	–	–

Output map

Primitive Flow table

y_1y_2 \ x_1x_2	00	01	11	10
a	(a)	b	c	(a)
b	a	(b)	c	d
c	a	(c)	(c)	(c)
d	a	c	c	b

3. An asynchronous sequential circuit is described by the excitation and output functions,

Y= x1x2'+ (x1+x2') y

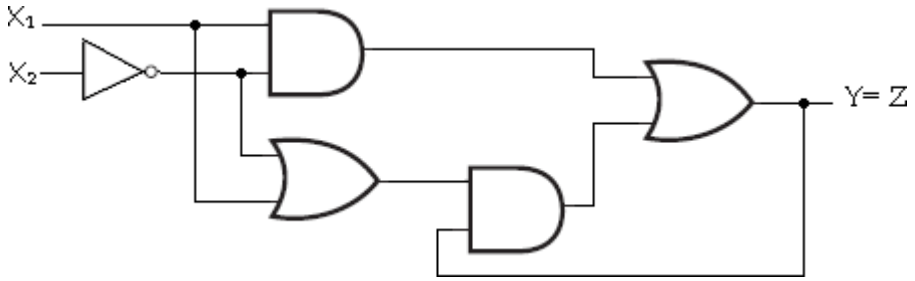
Z= Y

a) Draw the logic diagram of the circuit.

b) Derive the transition table, output map and flow table.

Soln:

i) Logic diagram



ii) Transition table, output map and flow table

y	x1	x2	x2'	x1x2'	(x1+x2')y	Y= x1x2'+ (x1+x2')y	Z= Y
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	1	0	1	1	0	1	1
0	1	1	0	0	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	0	0	0
1	1	0	1	1	1	1	1
1	1	1	0	0	1	1	1

Transition table:

y \ x1x2	00	01	11	10
0	(0)	(0)	(0)	1
1	(1)	0	(1)	(1)

Output map:

Output is mapped for all stable states. For unstable states output is mapped unspecified.

y \ x1x2	00	01	11	10
0	0	0	0	–
1	1	–	1	1

Flow table:

Assign a= 0; b= 1

y \ x1x2	00	01	11	10
0	(a)	(a)	(a)	b
1	(b)	a	(b)	(b)

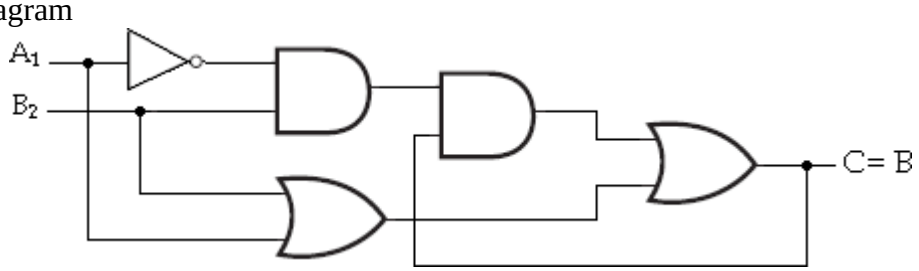
4. An asynchronous sequential circuit is described by the excitation and output functions, B= (A1'B2) b+ (A1+B2) C= B

a) Draw the logic diagram of the circuit.

b) Derive the transition table, output map and flow table.

Soln:

i) Logic diagram



ii) The transition table, output map and flow table

b	A_1	B_2	A_1'	$(A_1'B_2)b$	A_1+B_2	$B= (A_1'B_2)\ b+ (A_1+B_2)$	C= B
0	0	0	1	0	0	0	0
0	0	1	1	0	1	1	1
0	1	0	0	0	1	1	1
0	1	1	0	0	1	1	1
1	0	0	1	0	0	0	0
1	0	1	1	1	1	1	1
1	1	0	0	0	1	1	1
1	1	1	0	0	1	1	1

Transition table

b \ A_1B_2	00	01	11	10
0	(0)	1	1	1
1	0	(1)	(1)	(1)

Output map

Output is mapped for all stable states.

b \ A_1B_2	00	01	11	10
0	0	–	–	–
1	–	1	1	1

Flow table

Assign a= 0; b= 1

b \ A_1B_2	00	01	11	10
0	(a)	b	b	b
1	a	(b)	(b)	(b)

5. An asynchronous sequential circuit is described by the excitation and output functions,

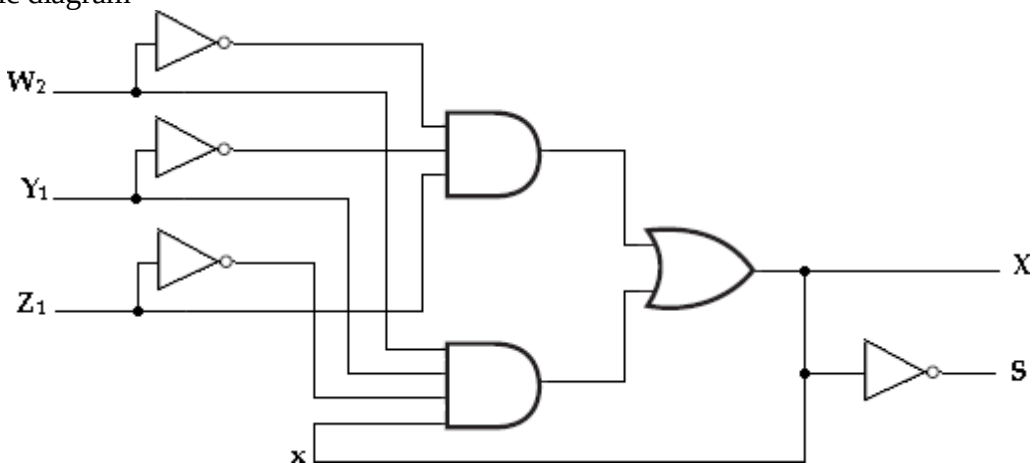
X= (Y1Z1'W2) x + (Y1'Z1W2') S=X'

a) Draw the logic diagram of the circuit

b) Derive the translation table and output map.

Soln:

i) Logic diagram



ii) The transition table, output map and flow table

x	W2	W2'	Y1	Y1'	Z1	Z1'	(Y1Z1' W2)x	Y1'Z1 W2'	X	S=X'
0	0	1	0	1	0	1	0	0	0	1
0	0	1	0	1	1	0	0	1	1	0
0	0	1	1	0	0	1	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1
0	1	0	0	1	0	1	0	0	0	1
0	1	0	0	1	1	0	0	0	0	1
0	1	0	1	0	0	1	0	0	0	1
0	1	0	1	0	1	0	0	0	0	1

1	0	1	0	1	0	1	0	0	0	1
1	0	1	0	1	1	0	0	1	1	0
1	0	1	1	0	0	1	0	0	0	1
1	0	1	1	0	1	0	0	0	0	1
1	1	0	0	1	0	1	0	0	0	1
1	1	0	0	1	1	0	0	0	0	1
1	1	0	1	0	0	1	1	0	1	0

Map for X

xW_2 \ Y_1Z_1	00	01	11	10
00	0	1	0	0
01	0	0	0	0
11	0	0	0	1
10	0	1	0	0

Map for S

xW_2 \ Y_1Z_1	00	01	11	10
00	1	0	1	1
01	1	1	1	1
11	1	1	1	0
10	1	0	1	1

Transition table and Output map:

Map for XS

xW_2 \ Y_1Z_1	00	01	11	10
00	01	10	01	01
01	(01)	(01)	(01)	(01)
11	01	01	01	10
10	01	(10)	01	01

xW_2 \ Y_1Z_1	00	01	11	10
00	–	–	–	–
01	1	1	1	1
11	–	–	–	–
10	–	0	–	–

ANALYSIS OF PULSE MODE CIRCUITS

Pulse mode asynchronous sequential circuits rely on the input pulses rather than levels. They allow only one input variable to change at a time. They can be implemented by employing a SR latch.

The procedure for analyzing an asynchronous sequential circuit with SR latches can be summarized as follows:

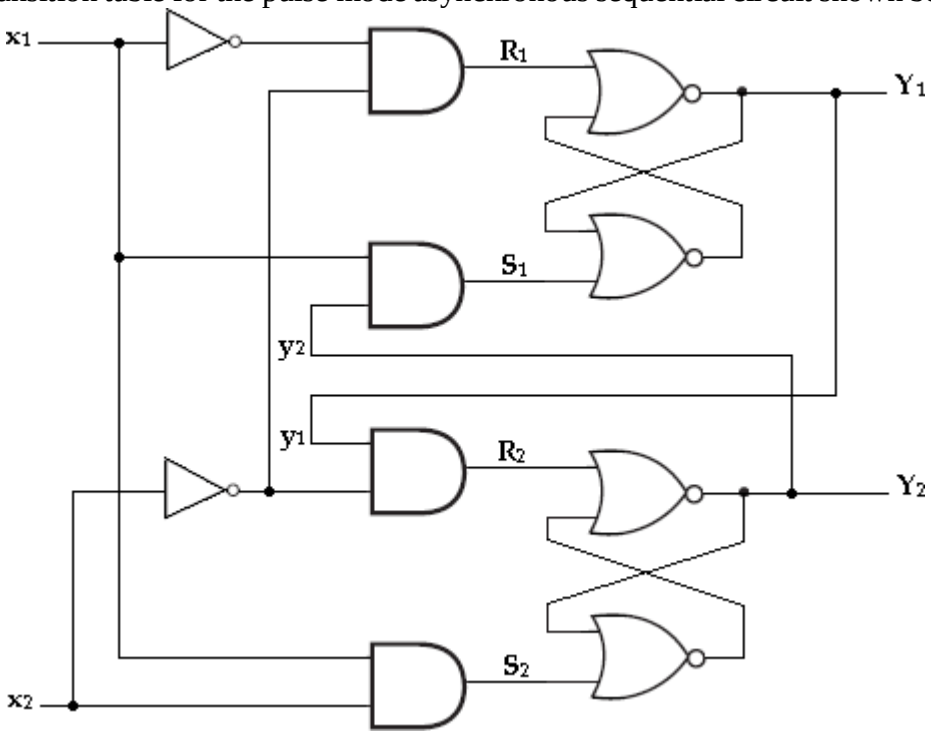
1. Label each latch output with Y_i and its external feedback path (if any) with y_i for $i = 1,2,...,k$.
2. Derive the Boolean functions for the S_i and R_i inputs in each latch.
3. Check whether $\boldsymbol{SR = 0}$ for each NOR latch or whether $\mathbf{S'R' = 0}$ for each NAND latch. If either of these condition is not satisfied, there is a possibility that the circuit may not operate properly.
4. Evaluate $\mathbf{Y = S + R'y}$ for each NOR latch or $\mathbf{Y = S' + Ry}$ for each NAND latch.

5. Construct a map with the y's representing the rows and the x inputs representing the columns.
6. Plot the value of Y= Y1Y2 ……Yk in the map.
7. Circle all stable states such that ***Y* = y**. The resulting map is the transition table.

The analysis of a circuit with latches will be demonstrated by means of the below example.

Example of a circuit with SR latches

1. Derive the transition table for the pulse mode asynchronous sequential circuit shown below.



Circuit with SR latches

Soln:

There are two inputs x1 and x2 and two external feedback loops giving rise to the secondary variables y1 and y2.

Step 1: The Boolean functions for the S and R inputs in each latch are:

S1= x1y2 **S2= x1x2**

R1= x1'x2' **R2= x2'y1**

Step 2: Check whether the conditions SR= 0 is satisfied to ensure proper operation of the circuit.

S1R1= x1y2 x1'x2' = 0

S2R2= x1x2 x2'y1 = 0

The result is 0 because x1x1' = x2x2' = 0

Step 3: Evaluate Y1 and Y2. The excitation functions are derived from the relation **Y= S+ R'y.**

Y1= S1+ R1'y1 = x1y2 +(x1'x2')' y1

= x1y2 +(x1+ x2) y1 = x1y2 +x1y1+ x2y1

Y2= S2+ R2'y2 = x1x2+ (x2'y1)'y2

= x1x2+ (x2+ y1') y2 = x1x2+ x2y2+ y1'y2

y_1	y_2	x_1	x_2	x_1y_2	x_1y_1	x_2y_1	x_1x_2	x_2y_2	$y_1'y_2$	Y_1	Y_2
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	1
0	1	0	0	0	0	0	0	0	1	0	1
0	1	0	1	0	0	0	0	1	1	0	1
0	1	1	0	1	0	0	0	0	1	1	1
0	1	1	1	1	0	0	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0	0	0	1	0
1	0	1	0	0	1	0	0	0	0	1	0
1	0	1	1	0	1	1	1	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	1	0	1	0	1	1
1	1	1	0	1	1	0	0	0	0	1	0
1	1	1	1	1	1	1	1	1	0	1	1

Step 4: Maps for Y1 and Y2.

Map for Y_1

y_1y_2 \ x_1x_2	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	1	1	1
10	0	1	1	1

Map for Y_2

y_1y_2 \ x_1x_2	00	01	11	10
00	0	0	1	0
01	1	1	1	1
11	0	1	1	0
10	0	0	1	0

Step 5: Transition table

Map for Y_1Y_2

y_1y_2 \ x_1x_2	00	01	11	10
00	(00)	(00)	01	(00)
01	(01)	(01)	11	11
11	00	(11)	(11)	10
10	00	(10)	11	(10)

RACES

A race condition is said to exist in an asynchronous sequential circuit when two or more binary state variables change value in response to a change in an input variable.

Races are classified as:

i. Non-critical races ii. Critical races.

Non-critical races:

If the final stable state that the circuit reaches does not depend on the order in which the state variables change, the race is called a non-critical race.

If a circuit, whose transition table (a) starts with the total stable state y1y2x= *000* and then change the input from 0 to 1. The state variables must then change from 00 to 11, which define a race condition.

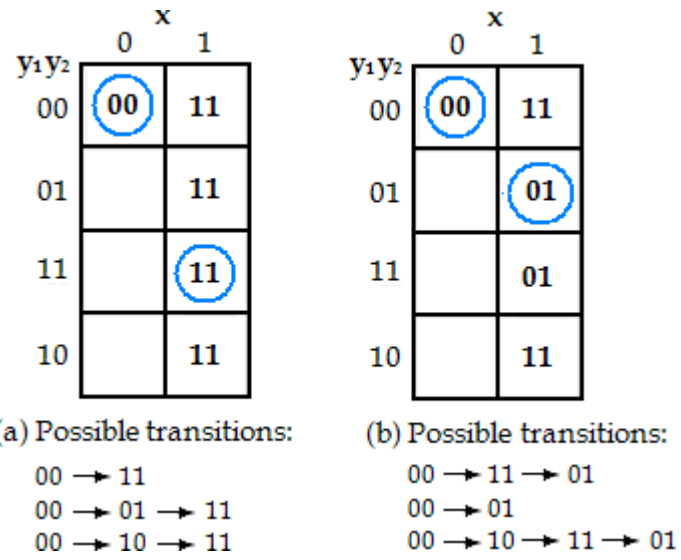
The possible transitions are:

00 → 11

00 → 01 → 11

00 → 10 → 11

In all cases, the final state is the same, which results in a non-critical condition. In (a), the final state is (y1y2x= 111), and in (b), it is (y1y2x= 011).



Examples of Non-critical Races

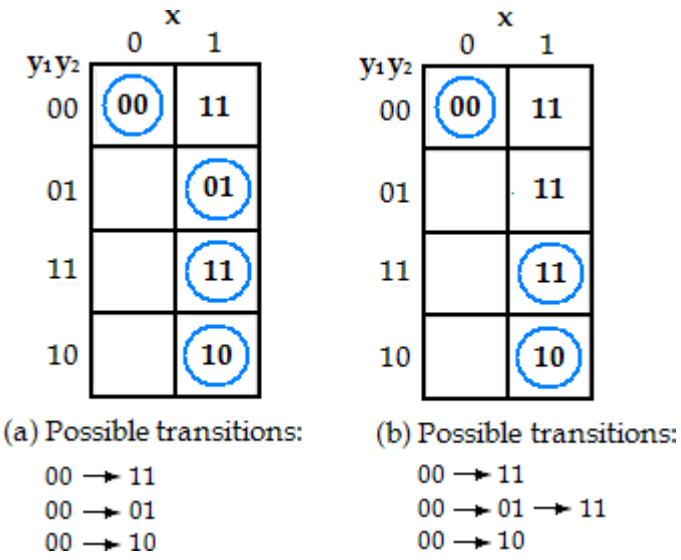
Critical races:

A race becomes critical if the correct next state is not reached during a state transition. If it is possible to end up in two or more different stable states, depending on the order in which the state variables change, then it is a critical race. For proper operation, critical races must be avoided.

The below transition table illustrates critical race condition. The transition table (a) starts in stable state (y1y2x= 000), and then change the input from 0 to 1. The state variables must then change from 00 to 11. If they change simultaneously, the final total stable state is 111. In the transition table (a), if, because of unequal propagation delay, Y2 changes to 1 before Y1 does, then the circuit goes to the total stable state 011 and remains there. If, however, *Y1* changes first, the internal state becomes 10 and the circuit will remain in the stable total state 101.

Hence, the race is critical because the circuit goes to different stable states, depending

on the order in which the state variables change.

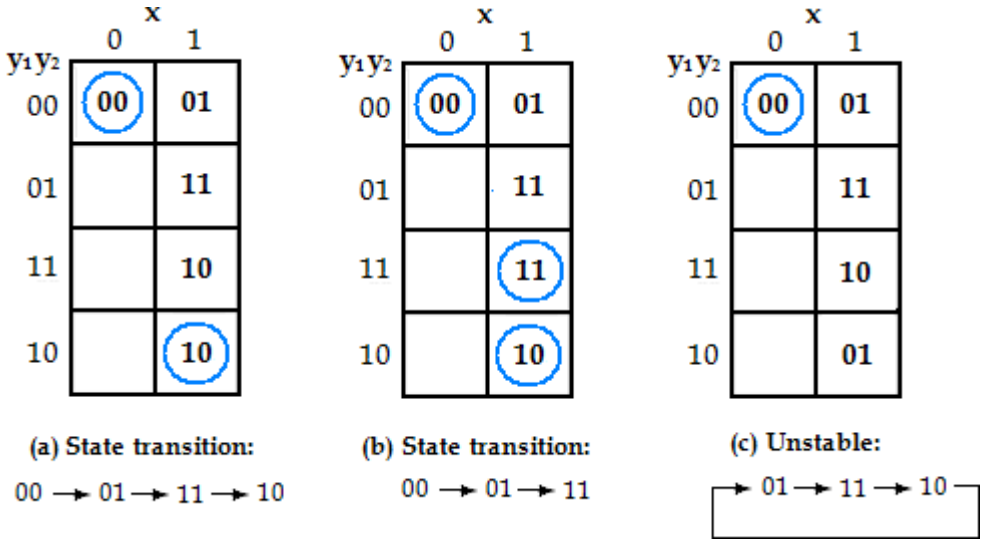


Examples of Critical Races

CYCLES

Races can be avoided by directing the circuit through intermediate unstable states with a unique state-variable change. When a circuit goes through a unique sequence of unstable states, it is said to have a ***cycle***.

Again, we start with $y_1y_2 = 00$ and change the input from *0* to 1. The transition table (a) gives a *unique* sequence that terminates in a total stable state 101. The table in (b) shows that even though the state variables change from 00 to 11, the cycle provides a unique transition from *00* to 01 and then to 11, Care must be taken when using a cycle that terminates with a stable state. If a cycle does not terminate with a stable state, the circuit will keep going from one unstable state to another, making the entire circuit unstable. This is demonstrated in the transition table (c).



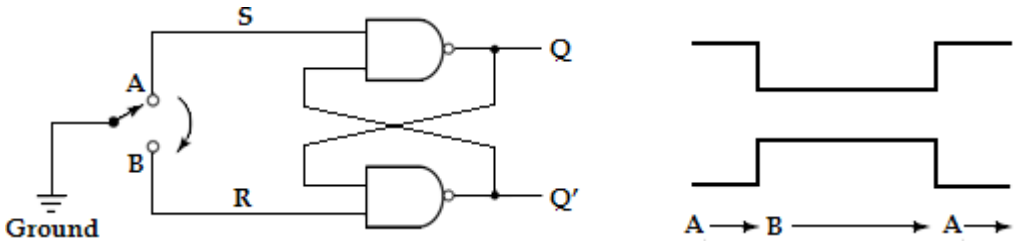
Examples of Cycles

Debounce Circuit:

Input binary information in binary information can be generated manually be means of mechanical switches. One position of the switch provides a voltage equivalent to logic 1,

and the other position provides a second voltage equivalent to logic 0. Mechanical switches are also used to start, stop, or reset the digital system. A common characteristic of a mechanical switch is that when the arm is thrown from one position to the other the switch contact vibrates or bounces several times before coming to a final rest. In a typical switch, the contact bounce may take several milliseconds to die out, causing the signal to oscillate between 1 and 0 because the switch contact is vibrating.

A debounce circuit is a circuit which removes the series of pulses that result from a contact bounce and produces a single smooth transition of the binary signal from *0* to 1 or from 1 to 0. One such circuit consists of a single-pole, double-throw switch connected to an *SR* latch, as shown below. The center contact is connected to ground that provides a signal equivalent to logic 0. When one of the two contacts, A or *B*, is not connected to ground through the switch, it behaves like a logic-1 signal. When the switch is thrown from position *A* to position *B* and back, the outputs of the latch produce a single pulse as shown, negative for *Q* and positive for *Q'*. The switch is usually a push button whose contact rests in position A. When the pushbutton is depressed, it goes to position B and when released, it returns to position A.



Debounce Circuit

The operation of the debounce circuit is as follows: When the switch resets in position A, we have the condition S = 0, *R* = 1 and *Q* = 1, *Q'* = 0. When the switch is moved to position *B*, the ground connection causes R to go to *0*, while *S* becomes a 1 because contact A is open. This condition in turn causes output Q to go to 0 and Q' to go to 1. After the switch makes an initial contact with *B*, it bounces several times. The output of the latch will be unaffected by the contact bounce because Q' remains 1 (and Q remains *0)* whether *R* is equal to *0* (*contact with ground*) or equal to 1 (*no contact with ground*). When the switch returns to position A, *S* becomes *0* and *Q* returns to 1. The output again will exhibit a smooth transition, even if there is a contact bounce in position A.

DESIGN OF FUNDAMENTAL MODE SEQUENTIAL CIRCUITS

The design of an asynchronous sequential circuit starts from the statement of the problem and concludes in a logic diagram. There are a number of design steps that must be carried out in order to minimize the circuit complexity and to produce a stable circuit without critical races.

The design steps are as follows:

1. State the design specifications.
2. Obtain a primitive flow table from the given design specifications.
3. Reduce the flow table by merging rows in the primitive flow table.
4. Assign binary state variables to each row of the reduced flow table to obtain the transition table. The procedure of state assignment eliminates any possible critical races.
5. Assign output values to the dashes associated with the unstable states to obtain the output maps.
6. Simplify the Boolean functions of the excitation and output variables and draw the logic diagram.

Example Problems:

1. Design a gated latch circuit with inputs, G (gate) and D (data), and one output, Q. Binary information present at the D input is transferred to the Q output when G is equal to 1. The Q output will follow the D input as long as G= 1. When G goes to 0, the information that was present at the D input at the time of transition occurred is retained at the Q output. The gated latch is a memory element that accepts the value of D when G= 1 and retains this value after G goes to 0, a change in D does not change the value of the output Q.

Soln:

Step 1: From the design specifications, we know that Q= 0 if DG= 01 and Q= 1 if DG= 11 because D must be equal to Q when G= 1. When G goes to 0, the output depends on the last value of D. Thus, if the transition is from 01 to 00 to 10, then Q must remain 0 because D is 0 at the time of the transition from 1 to 0 in G.

If the transition of DG is from 11 to 10 to 00, then Q must remain 1. This information results in six different total states, as shown in the table.

State	Inputs		Output	Comments
	D	G	Q	
a	0	1	0	D= Q because G= 1
b	1	1	1	D= Q because G= 1
c	0	0	0	After state a or d
d	1	0	0	After state c
e	1	0	1	After state b or f
f	0	0	1	After state e

Step 2: A primitive flow is a flow table with only one stable total state in each row. It has one row for each state and one column for each input combination.

	DG 00	01	11	10
a	c, –	(a), 0	b, –	–, –
b	–, –	a, –	(b), 1	e, –
c	(c), 0	a, –	–, –	d, –
d	c, –	–, –	b, –	(d), 0
e	f, –	–, –	b, –	(e), 1
f	(f), 1	a, –	–, –	e, –

Primitive flow table

Step 3: The primitive flow table has only stable state in each row. The table can be reduced to a smaller number of rows if two or more stable states are placed in the same row of the flow table. The grouping of stable states from separate rows into one common row is called ***merging***.

DG

	00	01	11	10
a	c, –	(a), 0	b, –	–, –
c	(c), 0	a, –	–, –	d, –
d	c, –	–, –	b, –	(d), 0

DG

	00	01	11	10
b	–, –	a, –	(b), 1	e, –
e	f, –	–, –	b, –	(e), 1
f	(f), 1	a, –	–, –	e, –

States that are candidates for merging

Thus, the three rows a, c, and d can be merged into one row. The second row of the reduced table results from the merging of rows b, e, and f of the primitive flow table.

Reduced table- 1

DG

	00	01	11	10
a, c, d	(c), 0	(a), 0	b, –	(d), 0
b, e, f	(f), 1	a, –	(b), 1	(e), 1

The states c & d are replaced by state a, and states e & f are replaced by state b

Reduced table- 2

DG

	00	01	11	10
a	(a), 0	(a), 0	b, –	(a), 0
b	(b), 1	a, –	(b), 1	(b), 1

Step 4: Assign distinct binary value to each state. This assignment converts the flow table into a transition table. A binary state assignment must be made to ensure that the circuit will be free of critical races.

Assign 0 to state a, and 1 to state b in the reduced state table.

DG

y \	00	01	11	10
0	0	0	1	0
1	1	0	1	1

$Y = DG + \overline{G}y$

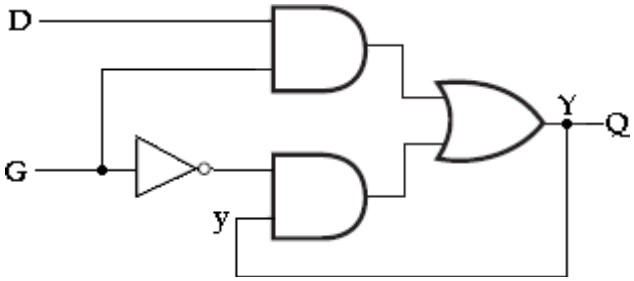
DG

y \	00	01	11	10
0	0	0	1	0
1	1	0	1	1

$Q = Y$

Transition table and output map

Step 5:



Gated-Latch Logic diagram

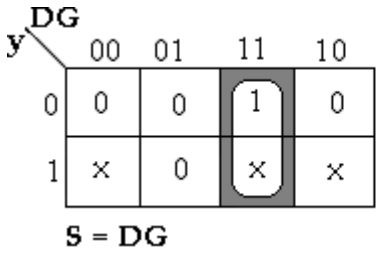
The diagram can be implemented also by means of an SR latch. Obtain the Boolean function for S and R inputs.

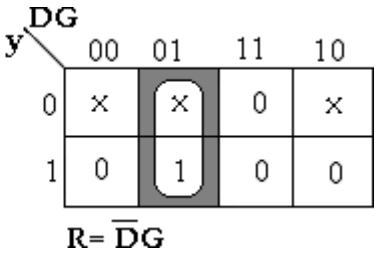
SR Latch excitation table

y	Y	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

From the information given in the transition table and from the latch excitation table conditions, we can obtain the maps for the S and R inputs of the latch.

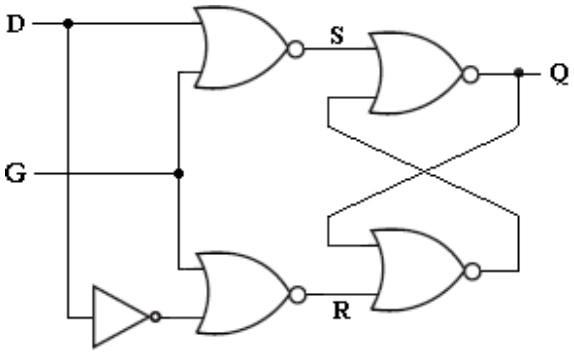
Maps for S and R



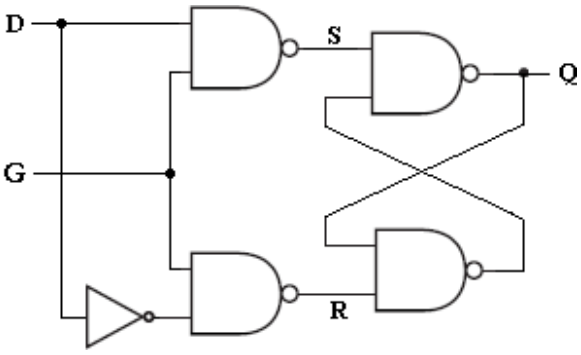


The logic diagram consists of an SR latch using NOR latch and the gates required to implement the S and R Boolean functions. With a NAND latch, we must use the complemented values for S and R.

S' = (DG)' and **R' = (D'G)'**



Logic diagram with NOR latch



Logic diagram with NAND latch

2. Design a negative-edge triggered T flip-flop. The circuit has two inputs, T (toggle) and G (clock), and one output, Q. the output state is complemented if T= 1 and the clock changes from 1 to 0 (negative-edge triggering). Otherwise, under any other input condition, the output Q remains unchanged.

Step 1: Starting with the input condition TC= 11 and assign it to a. The circuit goes to state b and output Q complements from 0 to 1 when C changes from 1 to 0 while T remains a 1. Another change in the output occurs when the circuit changes from state c to state d. In this case, T=1, C changes from 1 to 0, and the output Q complements from 1 to 0. The other four states in the table do not change the output, because T is equal to 0. If Q is initially 0, it stays at 0, and if initially at 1, it stays at 1 even though the clock input changes.

State	Inputs		Output	Com
	T	G	Q	
a	1	1	0	Initial output is 0
b	1	0	1	After state a
c	1	1	1	Initial output is 1
d	1	0	0	After state c
e	0	0	0	After state d or f
f	0	1	0	After state e or a
g	0	0	1	After state b or h
h	0	1	1	After state g or c

Specifications of total states

Step 2: Merging of the flow table

The information for the primitive flow table can be obtained directly from the condition listed in the above table. We first fill in one square in each row belonging to stable state in that row as listed in the table.

Then we enter dashes in those squares whose input differs by two variables from the input corresponding to the stable state. The unstable conditions are then determined by utilizing the information listed under the comments in the above table.

Step 3: Compatible pairs

	TC 00	01	11	10
a	–, –	f, –	(a), 0	b, –
b	g, –	–, –	c, –	(b), 1
c	–, –	h, –	(c), 1	d, –
d	e, –	–, –	a, –	(d), 0
e	(e), 0	f, –	–, –	d, –
f	e, –	(f), 0	a, –	–, –
g	(g), 1	h, –	–, –	b, –
h	g, –	(h), 1	c, –	–, –

Primitive flow table

The rows in the primitive flow table are merged by first obtaining all compatible pairs of states. This is done by means of the implication table.

	a	b	c	d	e	f	g
b	a,c x						
c	X	b,d x					
d	b,d x	X	a,c x				
e	b,d x	e,g x b,d x	f,h x	✓			
f	✓	e,g x a,c x	f,h x a,c x	✓	✓		
g	f,h x	✓	b,d x	e,g x b,d x	X	e,g x f,h x	
h	f,h x a,c x	✓	✓	d,e x c,f x	e,g x f,h x	X	✓

Implication table

The implication table is used to find the compatible states. The only difference is that when comparing rows, we are at liberty to adjust the dashes to fit any desired condition. The two states are compatible if in every column of the corresponding rows in the primitive flow table, there are identical or compatible pairs and if there is no conflict in the output values.

A check mark (√) designates a square whose pair of states is compatible. Those states that are not compatible are marked with a cross (x). The remaining squares are recorded with the implied pairs that need further investigation.

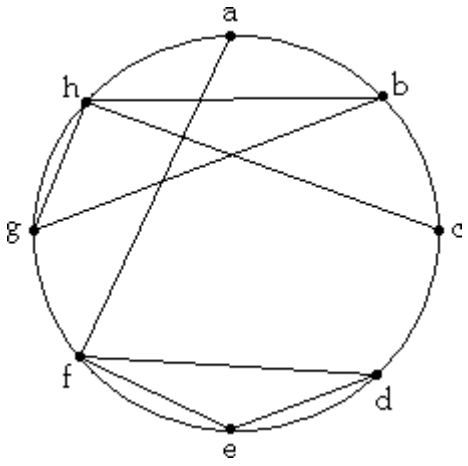
The squares that contain the check marks define the compatible pairs: (a, f) (b, g) (b, h) (c, h) (d, e) (d, f) (e, f) (g, h).

Step 4: Maximal compatibles

Having found all the compatible pairs, the next step is to find larger set of states that are compatible. The ***maximal compatible*** is a group of compatibles that contain all the possible combinations of compatible states. The maximal compatible can be obtained from a merger diagram.

The **merger diagram** is a graph in which each state is represented by a dot placed along the circumference of a circle. Lines are drawn between any two corresponding dots that form a compatible pair. All possible compatibles can be obtained from the merger diagram by observing the geometrical patterns in which states are connected to each other.

- A line represents a compatible pair.
- A triangle constitutes a compatible with three states.
- An n-state compatible is represented in the merger diagram by an n-sided polygon with all its diagonals connected.



Merger Diagram

The merger diagram is obtained from the list of compatible pairs derived from the implication table. There are eight straight lines connecting the dots, one for each compatible pair. The lines form a geometrical pattern consisting of two triangles connecting (b, g, h) & (d, e, f) and two lines (a, f) & (c, h). The maximal compatibles are:

(a, f) (b, g, h) (c, h) (d, e, f)

TC

	00	01	11	10
a, f	e, –	(f), 0	(a), 0	b, –
b, g, h	(g), 1	(h), 1	c, –	(b), 1
c, h	g, –	(h), 1	(c), 1	d, –
d, e, f	(e), 0	(f), 0	a, –	(d), 0

Reduced Flow table

The reduced flow table is drawn. The compatible states are merged into one row that retains the original letter symbols of the states. The four compatible set of states are used to merge the flow table into four rows.

TC

	00	01	11	10
a	d, –	(a), 0	(a), 0	b, –
b	(b), 1	(b), 1	c, –	(b), 1
c	b, –	(c), 1	(c), 1	d, –
d	(d), 0	(d), 0	a, –	(d), 0

Final Reduced Flow table

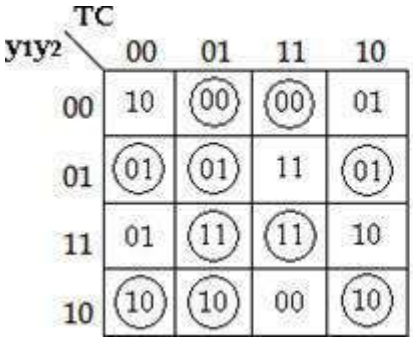
Here we assign a common letter symbol to all the stable states in each merged row. Thus, the symbol f is replaced by a; g & h are replaced by b, and similarly for the other two rows.

Step 5: State Assignment and Transition table

Find the race-free binary assignment for the four stable states in the reduced flow table. Assign a= 00, b= 01, c= 11 and d= 10.

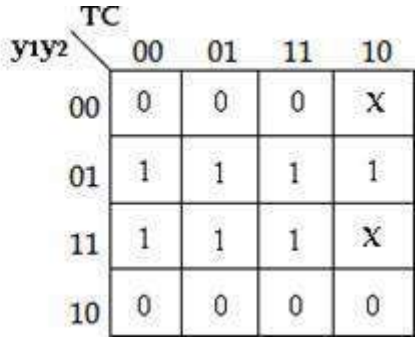
Substituting the binary assignment into the reduced flow table, the transition table is obtained. The output map is obtained from the reduced flow table.

Transition Table and Output Map:



y_1y_2 \ TC	00	01	11	10
00	10	(00)	(00)	01
01	(01)	(01)	11	(01)
11	01	(11)	(11)	10
10	(10)	(10)	00	(10)

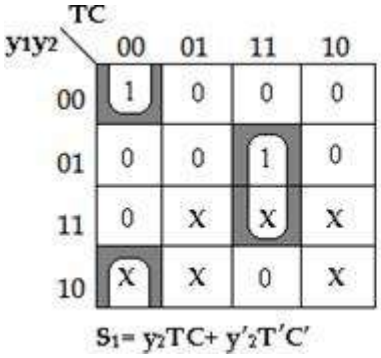
Transition table



y_1y_2 \ TC	00	01	11	10
00	0	0	0	X
01	1	1	1	1
11	1	1	1	X
10	0	0	0	0

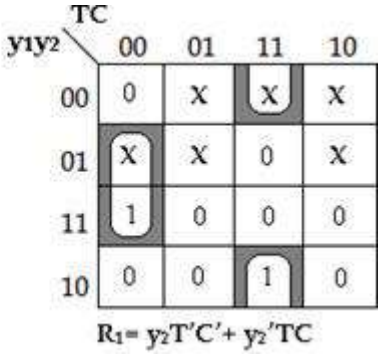
Output map Q= y2

Maps for Latch Inputs:



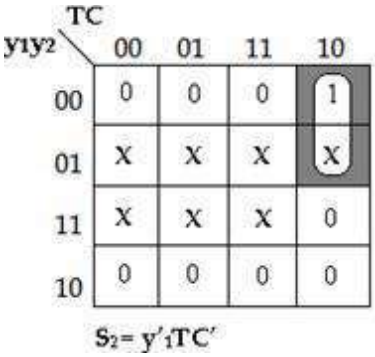
y_1y_2 \ TC	00	01	11	10
00	1	0	0	0
01	0	0	1	0
11	0	X	X	X
10	X	X	0	X

$S_1 = y_2TC + y'_2T'C'$



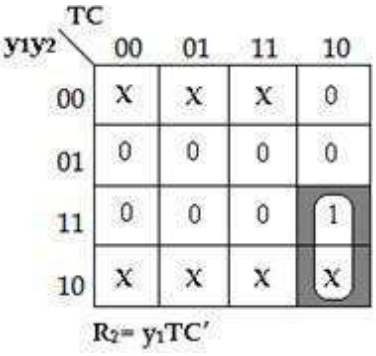
y_1y_2 \ TC	00	01	11	10
00	0	X	X	X
01	X	X	0	X
11	1	0	0	0
10	0	0	1	0

$R_1 = y_2T'C' + y_2'TC$



y_1y_2 \ TC	00	01	11	10
00	0	0	0	1
01	X	X	X	X
11	X	X	X	0
10	0	0	0	0

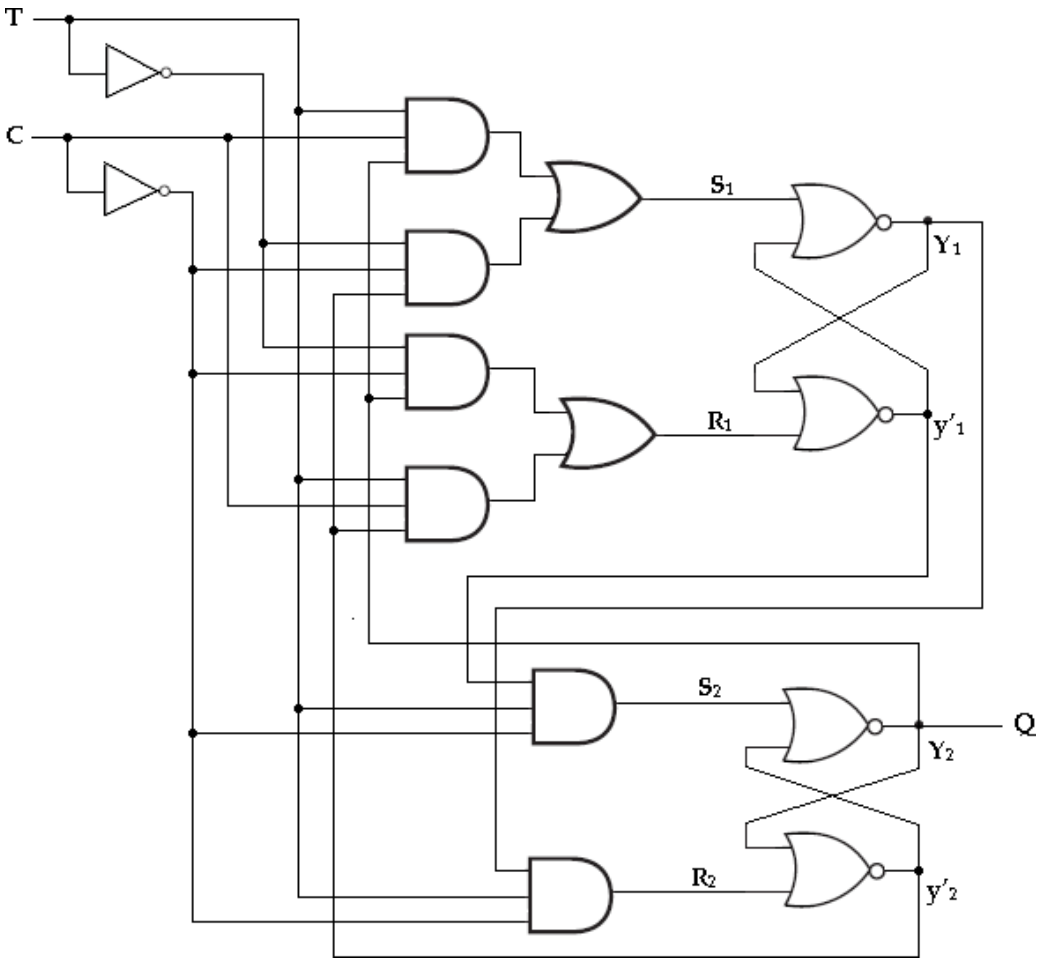
$S_2 = y'_1TC'$



y_1y_2 \ TC	00	01	11	10
00	X	X	X	0
01	0	0	0	0
11	0	0	0	1
10	X	X	X	X

$R_2 = y_1TC'$

Logic Diagram:

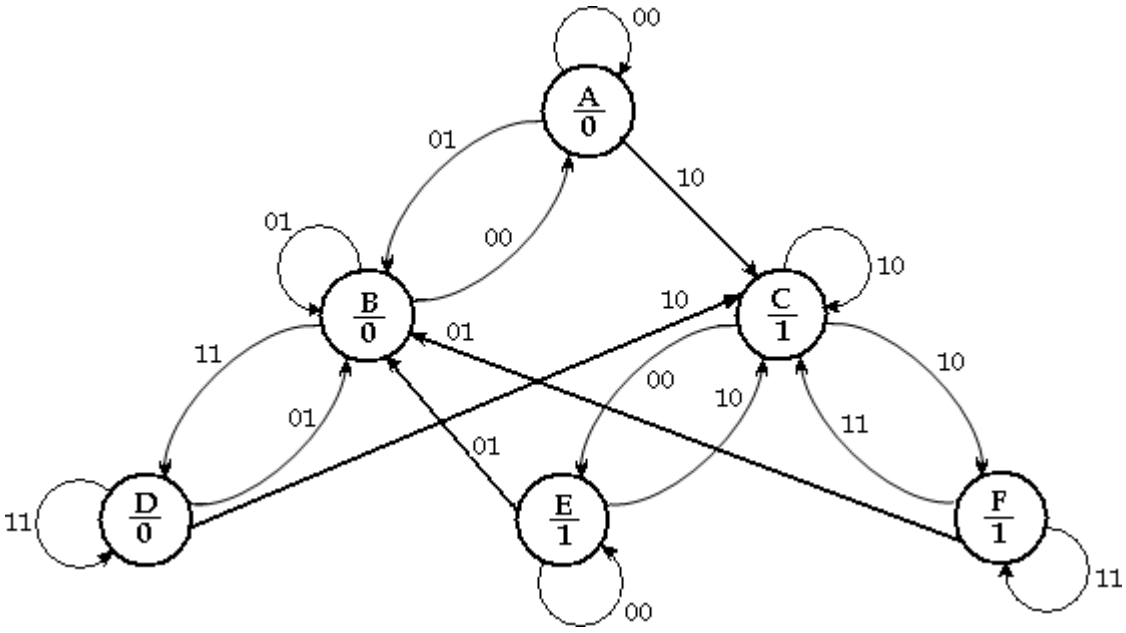


3. Develop a state diagram and primitive flow table for a logic system that has two inputs, X and Y, and a single output X, which is to behave in the following manner. Initially, both inputs and output are equal to 0. Whenever X= 1 and Y= 0, the Z becomes 1 and whenever X= 0 and Y= 1, the Z becomes 0. When inputs are zero, i.e. X= Y= 0 or inputs are one, i.e. X= Y= 1, the output Z does not change; it remains in the previous state. The logic system has edge triggered inputs without having a clock. The logic system changes state on the rising edges of the two inputs. Static input values are not to have any effect in changing the Z output.

Soln:

The conditions given are, Initially both inputs X and Y are 0.
When X=1, Y= 0; Z= 1
When X= 0, Y= 1; Z= 0
When X= Y= 0 or X= Y= 1, then Z does not change, it remains in the previous state.

Step 1: The above state transitions are represented in the state diagram as,



State diagram

Step 2: A primitive flow table is constructed from the state diagram. The primitive flow table has one row for each state and one column for each input combination. Only one stable state exists for each row in the table. The stable state can be easily identified from the state diagram. For example, state A is stable with output 0 when inputs are 00, state C is stable with output 1 when inputs are 10 and so on.

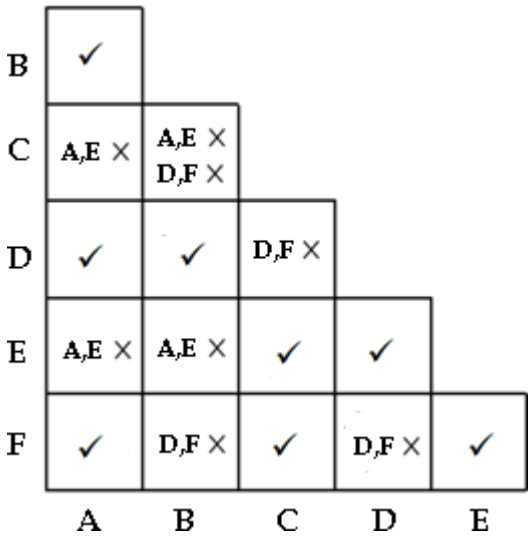
We know that both inputs are not allowed to change simultaneously, so we can enter dash marks in each row that differs in two or more variables from the input variables associated with the stable state. For example, the first row in the flow table shows a stable state with an input of 00. Since only one input can change at any given time, it can change to 01 or 10, but not to 11. Therefore we can enter two dashes in the 11 column of row A.

The remaining places in the primitive flow table can be filled by observing state diagram. For example, state B is the next state for present state A when input combination is 01; similarly state C is the next state for present state A when input combination is 10.

Step 3: Primitive flow table

	XY 00	01	11	10
A	(A), 0	B, –	–, –	C, –
B	A, –	(B), 0	D, –	–, –
C	E, –	–, –	F, –	(C), 1
D	–, –	B, –	(D), 0	C, –
E	(E), 1	B, –	–, –	C, –
F	–, –	B, –	(F), 1	C, –

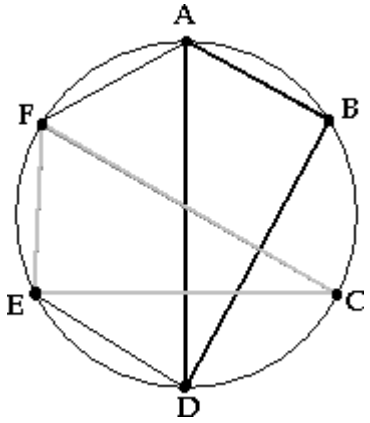
The rows in the primitive flow table are merged by first obtaining all compatible pairs of states. This is done by means of the implication table.



The squares that contain the check marks (✓) define the compatible pairs:
(A, B) (A, D) (A, F) (B, D) (C, E) (C, F) (D, E) (E, F).

Step 4: The merger diagram is obtained from the list of compatible pairs derived from the implication table. There are eight straight lines connecting the dots, one for each compatible pair. The lines form a geometrical pattern consisting of two triangles connecting (A, B, D) & (C, E, F) and two lines (A, F) & (D, E). The maximal compatibles are:

(A, B, D) (C, E, F) (A, F) (D, E)



Merger diagram

Closed covering condition:

The condition that must be satisfied for merging rows is that the set of chosen compatibles must *cover* all the states and must be *closed.* The set will cover all the states if it includes all the states of the original state table. The closure condition is satisfied if there are no implied states *or* if the implied states are included within the set. A closed set of compatibles that covers all the states is called a *closed covering*.

If we remove (A, F*)* and (D, E), we are left with a set of two compatibles:

(A, B, D) (C, E, F)

All six states from the primitive flow table are included in this set. Thus, the set

satisfies the covering condition. The reduced flow table is drawn as below.

	XY 00	01	11	10
A,B,D	(A),0	(B),0	(D),0	C,–
C,E,F	(E),1	B,–	(F),1	(C),1

Reduced flow table

Here we assign a common letter symbol to all the stable states in each merged row. Thus, the symbol B & D is replaced by A; E & F are replaced by C.

	XY 00	01	11	10
A	(A),0	(A),0	(A),0	C,–
C	(C),1	A,–	(C),1	(C),1

Step 5: Find the race-free binary assignment for the four stable states in the reduced flow table. Assign A= 0 and C= 1. Substituting the binary assignment into the reduced flow table, the transition table is obtained. The output map is obtained from the reduced flow table.

q \ XY	00	01	11	10
0	0	0	0	1
1	1	0	1	1

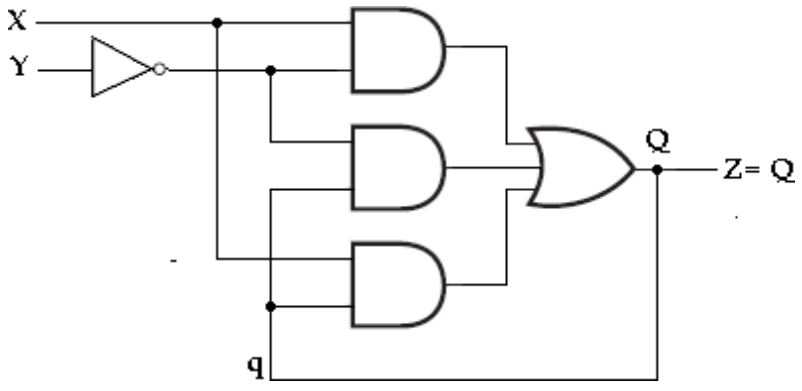
Q= qY' + XY' + qX

q \ XY	00	01	11	10
0	0	0	0	1
1	1	0	1	1

Z= Q

Transition table and output map

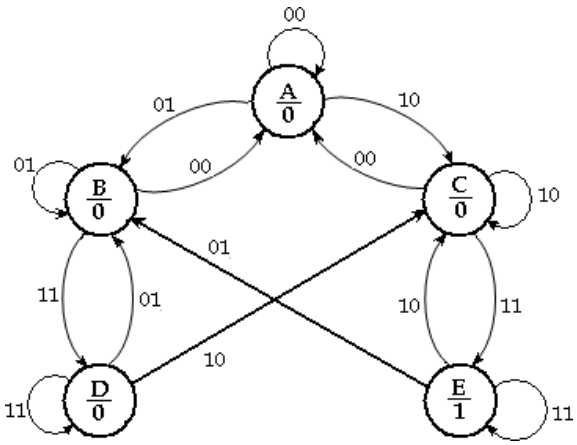
Step 6: Gated-Latch Logic diagram



4. Design a circuit with inputs X and Y to give an output Z= 1 when XY= 11 but only if X becomes 1 before Y, by drawing total state diagram, primitive flow table and output map in which transient state is included.

Soln:

Step 1: The state diagram can be drawn as,



State table

Step 2: A primitive flow table is constructed from the state table as,

	XY 00	01	11	10
A	(A), 0	B, –	–, –	C, –
B	A, –	(B), 0	D, –	–, –
C	A, –	–, –	E, –	(C), 0
D	–, –	B, –	(D), 0	C, –
E	–, –	B, –	(E), 1	C, –

Primitive flow table

Step 3: The rows in the primitive flow table are merged by first obtaining all compatible pairs of states. This is done by means of the implication table.

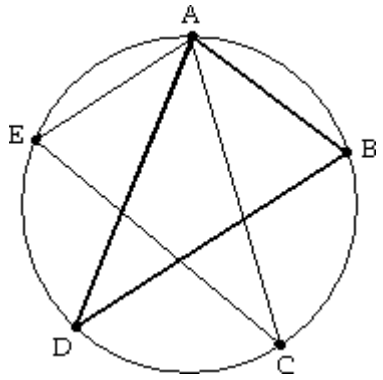
B	✓			
C	✓	D,E ×		
D	✓	✓	D,E ×	
E	✓	D,E ×	✓	D,E ×
	A	B	C	D

Implication table

The squares that contain the check marks (✓) define the compatible pairs:
(A, B) (A, C) (A, D) (A, E) (B, D) (C, E).

Step 4: The merger diagram is obtained from the list of compatible pairs derived from the implication table. There are six straight lines connecting the dots, one for each compatible pair. The lines form a geometrical pattern consisting of one triangle connecting (A, B, D) & a line (C, E). The maximal compatibles are:

(A, B, D) **(C, E)**



Merger diagram

The reduced flow table is drawn as below.

	XY 00	01	11	10
A, B, D	(A), 0	(B), 0	(D), 0	C, –
C, E	A, –	B, –	(E), 1	(C), 0

Reduced flow table

Here we assign a common letter symbol to all the stable states in each merged row. Thus, the symbol B & D is replaced by A; E is replaced by C.

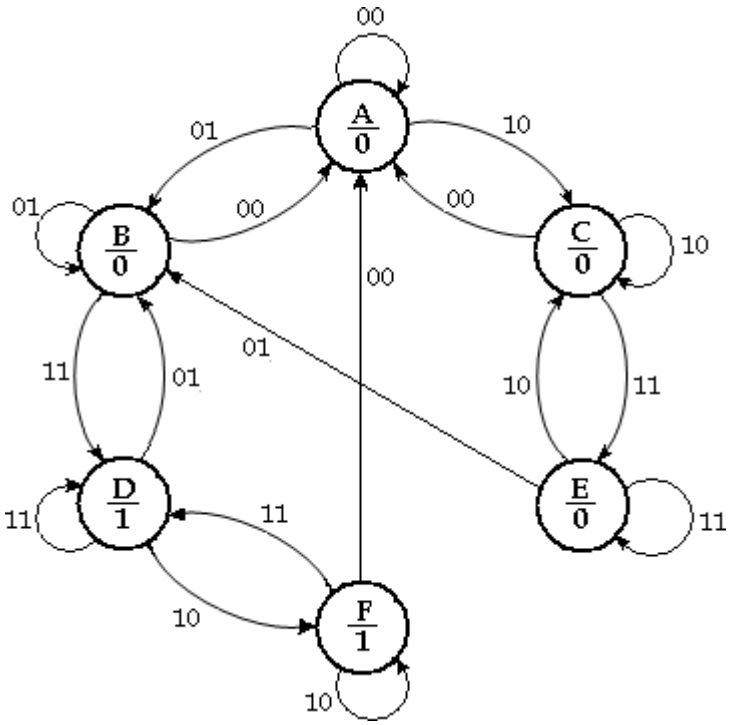
	XY 00	01	11	10
A	(A), 0	(A), 0	(A), 0	C, –
C	A, –	A, –	(C), 1	(C), 0

Transition table

5. Design a circuit with primary inputs A and B to give an output Z equal to 1 when A becomes 1 if B is already 1. Once Z= 1 it will remain so until A goes to 0. Draw the total state diagram, primitive flow table for designing this circuit.

Soln:

Step 1: The state diagram can be drawn as,



State diagram

Step 2: A primitive flow table is constructed from the state table as,

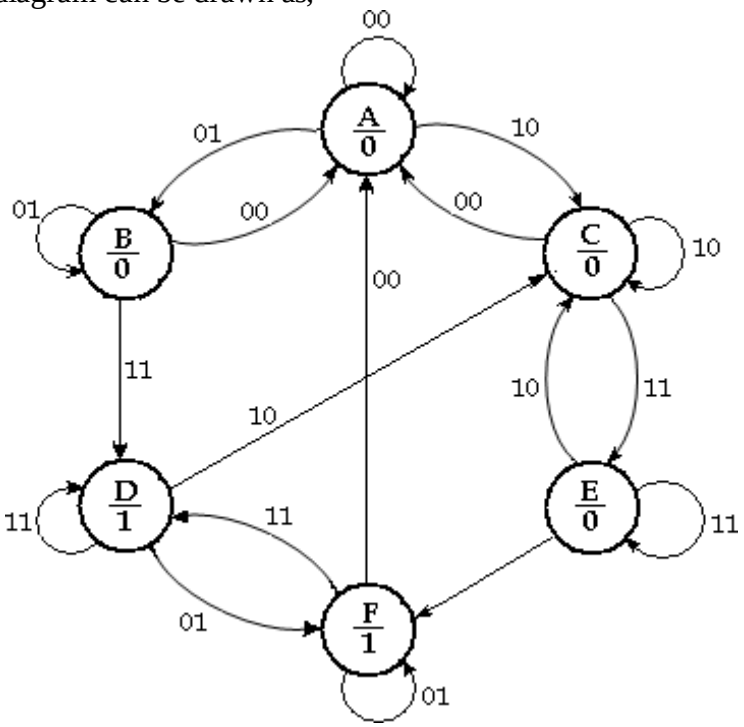
	AB 00	01	11	10
A	(A), 0	B, –	–, –	C, –
B	A, –	(B), 0	D, –	–, –
C	A, –	–, –	E, –	(C), 0
D	–, –	B, –	(D), 1	F, –
E	–, –	B, –	(E), 0	C, –
F	A, –	–, –	D, –	(F), 1

Primitive flow table

6. ***Design an asynchronous sequential circuit that has two inputs X2 and X1 and one output Z. When X1= 0, the output Z is 0. The first change in X2 that occurs while X1 is 1 will cause output Z to be 1. The output Z will remain 1 until X1 returns to 0.***

Soln:

Step 1: The state diagram can be drawn as,



State diagram

Step 2: A primitive flow table is constructed from the state table as,

	X_2X_1 = 00	01	11	10
A	(A), 0	B, –	–, –	C, –
B	A, –	(B), 0	D, –	–, –
C	A, –	–, –	E, –	(C), 0
D	–, –	F, –	(D), 1	C, –
E	–, –	F, –	(E), 0	C, –
F	A, –	(F), 1	D, –	–, –

Primitive flow table

Step 3: The rows in the primitive flow table are merged by obtaining all compatible pairs of states. This is done by means of the implication table.

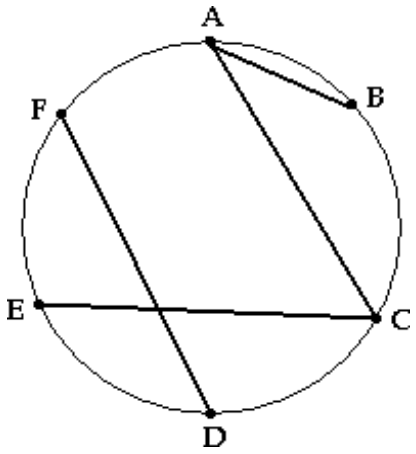
	A	B	C	D	E
B	✓				
C	✓	D,E ×			
D	B,F ×	B,F ×	D,F ×		
E	B,F ×	B,F × D,E ×	✓	D,E ×	
F	B,F ×	B,F ×	D,E ×	✓	D,E ×

Implication table

The squares that contain the check marks (✓) define the compatible pairs:

(A, B) (A, C) (C, E) (D, F)

Step 4: The merger diagram is obtained from the list of compatible pairs derived from the implication table. There are four straight lines connecting the dots, one for each compatible pair. It consists of four lines (A, B), (A, C), (C, E) and (D, F).



Merger diagram

The maximal compatibles are:

(A, B) **(C, E)** **(D, F)**

This set of maximal compatible covers all the original states resulting in the reduced flow table.

The reduced flow table is drawn as below.

X_2X_1	00	01	11	10
A, B	(A), 0	(B), 0	D, –	C, –
C, E	A, –	F, –	(E), 0	(C), 0
D, F	A, –	(F), 1	(D), 1	C, –

Flow table

Here we assign a common letter symbol to all the stable states in each merged row.

Thus, the symbol B is replaced by A; E is replaced by C and F is replaced by D.

X_2X_1	00	01	11	10
A	(A), 0	(A), 0	D, –	C, –
C	A, –	D, –	(C), 0	(C), 0
D	A, –	(D), 1	(D), 1	C, –

Reduced Flow table

Step 5: Find the race-free binary assignment for the four stable states in the reduced flow table. Assign A= S_0, C= S_1 and D= S_2.

X_2X_1	00	01	11	10
S_0	(S_0), 0	(S_0), 0	S_2, –	S_1, –
S_1	S_0, –	S_2, –	(S_1), 0	(S_1), 0
S_2	S_0, –	(S_2), 1	(S_2), 1	S_1, –

Now, if we assign S0= 00, S1 = 01 and S2 = 10, then we need one more state S3= 11 to prevent critical race during transition of S0 → S1 or S2 → S1. By introducing S3 the transitions S1 → S2 and S2 → S1 are routed through S4.

Thus after state assignment the flow table can be given as,

Present State	Next state for Inputs X_2X_1, Output			
F_2F_1	00	01	11	10
$S_0 \rightarrow 00$	(S_0), 0	(S_0), 0	S_2, –	S_1, –
$S_1 \rightarrow 01$	S_0, –	S_3, –	(S_1), 0	(S_1), 0
$S_2 \rightarrow 10$	S_0, –	(S_2), 1	(S_2), 1	S_3, –
$S_3 \rightarrow 11$	–, –	S_2, –	–, –	S_1, –

Flow table with state assignment

Substituting the binary assignment into the reduced flow table, the transition table is obtained. The output map is obtained from the reduced flow table.

Present State		Next state for Inputs X_2X_1, Output			
F_2	F_1	00	01	11	10
0	0	(00), 0	(00), 0	10, –	01, –
0	1	00, –	11, –	(01), 0	(01), 0
1	0	00, –	(10), 1	(10), 1	11, –
1	1	–, –	10, –	–, –	01, –

K- Map simplification:

For F_2^+

F_2F_1 \ X_2X_1	00	01	11	10
00	0	0	1	0
01	0	1	0	0
11	X	1	X	0
10	0	1	1	1

$F_2^+ = \overline{F}_1X_2X_1 + F_1\overline{X}_2X_1 + F_2X_1 + F_2\overline{F}_1X_2$

For F_1^+

F_2F_1 \ X_2X_1	00	01	11	10
00	0	0	0	1
01	0	1	1	1
11	X	0	X	1
10	0	0	0	1

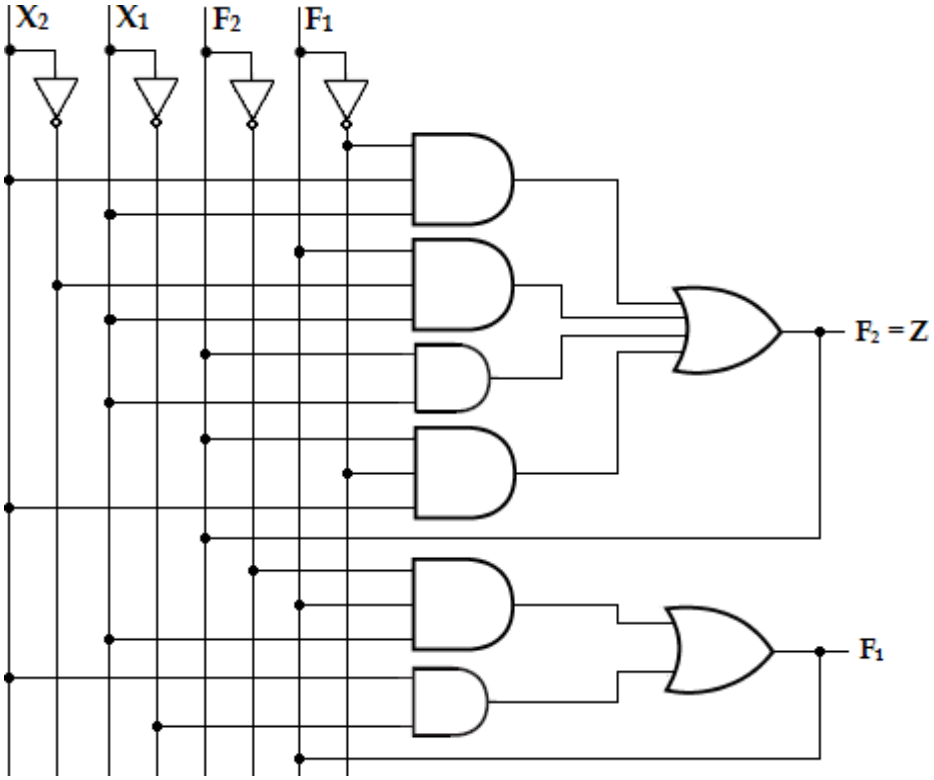
$F_1^+ = \overline{F}_2F_1X_1 + X_2\overline{X}_1$

For Z

F_2F_1 \ X_2X_1	00	01	11	10
00	0	0	X	X
01	X	X	0	0
11	X	X	X	X
10	X	1	1	X

$Z = F_2$

Logic Diagram:



7. Obtain a primitive flow table for a circuit with two inputs x1 and x2 and two outputs z1 and z2 that satisfies the following four conditions.

i) When x1x2 = 00, output z1z2 = 00.

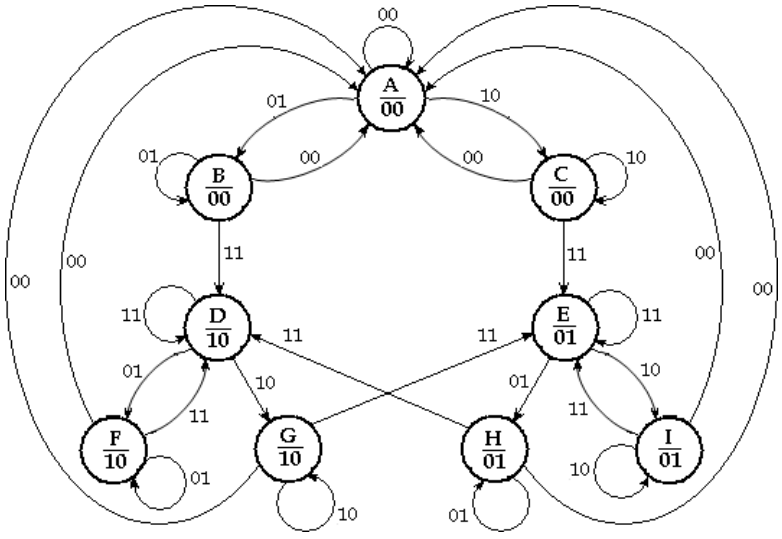
ii) When x1= 1 and x2 changes from 0 to 1, the output z1z2 = 01.

iii) When x2= 1 and x1 changes from 0 to 1, the output z1z2 = 10.

iv) Otherwise the output does not change.

Soln:

The state diagram can be drawn as,



State diagram

Step 2: A primitive flow table is constructed from the state table as,

	X_1X_2 = 00	01	11	10
A	(A), 00	B, –	–, –	C, –
B	A, –	(B), 00	D, –	–, –
C	A, –	–, –	E, –	(C), 00
D	–, –	F, –	(D), 10	G, –
E	–, –	H, –	(E), 01	I, –
F	A, –	(F), 10	D, –	–, –
G	A, –	–, –	E, –	(G), 10
H	A, –	(H), 01	D, –	–, –
I	A, –	–, –	E, –	(I), 01

Primitive flow table

HAZARDS

Hazards are unwanted switching transients that may appear at the output of a circuit because different paths exhibit different propagation delays.

Hazards occur in combinational circuits, where they may cause a temporary false-output value. When this condition occurs in asynchronous sequential circuits, it may result in a transition to a wrong stable state.

Hazards in Combinational Circuits

A hazard is a condition where a single variable change produces a momentary output change when no output change should occur.

Types of Hazards

- Static hazard
- Dynamic hazard

Static Hazard:

In digital systems, there are only two possible outputs, a ‘0’ or a ‘1’. The hazard may produce a wrong ‘0’ or a wrong ‘1’. Based on these observations, there are three types,

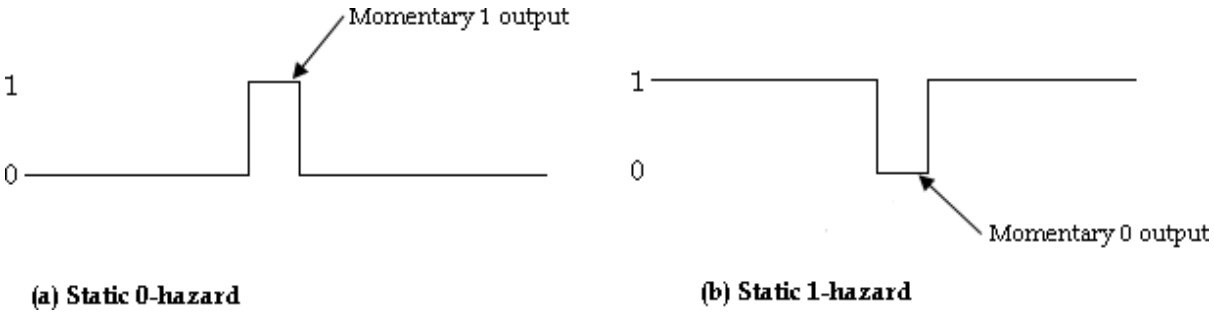
- Static- 0 hazard,
- Static- 1 hazard.

Static- 0 hazard:

When the output of the circuit is to remain at 0, and a momentary 1 output is possible during the transmission between the two inputs, then the hazard is called a static 0-hazard.

Static- 1 hazard:

When the output of the circuit is to remain at 1, and a momentary 0 output is possible during the transmission between the two inputs, then the hazard is called a static 1-hazard.

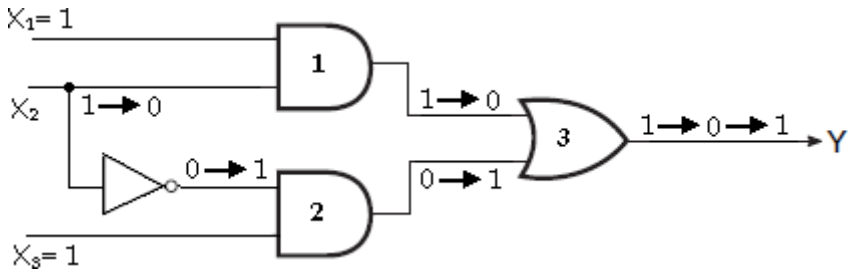


(a) Static 0-hazard **(b) Static 1-hazard**

The below circuit demonstrates the occurrence of a static 1-hazard. Assume that all three inputs are initially equal to 1 i.e., $X_1X_2X_3$= 111. This causes the output of the gate 1 to be 1, that of gate 2 to be 0, and the output of the circuit to be equal to 1. Now consider a change of X_2 from 1 to 0 i.e., $X_1X_2X_3$= 101. The output of gate 1 changes to 0 and that of gate 2 changes to 1, leaving the output at 1. The output may momentarily go to 0 if the propagation delay through the inverter is taken into consideration.

The delay in the inverter may cause the output of gate 1 to change to 0 before the output of gate 2 changes to 1. In that case, both inputs of gate 3 are momentarily equal to 0, causing the output to go to 0 for the short interval of time that the input signal from X_2 is delayed while it is propagating through the inverter circuit.

Thus, a static 1-hazard exists during the transition between the input states $X_1X_2X_3$=111 and $X_1X_2X_3$= 101.

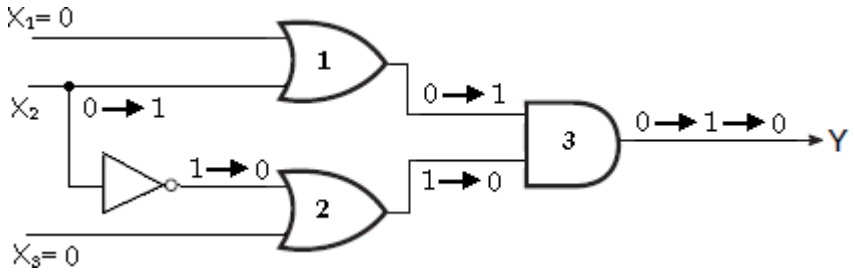


Circuit with static-1 hazard

Now consider the below network, and assume that the inverter has an appreciably greater propagation delay time than the other gates. In this case there is a static 0-hazard in the transition between the input states $X_1X_2X_3$= 000 and $X_1X_2X_3$= 010 since it is possible for a logic-1 signal to appear at both input terminals of the AND gate for a short duration.

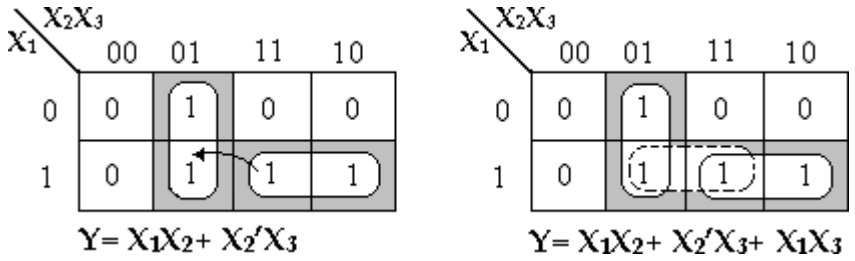
The delay in the inverter may cause the output of gate 1 to change to 1 before the output of gate 2 changes to 0. In that case, both inputs of gate 3 are momentarily equal to 0, causing the output to go to 1 for the short interval of time that the input signal from X_2 is delayed while it is propagating through the inverter circuit.

Thus, a static 0-hazard exists during the transition between the input states $X_1X_2X_3$= 000 and $X_1X_2X_3$= 010.



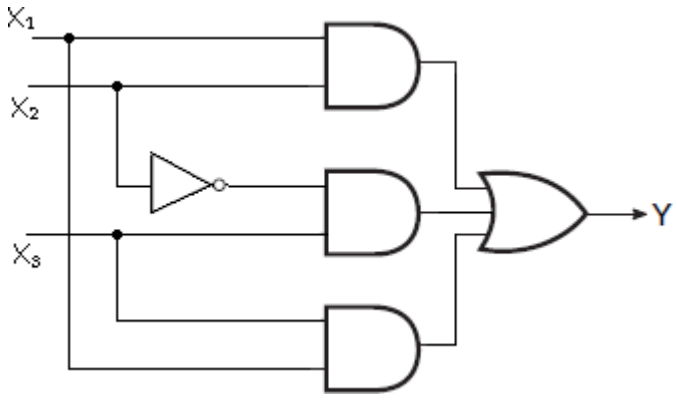
Circuit with static-0 hazard

A hazard can be detected by inspection of the map of the particular circuit. To illustrate, consider the map in the circuit with static 0-hazard, which is a plot of the function implemented. The change in X2 from *1* to 0 moves the circuit from minterm 111 to minterm 101. The hazard exists because the change in input results in a different product term covering the two minterrns.



Maps demonstrating a Hazard and its Removal

The minterm 111 is covered by the product term implemented in gate 1 and minterm 101 is covered by the product term implemented in gate 2. Whenever the circuit must move from one product term to another, there is a possibility of a momentary interval when neither term is equal to 1, giving rise to an undesirable 0 output. The remedy for eliminating a hazard is to enclose the two minterms in question with another product term that overlaps both groupings. This situation is shown in the *map* above, where the two terms that causes the hazard are combined into one product term. The hazard- free circuit obtained by this combinational is shown below.



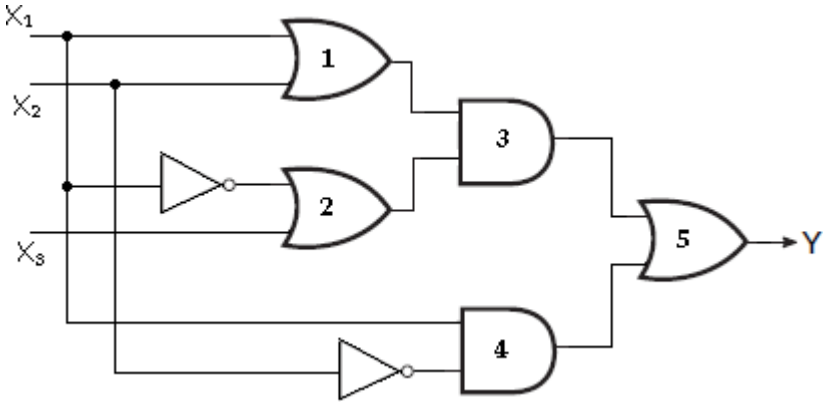
Hazard-free Circuit

The extra gate in the circuit generates the product term X1X4. The hazards in combinational circuits can be removed by covering any two minterms that may produce a hazard with a product term common to both. The removal of hazards requires the addition of redundant gates to the circuit.

Dynamic Hazard

A dynamic hazard is defined as a transient change occurring three or more times at an output terminal of a logic network when the output is supposed to change only once during a transition between two input states differing in the value of one variable.

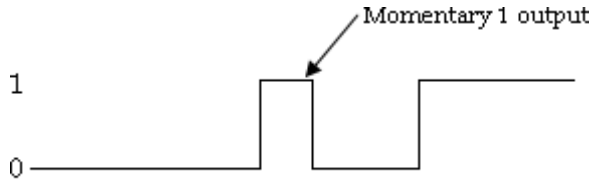
Now consider the input states $X_1X_2X_3$= 000 and $X_1X_2X_3$= 100. For the first input state, the steady state output is 0; while for the second input state, the steady state output is 1. To facilitate the discussion of the transient behavior of this network, assume there are no propagation delays through gates G_3 and G_5 and that the propagation delays of the other three gates are such that G_1 can switch faster than G_2 and G_2 can switch faster than G_4.



Circuit with Dynamic hazard

When X_1 changes from 0 to 1, the change propagates through gate G_1 before gate G_2 with the net effect that the inputs to gate G_3 are simultaneously 1 and the network output changes from 0 to 1. Then, when X_1 change propagates through gate G_2, the lower input to gate G_3 becomes 0 and the network output changes back to 0.

Finally, when the X_1= 1 signal propagates through gate G_4, the lower input to gate G_5 becomes 1 and the network output again changes to 1. It is therefore seen that during the change of X_1 variable from 0 to 1 the output undergoes the sequence, 0 → 1 → 0 → 1, which results in three changes when it should have undergone only a single change.



Dynamic hazard

Essential Hazard

An essential hazard is caused by unequal delays along two or more paths that originate from the same input. An excessive delay through an inverter circuit in comparison to the delay associated with the feedback path may cause such a hazard.

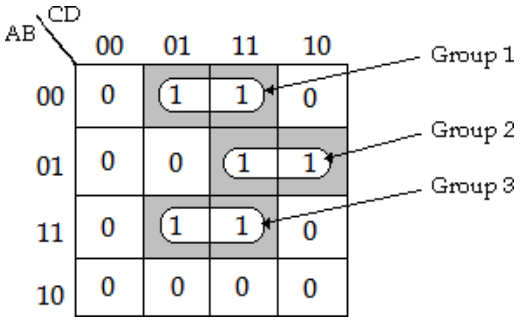
Essential hazards elimination

Essential hazards can be eliminated by adjusting the amount of delays in the affected path. To avoid essential hazards, each feedback loop must be handled with individual care to ensure that the delay in the feedback path is long enough compared with delays of other signals that originate from the input terminals.

Design of Hazard Free Circuits

1. Design a hazard-free circuit to implement the following function. F (A, B, C, D) = ∑m (1, 3, 6, 7, 13, 15).

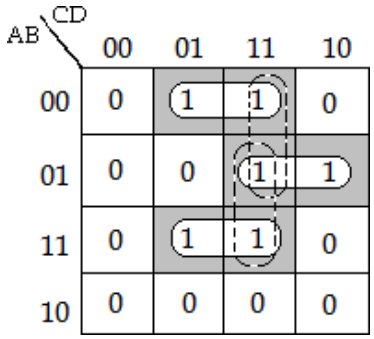
Soln:
a) K-map Implementation and grouping



F=A'B'D+ A'BC+ ABD

b) Hazard- free realization

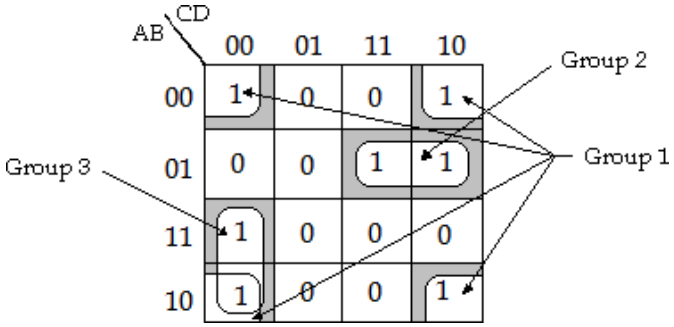
The first additional product term A'CD, overlapping two groups (group 1 & 2) and the second additional product term, BCD, overlapping the two groups (group 2 & 3).



F=A'B'D+ A'BC+ ABD+ A'CD+ BCD

2. Design a hazard-free circuit to implement the following function. F (A, B, C, D) = ∑m (0, 2, 6, 7, 8, 10, 12).

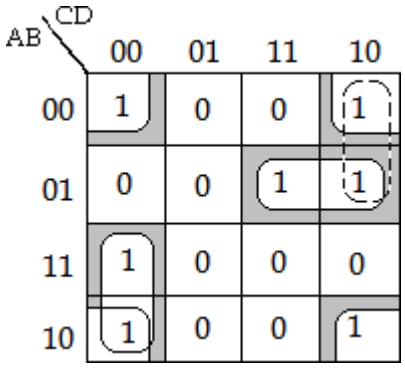
Soln:
a) K-map Implementation and grouping



F= B'D'+ A'BC+ AC'D'

b) Hazard- free realization

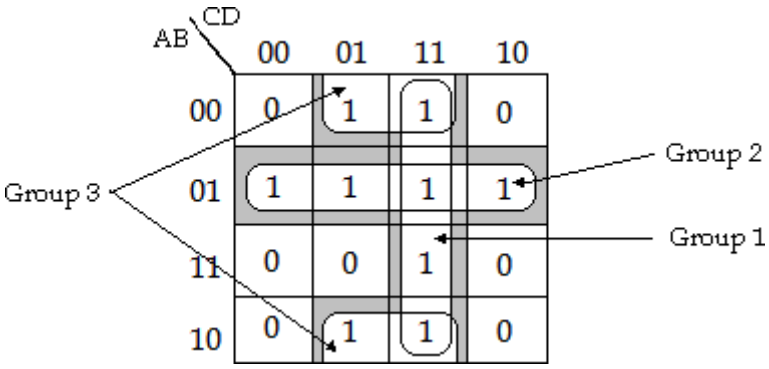
The additional product term, A'CD' overlapping two groups (group 1 & 2) for hazard free realization. Group 1 and 3 are already overlapped hence they do not require additional minterm for grouping.



F= B'D'+ A'BC+ AC'D'+ A'CD'

3. Design a hazard-free circuit to implement the following function. F (A, B, C, D) = ∑m (1, 3, 4, 5, 6, 7, 9, 11, 15).

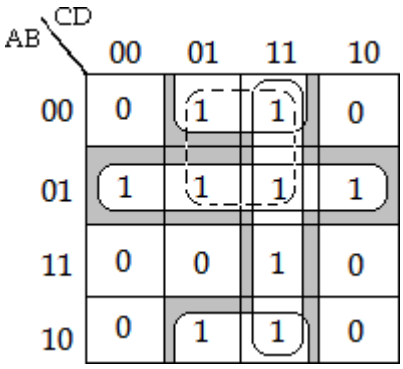
a) K-map Implementation and grouping



F= CD+ A'B+ B'D

b) Hazard- free realization

The additional product term, A'D overlapping two groups (group 2 & 3) for hazard free realization. Group 1 and 2 are already overlapped hence they do not require additional minterm for grouping.

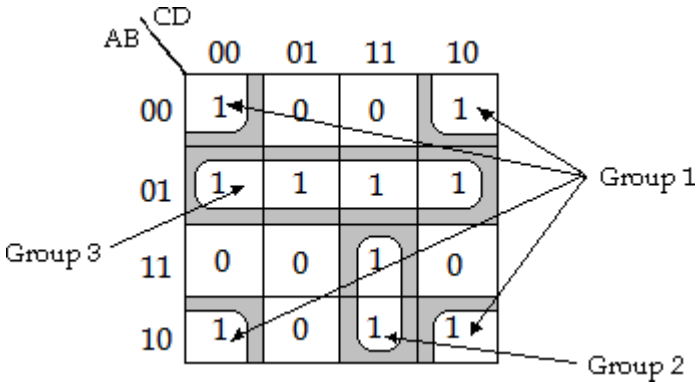


F= CD+ A'B+ B'D+ A'D

4. Design a hazard-free circuit to implement the following function. F (A, B, C, D) = ∑m (0, 2, 4, 5, 6, 7, 8, 10, 11, 15).

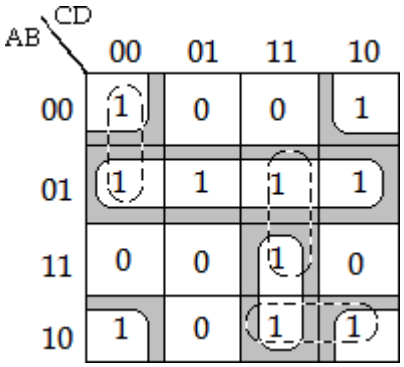
Soln:

a) K-map Implementation and grouping



F= B'D'+ A'B+ ACD

b) Hazard- free realization

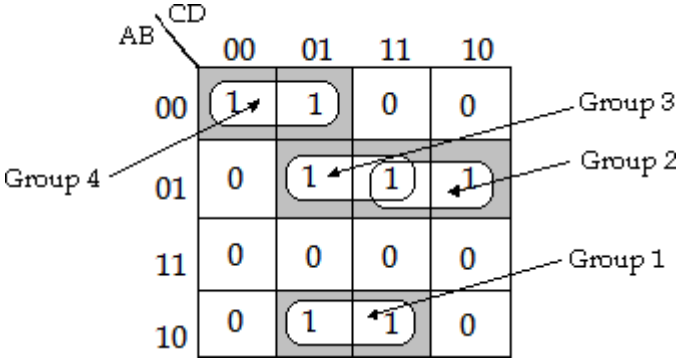


F= B'D'+ A'B+ ACD+ A'C'D'+ BCD+ AB'C

5. Design a hazard-free circuit to implement the following function. F (A, B, C, D) = ∑m (0, 1, 5, 6, 7, 9, 11).

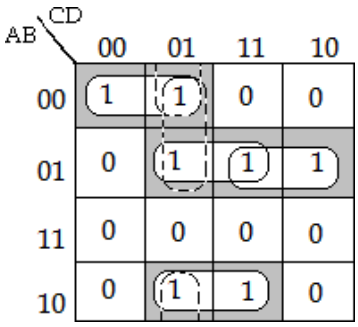
Soln:

a) K-map Implementation and grouping



F= AB'D+ A'BC+ A'BD+ A'B'C'

b) Hazard- free realization:



F= AB'D+ A'BC+ A'BD+ A'B'C'+ A'C'D+ B'C'D

PROGRAMMABLE LOGIC DEVICES

Programmable Logic Devices (PLDs) are the integrated circuits. They contain an array of AND gates & another array of OR gates.

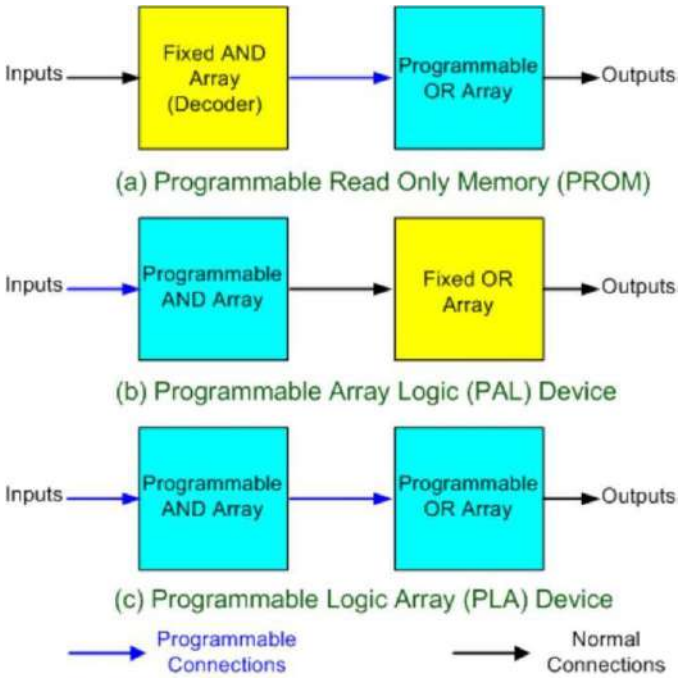
Types of PLDs:

PLDs are broadly classified into simple and complex programmable logic devices. Further, this is grouped as,

- SPLDs (Simple Programmable Logic Devices)
  - ROM (Read-Only Memory)
  - PLA (Programmable Logic Array)
  - PAL (Programmable Array Logic)
  - GAL (Generic Array Logic)
- HCPLD (High Capacity Programmable Logic Device)
  - CPLD (Complex Programmable Logic Device)
  - FPGA (Field-Programmable Gate Array)

Programmable Connections in PLDs:

The programmable connections of AND-OR arrays for different types of PLDs are described here. Figure shows the locations of the programmable connections for the three types.



The PROM (Programmable Read Only Memory) has a fixed AND array (constructed as a decoder) and programmable connections for the output OR gates array. The PROM implements Boolean functions in sum-of-minterms form.

The PAL (Programmable Array Logic) device has a programmable AND array and fixed connections for the OR array.

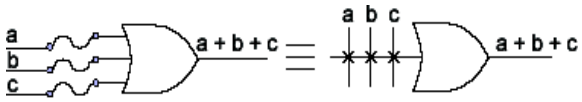
The PLA (Programmable Logic Array) has programmable connections for both AND and OR arrays. So it is the most flexible type of PLD.

The differences between the PROM, PLA and PAL

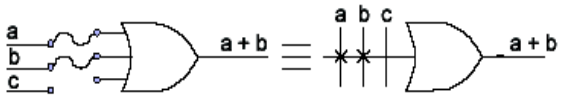
Device	AND array	OR array
PROM	Fixed	Programmable
PLA	Programmable	Programmable
PAL	Programmable	Fixed
GAL	Programmable	Fixed

PLD notation:

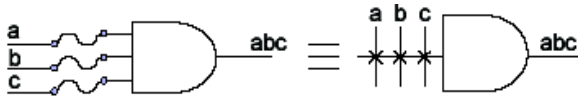
- To indicate the connections to an AND array and an OR array of a PLD, a simplified notation is frequently used.
- The notation is illustrated in Figures.
- Rather than drawing all the inputs to the AND gate or OR gate, a single line is drawn to the input to the gate.
- The inputs are indicated by the right-angled lines.
- The connected input variables are indicated by cross (×) at junctions and unconnected inputs are left blank.
- The cross-marked junctions represent the fusible joints while junctions with dots indicate permanent junctions that are not fusible.



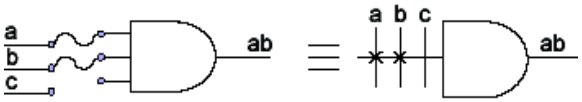
OR gate before programming



OR gate after programming



AND gate before programming

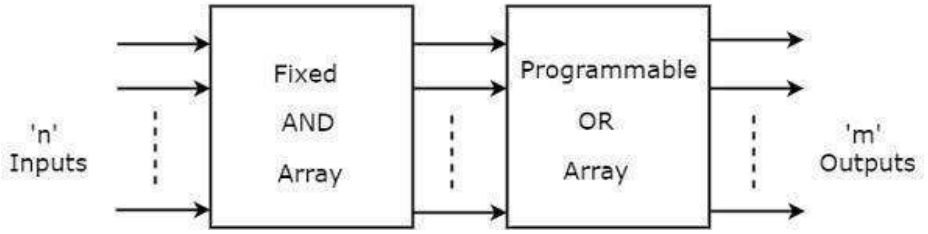


AND gate after programming

PROGRAMMABLE READ ONLY MEMORY (PROM)

Read Only Memory PROM is a memory device, which stores the binary information permanently. That means, we can't change that stored information by any means later. If the ROM has programmable feature, then it is called as **Programmable ROM (**PROM). The user has the flexibility to program the binary information electrically once by using PROM programmer.

PROM is a programmable logic device that has fixed AND array & Programmable OR array. The **block diagram** of PROM is shown in the following figure.



Here, the inputs of AND gates are not of programmable type. So, we have to generate 2^n product terms by using 2^n AND gates having n inputs each. We can implement these product terms by using n x 2^n decoder. So, this decoder generates 'n' **min terms**.

Here, the inputs of OR gates are programmable. That means, we can program any number of required product terms, since all the outputs of AND gates are applied as inputs to each OR gate. Therefore, the outputs of PROM will be in the form of **sum of min terms**.

Example 1:

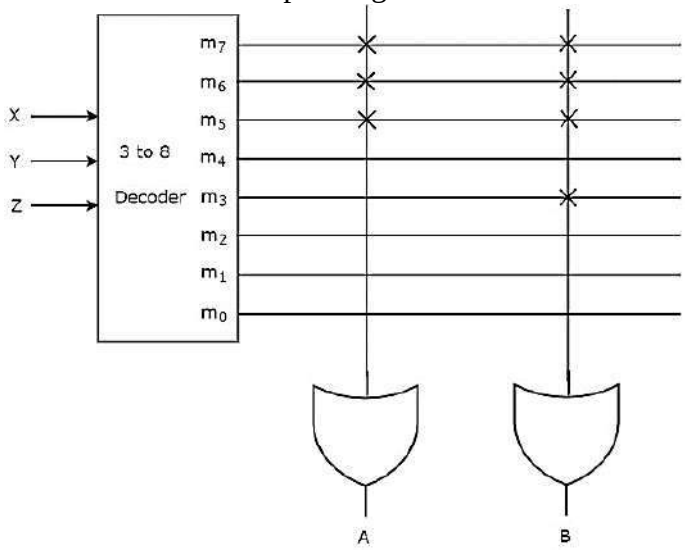
Let us implement the following **Boolean functions** using **PROM**.

A(X,Y,Z)=∑m(5,6,7)

B(X,Y,Z)=∑m(3,5,6,7)

The given two functions are in sum of min terms form and each function is having three variables X, Y & Z. So, we require a 3 to 8 decoder and two programmable OR gates for producing these two functions. The corresponding **PROM** is shown in the following figure.

The given two functions are in sum of min terms form and each function is having three variables X, Y & Z. So, we require a 3 to 8 decoder and two programmable OR gates for producing these two functions. The corresponding **PROM** is shown in the following figure.



Here, 3 to 8 decoder generates eight min terms. The two programmable OR gates have the access of all these min terms. But, only the required min terms are programmed in order to produce the respective Boolean functions by each OR gate. The symbol 'X' is used for programmable connections.

Example 2:

Implement the following **Boolean functions** using **PROM**.

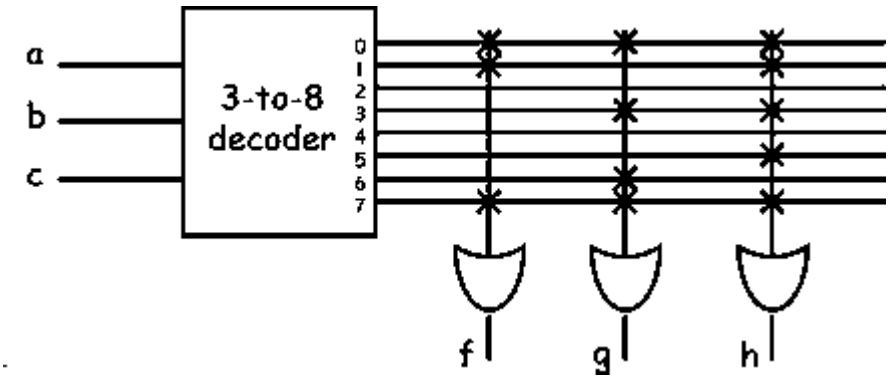
$f = \sum m\ (0, 1, 7)$

$g = \sum m\ (0, 3, 6, 7)$

$h = \sum m\ (0, 1, 3, 5, 7)$

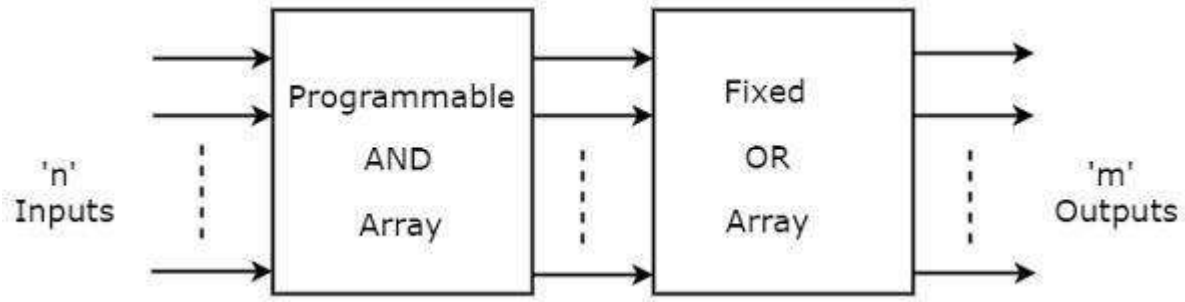
Soln:

There are 3 inputs (a, b, c) and 3 outputs (f, g, h), thus we need a 8x3 ROM block.



PROGRAMMABLE ARRAY LOGIC (PAL)

PAL is a programmable logic device that has Programmable AND array & fixed OR array. The advantage of PAL is that we can generate only the required product terms of Boolean function instead of generating all the min terms by using programmable AND gates. The **block diagram** of PAL is shown in the following figure.



Here, the inputs of AND gates are programmable. That means each AND gate has both normal and complemented inputs of variables. So, based on the requirement, we can program any of those inputs. So, we can generate only the required **product terms** by using these AND gates.

Here, the inputs of OR gates are not of programmable type. So, the number of inputs to each OR gate will be of fixed type. Hence, apply those required product terms to each OR gate as inputs. Therefore, the outputs of PAL will be in the form of **sum of products form**.

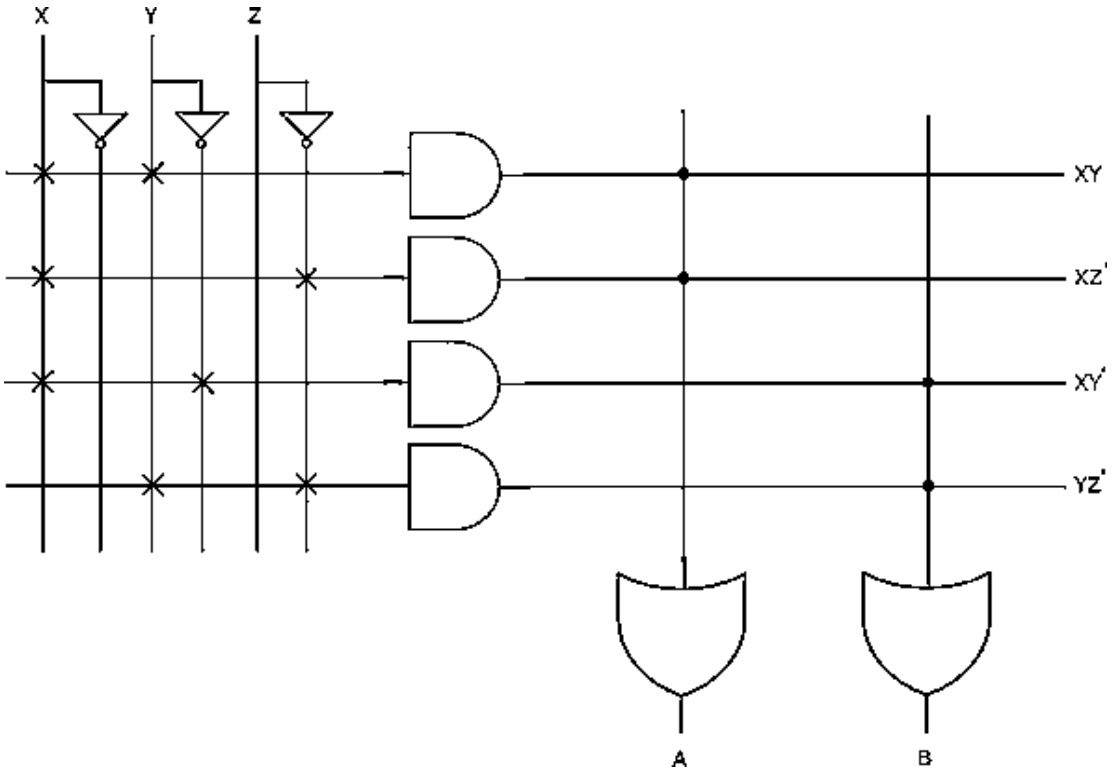
Example 1:

Let us implement the following **Boolean functions** using **PAL**.

$$A=XY+XZ'$$

$$B=XY'+YZ'$$

The given two functions are in sum of products form. There are two product terms present in each Boolean function. So, we require four programmable AND gates & two fixed OR gates for producing those two functions. The corresponding **PAL** is shown in the following figure.



The **programmable AND gates** have the access of both normal and complemented inputs of variables. In the above figure, the inputs X, X′X′, Y, Y′Y′, Z & Z′Z′, are available at the inputs of each AND gate. So, program only the required literals in order to generate one product term by each AND gate. The symbol 'X' is used for programmable connections.

Here, the inputs of OR gates are of fixed type. So, the necessary product terms are connected to inputs of each **OR gate**. So that the OR gates produce the respective Boolean functions. The symbol '.' is used for fixed connections.

Example 2:

Implement the following Boolean functions using the **PAL** device.

$$W(A, B, C, D) = \sum m(2, 12, 13)$$

$$X(A, B, C, D) = \sum m(7, 8, 9, 10, 11, 12, 13, 14, 15)$$

$$Y(A, B, C, D) = \sum m(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$$

$$Z(A, B, C, D) = \sum m(1, 2, 8, 12, 13)$$

Soln:

Simplifying the 4 functions using K-Map to a minimum number of terms results in the following Boolean functions:

W = ABC' + A'B'CD'

X = A + BCD

Y = A'B + CD + B'D'

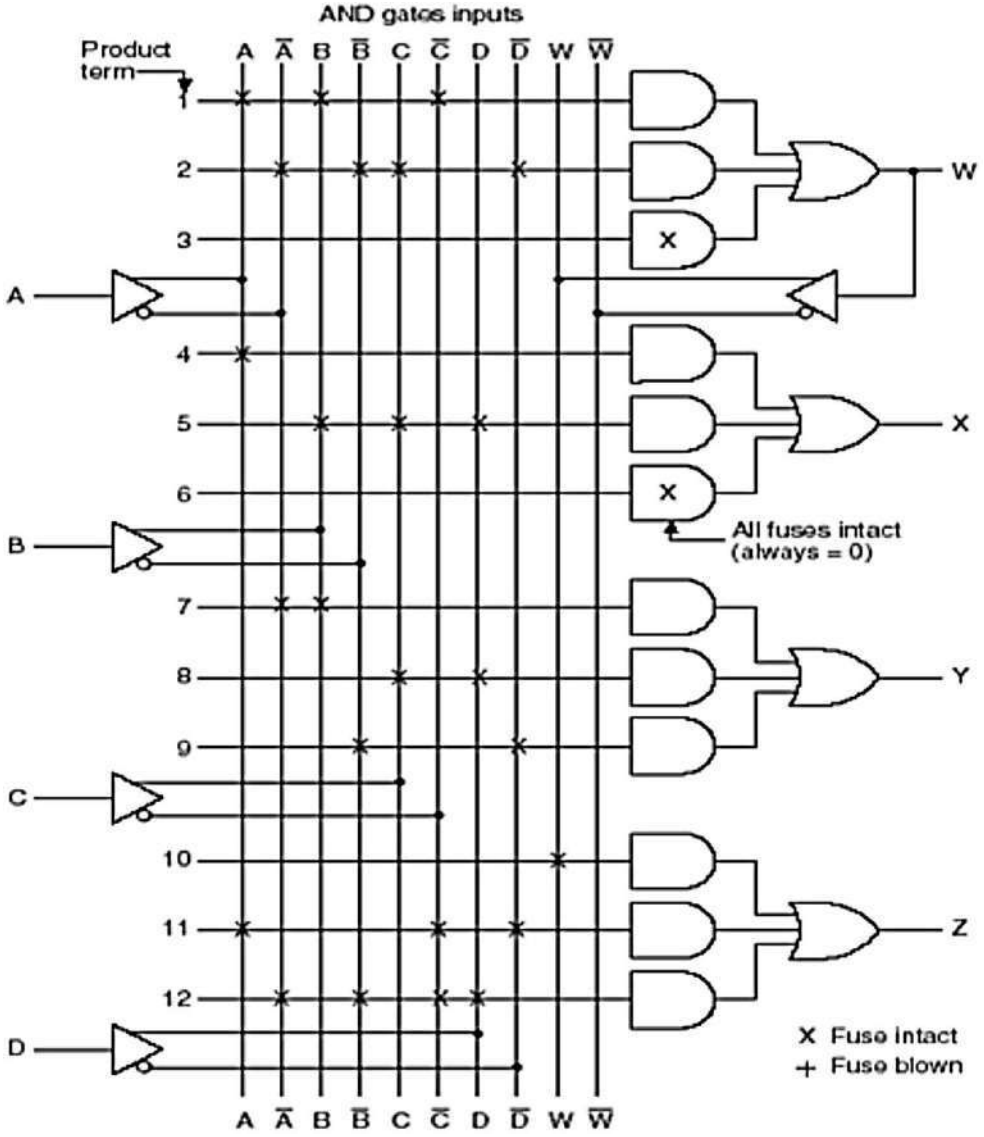
Z = ABC' + A'B'CD + AC'D' + A'B'C'D =W +AC'D' + A'B'C'D

Note that the function for Z has four product terms. The logical sum of two of these terms is equal to W. Thus, by using W, it is possible to reduce the number of terms for Z from four to three, so that the function can fit into the given PAL device.

Product term	AND Inputs A	B	C	D	W	Outputs
1	1	1	0	—	—	$W = AB\overline{C}$
2	0	0	1	0	—	$+\overline{A}\,\overline{B}CD$
3	—	—	—	—	—	
4	1	—	—	—	—	$X = A$
5	—	1	1	1	—	$+BCD$
6	—	—	—	—	—	
7	0	1	—	—	—	$Y = \overline{A}B$
8	—	—	1	1	—	$+CD$
9	—	0	—	0	—	$+\overline{B}\,\overline{D}$
10	—	—	—	—	1	$Z = W$
11	1	—	0	0	—	$+A\overline{C}\,\overline{D}$
12	0	0	0	1	—	$+\overline{A}\,\overline{B}\,\overline{C}D$

PAL program table

The PAL programming table is similar to the table used for the PLA, except that only the inputs of the AND gates need to be programmed. The following figure shows the connection map for the PAL device, as specified in the programming table.

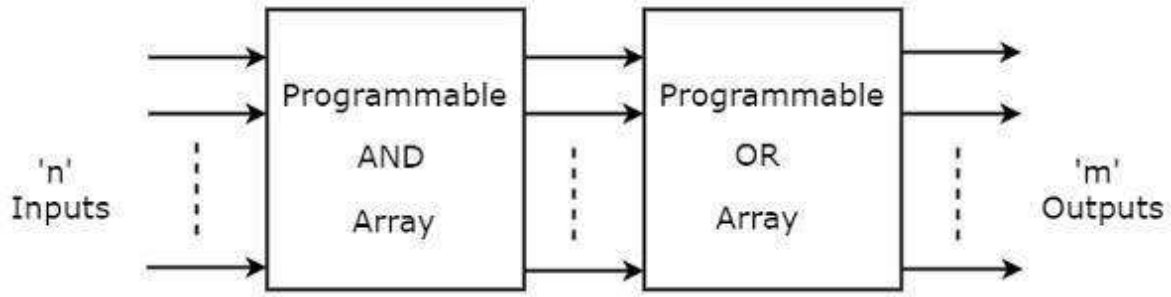


Logic diagram

Since both W and X have two product terms, third AND gate is not used. If all the inputs to this AND gate left intact, then its output will always be 0, because it receives both the true and complement of each input variable i.e., AA' =0

PROGRAMMABLE LOGIC ARRAY (PLA)

PLA is a programmable logic device that has both Programmable AND array & Programmable OR array. Hence, it is the most flexible PLD. The **block diagram** of PLA is shown in the following figure.



Here, the inputs of AND gates are programmable. That means each AND gate has both normal and complemented inputs of variables. So, based on the requirement, we can program any of those inputs. So, we can generate only the required **product terms** by using these AND gates.

Here, the inputs of OR gates are also programmable. So, we can program any number of required product terms, since all the outputs of AND gates are applied as inputs to each OR gate. Therefore, the outputs of PAL will be in the form of **sum of products form**.

Example

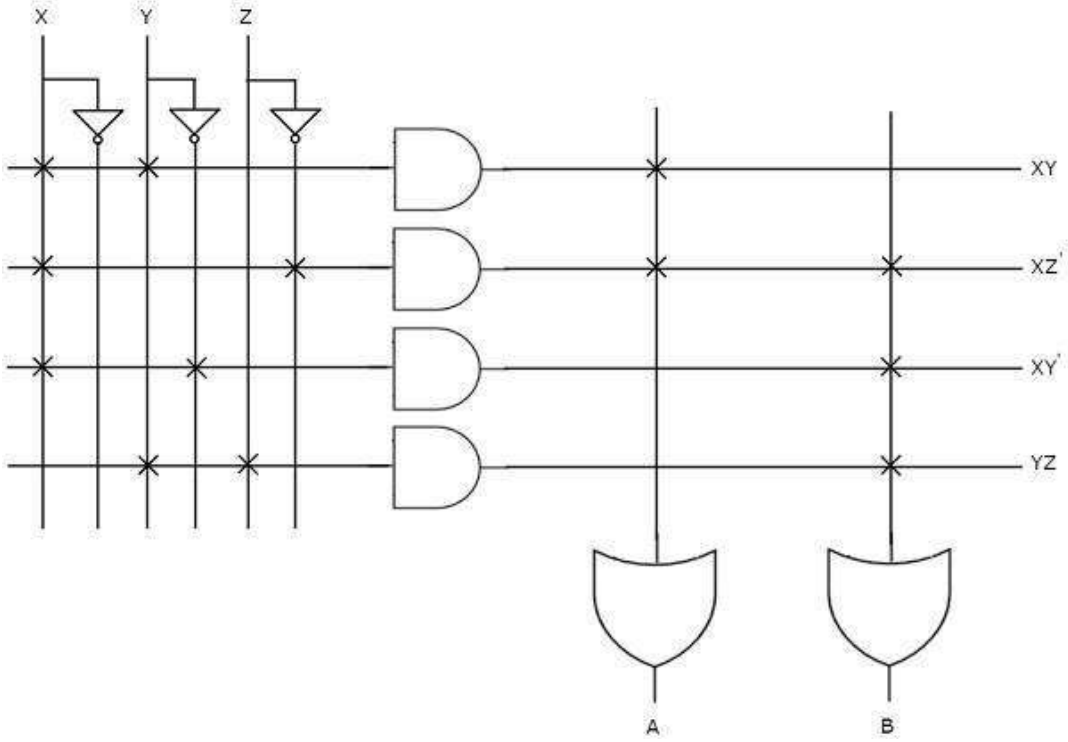
Let us implement the following **Boolean functions** using **PLA**.

$$A=XY+XZ'$$

$$B=XY'+YZ+XZ'$$

The given two functions are in sum of products form. The number of product terms present in the given Boolean functions A & B are two and three respectively. One product term, Z′XZ′X is common in each function.

So, we require four programmable AND gates & two programmable OR gates for producing those two functions. The corresponding **PLA** is shown in the following figure.



The **programmable AND gates** have the access of both normal and complemented inputs of variables. In the above figure, the inputs X, X′X′, Y, Y′Y′, Z & Z′Z′, are available at the inputs of each AND gate. So, program only the required literals in order to generate one product term by each AND gate.

All these product terms are available at the inputs of each **programmable OR gate**. But, only program the required product terms in order to produce the respective Boolean functions by each OR gate. The symbol ‘X’ is used for programmable connections.

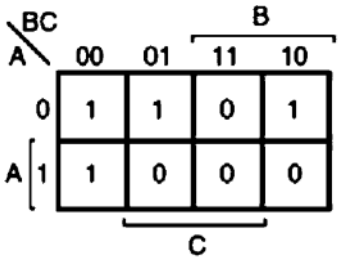
Solved Examples:

1. Implement the combinational circuit having the shown truth table, using PLA.

A	*B*	*C*	F_1	F_2
0	0	0	1	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

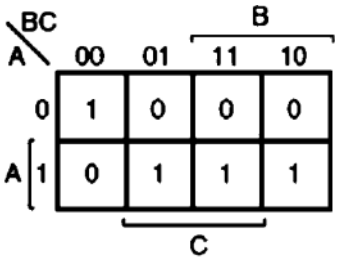
Soln:

Each product term in the expression requires an AND gate. To minimize the cost, it is necessary to simplify the function to a minimum number of product terms.



$F_1 = \overline{A}\,\overline{B} + \overline{A}\,\overline{C} + \overline{B}\,\overline{C}$

$\overline{F}_1 = AB + AC + BC$



$F_2 = AB + AC + \overline{A}\,\overline{B}\,\overline{C}$

$\overline{F}_2 = \overline{A}\,\overline{C} + \overline{A}\,B + A\,\overline{B}\,\overline{C}$

Designing using a PLA, a careful investigation must be taken in order to reduce the distinct product terms. Both the true and complement forms of each function should be simplified to see which one can be expressed with fewer product terms and which one provides product terms that are common to other functions.

The combination that gives a minimum number of product terms is,

$F_1 = AB + AC + BC$ or $F_1 = (AB + AC + BC)'$

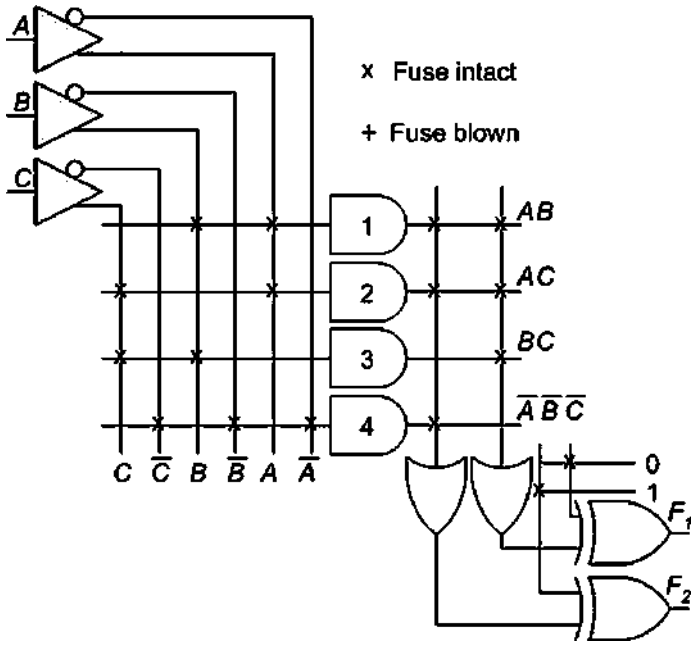
F2 = AB + AC + A'B'C'

This gives only 4 distinct product terms: AB, AC, BC, and A'B'C'. So the PLA table will be as follows,

PLA programming table

	Product term	Inputs A B C	Outputs (C) F_1	Outputs (T) F_2
AB	1	1 1 –	1	1
AC	2	1 – 1	1	1
BC	3	– 1 1	1	–
$\overline{A}\,\overline{B}\,\overline{C}$	4	0 0 0	–	1

For each product term, the inputs are marked with 1, 0, or – (dash). If a variable in the product term appears in its normal form (unprimed), the corresponding input variable is marked with a 1. A 1 in the Inputs column specifies a path from the corresponding input to the input of the AND gate that forms the product term. A 0 in the Inputs column specifies a path from the corresponding complemented input to the input of the AND gate. A dash specifies no connection.



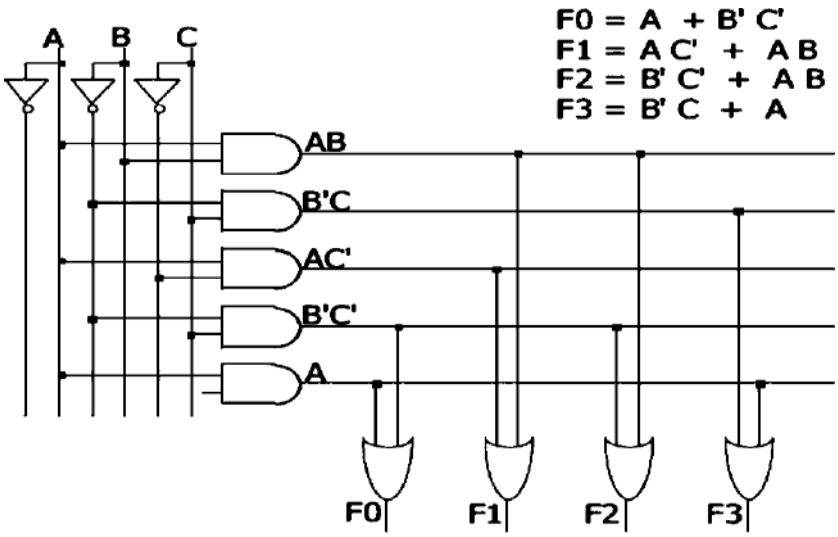
The appropriate fuses are blown and the ones left intact form the desired paths. It is assumed that the open terminals in the AND gate behave like a 1 input. In the Outputs column, a T (true) specifies that the other input of the corresponding XOR gate can be connected to 0, and a C (complement) specifies a connection to 1.

Note that output F_1 is the normal (or true) output even though a C (for complement) is marked over it. This is because F_1' is generated with AND-OR circuit prior to the output XOR. The output XOR complements the function F_1' to produce the true F_1 output as its second input is connected to logic 1.

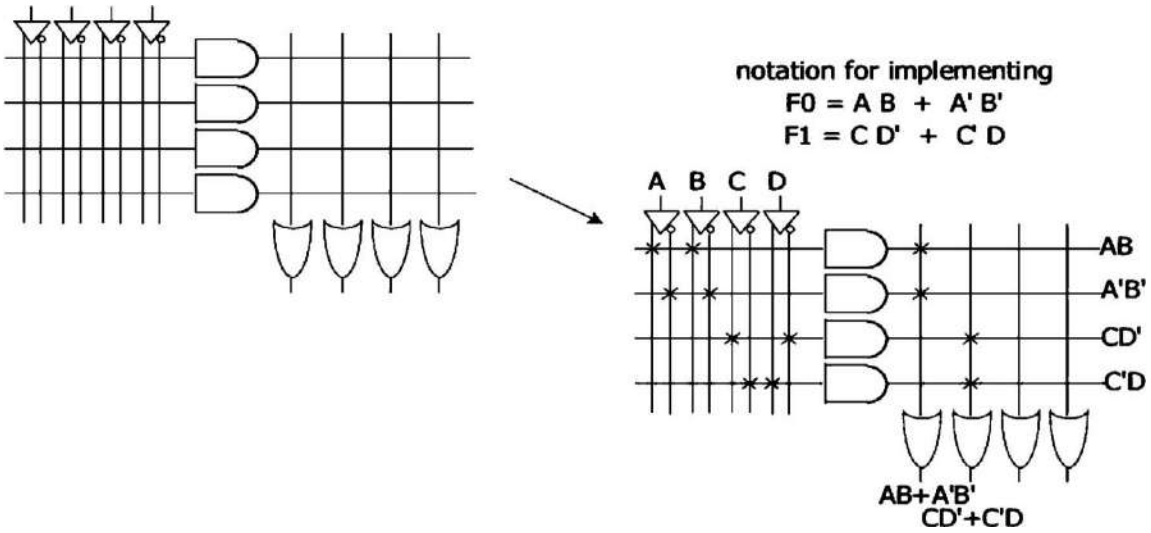
2. All possible connections are available before programming as follows,

F0 = A + B'C' F1 = AC' + AB F2 = B'C' + AB F3 = B'C +A

Soln:



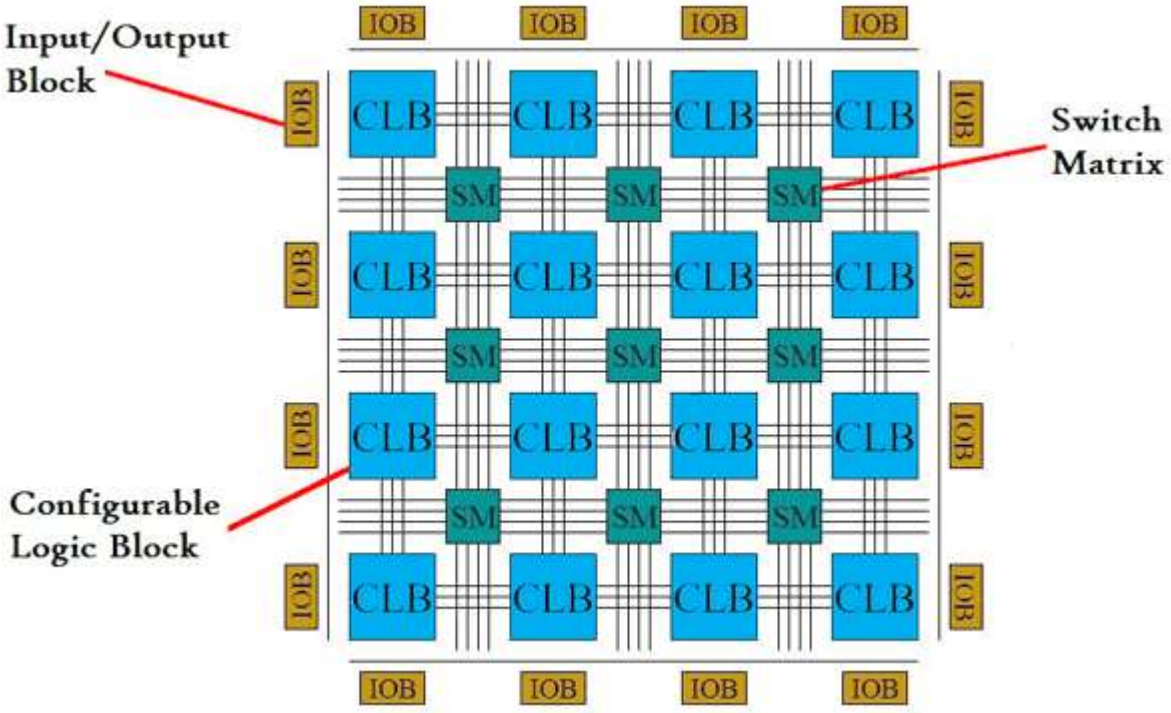
Unwanted connections are blown in the fuse (normally connected, break the unwanted ones) and in the anti-fuse (normally disconnected, make the wanted ones) after programming for the given example as follows,



FIELD PROGRAMMABLE GATE ARRAYS (FPGAs)

A Field Programmable Gate Array has an entire logic system integrated on a single chip. It offers excellent flexibility for reprogramming to the system designers. Logic circuitry involving more than a thousand gates use FPGAs. Compared to a normal custom system chip, the FPGA has ten times better integration density.

An FPGA has a regular structure of logic cells or modules and interlinks which is under the developers and designers complete control. The FPGA is built with mainly three major blocks such as **Configurable Logic Block (CLB), I/O Blocks or Pads and Switch Matrix/ Interconnection Wires**.

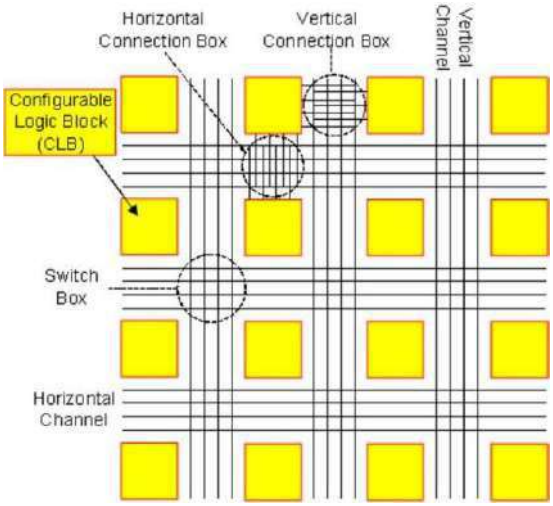


FPGA Architecture

- **CLB (Configurable Logic Block):** These are the basic cells of FPGA. It consists of one 8-bit function generator, two 16-bit function generators, two registers (flip-flops or latches), and reprogrammable routing controls (multiplexers). The CLBs are applied to implement other designed function and macros. Each CLBs have inputs on each side which makes them flexile for the mapping and partitioning of logic.

- **I/O Pads or Blocks:** The Input/Output pads are used for the outside peripherals to access the functions of FPGA and using the I/O pads it can also communicate with FPGA for different applications using different peripherals.
- **Switch Matrix/ Interconnection Wires:** Switch Matrix is used in FPGA to connect the long and short interconnection wires together in flexible combination. It also contains the transistors to turn on/off connections between different lines.

The FPGA consists of 3 main structures:
1. Programmable logic structure,
2. Programmable routing structure, and
3. Programmable Input/Output (I/O).



Programmable Logic Structure:

The programmable logic structure FPGA consists of a 2-dimensional array of configurable logic blocks (CLBs). These logic blocks have a lookup table in which the sequential circuitry is implemented. Each CLB can be configured (programmed) to implement any Boolean function of its input variables. Typically CLBs have between 4-6 input variables.

Functions of larger number of variables are implemented using more than one CLB. In addition, each CLB typically contains 1 or 2 FFs to allow implementation of sequential logic.

Large designs are partitioned and mapped to a number of CLBs with each CLB configured (programmed) to perform a particular function. These CLBs are then connected together to fully implement the target design. Connecting the CLBs is done using the FPGA programmable routing structure.

Configurable Logic Blocks (CLBs):

Look-up Table (LUT)-Based CLB: The basic unit of look-up table based FPGAs is the configurable logic block. The configurable logic block implements the logic functions. The look-up table based FPGA is the Xilinx 4000-series FPGA. Further, configurable logic block implements functions.

PLA-Based CLB:

PLA-based FPGA devices are based on conventional PLDs. The important advantage of this structure is the logic circuits are implemented using only a few level logic. To improve integration density logic expander is used.

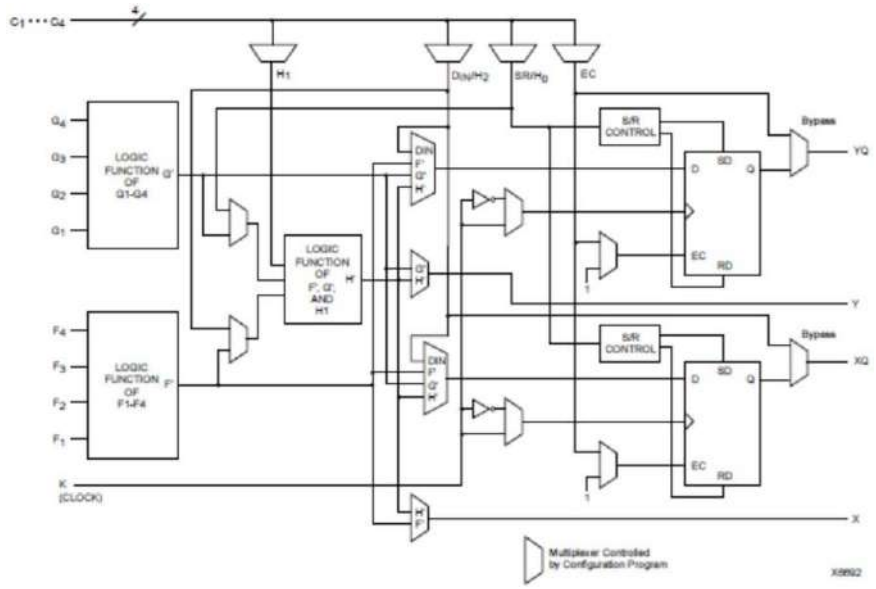
Multiplexer-Based CLB:

In Multiplexer-based FPGAs to implement the logic circuits the multiplexers are used. The main advantage of multiplexer-based FPGA is to provide more functionality by using minimum transistors. Due to large number of inputs, multiplexer-based FPGAs place high demands on routing.

CASE STUDY: Xilinx 4000 FPGA Family:

The principle CLB elements are shown in following figure. Each CLB contains a pair of flip-flops and two independent 4-input function generators. These function generators have a good deal of flexibility as most combinatorial logic functions need less than four inputs. Thirteen CLB inputs and four CLB outputs provide access to the functional flip-flops.

Configurable Logic Blocks implement most of the logic in an FPGA. Two 4-input function generators (F and G) offer unrestricted versatility. Most combinatorial logic functions need four or fewer inputs. However, a third function generator (H) is provided. The H function generator has three inputs. One or both of these inputs can be the outputs of F and G; the other input(s) are from outside the CLB. The CLB can therefore implement certain functions of up to nine variables, like parity check or expandable-identity comparison of two sets of four inputs.



Each CLB contains two flip-flops that can be used to store the function generator outputs. However, the flip-flops and function generators can also be used independently. DIN can be used as a direct input to either of the two flip-flops. H1 can drive the other flip-flop through the H function generator. Function generator outputs can also be accessed from outside the CLB, using two outputs independent of the flip-flop outputs. This versatility increases logic density and simplifies routing. Thirteen CLB inputs and four CLB outputs provide access to the function generators and flip-flops. These inputs and outputs connect to the programmable interconnect resources outside the block.

Four independent inputs are provided to each of two function generators (F1 - F4 and G1 - G4). These function generators, whose outputs are labelled F' and G', are each capable of implementing any arbitrarily defined Boolean function of four inputs. The function generators are implemented as memory look-up tables. The propagation delay is therefore independent of the function implemented. A third function generator, labelled H', can implement any Boolean function of its three inputs. Two of these inputs can optionally be the F' and G' functional

generator out-puts. Alternatively, one or both of these inputs can come from outside the CLB (H2, H0). The third input must come from outside the block (H1).

Signals from the function generators can exit the CLB on two outputs. F' or H' can be connected to the X output. G' or H' can be connected to the Y output. A CLB can be used to implement any of the following functions:

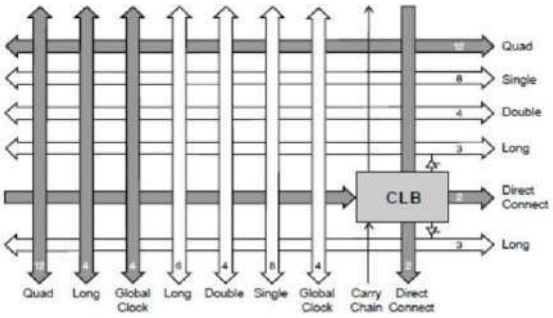
- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables.
- Any single function of five variables.
- Any function of four variables together with some functions of six variables.
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased density and speed. The versatility of the CLB function generators significantly improves system speed. In addition, the design software tools can deal with each function generator independently. This flexibility improves cell usage. The flexibility and symmetry of the CLB architecture facilitates the placement and routing of a given application. Since the function generators and flip-flops have independent inputs and outputs, each can be treated as a separate entity during placement to achieve high packing density. Inputs, outputs and the functions themselves can freely swap positions within the CLB to avoid routing congestion during the placement and routing operation.

Programmable Routing Structure:

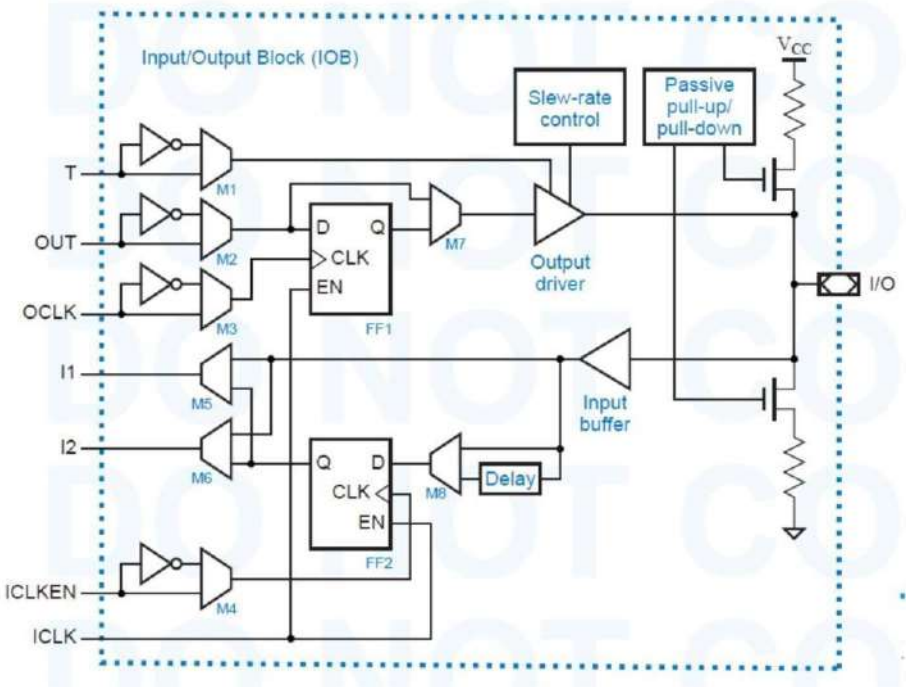
To allow for flexible interconnection of CLBs, FPGAs have 3 programmable routing resources:

1. Vertical and horizontal routing channels which consist of different length wires that can be connected together if needed. These channel run vertically and horizontally between columns and rows of CLBs as shown in the Figure.
2. Connection boxes, which are a set of programmable links that can connect input and output pins of the CLBs to wires of the vertical or the horizontal routing channels.
3. Switch boxes, located at the intersection of the vertical and horizontal channels. These are a set of programmable links that can connect wire segments in the horizontal and vertical channels.



Programmable I/O:

These are mainly buffers that can be configured either as input buffers, output buffers or input/output buffers. They allow the pins of the FPGA chip to function either as input pins, output pins or input/output pins. The IOBs provide a simple interface between the internal user logic and the package pins.



Input Signals:

Two paths, labelled I1 and I2, bring input signals into the array. Inputs also connect to an input register that can be programmed as either an edge-triggered flip-flop or a level sensitive transparent-Low latch.

The choice is made by placing the appropriate primitive from the symbol library. The inputs can be globally configured for either TTL (1.2V) or CMOS (2.5V) thresholds. The two global adjustments of input threshold and output level are independent of each other. There is a slight hysteresis of about 300mV.Seperate clock signals are provided for the input and output registers; these clocks can be inverted, generating either falling-edge or rising edge triggered flip-flops.

As is the case with the CLB registers, a global set/reset signal can be used to set or clear the input and output registers whenever the RESET net is alive.

Registered Inputs:

The I1 and I2 signals that exit the block can each carry either the direct or registered input signal. The input and output storage elements in each IOB have a common clock enable input, which through configuration can be activated individually for the input or output flip-flop or both. This clock enable operates exactly like the EC pin on the XC4000E CLB. It cannot be inverted within the IOB.

UNIT – V VHDL
RTL Design – combinational logic – Sequential circuit – Operators – Introduction to Packages – Subprograms – Test bench. (Simulation /Tutorial Examples: adders, counters, flip flops, Multiplexers & De multiplexers).

INTRODUCTION

VHDL stands for Very high-speed integrated circuit Hardware Description Language. It is a programming language used to model a digital system by dataflow, behavioral and structural style of modeling. This language was first introduced in 1981 for the department of Defense (DoD) under the VHSIC program.

DESCRIBING A DESIGN

In VHDL an entity is used to describe a hardware module. An entity can be described using,

- Entity declaration
- Architecture body
- Package declaration
- Package body
- Configuration

ENTITY DECLARATION

It defines the names, input output signals and modes of a hardware module.

Syntax:

```
entity entity-name is
port (
port-names: mode data-type;
port-names : mode data-type ;
port-names : mode data-type
...
);
end entity-name ;
```

An entity declaration should start with ‘entity’ and end with ‘end’ keywords. The direction will be input, output or inout.

In	Port can be read
Out	Port can be written
Inout	Port can be read and written
Buffer	Port can be read and written, it can have only one source.

ARCHITECTURE BODY

Architecture can be described using structural, dataflow, behavioral or mixed style.

Syntax:

```
architecture arch-name of entity-name is
        declarations;
begin
       concurrent  statement;
       concurrent statement ;
       concurrent statement ;
... end arch-name ;
```

The first line of the architecture body shows the name of the body and the corresponding entity. An architecture body may include an optional declarative section, which consists of the declarations of some objects, such as signals and constants, which are used in the architecture description.

Data Flow Modeling

In this modeling style, the flow of data through the entity is expressed using concurrent (parallel) signal. The concurrent statements in VHDL are WHEN and GENERATE.

Besides them, assignments using only operators (AND, NOT, +, *, sll, etc.) can also be used to construct code.

Finally, a special kind of assignment, called BLOCK, can also be employed in this kind of code.

In concurrent code, the following can be used;

- Operators
- The WHEN statement (WHEN/ELSE or WITH/SELECT/WHEN);
- The GENERATE statement;
- The BLOCK statement

Behavioral Modeling

In this modeling style, the behavior of an entity as set of statements is executed sequentially in the specified order. Only statements placed inside a PROCESS, FUNCTION, or PROCEDURE are sequential.

PROCESSES, FUNCTIONS, and PROCEDURES are the only sections of code that are executed sequentially.

However, as a whole, any of these blocks is still concurrent with any other statements placed outside it.

One important aspect of behavior code is that it is not limited to sequential logic. Indeed, with it, we can build sequential circuits as well as combinational circuits.

The behavior statements are IF, WAIT, CASE, and LOOP. VARIABLES are also restricted and they are supposed to be used in sequential code only. VARIABLE can never be global, so its value cannot be passed out directly.

Structural Modeling

In this modeling, an entity is described as a set of interconnected components. A component instantiation statement is a concurrent statement. Therefore, the order of these

statements is not important. The structural style of modeling describes only an interconnection of components (viewed as black boxes), without implying any behavior of the components themselves nor of the entity that they collectively represent.

In Structural modeling, architecture body is composed of two parts − the declarative part (before the keyword begin) and the statement part (after the keyword begin).

OPERATORS

Operators are means for constructing expressions.

Syntax:

adding_operator ::= **+** | **-** | **&**

+	Addition
-	Subtraction
&	Concatenation

logical_operator ::= **and** | **or** | **nand** | **nor** | **xor** | **xnor**

miscellaneous_operator ::= ****** | **abs** | **not**

**	Exponentiation
Abs	Absolute value

multiplying_operator ::= ***** | **/** | **mod** | **rem**

*	Multiplication
/	Division
mod	Modulus
rem	Remainder

relational_operator ::= **=** | **/=** | **<** | **<=** | **>** | **>=**

=	Equality
/=	Inequality
<	Ordering „less than”
<=	Ordering „less than or equal”
>	Ordering „greater than”
>=	Ordering „greater than or equal”

shift_operator ::= **sll** | **srl** | **sla** | **sra** | **rol** | **ror**

sll	Shift left logical
srl	Shift right logical
sla	Shift left arithmetic

sra	Shift right arithmetic
rol	Rotate left logical
ror	Rotate right logical

Description

VHDL has a wide set of different operators, which can be divided into groups of the same precedence level (priority). The table below lists operators grouped according to priority level, highest priority first.

Table shows the Operator priority

miscellaneous operators	****** | **abs** | **not**
multiplying operators	***** | **/** | **mod** | **rem**
sign operators	**+** | **-**
adding operators	**+** | **-** | **&**
shift operators	**sll** | **srl** | **sla** | **sra** | **rol** | **ror**
relational operators	= | /= | < | <= | > | >=
logical operators	**and** | **or** | **nand**| **nor** | **xor** | **xnor**

The expressions are evaluated form left to right, operations with higher precedence are evaluated first. If the order should be different from the one resulting from this rule, parentheses can be used (Example 1).

Example 1

```
v := a + y * x;
```

The multiplication y*x is carried out first, then a is added to the result of multiplication. This is because the multiplication operator has higher level of priority than the adding operator.

Example 2

```
variable We1, We2, We3, Wy : BIT := '1';
Wy := We1 and We2 xnor We1 nor We3;
```

For the initial value of the variables We1, We2, We3 equal to '1', the result is assigned to the variable Wy and is equal to '0'.

Example 3

variable Zm1: REAL := 100.0;
variable Zm2 : BIT_VECTOR(7 **downto** 0) := ('0','0','0','0','0','0','0','0');
variable Zm3, Zm4 : BIT_VECTOR(1 **to** 0);
Zm1 /= 342.54 -- True
Zm1 = 100.0 -- True
Zm2 /= ('1', '0', '0', '0', '0', '0', '0', '0') -- True
Zm3 = Zm4 -- True

Example 4

Zm1 > 42.54 -- True
Zm1 >= 100.0 -- True
Zm2 < ('1', '0', '0', '0', '0', '0', '0', '0') -- True
Zm3 <= Zm2 – True

Example 5

variable Zm5 : BIT_VECTOR(3 **downto** 0) := ('1','0','1','1');
Zm5 **sll** 1 -- ('0', '1', '1', '0')
Zm5 **sll** 3 -- ('1', '0', '0', '0')
Zm5 **sll** -3 -- Zm5 srl 3
Zm5 **srl** 1 -- ('0', '1', '0', '1')
Zm5 **srl** 3 -- ('0', '0', '0', '1')
Zm5 **srl** -3 -- Zm5 sll 3
Zm5 **sla** 1 -- ('0', '1', '1', '1')
Zm5 **sla** 3 -- ('1', '1', '1', '1')
Zm5 **sla** -3 -- Zm5 sra 3
Zm5 **sra** 1 -- ('1', '1', '0', '1')
Zm5 **sra** 3 -- ('1', '1', '1', '1')
Zm5 **sra** -3 -- Zm5 sla 3
Zm5 **rol** 1 -- ('0', '1', '1', '1')
Zm5 **rol** 3 -- ('1', '1', '0', '1')
Zm5 **rol** -3 -- Zm5 ror 3
Zm5 **ror** 1 -- ('1', '1', '0', '1')
Zm5 **ror** 3 -- ('0', '1', '1', '1')
Zm5 **ror** -3 -- Zm5 rol 3

Example 6

constant B1: BIT_VECTOR := "0000"; -- four element array
constant B2: BIT_VECTOR := "1111"; -- four element array
constant B3: BIT_VECTOR := B1 & B2; -- eight element array, ascending
-- direction, value "00001111"
subtype BIT_VECTOR_TAB **is** BIT_VECTOR (1 **downto** 0);
constant B4: BIT_VECTOR_TAB := "01";
constant B5: BIT_VECTOR:= B4 & B2; -- six element array, descending

-- direction, value "011111"
constant B6 : BIT := '0' ;
constant B7 : BIT_VECTOR := B2 & B6;-- five element array, ascending
-- direction, value "11110"
constant B8: BIT := '1';
constant B9: BIT_VECTOR := B6 & B8; -- two element array, ascending
-- direction value "01"
Example 7
z := x * (-y) -- A legal expression
z := x / (**not** y) -- A legal expression

The same expressions without parentheses would be illegal.

Example 7

variable A,B :Integer;
variable C : Real;
C:= 12.34 * (234.4 / 43.89);
A:= B **mod** 2;

Example 8

2 ** 8 = 256
3.8 ** 3 = 54.872
4 ** (-2) = 1 / (4**2) = 0.0625

Libraries and Packages in VHDL

Built-in Libraries and Packages in VHDL programs are;

```
library ieee;

use ieee.std_logic_1164.all;

use ieee.std_logic_signed.all;
```

The packages are "std_logic_1164" and "std_logic_signed" and the library is "ieee". Since the "scope" of the library statement extends over the entire file, it is not necessary to repeat that for the second package.

It's instructive to show where the packages are physically located. For Altera Max+2 and Xilinx Foundation these locations typically are:

Altera: ~\maxplus2\vhdl93\ieee\std1164.vhd

Xilinx: ~\fndtn\synth\lib\packages\ieee\src\std_logic_1164.vhd

It is thus tempting to come to the conclusion that the "library ieee;" statement indicates the "directory" in which the std_logic_1164 package is located. Note, however, where it is in Synplicity:

Synplicty: ~\synplcty\LIB\vhd\std1164.vhd

In the latter there is no mention of "ieee" at all. It is thus more appropriate to think of "ieee" as a *pointer* to the location of the package. The directory structure shown in those three examples depicts the directories where the packages are loaded when the software is installed. The pointer "ieee" is hardcoded in the compilers and thus there is no need for the user to associate that pointer with the directory structure, nor is it possible to put the packages anywhere else after the software has been loaded.

The files "std1164.vhd" (Altera and Synplicty) and "std_logic_1164.vhd" (Xilinx) show a close resemblance to the package name as given in the "use" statement, but apparently they don't have to be the same as the package name. The actual *package* is in those files and shows up in there as the following statement:

```
package std_logic_1164 is
```

which is identical for all three .vhd files. That statement is reminiscent of the entity statement and indeed, a package is also considered a design unit, similar to an entity and an architecture.

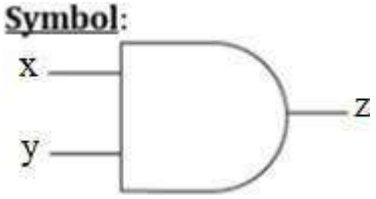
The pertinent excerpt from that file is shown below:

```
package STD_LOGIC_SIGNED is

            function "+"(L: STD_LOGIC_VECTOR; R: STD_LOGIC_VECTOR) return

            STD_LOGIC_VECTOR;

            -- other similar function definitions

end STD_LOGIC_SIGNED;

package body STD_LOGIC_SIGNED is

            function "+"(L: STD_LOGIC_VECTOR; R: STD_LOGIC_VECTOR) return
            STD_LOGIC_VECTOR is

constant length: INTEGER := maximum(L'length, R'length);

variable result : STD_LOGIC_VECTOR (length-1 downto 0);

begin

                  result := SIGNED(L) + SIGNED(R); return
                  std_logic_vector(result);

end;
```

VHDL Programming for Logic Gates:

VHDL Code for AND GATE

Symbol:

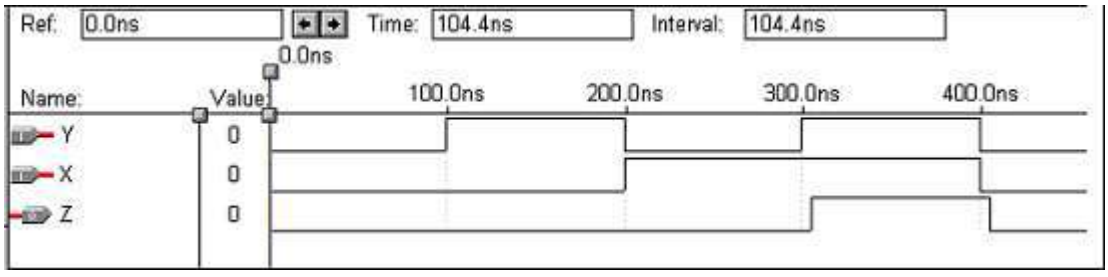


X	y	Z
0	0	0
0	1	0
1	0	0
1	1	1

VHDL Code:

```
Library ieee;
use ieee.std_logic_1164.all;

entity and1 is
  port(x,y:in bit ; z:out bit);
end and1;

architecture dataflow of and1 is
begin
  z<=x and y;
end dataflow;
```

Waveforms



VHDL Code for OR GATE

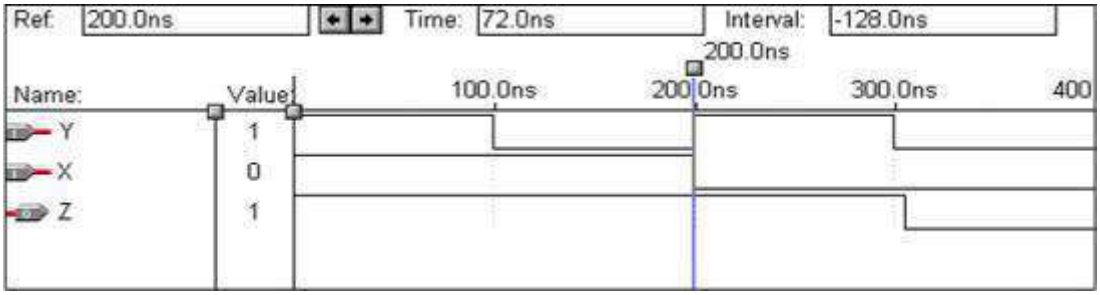
Symbol:

X	y	z
0	0	0
0	1	1
1	0	1
1	1	1

VHDL Code:

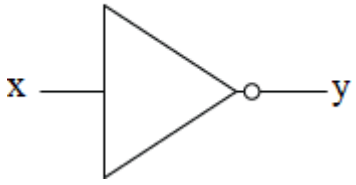
```
Library ieee;
use ieee.std_logic_1164.all;

entity or1 is
  port(x,y:in bit ; z:out bit);
end or1;

architecture dataflow of or1 is
begin
  z<=x or y;
end dataflow;
```

Waveforms



VHDL Code for NOT GATE

Symbol :



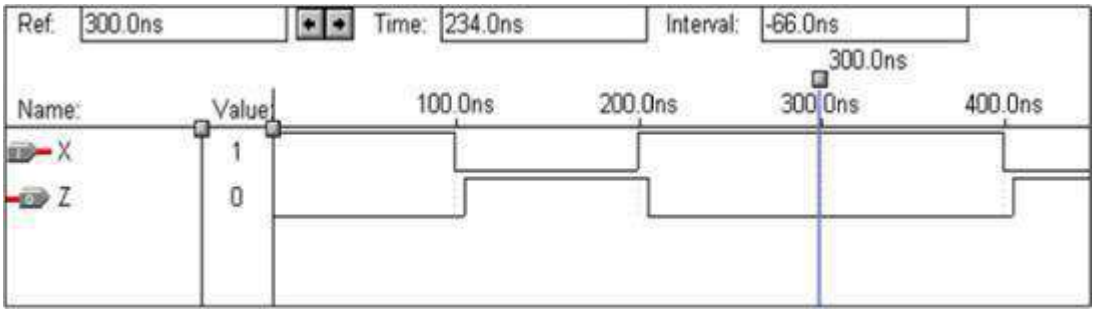
X	Y
0	1
1	0

VHDL Code:

```
Library ieee;
use ieee.std_logic_1164.all;
```

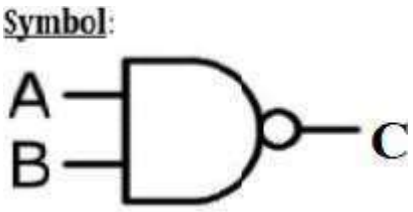
```
entity not1 is
  port(x:in bit ; y:out bit);
end not1;

architecture dataflow of not1 is
begin
  y<=not x;
end dataflow;
```

Waveforms



VHDL Code for NAND GATE

Symbol:



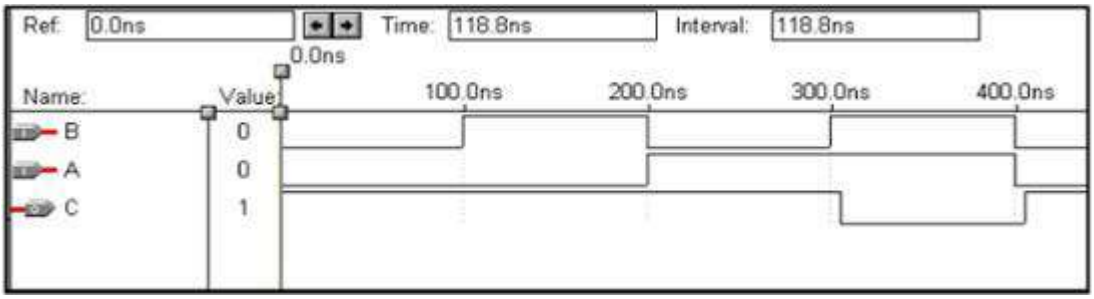
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

VHDL Code:

```
Library ieee;
use ieee.std_logic_1164.all;

entity nand1 is
  port(a,b:in bit ; c:out bit);
end nand1;

architecture dataflow of nand1 is
begin
  c<=a nand b;
```

```
end dataflow;
```

Waveforms



VHDL Code for NOR GATE

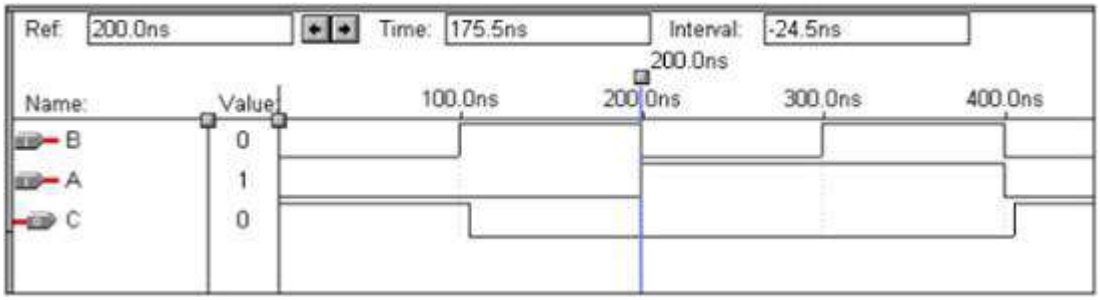
Symbol:

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

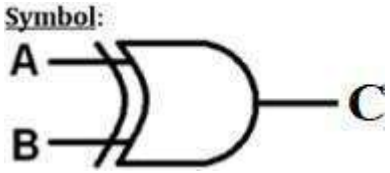
VHDL Code:

```
Library ieee;
use ieee.std_logic_1164.all;

entity nor1 is
  port(a,b:in bit ; c:out bit);
end nor1;

architecture dataflow of nor1 is
begin
  c<=a nor b;
end dataflow;
```

Waveforms



VHDL Code for XOR GATE

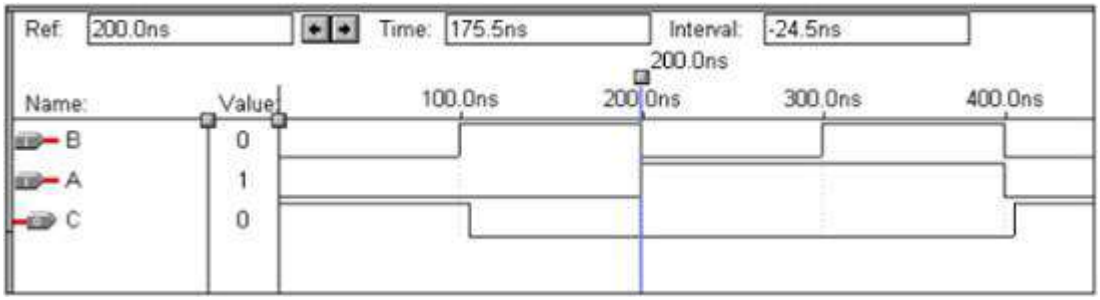


A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

VHDL Code:

```
Library ieee;
use ieee.std_logic_1164.all;

entity xor1 is
  port(a,b:in bit ; c:out bit);
end xor1;

architecture dataflow of xor1 is
begin
  c<=a xor b;
end dataflow;
```

Waveforms



VHDL Code for X-NOR GATE

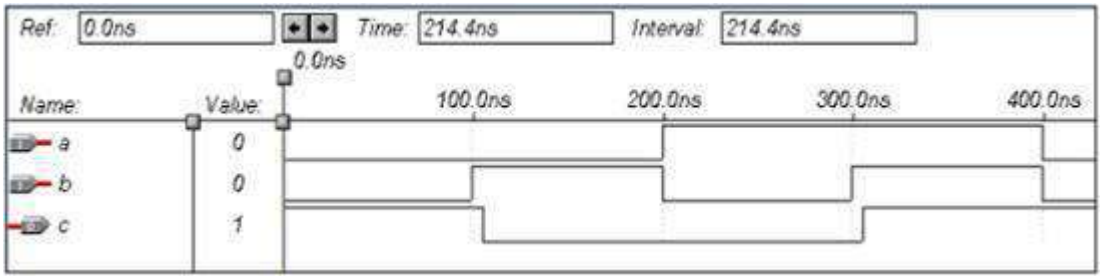
Symbol:

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

VHDL Code:

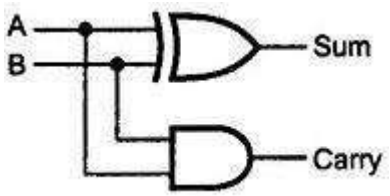
```
Library ieee;
use ieee.std_logic_1164.all;

entity xnor1 is
  port(a,b:in bit ; c:out bit);
end xnor1;

architecture dataflow of xnor1 is
begin
  c<=not(a xor b);
end dataflow;
```

Waveforms



VHDL Programming for Combinational Circuits:

Logic Diagram for a Half-Adder

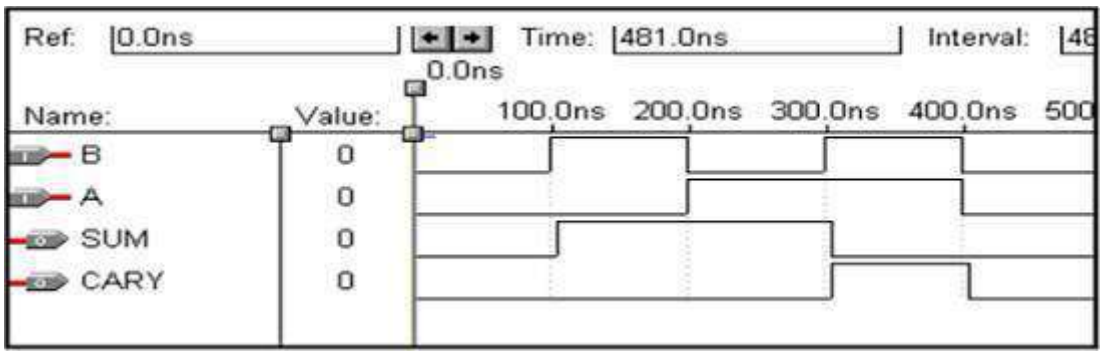


VHDL Code for a Half-Adder

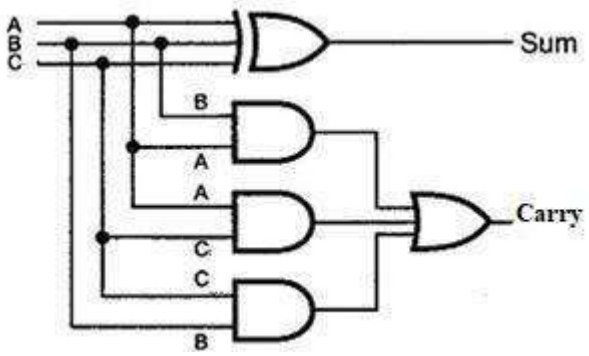
VHDL Code:

```
Library ieee;
use ieee.std_logic_1164.all;

entity half_adder is
  port(a,b:in bit; sum,carry:out bit);
end half_adder;

architecture data of half_adder is
begin
  sum<= a xor b;
  carry <= a and b;
end data;
```

Waveforms



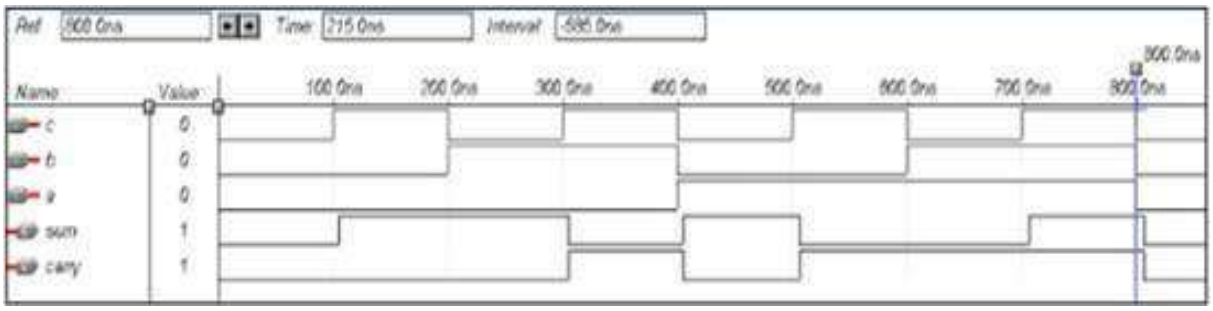
Logic Diagram for a Full Adder



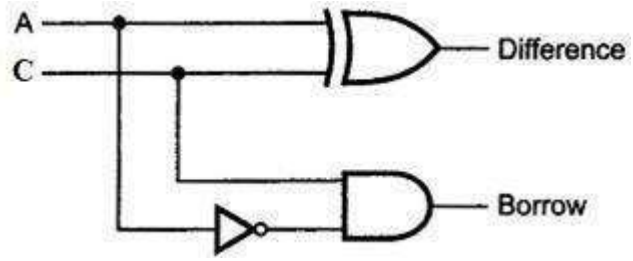
VHDL Code for a Full Adder

```
Library ieee;
use ieee.std_logic_1164.all;

entity full_adder is port(a,b,c:in bit; sum,carry:out bit);
end full_adder;

architecture data of full_adder is
begin
  sum<= a xor b xor c;
  carry <= ((a and b) or (b and c) or (a and c));
end data;
```

Waveforms



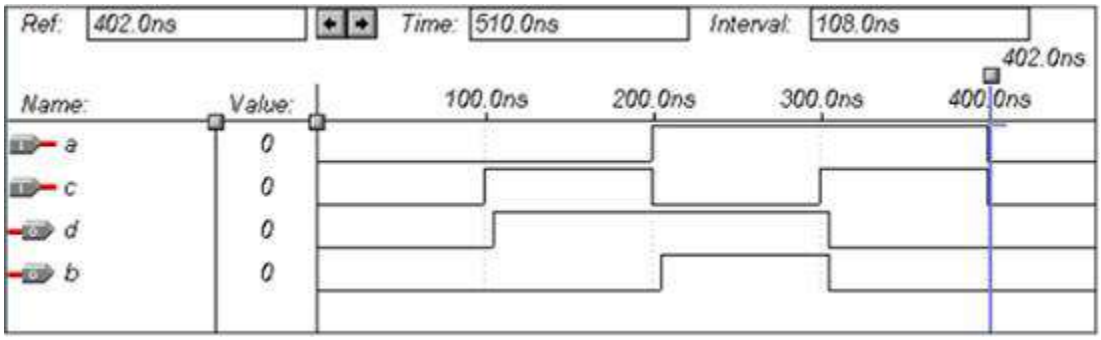
Logic Diagram for a Half-Subtractor



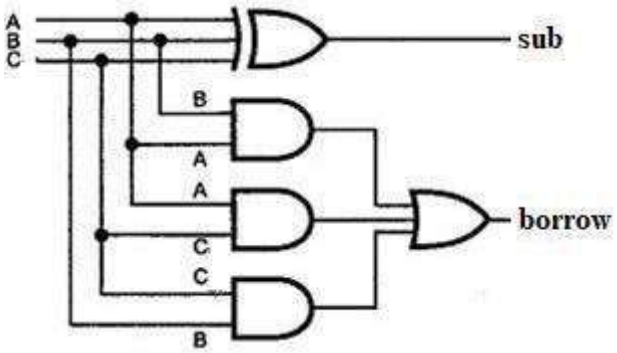
VHDL Code for a Half-Subtractor

```
Library ieee;
use ieee.std_logic_1164.all;

entity half_sub is
port(a,c:in bit; d,b:out bit);
end half_sub;

architecture data of half_sub is
begin
d<= a xor c;
b<= (a and (not c));
end data;
```

Waveforms



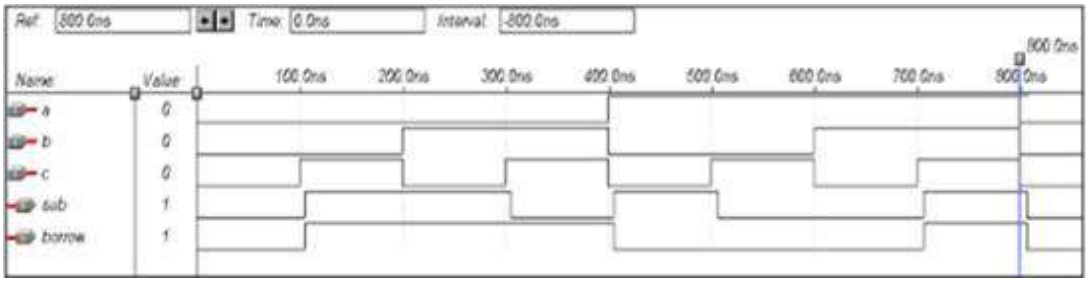
Logic Diagram for a Full Subtractor



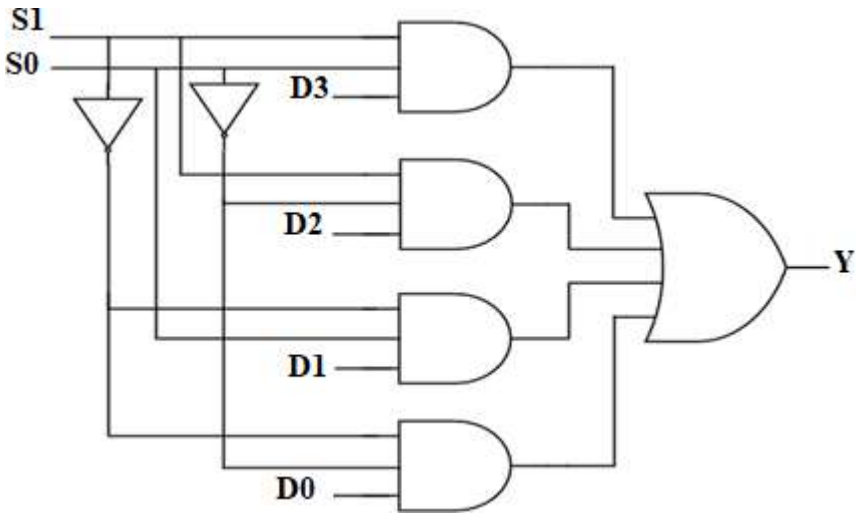
VHDL Code for a Full Subtractor

```
Library ieee;
use ieee.std_logic_1164.all;

entity full_sub is
  port(a,b,c:in bit; sub,borrow:out bit);
end full_sub;

architecture data of full_sub is
begin
  sub<= a xor b xor c;
  borrow <= ((b xor c) and (not a)) or (b and c);
end data;
```

Waveforms



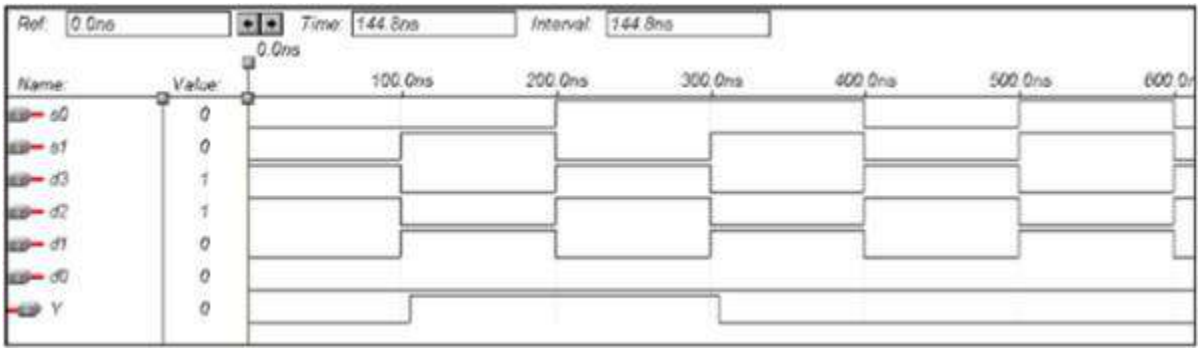
Logic Diagram for a 4 x 1 Multiplexer



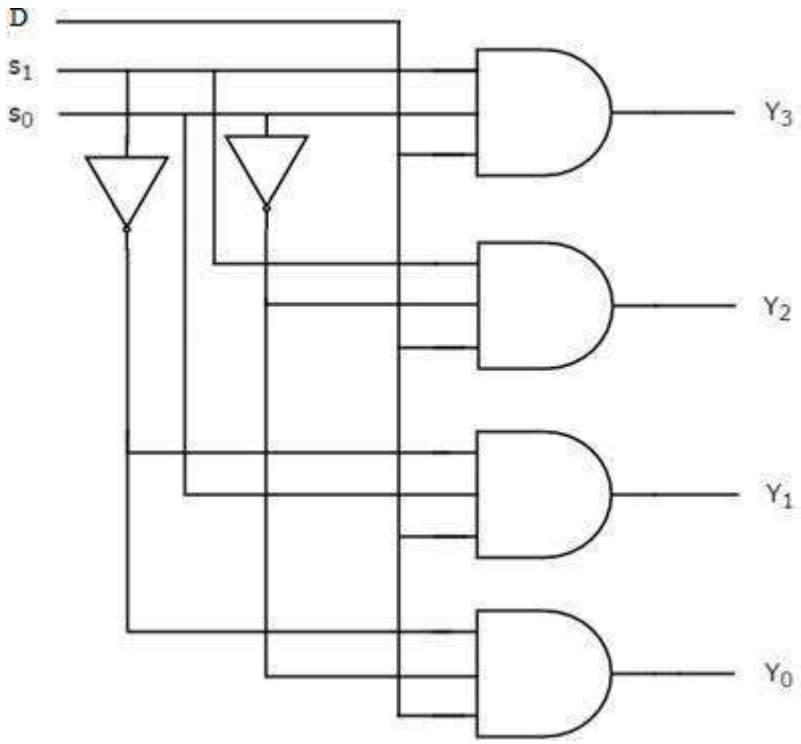
VHDL Code for a Multiplexer

```
Library ieee;
use ieee.std_logic_1164.all;

entity mux is
  port(S1,S0,D0,D1,D2,D3:in bit; Y:out bit);
end mux;

architecture data of mux is
begin
  Y<= (not S0 and not S1 and D0) or
    (S0 and not S1 and D1) or
    (not S0 and S1 and D2) or
    (S0 and S1 and D3);
end data;
```

Waveforms



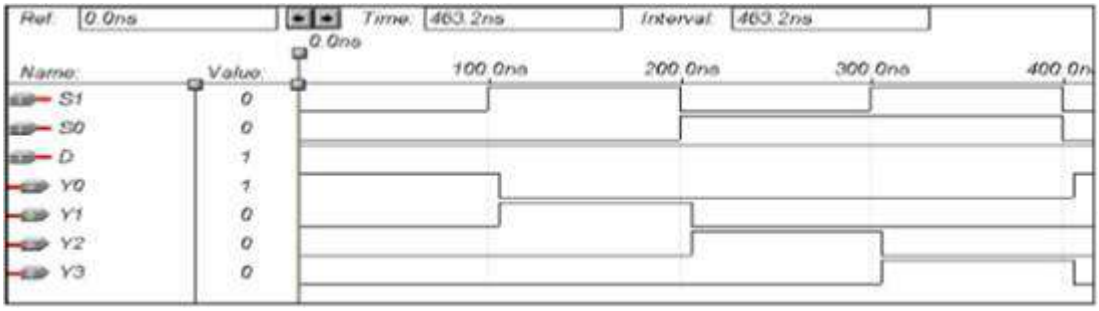
Logic Diagram for a 1 x 4 De-multiplexer



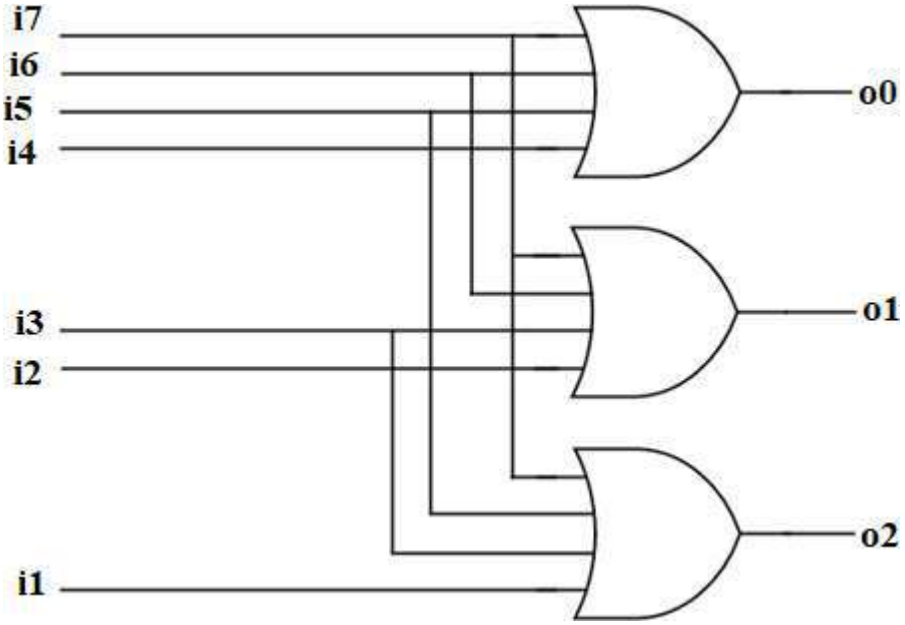
VHDL Code for a De-multiplexer

```
Library ieee;
use ieee.std_logic_1164.all;

entity demux is
  port(S1,S0,D:in bit; Y0,Y1,Y2,Y3:out bit);
end demux;

architecture data of demux is
begin
  Y0<=  ((Not S0) and (Not S1) and D);
  Y1<=  ((Not S0) and S1 and D);
  Y2<=  (S0 and (Not S1) and D);
  Y3<=  (S0 and S1 and D);
end data;
```

Waveforms



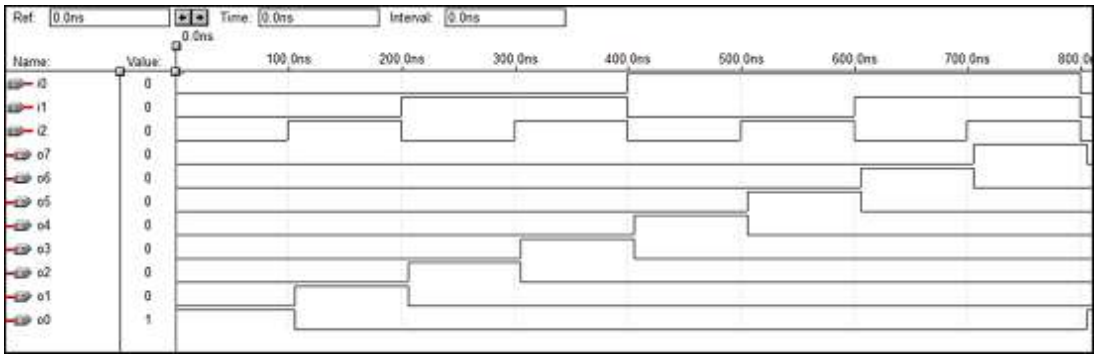
Logic Diagram for a 8 x 3 Encoder



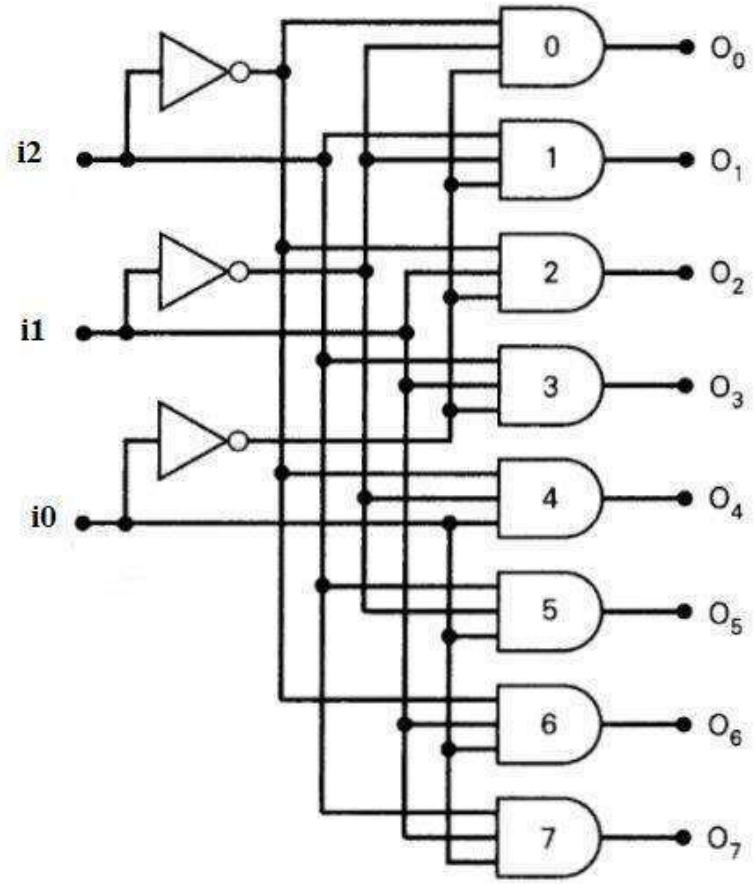
VHDL Code for a 8 x 3 Encoder

```
library ieee;
use ieee.std_logic_1164.all;

entity enc is
  port(i0,i1,i2,i3,i4,i5,i6,i7:in bit; o0,o1,o2: out bit);
end enc;

architecture dataflow of enc is
begin
  o0<=i4 or i5 or i6 or i7;
  o1<=i2 or i3 or i6 or i7;
  o2<=i1 or i3 or i5 or i7;
end dataflow;
```

Waveforms



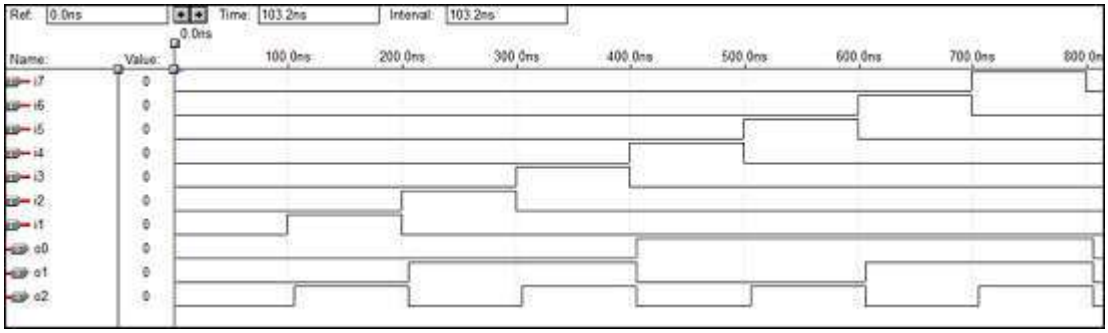
Logic Diagram for a 3 x 8 Decoder



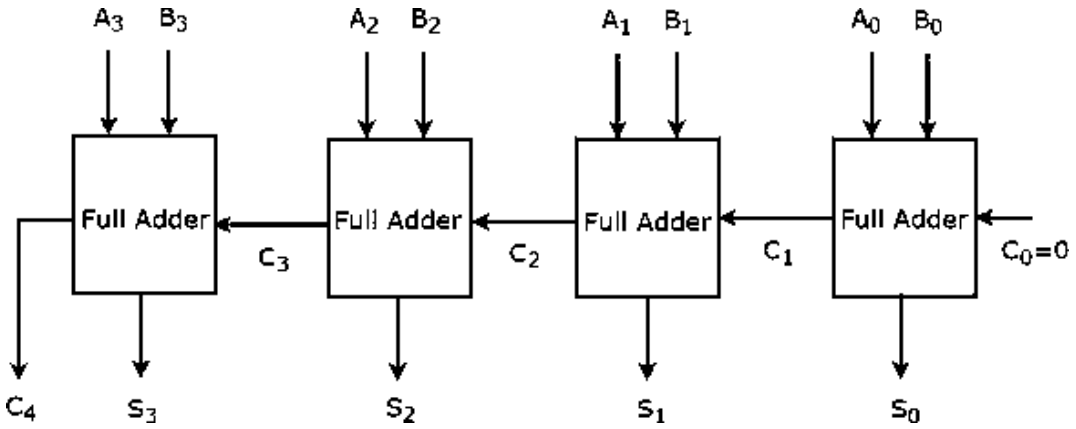
VHDL Code for a 3 x 8 Decoder

```
library ieee;
use ieee.std_logic_1164.all;

entity dec is
  port(i0,i1,i2:in bit; o0,o1,o2,o3,o4,o5,o6,o7: out bit);
end dec;

architecture dataflow of dec is
begin
  o0<=(not i0) and (not i1) and (not i2);
  o1<=(not i0) and (not i1) and i2;
  o2<=(not i0) and i1 and (not i2);
  o3<=(not i0) and i1 and i2;
  o4<=i0 and (not i1) and (not i2);
  o5<=i0 and (not i1) and i2;
  o6<=i0 and i1 and (not i2);
  o7<=i0 and i1 and i2;
end dataflow;
```

Waveforms



Logic Diagram – 4 bit Parallel adder

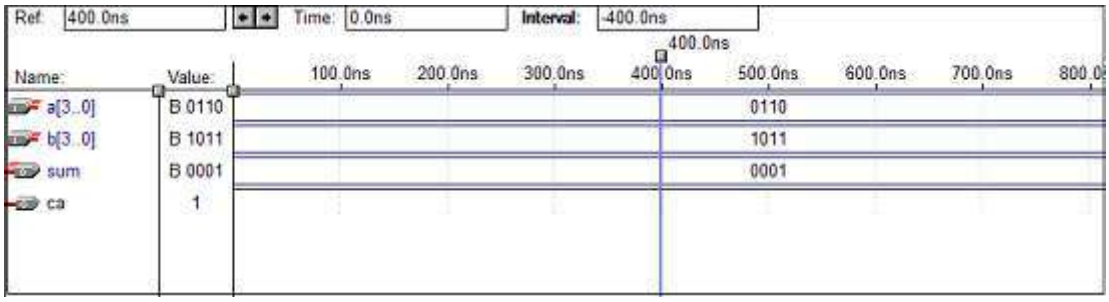


VHDL Code – 4 bit Parallel adder

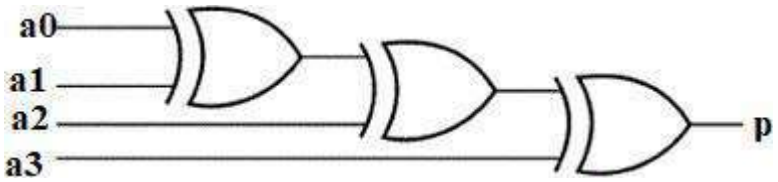
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity pa is
  port(a : in STD_LOGIC_VECTOR(3 downto 0);
    b : in STD_LOGIC_VECTOR(3 downto 0);
    ca : out STD_LOGIC;
    sum : out STD_LOGIC_VECTOR(3 downto 0)
  );
end pa;

architecture dataflow of pa is
  Component fa is
    port (a : in STD_LOGIC;
      b : in STD_LOGIC;
      c : in STD_LOGIC;
      sum : out STD_LOGIC;
      ca : out STD_LOGIC
    );
  end component;
  signal s : std_logic_vector (2 downto 0);
  signal temp: std_logic;
begin
  temp<='0';
  u0 : fa port map (a(0),b(0),temp,sum(0),s(0));
  u1 : fa port map (a(1),b(1),s(0),sum(1),s(1));
```

```
  u2 : fa port map (a(2),b(2),s(1),sum(2),s(2));
  ue : fa port map (a(3),b(3),s(2),sum(3),ca);
end dataflow;
```

Waveforms



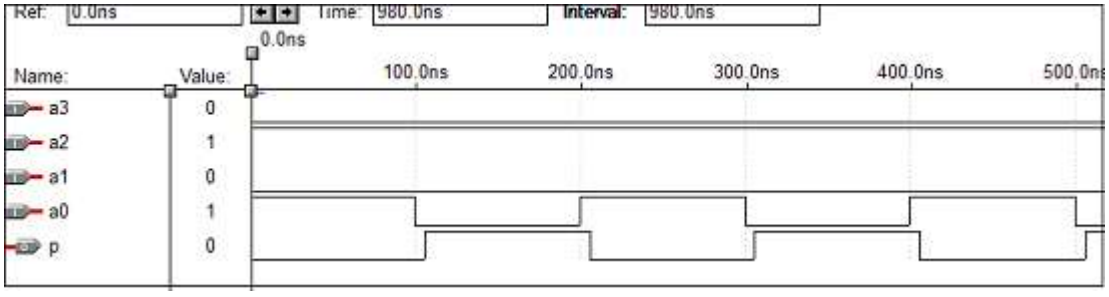
Logic Diagram – 4 bit Parity Checker



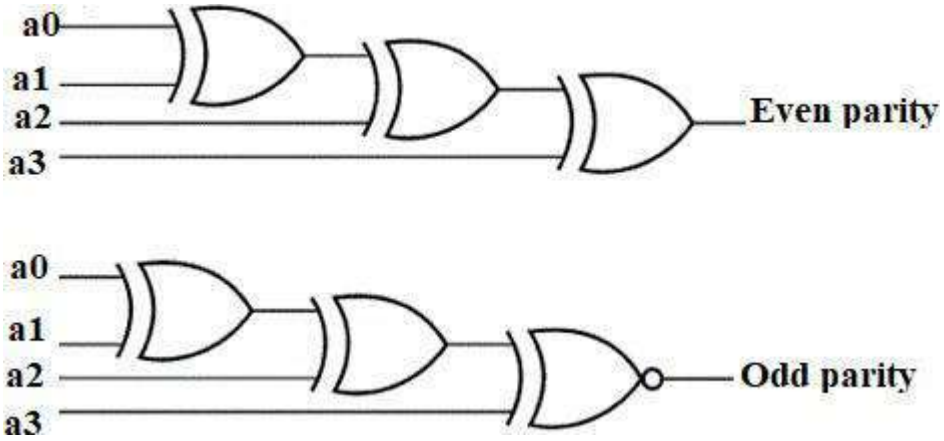
VHDL Code – 4 bit Parity Checker

```
library ieee;
use ieee.std_logic_1164.all;

entity parity_checker is
  port (a0,a1,a2,a3 : in std_logic;
     p : out std_logic);
end parity_checker;

architecture vcgandhi of parity_checker is
begin
  p <= (((a0 xor a1) xor a2) xor a3);
end vcgandhi;
```

Waveforms



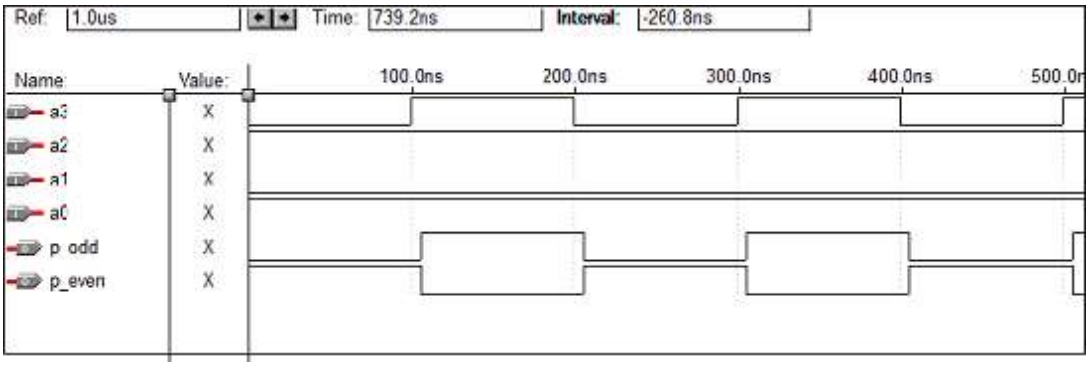
VHDL Code – 4 bit Parity Generator



VHDL Code – 4 bit Parity Generator

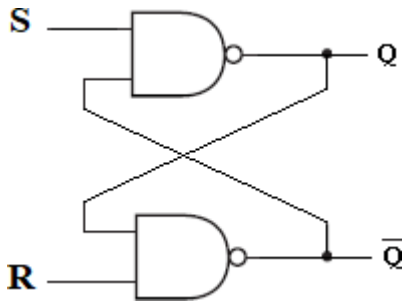
```
library ieee;
use ieee.std_logic_1164.all;

entity paritygen is
  port (a0, a1, a2, a3: in std_logic; p_odd, p_even: out std_logic);
end paritygen;

architecture dataflow of paritygen is
begin
  process (a0, a1, a2, a3)

  if (a0 ='0' and a1 ='0' and a2 ='0' and a3 ='0')
    then odd_out <= "0";
    even_out <= "0";
  else
    p_odd <= (((a0 xor a1) xor a2) xor a3);
    p_even <= not(((a0 xor a1) xor a2) xor a3);
end dataflow
```

Waveforms



VHDL Programming for Sequential Circuits:

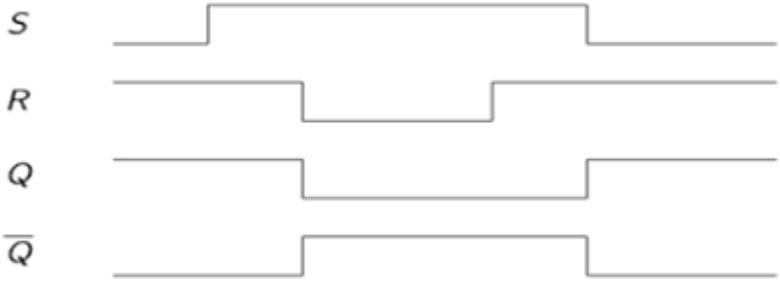
Logic Diagram for an SR Latch



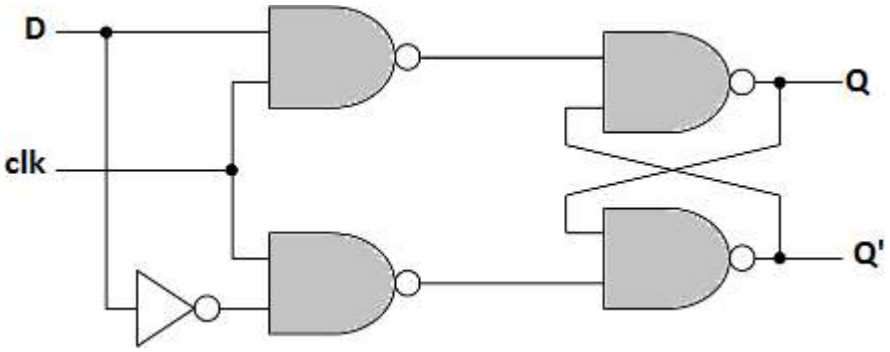
VHDL Code for an SR Latch

```
library ieee;
use ieee.std_logic_1164.all;

entity srl is
  port(r,s:in bit; q,qbar:buffer bit);
end srl;

architecture data of srl is
  signal s1,r1:bit;
begin
  q<= s nand qbar;
  qbar<= r nand q;
end data;
```

Waveforms



Logic Diagram for a D Latch

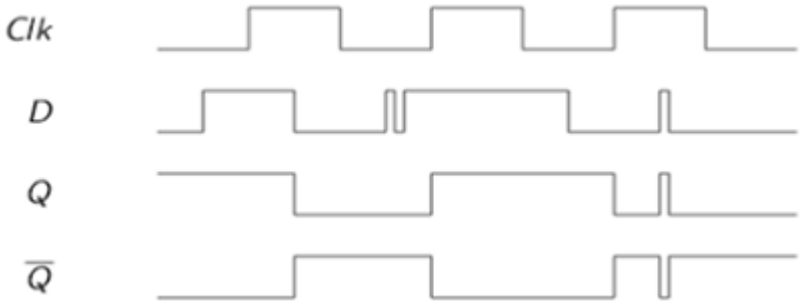


VHDL Code for a D Latch

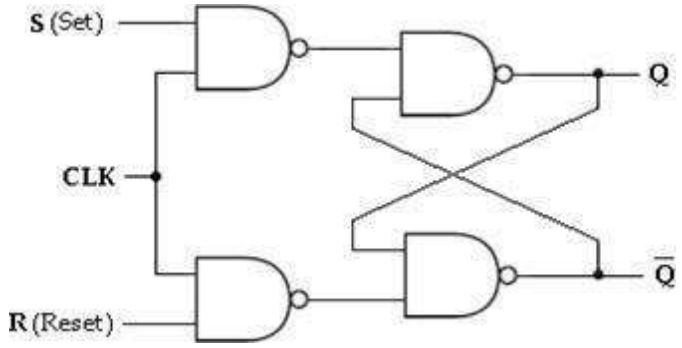
```
library ieee;
```

```
use ieee.std_logic_1164.all;

entity Dl is
  port(d:in bit; q,qbar:buffer bit);
end Dl;

architecture data of Dl is
  signal s1,r1:bit;
begin
  q<= d nand qbar;
  qbar<= d nand q;
end data;
```

Waveforms



Logic Diagram for an SR Flip Flop

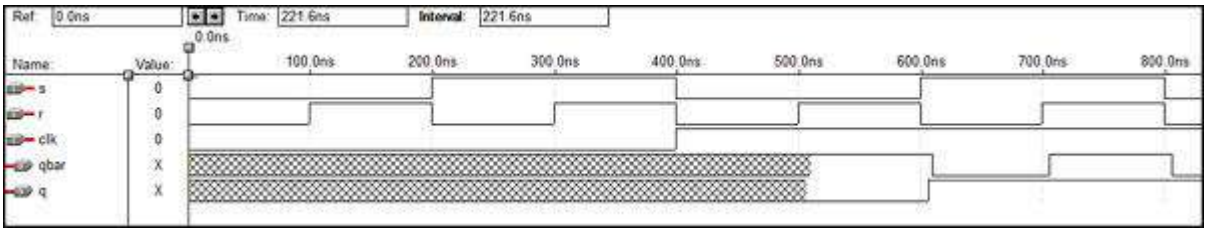


VHDL Code for an SR Flip Flop

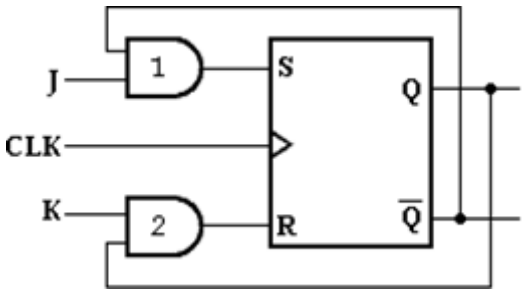
```
library ieee;
use ieee.std_logic_1164.all;

entity srflip is
  port(r,s,clk:in bit; q,qbar:buffer bit);
end srflip;

architecture data of srflip is
  signal s1,r1:bit;
begin
  s1<=s nand clk;
  r1<=r nand clk;
  q<= s1 nand qbar;
```

```
  qbar<= r1 nand q;
end data;
```

Waveforms



Logic Diagram for a JK Flip Flop

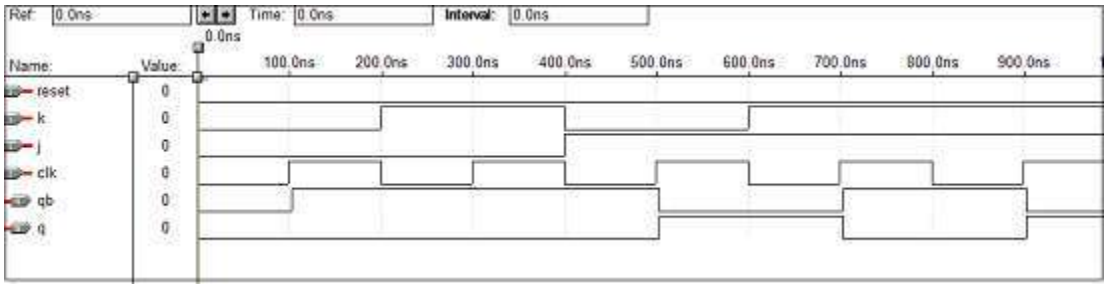


VHDL code for a JK Flip Flop

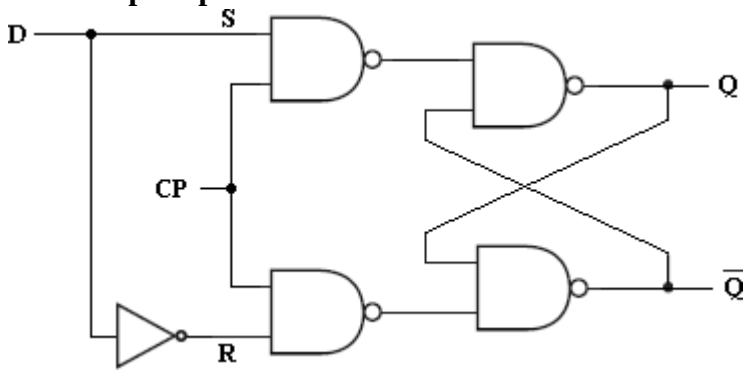
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity jk is
  port(
    j : in STD_LOGIC;
    k : in STD_LOGIC;
    clk : in STD_LOGIC;
    reset : in STD_LOGIC;
    q : out STD_LOGIC;
    qb : out STD_LOGIC
  );
end jk;

architecture data of jk is
begin
  jkff : process (j,k,clk,reset) is
  variable m : std_logic := '0';

  begin
    if (reset = '1') then
      m : = '0';
    elsif (rising_edge (clk)) then
      if (j/ = k) then
        m : = j;
      elsif (j = '1' and k = '1') then
        m : = not m;
      end if;
    end if;
```

```
    q <= m;
    qb <= not m;
  end process jkff;
end data;
```

Waveforms



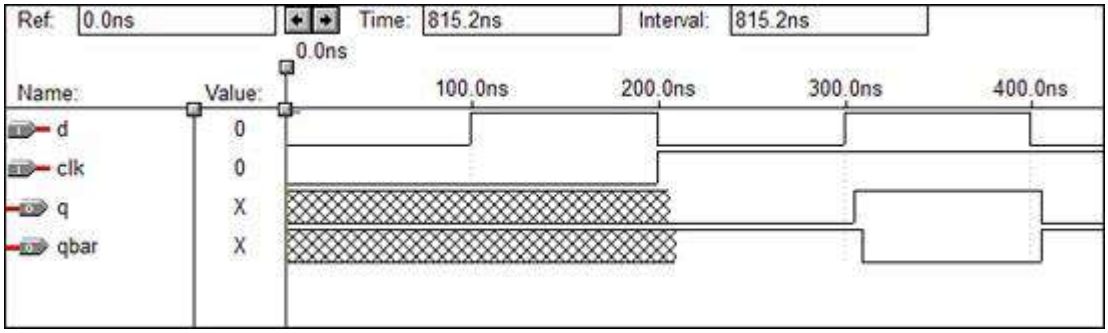
Logic Diagram for a D Flip Flop



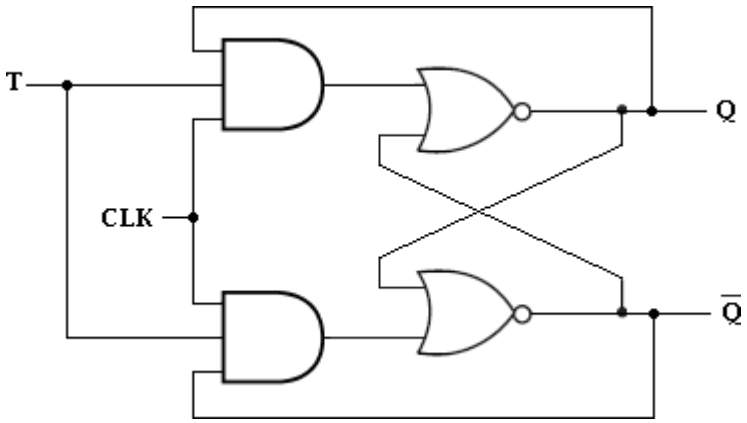
VHDL Code for a D Flip Flop

```
Library ieee;
use ieee.std_logic_1164.all;

entity dflip is
  port(d,clk:in bit; q,qbar:buffer bit);
end dflip;

architecture data of dflip is
  signal d1,d2:bit;
begin
  d1<=d nand clk;
  d2<=(not d) nand clk;
  q<= d1 nand qbar;
  qbar<= d2 nand q;
end data;
```

Waveforms



Logic Diagram for a T Flip Flop

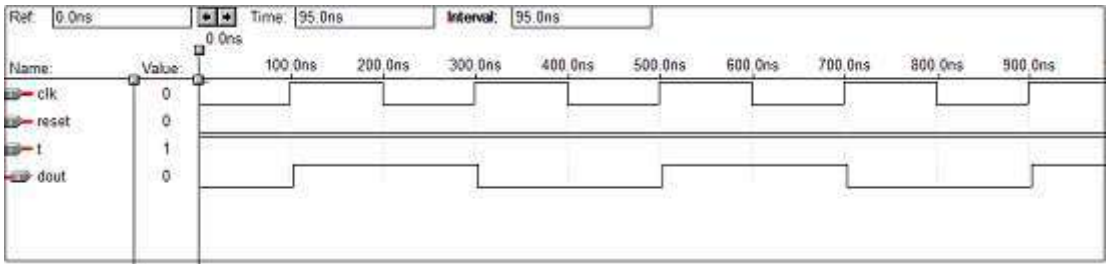


VHDL Code for a T Flip Flop

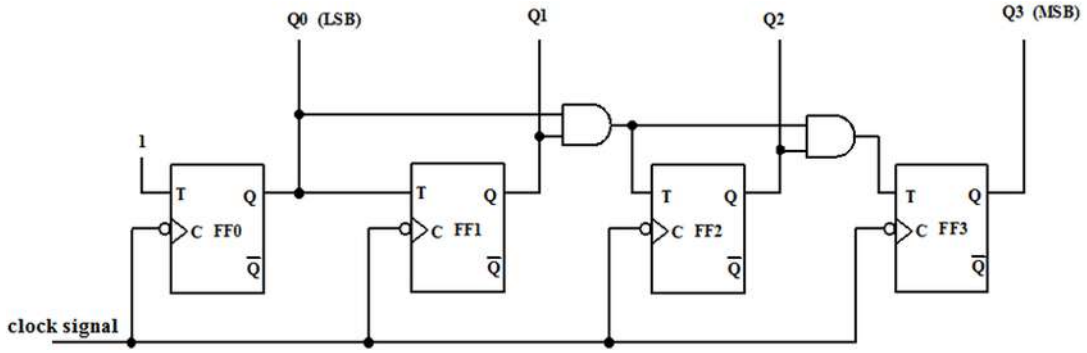
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity Toggle_flip_flop is
  port(
    t : in STD_LOGIC;
    clk : in STD_LOGIC;
    reset : in STD_LOGIC;
    dout : out STD_LOGIC
  );
end Toggle_flip_flop;

architecture data of Toggle_flip_flop is
begin
  tff : process (t,clk,reset) is
  variable m : std_logic : = '0';

  begin
    if (reset = '1') then
      m : = '0';
    elsif (rising_edge (clk)) then
      if (t = '1') then
        m : = not m;
      end if;
    end if;
```

```
    dout < = m;
  end process tff;
end data;
```

Waveforms



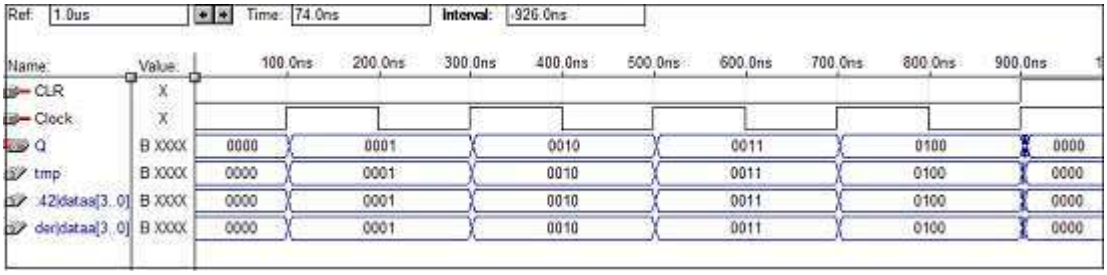
Logic Diagram for a 4 - bit Up Counter



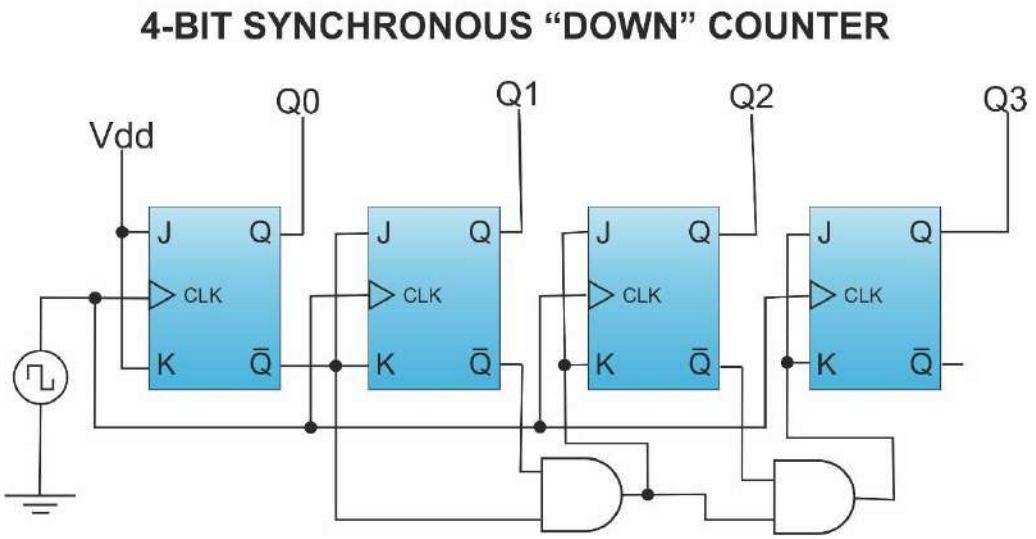
VHDL Code for a 4 - bit Up Counter

```
library IEEE;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity counter is
  port(Clock, CLR : in std_logic;
    Q : out std_logic_vector(3 downto 0)
  );
end counter;

architecture data of counter is
  signal tmp: std_logic_vector(3 downto 0);
begin
  process (Clock, CLR)

  begin
    if (CLR = '1') then
      tmp < = "0000";
    elsif (Clock'event and Clock = '1') then
      mp <= tmp + 1;
    end  if;
  end process;
  Q <= tmp;
end data;
```

Waveforms



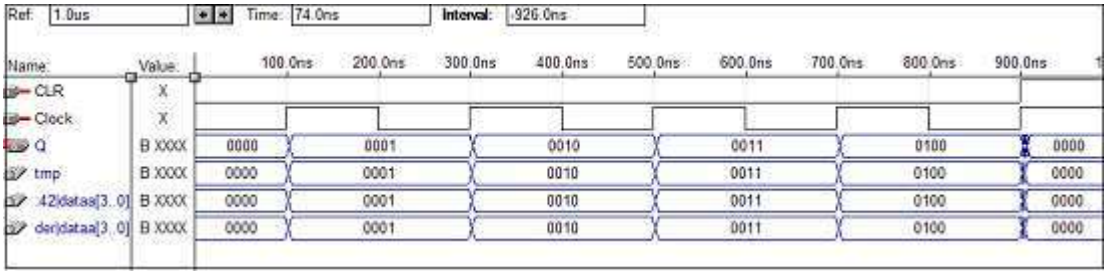
Logic Diagram for a 4-bit Down Counter



VHDL Code for a 4-bit Down Counter

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity dcounter is
  port(Clock, CLR : in std_logic;
    Q : out std_logic_vector(3 downto 0));
end dcounter;

architecture virat of dcounter is
  signal tmp: std_logic_vector(3 downto 0);

begin
  process (Clock, CLR)
  begin
    if (CLR = '1') then
      tmp <= "1111";
    elsif (Clock'event and Clock = '1') then
      tmp <= tmp - 1;
    end  if;
  end process;
  Q <= tmp;
end virat;
```

Waveforms


Ref: 1.0us
Time: 74.0ns
Interval: 926.0ns
Name:
Value:
100.0ns
200.0ns
300.0ns
400.0ns
500.0ns
600.0ns
700.0ns
800.0ns
900.0ns
CLR
X
Clock
X
Q
B XXXX
0000
0001
0010
0011
0100
0000
tmp
B XXXX
0000
0001
0010
0011
0100
0000
42|dataa[3..0]
B XXXX
0000
0001
0010
0011
0100
0000
der|dataa[3..0]
B XXXX
0000
0001
0010
0011
0100
0000

UNIT – I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES		
	PART-A	**Knowledge level**
1.	**How many bits are required to represent the decimal numbers in the range 0 to 999 using Straight binary codes and using BCD codes?** 2^n= maximum value with n bits 2^9=512; 2^{10}=1024; So to represent decimal number in the range 0 to 999 using straight binary code, 10 bits are required. In BCD Code - 1 decimal digit requires 4 bits. So to represent decimal number in the range 0 to 999 using BCD code (3 digits), 12 bits are required.	**BL2**
2.	**Show that the excess-3 code is self-complementing.** **Self-complementing property:** 1's complement of Excess3 code of a decimal digit is equal to Excess-3 code of 9's complement of the corresponding decimal digit. **Example:** Excess -3code of the decimal digit 2= 0101 1's complement of 0101= 1010 ---------- (1) 9's complement of 2 = 9-2 = 7 Excess -3 code of 7 = 1010 ---------- (2) From (1) and (2), 1's complement is equal to 9's complement The self-complementing property of Excess -3 code is proved.	**BL3**
3.	**Determine $(377)_{10}$ in Octal and Hexa-decimal equivalent. (Nov 2014)** 8 | 377 8 | 47 — 1 5 — 7 **$(377)_{10} = (571)_8$** 16 | 377 16 | 23 — 9 1 — 7 **$(377)_{10} = (179)_{16}$**	**BL3**
4.	**Add the decimals 67and 78 using excess-3 code.** $67 = (0110\ \ 0111\ )_{BCD} = (1001\ \ 1010)_{XS-3}$ $78 = (0111\ \ 1000\ )_{BCD} = (1010\ \ 1011)_{XS-3}$ ---------- 0001 0100 0101 → (1) After excess 3 addition, if carry is available after nibble, subtract 3 to the result, Else if no carry after nibble, add 3 to the result. From (1), no carry after each nibble, so adding 3 to each nibble. (1) 0001 0100 0101 0011(+) 0011(+) 0011(+) ---------- $(0100\ \ 0111\ \ 1000)_{XS-3}$	**BL3**
5.	**What is meant by weighted and non-weighted code?** **Weighted codes** are those, which obey the positional weighting principles. In weighed code, each position of the number represents a specific weight. Example:8421 &2421 **Non-Weighted Codes** are codes that are not positionally weighted. Each position of the number is not assigned a fixed value. Example: Excess-3 & Gray code	**BL2**

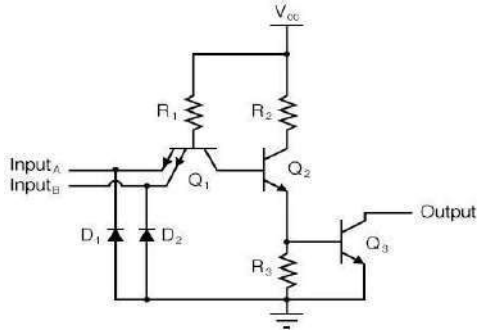
6.	**Add the decimals 57and 68 using 8421 BCD code.** 57 = (0101 0111) 68 = (0110 1000) --- 1011 1111 → (1) After BCD addition, if nibble is greater than 9, add 6, else if nibble is less than 9, subtract 6 for each nibble. From (1) each nibble is greater than 9, hence adding 6 to each nibble (1) 1011 1111(+) 0110 0110 --- (0001 0010 0101)	**BL3**
7.	**What is Gray code &mention the advantages and application of Gray code (Nov 2017)** The gray code is non-weighted code, which means that there are no specific weights assigned to the bit positions. In gray code, only one bit changes from one number to the next. **Advantages of Gray Code:** Switching activity is reduced because of one digit change in consequence code words. Low power consumption, Fast response & Minimum error in coding are the advantages of gray code. **Application:** Shaft position encoder in which analog data are represented by continuous change of a shaft position. The shaft is partitioned into segments, and each segment is assigned a number.	**BL1**
8.	**Convert the following hexadecimal numbers into decimal numbers:263 and 1C3 (Nov 2022)** $263_H = 2x16^2+6x16^1+3x16^0=(611)$**10** $1C3_H=1x16^2+12x16^1+3x16^0=(451)$**10**	**BL3**
9.	**i) Convert $(11001010)_2$ into gray code. ii) (11101101) gray code into binary code. (Nov 2021)** (i) 11001010 to gray code 1 1 0 0 1 0 1 0 ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ 1 0 1 0 1 1 1 1 $(11001010)_2 = (10101111)_{gray}$ (ii) 11101101 to binary 1 1 1 0 1 1 0 1 ↓ (+) ↓ (+) ↓ (+) ↓ (+) ↓ (+) ↓ (+) ↓ (+) ↓ 1 0 1 1 0 1 1 0 1 0 1 1 0 1 1 0 $(11101101)_{gray} = (10110110)_2$	**BL3**
10.	**Convert: a)$(475.25)_8$to its decimal equivalent &b)$(549.B4)_{16}$to its binary equivalent (Apr 2015)** **a) $(475.25)_8$to its decimal equivalent** $(475.25)_8 = 4 \times 8^2 + 7 \times 8^1 + 5 \times 8^0 + 2 \times 8^{-1} + 5 \times 8^{-2}$ $(475.25)_8 = 4 \times 64 + 7 \times 8 + 5 \times 1 + 2 \times 0.125 + 5 \times 0.0156 = 317.25$ **$(475.25)_8=(317.25)_{10}$**	**BL3**

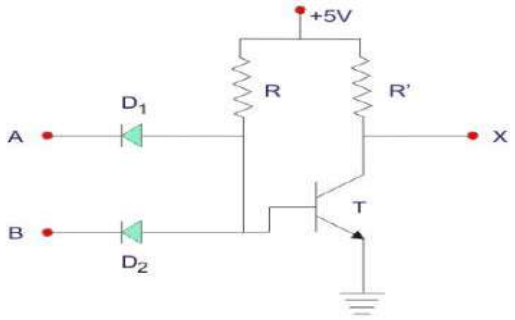
	b) $(549.B4)_{16}$ to its binary equivalent 5 4 9 . B 4 0101 0100 1001 1011 0100 **$(549.B4)_{16}$** = $(010101001001.10110100)_2$	
11.	**What is unit distance code? Give an example. (Nov 2015)** Unit distance code is a non-weighted code in which next increment or decrement causes the bit transition only at one place. Ex: Gray code.	**BL1**
12.	**Convert the following binary code into gray code 1010111000_2. (May 2016)** 1 + 0 + 1 + 0 + 1 + 1 + 1 + 0 + 0 + 0 ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ 1 1 1 1 1 0 0 1 0 0 $(1010111000)_2$= $(1111100100)_{gray}$	**BL3**
13.	**Convert $(115)_{10}$ and $(235)_{10}$ to hexadecimal numbers. (Nov 2017)** 16 | 115 16 | 7 — 3 0 — 7 **$(115)_{10}$= $(73)_{16}$** 16 | 235 16 | 14 — B 0 — E **$(235)_{10}$= $(BE)_{16}$**	**BL3**
14.	**Convert the following Excess 3 numbers into decimal numbers. (Nov 2016)** a) 1011 - 0011 ------ 1000 = $(8)_{10}$ b) 1001 0011 0111 - 0011 0011 0011 ---------- 0100 0000 0100 = $(404)_{10}$	**BL3**
15.	**Convert 143_{10} into its binary and binary coded decimal equivalent. (Nov 2022)** 2 | 143 2 | 71 — 1 2 | 35 — 1 2 | 17 — 1 2 | 8 — 1 2 | 4 — 0 2 | 2 — 0 1 — 0 **In binary, $(143)_{10}$= $(1000\ 1111)_2$** **In BCD, $(143)_{10}$= $(0001\ 0100\ 0011)_{BCD}$**	**BL3**
16.	**Perform subtraction on the following unsigned binary numbers using 2's complement of subtrahend (a) 11011- 11001 (b) 110100- 10101.** **a) 11011- 11001** 1's complement of 11001 =00110 2's Complement of 11001 = (1's complement of 11001+1) 2's Complement of 11001 =00111 Add 00111 with 11011 1 1 1 1 1 1 0 1 1 0 0 1 1 1 (+) ------- **1** 0 0 0 1 0 (Eliminate the carry, 2's compliment) Ans =11011-11001 =00010	**BL3**

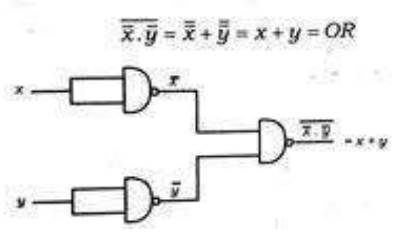
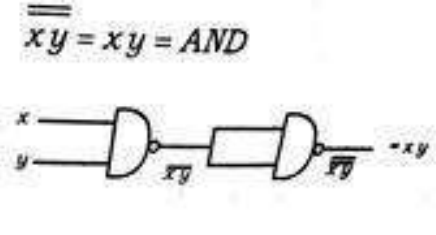
	b)110100- 10101 1's complement of 010101 =101010 2's Complement of 010101=101010+1=101011 Add 101011 with 110100 1 1 0 1 0 0 (+) 1 0 1 0 1 1 - - - - - - - - - - - **1** 0 1 1 1 1 1 (Eliminate Carry) Ans = 011111	
17.	**Convert $(101.01)_2$ to decimal number. (April 2019)** $(101.01)_2 = [(1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0) + (0 \times 2^{-1}) + (1 \times 2^{-2})]_{10}$ $(101.01)_2 = 5.25_{10}$.	**BL3**
18.	**Give each one example for error detecting code and error correcting code. (April 2019)** Error detection codes are used to detect the errors present in the received data bit stream. These codes contain some parity bits which are appended to the original data bit stream. It detects the error, if it occurrs during transmission of the data bit stream. Examples: Parity code, Hamming code. Error correction Codes are used to correct the errors present in the received data bit stream. Error correction codes also use the similar strategy of error detection codes. Example − Hamming code.	**BL1**
19.	**A 16-bit data word given by 1001100001110110 is to be transmitted by using a fourfold repetition code. If the data word is broken into four blocks of four bits each, then write the transmitted bitstream. (Nov 2020 ,May 2021)** A 16-bit data word given by 1001100001110110 is to be transmitted by using a fourfold repetition code. If the data word is broken into four blocks of four bits each, then the transmitted bit stream is 1001 1001 1001 1001 1000 1000 1000 1000 0111 0111 0111 0111 0110 0110 0110 0110	**BL3**
20.	**Give the classification of logic families.** The classifications of logic families are (i) Saturated Logic Family (ii)Non Saturated Logic Family **Saturated Logic Family** | **Non-Saturated Logic Family** Register Transistor Logic(RTL) | Schottky TTL Diode Transistor Logic (DTL) | Emitter Coupled Logic(ECL) Transistor Transistor Logic (TTL) |	**BL2**
21.	**Mention the important characteristics of digital IC's?** The important characteristics of digital IC's are Fan out, Power dissipation, Propagation Delay, Noise Margin, Fan In, Operating temperature and Power supply requirements.	**BL1**
22.	**Define Fan- In and Fan-Out? (Nov 2015, May 2016)** Fan- In is the number of inputs connected to the gate without any degradation in the voltage level. Fan-Out is defined as the maximum number of inputs of several gates that can be driven by the output of logic gate maintaining its output levels within the specified limits.	**BL1**
23.	**What is propagation delay? (Apr 2015)** Propagation delay is the average transition delay time for the signal to propagate from input to the output. It is expressed in ns.	**BL1**

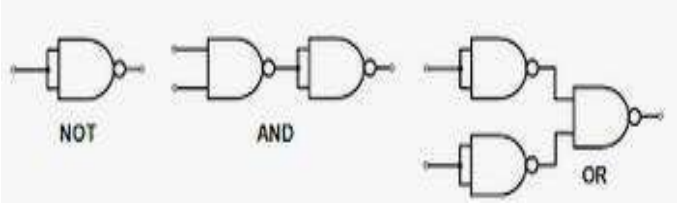
24.	**Define power dissipation and noise margin?** Power dissipation is measure of power consumed by the gate when fully driven by all its inputs. Noise margin is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output. It is expressed in volts.	**BL1**
25.	**Mention the characteristics of MOS transistor?** The n-channel MOS conducts when its gate-to-source voltage is positive. The p-channel MOS conducts when its gate-to-source voltage is negative. Either type of device is turned off if its gate-to-source voltage is zero.	**BL1**
26.	**Why totem pole outputs cannot be connected together?** Totem pole outputs cannot be connected together because such a connection might produce excessive current and may result in damage to the devices.	**BL2**
27.	**State advantages and disadvantages of TTL** **Advantages of TTL**: Easily compatible with other ICs, Low output impedance. **Disadvantages of TTL:** Wired output capability is possible only with tristate and open collector type special circuits in circuit layout and system design are required.	**BL2**
28.	**What is the advantages of ECL over TTL? (Nov 2014, Nov 2021)** Transistors in ECL logic families do not saturate which eliminates the storage time delay. So ECL families have the fastest operating speed and the propagation delay time per gate is 1ns while that of TTL is 12ns. (approx.)	**BL2**
29.	**Compare the totem pole output with open collector output. (Nov 2014)**	**BL2**

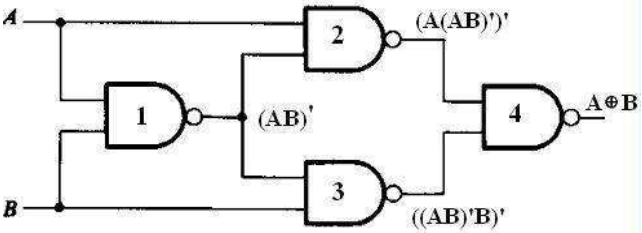
Totem pole	**Open collector**
Output stage consists of Pull up transistor, Diode resistor and pull -	Output stage consists of only pull down transistor.
External pull-up resistor is not required for operation of totem pole output configuration.	External pull-up resistor is required for proper operation of Open collector output configuration.
Output of two gates cannot be tied together.	Output of two gates can be tied together using wired AND technique.
Operating speed is high.	Operating speed is low.

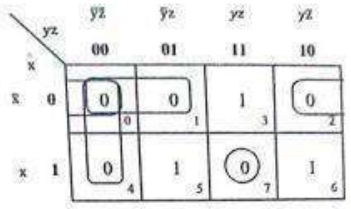
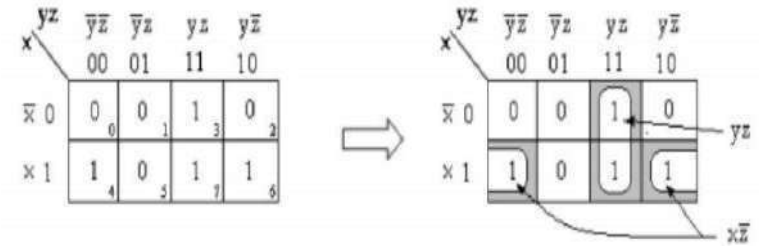
30.	**Draw the circuit diagram of standard TTL NAND gate. (Nov 2020: May 2021).**  **TTL based NAND gate**	**BL1**

31.	**List the different types of output configuration in TTL (Nov 2019)** There are three different types of output configuration in TTL. They are i) Totem pole configuration , ii) Open Collector configuration iii) Tristate configuration	**BL1**
32.	**Draw the DTL based NAND gate. (Nov 2018)**  	**BL1**
	PART-B	
1.	(i) A 12 bit hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8 bit data word that was written into memory if the 12 bit word read out is as (1) 101110010100 and (2) 111111110100. (ii) Briefly discuss weighted binary code.**(Nov2015)**	**BL3** **BL2**
2.	(i) State the differences between 1's complement and 2's complement subtraction with suitable examples. (ii) Explain about error detection and correction codes.**(Nov 2017)**	**BL3** **BL4**
3.	(i) Convert 1010111011101100_2 into its octal, decimal and hexadecimal equivalent. (ii) Deduce the odd parity hamming code for the data: 1010. Introduce an error in the LSB of the hamming code and deduce the steps to detect the error. **(May 2016)**	**BL3** **BL5**
4.	(i) Perform the following addition using BCD and Excess-3 addition (205+569). (ii) Encode the following binary word 1011into seven bit even parity hamming code**. (Apr2015)**	**BL3** **BL3**
5.	(i) Explain in detail the usage of hamming codes for error detection and error correction with an example considering the data bits as 0101 and even parity **(Nov 2022)** (ii) Convert $FACE_{16}$ into its binary octal and decimal equivalent.**(Nov 2021)**	**BL4** **BL3**
6.	Explain the basic working principles of following digital logic families. (i) TTL (ii) ECL and (iii) CMOS**(May2013, Nov 2019)**	**BL4**
7.	Explain the characteristics and implementation of the given digital logic families: (i) DTL and (ii) RTL **(Apr 2018)**	**BL4**
8.	(i) Given that a frame with bit sequence 1101011011 is transmitted, it has been received as1101011010. Detect the error using any one error detecting code. (ii) Draw the MOS logic circuit for NOT gate and explain its operation**. (Nov 2014)**	**BL3** **BL4**
9.	(i) Explain the Hamming code with an example. State its advantages over parity codes. (ii) Design a TTL logic circuit for a 3 input and 2 input NAND gate.**(Nov 2014, Apr 2017)**	**BL4** **BL6**

10.	Explain the two types of MOS families.**(Nov 2019)**	**BL4**
11.	(i) With circuit schematic, explain the operation of a two input TTL NAND gate with totem pole output. **(Nov 2018, Nov 2021, Nov 2022)** (ii) Compare totem pole and open collector outputs**.(Apr 2017, Nov 2021)**	**BL4** **BL2**
12.	(i) Explain with an aid of circuit diagram the operation of 2 input CMOS NAND gate and list out its advantages over other logic families. (ii) Given the two binary numbers X=1010100 and Y=1000011, perform the subtraction Y-X using 2's complements.**(Nov 2016)**	**BL4** **BL3**
13.	With circuit schematic and explain the operation and characteristics of an ECL. **(May'16)**	**BL4**
14.	Give notes on different arithmetic operator and bitwise operator**. (Apr2018)**	**BL2**
15.	(i) Design a 2-input NOR gate using CMOS logic. **(April 2019)** **(ii)** Explain the operation of RTL inverter circuit with relevant diagrams.	**BL6** **BL4**
16.	i) Find the decimal equivalent of the following binary numbers expressed in the 2's complement format, 00001110; 10001110. (3) ii) Explain in detail about cyclic redundancy check code for digital code transmission and reception. (5) iii) Explain in detail about Ex-NOR gate and draw the CMOS logic diagram of it. (5) **(Nov 2020, May 2021)**	**BL3** **BL4** **BL4**
17.	i) Why is ECL called non-saturating logic ? What is the main advantage accruing from ECL? With the help of a relevant circuit schematic, briefly describe the operation of ECL OR/NOR logic. (6) ii) With neat internal schematic diagram explain BiCMOS logic two input NAND gate. (7) **(Nov 2020,May 2021)**	**BL4** **BL4**
	Part C (C201.1)	
1.	Design a CMOS inverter and explain its operation. Comment on its characteristics such as Fan-in, Fan-out, power dissipation, propagation delay and noise margin. Compare its advantages over other logic families.**(Apr 2017)**	**BL6**
2.	(i) Design a 3- input NAND gate circuit using TTL Logic. (**April 2019)** (ii) Explain in detail the generation of hamming code for 4- bit data.	**BL6** **BL4**
UNIT II COMBINATIONAL CIRCUITS		
	PART-A	
1.	**Construct OR gate and AND gate using NAND gate. (Nov 2016)** **OR Gate**  **AND Gate** 	**BL2**
2.	**Which gates are called as the universal gates? What are its advantages?** A universal gates is a gate that can implement any Boolean function without using any other gate type. For example, the NAND and NOR gates are universal gates. The NAND and NOR gates are used to perform any type of logic operations like AND, OR, NOT, etc. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.	**BL2**

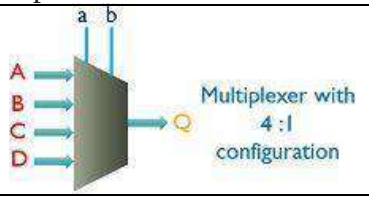
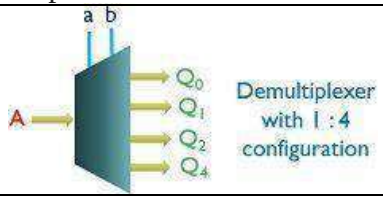
3.	**Simplify the expression: X = (A'+B) (A+B+D) D'.** X=(A'+B)(A+B+D)D'=(AA'+ A'B + A'D+ AB +BB + BD)D' X=(0 + A'B + A'D+AB + B + BD)D' X=(A'D+ B(A'+ A+1+ D))D'= (A'D+ B)D' X= A'DD'+ BD'= 0 + BD' therefore X= BD'	**BL3**
4.	**Give the canonical product form of $F=x_1'x_2'x_3+x_1'x_2x_3'+x_1x_2'x_3'+x_1'x_2x_3$** $F=x_1'x_2'x_3+x_1'x_2x_3'+x_1x_2'x_3'+x_1'x_2x_3$ F=001+010+100+011= m1+m2+m4+m3 $F=\sum_m(1, 2, 3, 4)$ --------- This is Sum form of F. Collecting the missing terms in the Sum form of F derives the product form of F. **Product form:** $F=\prod_M(0, 5,6, 7) = M0M5M6M7$ F=(000)(101)(110) (111) F=(x1+x2+x3)(x1'+x2+x3')(x1'+x2'+x3)(x1'+x2'+x3')	**BL3**
5.	**Using NAND gate represent NOT,AND & OR Gates. (Nov 2018)**  	**BL1**
6.	**State the Associative property of Boolean algebra. (Apr 2018)** Associative property of Boolean algebra states that the order in which the logic operations are performed is irrelevant as their effect is the same. A + (B + C) = (A + B) + C A · (B · C) = (A · B) · C	**BL1**
7.	**Define Duality Property (Apr 2018)** Duality property states that the dual of the Boolean function is obtained by interchanging the logical AND operator with logical OR operator and zeros with ones. For every Boolean function, there will be a corresponding Dual function.	**BL1**
8.	**State &prove De-Morgan's theorem. (Nov 2012)** **De-Morgan's theorem 1:** The complement of product of any number of variables is equivalent to sum of the individual complements. **De-Morgan's theorem 2:** The complement of sum of any number of variables is equivalent to product of the individual complements. **Proof:** a) (AB)' = A'+ B' b) (A+B)'=A'B' Inputs / Truth Table Outputs For Each Term B A AB $\overline{AB}$ $\overline{A}$ $\overline{B}$ $\overline{A}+\overline{B}$ 0 0 0 1 1 1 1 0 1 0 1 0 1 1 1 0 0 1 1 0 1 1 1 1 0 0 0 0 Inputs / Truth Table Outputs For Each Term B A A+B $\overline{A+B}$ $\overline{A}$ $\overline{B}$ $\overline{A}.\overline{B}$ 0 0 0 1 1 1 1 0 1 1 0 0 1 0 1 0 1 0 1 0 0 1 1 1 0 0 0 0	**BL1**
9.	**Simplify Y=(A+B)(A'+C)** Y= (A+B)(A'+C) = AA'+AC + A'B + BC = 0+ AC + A'B + BC Y = AC+ A'B (using consensus theorem XY+X'Z+YZ=XY+X'Z)	**BL3**

10.	**What is a prime implicant?** A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map i.e all the possible groups that are formed in K-Map.	**BL1**
11.	**Mention the dependency of output in combinational circuits. (Nov 2018)** In combinational circuits, the output depends only on the present value of input. But in case of sequential circuits output depends on present input and past output.	**BL2**
12.	**Simplify A+AB+A'+B. (Nov 2022)** A+AB+A'+B = A+A'+ AB + B = 1+ AB + B (Since X+X'=1) = 1 (Since X+1 = 1)	**BL3**
13.	**Find the result of A+A'D+AC'. (April 2019)** A+A'D+AC'= A(1+C')+ A'D [since 1+C' = 1] =A+A'D A+A'D+AC' =A+D	**BL3**
14.	**Express x+yz as the sum of minterms.** x + yz= x(1) +(1)yz= x(y+ y') + (x + x')yz= xy+ xy'+ xyz+ x'yz = xy(1) +xy'(1)+ xyz+ x'yz= xy(z+z') + xy'(z+ z') +xyz+ x'yz = xyz+ xyz'+ xy'z+ xy'z'+ xyz+ x'yz =xyz+ xyz'+ xy'z+ xy'z'+ x'yz ---------- (x + x = x) =111 + 110 + 101 + 100 +011 =m7 + m6 + m5 +m4 +m3 x+yz =∑m(3,4, 5, 6,7)	**BL3**
15.	**Describe the canonical forms of the Boolean function.** **Sum of minterms:** Combination of minterms using OR operation. Example: F = A'B+ AB = m_1+m_3, F= ∑m(1,3) **Product of maxterms:** Combination of maxterms using AND operation. Example: F =(A+B)(A'+B) = M_0M_2, F=∏M(0,2)	**BL1**
16.	**Define the following: min term and max term?** **Minterm** (standard product) is a combination of n variables using AND operation for the function of n variables. Possible minterm for a function of two variables A & B: A'B', A'B, AB', AB **Maxterm** (standard sum) is a combination of n variables using OR operation for the function of n variables. Possible maxterms for a function of two variables A& B: A+B, A+B',A'+B, A'+B'	**BL1**
17.	**Draw the logical diagram for Ex-OR gate using NAND gates.(Nov 2015)** 	**BL1**
18.	**Simplify the expression Z=AB+AB'(A'C')'(Apr 2015)** Z=A(B+B'(A'C')') =AB+ AB'(A+C) (Demorgan's Law) =A(B+ B'(A+C))[A+ A'B=A+B] Z= A(B+ A+C) =A+A(B+C) [A+ AB=A] Z=A	**BL3**

19.	**Convert the given expression in canonical SOP from Y=AB+A`C+BC`.** Y = AB+A`C+BC` =AB (C +C') +A`C (B+B') +BC` (A +A') =ABC+ABC'+A`BC+ A`B'C+A BC`+ A'BC` =ABC+ABC`+A`BC+A`B`C+A`BC`. [A +A =A] Y=∑(1,2,3,6,7)	**BL3**
20.	**Reduce A · (A + B). (Apr 2018)** A · (A + B) = AA+AB [Since A.A =A] = A+AB = A (1+ B) [Since 1+B =1] A · (A + B) = A.	**BL3**
21.	**Write the POS form of the SOP Expression f(x,y,z) = x'yz+xyz'+xy'z. (Apr 2017)**  Let $\bar{f} = \bar{y}\bar{z} + \bar{x}\bar{y} + \bar{x}\bar{z} + xyz$ By demorgan's law $f = \overline{\bar{y}\bar{z} + \bar{x}\bar{y} + \bar{x}\bar{z} + xyz}$ Therefore the POS expression is $f = (y+z)(x+y)(x+z)(\bar{x}+\bar{y}+\bar{z})$	**BL3**
22.	**Simplify F(x,y,z) =$\sum m(3,4,6,7)$ (May 2016)**  **F=yz+xz'**	**BL3**
23.	**What is K map? (Apr 2018, Nov 2021)** A Karnaugh Map (K-Map) is a pictorial method used to minimize Boolean expressions without having to use Boolean algebra theorems and equation manipulations.	**BL1**
24.	**Give some of the major applications of multiplexers and decoders. (Nov2014)** **Multiplexers**: Data selection, Data routing, parallel to serial conversion, Logic-function generation. **Decoders:** Memory addressing, Instruction decoding.	**BL3**
25.	**Draw the truth table of 2: 1 MUX. (Nov 2016)** The truth table of 2:1 MUX is	**BL1**

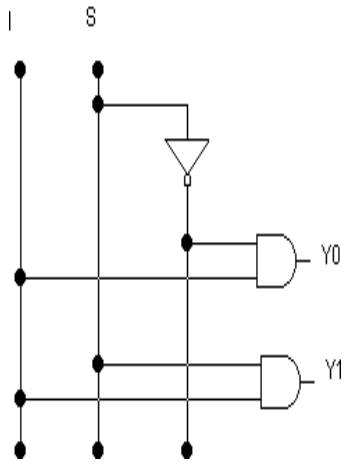
Input		**Output**
E	**S**	**Y**
1	**0**	**D_0**
1	**1**	**D_1**
0	**X**	**0**

26. **Mention the difference between a DEMUX and a MUX. (Nov 2022)** **BL2**

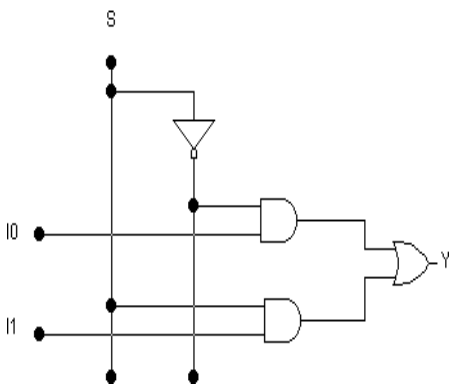
Parameter	MULTIPLEXER	DEMULTIPLEXER
Definition	Multiplexer is a combinational circuit that provides single output but accepts multiple data inputs.	Demultiplexer is a combinational circuit that takes single input but that input can be directed through multiple outputs.
Symbol		
Conversion technique	It performs parallel to serial conversion.	It performs serial to parallel conversion.
Device configuration	It is N to 1 device and thus behaves as data selector.	It is 1 to N device and thus behaves as data distributor.

27. **Draw a 1to 2 demultiplexer circuit and 2to 1multiplexer circuit. (Nov 2021)** **BL1**

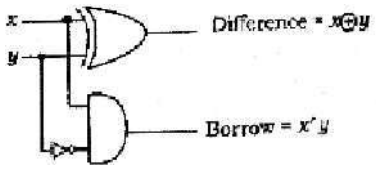
1 to 2 line Demultiplexer



2 to 1 line Multiplexer



28. **Design a half subtractor. (May 2016, Apr 2017)** **BL6**



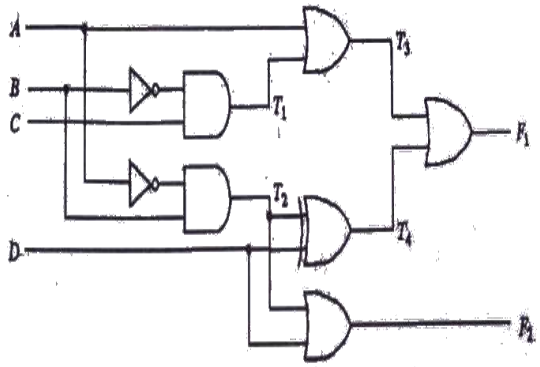
Input		Output	
x	Y	Borrow	Difference
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

29. **Write the truth table of a full subtractor. (Nov/ Dec 2020: May 2021)** **BL1**

Input			Output	
A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

30.	**Compare DECODER and DEMUX (Nov 2017)** **DECODER** | **DEMUX** A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. | A demultiplexer is a circuit that receives information on a single line and transmits this information on one of many output lines. A decoder accepts a set of binary Inputs and activates only the output that corresponds to that input number. Example: Binary to Octal decoder | Demux is used as a Data Distributor. Example: Serial to parallel converter.	**BL2**
31.	**Determine the exact number of half adders and full adders required for performing the addition of two binary number of 5-bit length each. (April 2019)** Addition of two binary number of 5-bit length each need Number of Full adder = 4 and Number of Half adder = 1.	**BL3**
	PART B	
1.	Design BCD to Excess-3 code converter**.(Apr 2015, Nov 2015)**	**BL6**
2.	What are Magnitude comparators? Explain the design of magnitude comparators with the help of a suitable example. Construct 16-bit comparator using 4-bit comparator as a building block.	**BL6**
3.	Design 4bit Gray Code to (i) binary converters using logic gates. ii) Excess-3 Code converter using NAND gates.**(Nov 2017)**	**BL6**
4.	(i) Prove that ABC+ABC'+AB'C+A'BC =AB+AC+BC. **(Apr 2018)** (ii) Convert the given expression on canonical SOP form Y= AC+AB+BC.	**BL3**
5.	(i) Show that a function expressed as a sum of its minterms is equivalent to a function expressed as a product of its maxterms. (ii) Using K-map simplify the following function and implement the function using logic gates f(A,B,C) =∏(0, 4, 6).**(Nov 2012)**	**BL4** **BL3**
6.	Prove that for constructing XOR from NANDs we need four NAND gates.**(May 2013)**	**BL4**
7.	Show that a possible logic NAND gate is a negative logic NOR gate and vice versa. **(Nov 2018).**	**BL4**
8.	Write down the steps in implementing a Boolean function with levels of AND gate.**(Apr 2018)**	**BL2**
9.	Give the general procedure for converting a Boolean expression into multilevel NAND diagram.**(Apr 2018)**	**BL2**
10.	i) Apply suitable Boolean laws and theorems to modify the expression for a two-input EX-OR gate in such a way as to implement a two-input EX-OR gate by using the minimum number of two-input NAND gates only. **(6)** ii) Write a simplified maxterm Boolean expression for Π (0, 4, 5, 6, 7, 10, 14) using the Karnaugh mapping method. (7) **(Nov 2020: May 2021**)	**BL3** **BL3**
11.	Simplify the logical expression using K map in SOP and POS form F(A,B,C,D) = Σm(0,2,3,6,7)+d(8,10,11,15).**(Nov 2016).**	**BL3**
12.	(i) Simply the following function using karnaugh Map. f(w,x,y,z) = Σm(0,1,3,9,10,12,13,14)+Σd(2,5,6,11). (ii) Implement the following function using only NAND gates: f(x,y,z) = Σm(0,2,4,6).**(May 2016)**	**BL3** **BL3**

13.	(i)Implement the function F(p,q,r,s)=Σ(0,1,2,4,7,10,11,12) using decoder. (ii)Design a 4 bit Binary to gray code converter and implement using logic gates. **(Nov 2021)**	**BL3** **BL6**
14.	Given the following Boolean functions F=A'C+A'B+AB'C+BC. i) Express it in sum of Min terms. ii) Find the minimal sum of products expression. **(Nov 2018)**	**BL3**
15.	Simplify the Boolean function using K-map and implement using only. NAND gates. F(A,B,C,D)=Σm(0,8,11,12,15)+Σd(1,2,4,7,10,14) **(Nov 2015).** Mark the essential and non-essential prime implicants.	**BL3**
16.	Simplify the following Expressions in 1) Sum of products 2)Product of Sums a) x'z'+y'z'+yz'+xy b) AC'+B'D+A'CD+ABCD c)(A'+B'+D')(A+B'+C')(A'+B+D')(B+C'+D') **(Nov 2019)**	**BL3**
17.	Implement the Boolean function using 8:1 mux: F(A,B,C,D)=Σm(0,1,3,4,8,9,15) **(Apr 2015)**	**BL3**
18.	(i) Design a BCD to EXCESS 3 code converter. .**(Nov 2017)** (ii) Design a full adder and implement it using suitable multiplexer	**BL6**
19.	Design a half subtractor circuit with inputs x and y and outputs D and B. The circuit subtracts the bits x-y and places the difference in D and the borrow in B **(Nov 2019)**	**BL6**
20.	(i)Reduce the following function using K-map. F (A,B,C,D)=∏M(0,2,3,8 ,9,12,13,15) (ii)Design a full adder using two half adders and an OR gate. **(Nov 22)**	**BL3** **BL6**
21.	Design a full adder and subtractor using two half adders and subtractor and OR gate.**(Nov 2014, Nov 2015, Nov 2016, Nov 2021)**	**BL6**
22.	Simplify the Boolean function using K-map F(w,x,y,z)=Σ(0,1,3,5,6,7,8,12,14) which has the don't care conditions d(w,x,y,z)= Σ(9,15).**(**8 marks) (ii) Implement the following function using only NAND gates: f(x,y,z) = Σm(0,2,4,6). (5 marks) **(Nov 2022)**	**BL3**
23.	i) Design a 3*8 decoder and explain its operation as a minterm generator. ii) Design a full adder using NOR gates.**(Apr 2017)**	**BL6**
24.	Draw the logic diagram of 2 to 4 line Decoder using NOR gates only. Include an enable input. **(Nov 2018)**	**BL3**
25.	(i) Design a 3×8 decoder using 2×4 decoders. Draw the truth table. (ii) Design a full adder circuit using logic gates. **(Apr 2019)**	**BL6**
26.	(i) Find the minterms of the following Boolean expression by first plotting the function in a map : F=C'D+ABC'+ABD'+A'B'D. (5) (ii) Design a 4 bit gray to binary code converter. **(8) (Nov/Dec 20 May 21)**	**BL5** **BL6**
27.	(i) Simplify and implement the logic function F(A, B, C)= ∑(0, 1, 4, 5, 7) using logic gates. (ii) Design a 4×2 priority encoder using logic gates. **(Apr 2019)**	**BL3** **BL6**
	Part-C (C201.2)	
1.	Design a combinational circuit with three inputs x,y and z and three outputs A,B and C. When the binary input is 0,1,2 or 3 the binary output is one greater than the input. When the binary input is 4,5,6 or 7 the binary output is one less than the input. **(Nov 2018, Nov 2022)**	**BL6**

2.	Simplify the following function and implement it using NAND gates only; F(w, x, y, z)=∑(1, 3, 5, 7, 9, 11,13,15), with don't care states d(w, x, y,z)= ∑(0, 2, 4, 6, 8). **(Apr 2019)**	**BL6**
3.	Consider the combinational circuit shown in fig  i) Derive the Boolean Expression for T1 through T4. Evaluate the outputs of F1 and F2 as a function of the four inputs. ii) List the truth table with 16 binary combinations of the four inputs variables. Then list the binary values for T1 through T4 and outputs F1 and F2 in the table. iii) Plot the output Boolean function obtained in part (ii) on maps and show that the simplified Boolean expressions are equivalent to the ones obtained in part (i) **(Nov 2019)**	**BL5**
	UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS	
	PART A	
1.	**Define sequential circuit?** In sequential circuits the output variables dependent not only on the present input variables but they also depend upon the past history of these input variables.	**BL1**
2.	**What is the classification of sequential circuits?** The sequential circuits are classified on the basis of timing of their signals into two types. They are, 1) Synchronous sequential circuit. 2) Asynchronous sequential circuit.	**BL1**
3.	**Define synchronous sequential circuit (Nov 2019)** In sequential circuits the output variables dependent not only on the present input variables but they also depend upon the past history of these input variables. In synchronous sequential circuit ,change in input signals affect the memory element upon activation of clock signal. Clocked flip flops are used as memory elements. Common clock pulse is given to all the units in the design.	**BL1**
4.	**Define Flip flop. What are the different types of flip-flop? (Nov 2021)** The basic unit for storage is flip-flop. A flip-flop maintains its output state either at 1or 0 until directed by an input signal to change its state. **Types of flip flop**: 1. RS flip-flop 2. SR flip-flop 3. D flip-flop 4. JKflip-flop 5.T flip-flop	**BL1**
5.	**Define rise time and fall time.** The time required to change the voltage level from10% to 90% is known as rise time (t_r). The time required to change the voltage level from 90% to10% is known as fall time (t_f).	**BL1**

6. **Compare synchronous and asynchronous sequential circuit. (Nov 2021)** **BL2**

Synchronous Sequential circuits	Asynchronous Sequential circuits
Clocked flip flops are used as Memory elements	Either un-clocked flip flops or time Delay elements (latches) are used as memory elements.
Change in input signals can affect Memory element upon activation of clock signal	Change in input signals can affect Memory element at any instant of time
Clock frequency selection is based on total time delay. Hence slower response.	Because of absence of clock, faster Response
Common clock pulse is given to all the units in the design.	No common clock pulse.

7. **Define race around condition. (Nov 2017)** **BL1**

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called 'race around condition'.

8. **What is the operation of JK flip-flop? Why it is called a universal flip-flop. (Nov 2012)** **BL2**

When K input is low and J input is high the Q output of flip-flop is set.
When K input is high and J input is low the Q output of flip-flop is reset.
When both the inputs K and J are low the output does not change.
When both the inputs K and J are high it is possible to set or reset the flip-flop (ie) the output toggle on the next positive clock edge.
All other types of flip flop cane realized with JK flip flop.

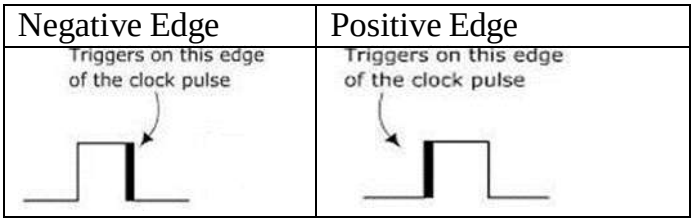
9. **Write down the characteristics table of JK flip- flop. (Apr 2019)** **BL1**

The characteristics table shows the relationship between Flip- flop inputs, present state and next state. The characteristics table for JK Flip- Flop is given below:

Present State (Q_n)	**Next State (Q_{n+1})**	**Excitation Inputs**	
		J	**K**
0	0	0	0
0	0	0	1
0	1	1	0
0	1	1	1
1	1	0	0
1	0	0	1
1	1	1	0
1	0	1	1

10. **Why is edge-triggered flip-flop is used?** **BL2**

The problem of race around condition can solved by edge triggering flip flop. The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

11.	**What is an edge triggered flip flop?(Nov 2015)** Edge triggered flipflop changes state either at positive edge (rising edge) or at negative edge (falling edge) of clock pulse and is sensitive to its inputs only at this transition of the clock. 	**BL1**
12.	**What is the difference between level and edge triggering? (or) Compare level triggered flip flops and edge triggered flip flops. (Nov/ 2020, May 2021)** **Level triggering**: 1.It is of two types -High level triggering -Low Level triggering 2.Latch or flip flop circuits will change their outputs only when the clock is either at active high or low level. **Edge triggering**: 1.It is of two types -Positive edge triggering -Negative edge triggering 2.Flip flop circuits will change their outputs only when there is either Positive edge or negative edge clock transition.	**BL2**
13.	**Define setup time.** The setup time is the minimum time required to maintain a constant voltage levels at the excitation inputs of the flip-flop device prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as t_{setup}.	**BL1**
14.	**Why gated D latch is called transparent latch?** D / Q_{n+1} / Comments: 0 / 0 / Set; 1 / 1 / Reset From the truth table of D flip flop it is found that, the output Q will look exactly like D. Hence, the D latch is said to be transparent latch.	**BL2**
15.	**Define hold time.** The hold time is the minimum time for which the voltage levels at the excitation inputs must remain constant after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as t_{hold}.	**BL1**
16.	**What is the operation of D flip-flop and T flip-flop?** In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset. T flip-flop is also known as Toggle flip-flop. When T=0 there is no change in the output. When T=1the output switch to the complement state (i.e.) the output toggles.	**BL1**
17.	**Explain the flip-flop excitation tables for RS FF.** Excitation table of RS Flip-flop is as follows:	**BL4**

SR Flip-flop

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

18. **What is a master-slave flip-flop? (Apr 2018)** **BL1**

A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave. The advantage for using a master-slave instead of a JK for toggling is the master-slave doesn't allow the output to change when q changes and waits for a clock pulse. This prevents false triggering that is referred to as "race".

19. **Give the comparison between combinational circuits and sequential circuits. (Nov 2019)** **BL2**

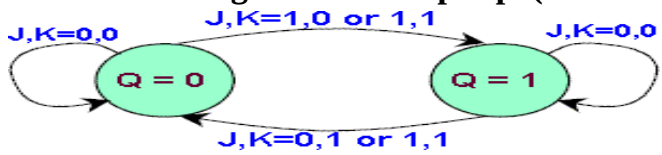
S.	Combinational circuits	Sequential circuits
1.	Output variables depend on the input alone.	The output variable depends on the Present input and previous output
2.	Memory unit is not required	Memory unit is required to store the previous output.
3.	Faster response since propagation Delay alone is present.	Slower response due to the delay caused by feedback of output.
4.	Simple design	Complex design
5.	Eg. Parallel adder	Eg. Serial adder

20. **Draw truth table for D flipflop and JK flipflop. (May2013)** **BL1**

J	K	Qn+1	Comments
0	0	Qn	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q'n	Complement

D	Q_{n+1}	Comments
0	0	Set
1	1	Reset

21. **Draw the state diagram of JK flipflop?(Nov 2016)** **BL1**



22. **Show how the JK flip-flop can be modified into a D flip-flop or a T flip-flop. (Nov2014)** **BL2**

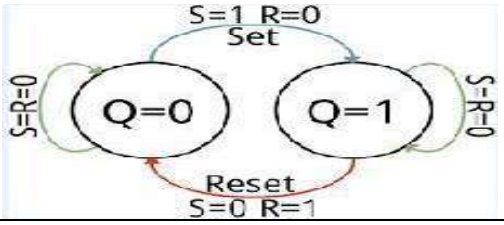
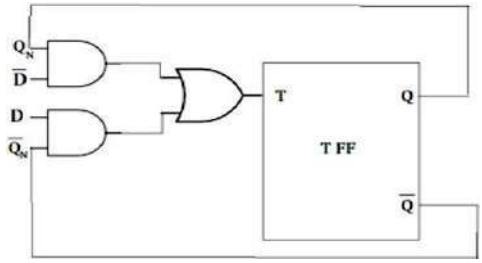
From the truth table of JK flip-flop, it is observed that when J=K, It operates similar to T flip-flop and When J=K' it operates similar to D flip flop.

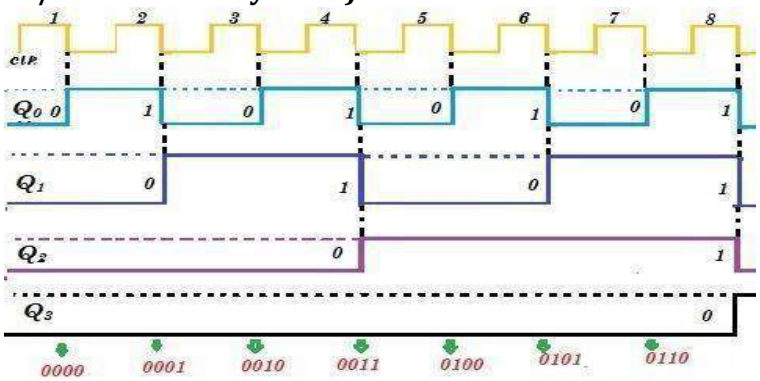
J	K	Qn+	Comments
0	0	Qn	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q'n	Complement

T	Qn+1	Comments	D	Q_{n+1}	Comments
0	Qn	No Change	0	0	Set
1	Q'n	Complement	1	1	Reset

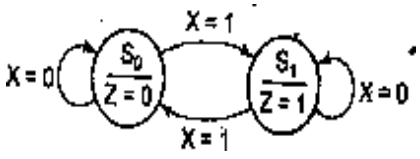
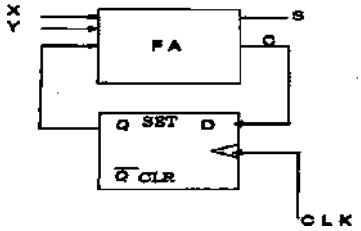
23. **Write the role Master clock generator in synchronous circuits. (Nov 2019)** **BL2**

Practical synchronous sequential logic systems use fixed amplitude such as voltage level for the binary signals. Synchronization is achieved by a timing device called a Master clock generator, which generate a periodic train of clock pulses.

24.	**Give the Characteristic equation and Characteristic table of a T Flip Flop. (Apr 2017, Nov 2022)** Characteristics equation for T- Flip : '+T'. Q_n Characteristics table of T Flip flop: | T	Q_{n+1}	State | |---|---|---| | 0 | Q_n | No change | | 1 | $\overline{Q}_n$ | Toggles |	**BL1**
25.	**Draw state diagram and give its characteristics equation and truth table of SR flipflop?(Nov 2015)(May 2016)** **Truth table** **State Diagram** | S | R | Next state of Q | |---|---|---| | X | X | No change | | 0 | 0 | No change | | 0 | 1 | $Q = 0$; reset state | | 1 | 0 | $Q = 1$; set state | | 1 | 1 | Indeterminate | 	**BL1**
26.	**Differentiate between Mealy and Moore models. (Nov2014) (Nov2016) (May2016) (Apr 2017).** | **Mealy models** | **Moore models** | |---|---| | Output is a function of both the present state and input. | Output is a function of present state only. | | In state diagram representation, both the input and output values are separated by a slash along the directed lines between the states. | Inputs alone are marked along the directed lines in their state diagram representation. |	**BL2**
27.	**Convert T Flip Flop to D Flip Flop. (Apr 2015)**  **$T = D'Q_N + DQ_N'$**	**BL3**
28.	**What is a preset table counter and Ripple Counter (Nov 2018, Nov 2022)** **Preset Table Counter:** This counter can be cleared by a high level on the RESET line, and can be preset to any binary number present on the inputs by a high level on the PRESET ENABLE line. **Ripple Counter:** A **ripple counter** is an **asynchronous counter** where only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop. **Asynchronous** counters are also called **ripple**-counters because of the way the clock pulse **ripples** it way through the flip-flops.	**BL2**

29.	**Comparison between synchronous and asynchronous counter? (Apr 2018)** <table><tr><th>Synchronous Counter</th><th>Asynchronous Counter</th></tr><tr><td>All flipflops are applied with same clock.</td><td>Different flipflops are applied with different clocks</td></tr><tr><td>It is faster in operation</td><td>It is slower in operation</td></tr><tr><td>Any count sequence is possible</td><td>Fixed count sequence either up or down.</td></tr><tr><td>Produces no decoding error</td><td>Produces decoding error</td></tr></table>	**BL2**
30.	**Draw the timing diagram of four bit binary ripple counter each flip flop outputs. (Nov/ Dec 2020: May 2021)** 	**BL1**
31.	**What is FSM? List its two basic types. (Apr 2019)** **Finite State Machine's (FSMs)** are at the heart of most digital design. The basic idea of an FSM is to store a sequence of different unique states and transition between them depending on the values of the inputs and the current state of the machine. **The FSM can be of two types:** (i) Moore FSM- where the output of the state machine is purely dependent on the state variables. (ii) Mealy FSM- where the output can depend on the current state variable values and the input values.	**BL1**
	PART-B	
1.	Explain T-flip-flop, SR Flip Flop and JK Flip Flop with suitable internal structure**. (Apr 2018)**	**BL4**
2.	(i) Describe the difference between a gated S-R latch and an edge-triggered S-R flipflop. (ii) Draw the logic circuits and the excitation tables for the T, JK flip-flops.	**BL4**
3.	(i) Draw a master-slave J-K flip-flop system. Explain its operation and show that the race- around condition is eliminated**.** (ii) Draw the circuit of a S-R flip-flop using NAND gates. Modify it to include clock. Derive J-K circuit from S-R flip-flop circuit and explain its truth table. **(Nov 2019, Nov 2018, Nov 2022)**	**BL4** **BL3**
4.	(i) Explain what is universal shift register? Explain its working. (ii) Perform the following conversions T flip-flop to D flip-flop.	**BL4**
5.	Explain in detail about shift Registers **(Nov 2017, Apr 2017)**	**BL4**
6.	(i) Design a BCD counter using JK flip-flops. (ii) Design an up-down counter using D-flip-flops to count 0,3, 2, 6,4, and 0.	**BL6**
7.	Design a 3-bit binary counter using T-flipflop **(May 2013).**	**BL6**

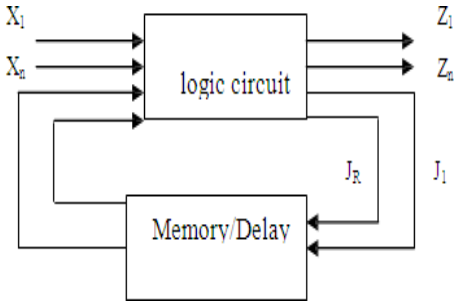
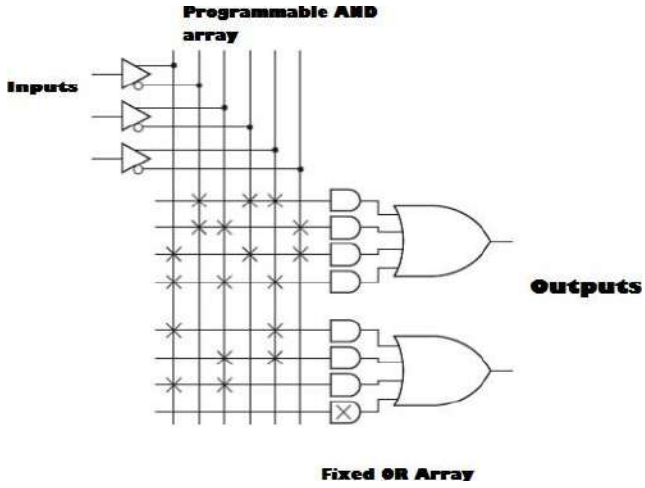
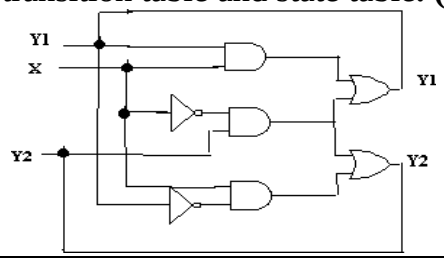
8.	(i)Design an asynchronousModulo-8 Down counter using JK flipflops**.** (ii)Explain the circuit of SR flipflop and explain its operation. **(Nov 14)**	**BL6** **BL4**
9.	(i)Design synchronous sequential circuit that goes through the count sequence 1,3,4,5 repeatedly. Use T flipflop for your design. (ii)Explain the various types of triggering with suitable diagrams. Compare their merits and demerits.**(Nov 2014, Nov 2017)**	**BL6** **BL4**
10.	(i)Design a synchronous decade counter using T flipflop and construct the timing diagram. (ii)Design a mealy model of sequence detector to detect the pattern 1001.**(Nov 2015)**	**BL6**
11.	Draw and explain bit shift register. Also give it's truth table with it's input and output waveform. **(Apr 2018)**	**BL4**
12.	(i)Design a MOD5 Synchronous counter using JK flipflops. **(Apr 2015)** (ii)Design a sequence detector to detect the sequence 101 using JK flipflop.	**BL6**
13.	Design a sequence detector that produces an output '1' whenever the non-overlapping sequence 101101 is detected**.(Nov 2016)**	**BL6**
14.	Explain Flip Flop Excitation table for JK and RS Flip Flop **(Apr 2018)**	**BL4**
15.	Design a MOD5 Synchronous counter using T flipflops. **(Nov 21, Nov 22)**	**BL6**
16.	(i)Design a serial adder using mealy state model. (**May 2016)** (ii)Explain the state minimization using portioning procedure with suitable example. **(May 2016)**	**BL6**
17.	Assume that there is parking area in a sop whose capacity is 10. No more than 10 cars are allowed inside the parking area and the gate is closed as soon as the capacity is reached. There is a gate sensor to detect the entry of car which is to be synchronized with the clock pulse. Design and implement a suitable counter using JK flip flops. Also, determine the number of flip flops to be used if the capacity is increased to 50. **(Nov 2016)**	**BL6**
18.	(i)A sequential circuit with two D flip flops A and B, input X and output Y is specified by the following next state and output equations A(t+1)=AX+BX, B(t+1)= A`X, Y=(A+B)X`. Draw the logic diagram, derive state table and state diagram. (ii) Realize T flip-flop using JK flip-flop. **(Nov 2015)**	**BL5**
19.	Design a 5 bit Ring counter and mention its applications **(Nov 2021)**	**BL6**
20.	Describe the design procedure with neat diagram about 4 bit bidirectional shift register with parallel load. **(Nov 2018)**	**BL4**
21.	Design a sequential circuit with two D flip-flops A and B and one input X. When X=0, the state of the circuit remains same. When X=1, the circuit goes through the state transition from 00 to 01 to 11 to 10 back to 00 and repeats. **(Nov 2018)**	**BL6**
22.	i) Explain in detail about master slave D flip flop with neat diagram. (5) ii) A four-bit ring counter and a four-bit Johnson counter are in turn clocked by a 10 MHz clock signal. Determine the frequency and duty cycle of the output flip-flop in the two cases. (8) **(Nov/ Dec 2020, May 2021)**	**BL4** **BL5**
23.	(i) Design a 2- bit synchronous sequential down counter. (ii) Explain the operation of a 3- bit universal shift register. **(Apr 2019)**	**BL6** **BL4**
24.	Design a synchronous counter to count the sequence 0,1,2,4,5,6 using SR flip flop. **(Nov 2022)**	**BL6**
25.	Design a Modulo- 6 asynchronous binary up- counter. **(Apr 2019)**	**BL6**

26.	(i) Explain Moore and Mealy models with the help of block diagrams. (ii) Draw the state table for the following state diagrams. **(Apr 2019)** 	**BL4**
27.	A sequential circuit has one flip flop Q, two inputs x and y and one output S. It consists of a full adder circuit connected to a D Flip flop, as shown in figure. Derive the state table and state diagram of the sequential circuit. **(Nov 2019)** 	**BL3**
28.	i) With the help of a schematic arrangement, explain how a J-K flip-flop can be used as a T flip-flop. (6) ii) Three four-bit BCD decade counters are connected in cascade. The MSB output of the first counter is fed to the clock input of the second counter, and the MSB output of the second counter is fed to the clock input of the third counter. If the counters are negatively edge triggered and the input clock frequency is 256 kHz, what is the frequency of the waveform available at the MSB of the third counter ? (7) **(Nov 2020, May 2021)**	**BL4** **BL5**
	Part-C (C201.3)	
1	Design a synchronous sequential logic circuit that goes through the sequence 0, 2, 4, 6, 8, 10, 12, 14 repeatedly. Use D flip- flop for your design. **(Apr 19)**	**BL6**
2	i) Design a synchronous counter that counts as 000, 010, 101, 110, 000, 010,. Ensure that the unused states of 001, 011, 100 and 111 go to 000 on the next clock pulse. Use J-K flip-flops. What will the counter hardware look like if the unused states are to be considered as 'don't care's? (10) **(Nov20 May 21)** ii) Implement a full adder circuit using a 3-to-8 line decoder. (5**)**	**BL6**
3	i) Design and explain the working of asynchronous BCD counter. Draw the timing diagram **(7) (Nov 2021)** ii) Design a counter for 000,001,111,101,110,000 by using JK flip flop **(8)**	**BL6**
	UNIT IV-ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABLE LOGIC DEVICES	
	PART A	
1.	**Define secondary variables and excitation variables.** The delay elements provide a short-term memory for the sequential circuit. The present state and next state variables in asynchronous sequential circuits are called secondary variables. Excitation Variables are next state variables in asynchronous sequential circuits	**BL1**
2.	**What are races? (Nov2012) or Define race conditions in asynchronous sequential circuit? (May2013, Nov 2016, Nov22)** When 2 or more binary state variables change their value in response to a change in an input variable, race condition occurs in an asynchronous sequential circuit. In case of unequal delays, a race condition may cause the state variables to change in an unpredictable manner.	**BL1**

3.	**Define non critical and critical race.** ➢ If the final stable state that the circuit reaches does not depend on the order in which the state variable changes, the race condition is not harmful and it is called a non-critical race. ➢ If the final stable state depends on the order in which the state variable changes, the race condition is harmful and it is called a critical race.	**BL1**
4.	**What is a dead lock condition? (Nov2014)** A condition resulting when one task is waiting to access are source that another is holding, and vice versa. In an operating system, a deadlock occurs when a process or thread enters a waiting state because a requested system resource is held by another waiting process, which in turn is waiting for another resource held by another waiting process. If a process is unable to change its state indefinitely because the resources requested by it are being used by another waiting process, then the system is said to be in a deadlock.	**BL2**
5.	**What is hazard and mention its types?** Hazard is an unwanted switching transients. The different types of hazard are as follows: ➢ Static 1 hazard: Output goes momentarily 0 when it should remain at 1 ➢ Static 0 hazard: Output goes momentarily 1 when it should remain at 0 ➢ Dynamic hazards: Output changes 3 or more times when it changes from1 to 0 or 0 to 1	**BL1**
6.	**Define merger graph.** The merger graph is defined as follows. It contains the same number of vertices as the state table contains states. A line drawn between the two state vertices indicates each compatible state pair. It two states are in compatible no connecting line is drawn.	**BL1**
7.	**Define state table**. For the design of sequential counters, we have to relate present states and next states. The table which represents the relationship between present states and next states, is called state table.	**BL1**
8.	**What are the steps for the design of asynchronous sequential circuit?** Construction of a primitive flow table from the problem statement is as follows, (i) Primitive flow table is reduced by eliminating redundant states using the state reduction (ii) State assignment is made (iii) The primitive flow table is realized using appropriate logic elements.	**BL1**
9.	**Define primitive flow table (Apr 2017)** It is defined as a flow table which has exactly one stable state for each row in the table. The design process begins with the construction of primitive flow table.	**BL1**
10.	**Brief about state Assignment in Synchronous circuit and asynchronous circuit. (Nov 2019)** In synchronous circuit, the state assignments are made with the objective of circuit reduction. In asynchronous circuits, the objective of state assignment is to avoid critical races.	**BL2**
11.	**Define PLA. (Nov 2012, Nov 2017, Nov 2018)** PLA is Programmable Logic Array (PLA). The PLA is a PLD that consists of a programmable AND array and a programmable OR array.	**BL1**

<table>
<tr><td>12.</td><td>Write a short note on fundamental mode asynchronous circuit and pulse mode asynchronous circuit. (Nov 2015)
Fundamental mode circuit–Input signals change only one at a time and fixed only when the clock is in stable condition.
Pulse mode circuit–Inputs are pulse triggered and pulse width is long enough for the circuit to responds to inputs.</td><td>BL1</td></tr>
<tr><td>13.</td><td>What is the difference between PROM AND EPROM? (Nov 2021, 2022)
<table>
<tr><th>TERMS</th><th>PROM</th><th>EPROM</th></tr>
<tr><td>Expands to</td><td>Programmable Read Only Memory.</td><td>Erasable Programmable Read Only Memory.</td></tr>
<tr><td>Basic</td><td>The chip is one- time programmable only.</td><td>The chip is reprogrammable.</td></tr>
<tr><td>Cost</td><td>Inexpensive.</td><td>Costly as compare to PROM.</td></tr>
<tr><td>Construction</td><td>PROM is encased in a plastic covering.</td><td>A transparent quartz window covers EPROM.</td></tr>
<tr><td>Storage Capacity</td><td>High</td><td>Low comparatively.</td></tr>
</table></td><td>BL2</td></tr>
<tr><td>14.</td><td>Write note on PROM. (Nov2012, Apr2015)
PROM (Programmable Read Only Memory). It allows user to store data or program. PROMs use the fuses with material like nichrome and polycrystalline. The user can blow these fuses by passing around 20 to 50mA of current for the period 5 to20μs.Theblowing of fuses is called programming of ROM. The PROMs are one time programmable. Once programmed, the information is stored permanent.</td><td>BL1</td></tr>
<tr><td>15.</td><td>What are the two types of asynchronous sequential circuits? (May 2016)
The two types of asynchronous sequential circuits are
1) Fundamental mode sequential circuit
2) Pulse mode sequential circuits.</td><td>BL2</td></tr>
<tr><td>16.</td><td>What is the difference between flow table and transition table?
Transition table is useful to analyze an asynchronous circuit from the circuit diagram. Flow table is similar to a transition table except the states are represented by letter symbols; it can also include the output values. Suitable to obtain the logic diagram from it. Flow table is similar to transition table, except that the internal states are symbolized with letters.</td><td>BL2</td></tr>
<tr><td>17.</td><td>What are state table and state diagram as applicable to sequential logic circuits? (Nov 2012)
The table which represents the relationship between present states and next states is called state table. State diagram is a pictorial representation of a behavior of a sequential circuit.</td><td>BL2</td></tr>
<tr><td>18.</td><td>What is PROM? (Nov2015, Apr2015)
PROM-Programmable Read Only Memory is a device that contains Fixed AND and Programmable OR functions. It contains fuses in act giving all 1`s in the stored bits and blown fuses by applying high voltage defining 0 states.</td><td>BL1</td></tr>
<tr><td>19.</td><td>What is static hazard and dynamic hazard, (Nov 2019, Nov 2021)
The different types of hazards are
(1)A static hazard in a logic network is a transient change of an output value which is supposed to remain fixed during the transition between two input states differing in the value of only one variable.</td><td>BL1</td></tr>
</table>

	(i) Static-1 Hazard: the output is currently 1 and after the inputs change, the output momentarily changes to 0 before settling on 1. **(ii) Static-0 Hazard:** the output is currently 0 and after the inputs change, the output momentarily changes to 1 before settling on 0. **(2) Dynamic hazard** is defined as a transient change which occurs three or more times at the output of logic circuit, when the output is supposed to change only once during the transient between two inputs which differ in the value of one variable.	
20.	**Determine the size of the PROM required for implementing a dual 8 to 1 multiplexer with common selection inputs logic circuits. (May 2021).** Dual with common selection so the number of inputs =8+8+3=19 The number of outputs= 2. Therefore, the size of the PROM =219×2=512K×2	**BL5**
21.	**Why PAL is developed? (Apr 2018)** The PAL is programmable logic device with a fixed OR array and a programmable AND array. Because only the AND gate are programmable, the PAL is easier to program, but is not as flexible as the PLA.	**BL2**
22.	**List the basic configuration of three PLD's. (Nov 2019)** The three basic configuration of PLD's are: i)PROM (Programmable Read Only Memory) ii)PLA (Programmable Logic Array) iii)PAL (Programmable Array Logic)	**BL1**
23.	**Define metastable state. (Apr 2019)** Whenever there are setup and hold time violations in any flip-flop, it enters a state where its output is unpredictable: this state is known as metastable state (quasi stable state); at the end of metastable state, the flip-flop settles down to either '1' or '0'.	**BL1**
24.	**State the difference between PROM, PLA and PAL. (May 16, Apr 17)** **PROM** / **PLA** / **PAL** PROM stands for Programmable read only memory / PLA stands for Programmable Logic Array / PAL stands for Programmable Array Logic One time programmable by user / Both AND and OR arrays are programmable / OR array is fixed and AND array is programmable Its content cannot be erased / Costlier and complex than PAL and PROM's / Cheaper and simpler	**BL2**
25.	**When dynamic hazard occurs in digital circuits? (Nov 2020, May 2021)** Dynamic hazard is defined as a transient change which occurs three or more times at the output of logic circuit, when the output is supposed to change only once during the transient between two inputs which differ in the value of one variable.	**BL2**

26.	**Sketch the block diagram of an asynchronous sequential circuit? (Nov 12, Nov 18)** 	**BL1**
27.	**Draw the structure of PAL. (Apr 2019)** 	**BL1**
	PART-B	
1.	(i)Give the design procedure for Mealy and Moore machine. (ii)Give the design Procedure for asynchronous sequential circuit.	**BL4**
2.	Design a gated latch circuit with two inputs, *G* (gate) and *D*(data), and one output *Q*. The gated latch is a memory element that accepts the value of *D* when *G*=1and retains this value after *G* goes to 0. Once *G*=0, a change in *D* does not change the value of the output *Q*.	**BL6**
3.	(i)What is PAL? (ii)Implement the Boolean function using PAL: $Y_1=\sum m(1,3,5,7)$& $Y_2=\sum m(2,4)$	**BL3**
4.	Explain the various types of hazards in sequential circuit design and the methods to eliminate them. Give suitable examples**. (Nov 2017, 2021, 2022)**	**BL4**
5.	Describe with reasons, the effect of races in asynchronous sequential circuit design. Explain its types with illustrations. Show the method of race-free state assignments with examples**.(Nov2019)**	**BL4**
6.	Consider the following asynchronous sequential circuit and draw maps and transition table and state table**. (May2013)** 	**BL4**
7.	(i)Sketch the transition table and state table for an asynchronous sequential circuit described by the following Boolean expressions:	**BL3**

	$Y_1=X_1X_2+X_1Y_2+X_2Y_1$, $Y_1=X_2+X_2Y_1Y_2+X_1Y_1$, $Z=X_2+Y_1$**(Nov2012)** (ii)Discuss the steps involved in the design of a synchronous sequential circuit with a suitable example.	
8.	Show how to program the fusible links to get a 4 bit gray code from the binary inputs using PLA and PAL and compare the design requirements with PROM. **(Nov 2015)**	**BL4**
9.	Design an asynchronous sequential circuit that has two inputs $X_2$and $X_1$and one output Z. The circuit is required to give an output whenever the input sequence (0,0),(0,1) and (1,1) received but only in that order**. (May 2016)**	**BL6**
10.	(i) What are static-0 and static-1 hazards? Explain the removal of hazards using hazard covers in k-map. (ii) Explain cycles and races in asynchronous sequential circuits**. (Nov 2018, 2019)**	**BL4**
11.	(i) What are transition table and flow table? Give suitable examples**.** (ii) Implement the following function using PLA and PAL:$F(X,Y,Z)=\sum m(0,1,3,5,7)$ **(May 2016, Apr 2017, Nov 2022)**	**BL3**
12.	(i) Implement the following function using PLA: $F(x,y,z)=\sum m(1,2,4,6)$ (ii)For the given Booleanfunction, obtain the hazard free circuit $F(A,B,C,D)=\sum m(1,3,6,7,13,15)$ **(Apr 2015, Apr 2017)**	**BL3**
13.	Design an asynchronous sequential circuit that has two inputs $X_2$and $X_1$and one output Z. When X_1=0, the output Z is 0. The first change in X_2 that occurs while $X_1$is 1 will cause output Z to be1.The output Z will remain1until X_1 returns to 0. **(Apr2015)**	**BL6**
14.	Write short notes on PLA and PAL. **(Nov 2017)**	**BL4**
15.	Explain the concept of PROM, EPROM and EEPROM in detail.**(Apr 2018)**	**BL4**
16.	Explain the concept of bipolar RAM cell with suitable diagram.**(Apr 2018)**	**BL4**
17.	Discuss the operation of SR latch with NOR and NAND gates analysis. **(Nov 2018)**	**BL4**
18.	Design an asynchronous sequential circuit that has two inputs $X_2$and $X_1$and one output Z. Initially both inputs are equal to zero. When X_1 or X_2 =1, the output Z is 1. When the second input also becomes 1 the output changes to 0.The output stays at 0 until the circuit goes back to the initial state **(Nov 2017)**	**BL6**
19.	Implement the functions $F_1(X, Y, Z)= \sum(1, 2, 4, 5)$, $F_3(X, Y, Z)= \sum(0, 1, 3,4)$ and $F_2(X, Y, Z)= \sum(2, 3, 6, 7)$ using a single PROM grid. **(Apr 2019)**	**BL3**
20.	(i) Differentiate PAL and PLA implementations with the help of the same example $F(a, b, c)= \sum(0, 1, 3, 4, 6, 7)$. (ii) Explain the structure of CPLD with the help of block diagram. **(Apr 2019)**	**BL4**
21.	i) What are complex programmable logic devices (CPLDs) ? Briefly outline salient features of these devices and application areas where these devices fit the best. (7) ii) Show that a BCD ripple counter can be constructed using a four-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010. (6) **(Nov 2020, May 2021)**.	**BL4**

	Part-C	
1.	i) Design a binary ripple counter that counts 000 and 111 and skips the remaining six states, that is 001, 010, 011, 100, 101 and 110. Use presentable, clearable negative edge-triggered J-K flip-flops with active LOW PRESET and CLEAR inputs. Also, draw the timing waveforms and determine the frequency of different flip-flop outputs for a given clock frequency, fc. (8) **(Nov 2020, May 2021).** ii) You have two two-bit binary numbers A1 A0 and B1B0. Design a PLAdevice to implement a magnitude comparator to produce outputs for A1 A0 being 'equal to', 'not equal to', 'less than' and 'greater than' B1B0. (5)	**BL6**
2.	Implement the following function using PLA and PAL :F1 (A,B,C)= Σm(3,5,6,7) and F2 (A,B,C)= Σm(0,4,2,7) **(Nov 2019)**	**BL3**
3.	Design a combinational circuit which accepts three bit number and outputs a binary number equal to the square of input number using PROM and PLDs**.(Nov 2021)**	**BL6**
4.	Design an asynchronous sequential circuit (with detailed steps involved) that has 2 inputs $x_1$and x_2 and one output z. The circuit is required to give an output z=1 when x_1=1, x_2=1 and x_1=1 being first.**(Nov 2015)**	**BL6**
5.	(i) Design a combinational circuit which accepts three bit number and outputs a binary number equal to the square of the input number using PROM. (ii) Implement the Boolean function using PLA:$F_1(A,B,C)=\sum(0,1,2,4)$, $F_2(A,B,C)=\sum(0,5,6,7)$.	**BL6**
	UNIT V-VHDL	
	PART A	
1.	**Write some of the Low Level Languages and High Level Languages?** Low Level Languages are as follows: ABEL, CUPL, PALASM High Level Languages are as follows: VHDL VERILOG	**BL1**
2.	**What are the different modeling techniques used to describe a module?** The different modeling techniques used to describe a module are Behavioral simulation, Functional simulation, Logic or gate level simulation, Switch level simulation, Transistor level simulation.	**BL1**
3.	**Define gate level simulation.** Gate level simulation can be also used to check the timing performance of an ASIC. In a gate level simulation a logic gate or logic cell is treated as a black box modeled by a function whose variable are single inputs. The functional so mode the delay through the logic cell setting all the delay value to unit value is the equivalent of functional simulation.	**BL1**
4.	**What is the purpose of VHDL programming?** **Or What is the need for VHDL? (May2013)** Very high speed integrated circuit hardware description language. It is a language for describing a hardware, which has to be readable for machines and humans at the same time & it structured and comprehensible code, so that the source code can serve as a kind of specification document. Thus it is used for studying digital logic circuits and testing its functions.	**BL2**

5.	**What is the use of repeat statement in Verilog HDL? (Nov/ Dec 2020: May 2021)** A repeat loop in Verilog will repeat a block of code for defined number of times. It is very similar to a for loop, except that a repeat loop's index can never be used inside the loop. Repeat loops just blindly run the code as many times as it is specified.	**BL2**
6.	**What are sequential and concurrent statements?** Sequential statements are executed one after other, like in software programming languages. The order of assignment must be considered when sequential statements are used. In VHDL, it is used in behavioral description of the design. Statements within the "process" unit are executed sequentially. Concurrent statements are active continuously. So the order of the statements is not relevant. Concurrent statements are especially suited model the parallelism of hardware. In VHDL, all statements except within "process" are executed concurrently.	**BL1**
7.	**What are the main components of a VHDL description?** The main components of VHDL descriptions are, 1. Package (optional) 2.Entity 3. Architecture 4. Configuration**.**	**. BL1**
8.	**What is entity in VHDL? (Nov 2021)** Entity gives the specification of input/output signals to external circuitry. It gives interfacing between device and the other peripherals. An entity usually has one or more ports, which are analogous to the pins on a schematic symbol. All information must flow into and out of the entity through the ports. Each port must contain name, data flow direction and type.	**BL1**
9.	**Give the syntax for VHDL entity declaration?** The syntax of a VHDL entity declaration is as shown below: Entity entity_name is Port(signal_names:mode signal_type; Signal_names:mode signal_type); end entityname;	**BL1**
10.	**Give the classification of data types supported by VHDL.** The VHDL data types can be broadly classified into following five data types: **Scalar types:** The scalar types include numeric data types and enumerated data types. The numeric types consist of integer, floating point (real) and physical types. Bit, Boolean and character are all enumerated types. **Composite types:** Array and record types are composite data types. The values of these types are collection of their elements**.** **Access types:** They are pointers, they provide access to objects of a given data type. **File type:** They provide access to object that contain a sequence of values of given type. **Other types:** They include the data types provided by the several external libraries.	**BL2**

11.	**What is architecture in VHDL?** Architecture specifies behavior, functionality, interconnections or relationship between inputs and outputs. It is the actual description of the design. An architecture consists of two portions: architecture declaration and architecture body.	**BL1**
12.	**List the internal details of an entity specified by architecture body.** An architecture body specifies following internal details of an entity: (i) As a set of concurrent assignment statements to represent data flow. (ii) As a set of interconnected components to represent structure. (iii) As a set of sequential assignment statement to represent behavior.	**BL1**
13.	**What is the use of configuration declaration?** Configuration declarations may associate particular design entities to component instances (unique references to lower level components) in a hierarical design or to associate a particular architecture to an entity.	**BL1**
14.	**Give the syntax for VHDL architecture declaration. (Nov 2022)** The syntax for architecture is given below: Architecture architecture_name of entity_name is Begin Concurrentstatements; Sequentialstatements; End architecture_name;	**BL1**
15.	**What is package declaration? (Nov 2022)** A package is a convenient mechanism to store and share some declarations that are common for various design units. A set of declarations contained in a package declaration maybe shared by many design units. It defines items that can be made visible to other design units.	**BL1**
16.	**What is subprogram?** A subprogram defines a sequential algorithm that performs particular task. Two types of subprograms are used in VHDL, **Functions** are used for computing single value and it executes in zero simulation time. **Procedures** are used to partition a large behavioral descriptions. Procedure returns zero or more values.	**BL1**
17.	**The 'module' is the basic building block of VHDL. What are the different modeling techniques used to describe a module? (Nov 2012)** The different modeling techniques used to describe a module are ➢ Structural modeling ➢ Dataflow modeling ➢ Behavioral modeling	**BL1**
18.	**Write behavioral model of D flipflop.(Nov 2015, Nov 2016, Apr 2015)** Library IEEE; use IEEE.STD_LOGIC_1164.all; use IEEE.STD_LOGIC_ARITH.ALL; use IEEE.STD_LOGIC_UNSIGNED.ALL; entity dff is Port(D,CLK:in STD_LOGIC; Qn:out STD_LOGIC); end dff;	**BL3**

	architecture Behavioral of dff is
	begin
	process(CLK)
	begin
	if (CLK' event and CLK='1') then
	if(D='0') then
	Qn<='0';
	else
	Qn<='1';
	end if ;
	end if ;
	end process ;
	end Behavioral;	

19.	**What is a package in VHDL?(Apr 2015)** A VHDL package contains subprograms, constant definitions, and/or type definitions to be used throughout one or more design units. Each package comprises a "declaration section", in which the available (i.e. exportable) subprograms, constants, and types are declared, and a "package body", in which the subprogram implementations are defined, along with any internally-used constants and types.	**BL1**
20.	**Write a VHDL code for 2:1MUX using Behavioral model (May 2016, Apr 2017, Nov 2021)** Library IEEE; use IEEE.STD_LOGIC_1164.all; entity mux2to1 is Port(I0 :in STD_LOGIC; I1: in STD_LOGIC; S: in STD_LOGIC; Y: out STD_LOGIC); end mux2to1; architecture Behavioral of mux2to1 is begin Y<=I0 when (S= '0') else I1; end Behavioral;	**BL3**
21.	**State the advantage of package declaration over component declaration.** Package declaration is used to declare components, types, constants, functions and so on.Declared Packages will be shared by many design units. Component declaration declares the name of the entity and interface of a component which is used by the design unit. Declared Component will be used by the corresponding design unit.	**BL2**
22.	**Write the VHDL code for a logical gate which gives output only when both the inputs are high. (Nov 2016)** The logical gate which gives output only when both the inputs are high is AND gate. The code is as follows, Library IEEE; use IEEE.STD_LOGIC_1164.all; entity and1 is port (a: in STD_LOGIC; b: in STD_LOGIC;	**BL3**

```
        Y : out STD_LOGIC);
    end and1;
    architecture gates of and1 is
    begin
    Y<=a and b;
    end gates;
```

23. **What is data modeling in VHDL? Give its basic mechanism. (May 2016)** **BL1**

A data flow model specifies the functionality of the entity without explicitly specifying its structure. The entity is not modelled as a set of components rather it represents sequential flow.

Example:

```
Library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity hadd is
port (a: in STD_LOGIC;
      b: in STD_LOGIC;
      sum : out STD_LOGIC;
      carry : out STD_LOGIC);
end hadd;
architecture dataflow of hadd is
begin
sum<= a XOR b;
carry<= a AND b;
end dataflow;
```

24. **Define Modularity. (Nov 2017)** **BL1**

Modularity allows the partitioning of big functional blocks into smaller units and to group closely related parts in self-contained subblocks, called modules.

25. **List out the logical operator present in VHDL.(Nov2015)** **BL1**

SYMBOL	OPERATION
^	Bitwise XOR
~	Bitwise NOT
&	Bitwise AND
|	Bitwise OR
&&	Logical AND
||	Logical OR
!	Logical NOT

26. **Give the Syntax for Package declaration and Package Body in VHDL. (Apr 2017)** **BL1**

Package Body Declaration:

Package body package_name is

Subprogram bodies

Complete constant declarations

Subprogram declarations

Type and subtype declarations

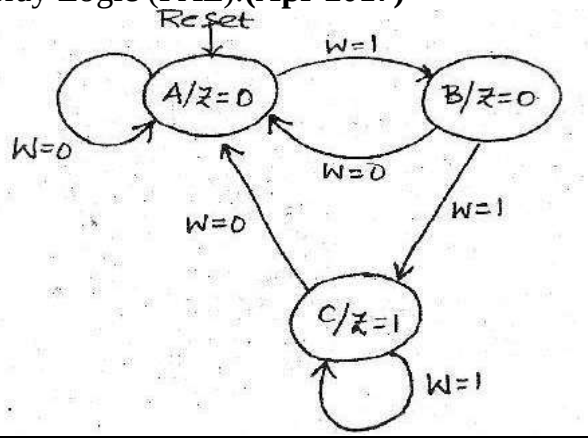
File and alias declarations

Use clauses

	End package_name Package Declaration: **package** package_name **is** package_declarations **endpackage** package_name;	
27.	**Infer the concept of switch level modeling.(Apr 2018)** In switch level modeling, a hardware component is described at the transistor level , but transistors only exhibit digital behavior and their input and output signal values are only limited to digital values. At the switch level transistors behave as on-off switch.	**BL2**
28.	**List the languages that are combined together to get VHDL language. (Nov 2019)** The languages that are combined together to get VHSL language are 1. Sequential language 2. Concurrent language 3. Net- List language 4. Waveform generation language	**BL2**
29.	**Explain the T Base and T Low predefined attributes (Nov 2019)** An attribute gives extra information about a specific part of a VHDL description. Predefined attributes can be constants, functions or signals. In the VHDL standard a set of predefined attributes is defined T'BASE is the base type of the type T T'LOW is the lowest value of type T.	**BL2**
30.	**State the purpose of Test bench. (Apr 2019)** Test Bench are mainly used for: i. Generating stimulus for simulation. ii. Applying the stimulus to the entity under test and to collect the output.Comparing obtained output with expected output.	**BL1**

31.	**Write a VHDL program for an EX-NOR gate using behavioral coding. (Apr 2019)**
	VHDL Program:
	library IEEE;
	Use IEEE.STD_LOGIC_1164.ALL;
	Use IEEE.STD_LOGIC_ARITH.ALL;
	Use IEEE.STD_LOGIC_UNSIGNED.ALL;
	entity xnorgate is
	Port(a,b: in std_logic; c: out std_logic);
	end xnorgate;
	architecture gates of xnorgate is
	begin
	process (a,b)
	begin
	if (a=’0’ and b=’0’) then
	y<=1;
	elsif (a=’0’ and b=’1’) then
	y<=’0’;
	elsif (a=’1’ and b=’0’) then
	y<=’0’;
	elsif (a=’1’ and b=’1’) then
		BL3

	y<='1'; end if; end process; end gates;	
	PART-B	
1.	(i)Briefly explain about the features of VHDL (ii)Write VHDL program for the half-adder circuit.	**BL4**
2.	Explain about the different types of architectural description. Write VHDL code for MUX using any two description type.	**BL4**
3.	Explain the digital system design flow sequence with the help of a flowchart. **(Nov 2014)**	**BL4**
4.	Compare VHDL code used to realize a full adder using behavioral modeling and structural modeling. **(Apr 2015, Nov 2016, 2017, 2021, 2022) (Part C)**	**BL4**
5.	Construct a VHDL program to implement SR latch and JK-flipflop using behavioral model**.(Nov 2017)**	**BL3**
6.	(i) Briefly discuss the use of Packages in VHDL. **(Nov 2012)** (ii)Write a VHDL code that implements an 8:1multiplexer.	**BL4**
7.	Test VHDL code for 4-bit binary counter with parallel load and explain.	**BL5**
8.	Construct VHDL code for JK master flip-flops and using JK flipflop as structural element, write code for 4 bit asynchronous counter.	**BL3**
9.	Explain test bench with suitable example.	**BL4**
10.	Explain in details the RTL design procedure.**(Nov 2015)**	**BL4**
11.	Write VHDL Program (i)1 to 4 DMUX 9. (ii) MOD 8 Counter **(Nov 2015, Nov 2021)**	**BL3**
12.	Write the VHDL code to realize 3-bit Gray code counter using case statement**. (Nov 2019)**	**BL3**
13.	(i) Write short notes on built in operators used in VHDL programming. (ii) Write VHDL coding for 4 × 1 MUX (**Nov 2016, Nov 2022)**	**BL4** **BL3**
14.	Discuss briefly the operators and packages in VHDL. **(Nov 2019)**	**BL4**
15.	(i)Explain functions and subprograms with suitable examples. (ii)Write the VHDL code to realize a 4 bit parallel binary adder with structural modeling and write the test bench to verify is functionality**.**	**BL4**
16.	(i) Write a VHDL code for a 4-bit universal shift register. **(Nov 2014)** (ii) Write HDL for four bit adder. **(Apr2013)**	**BL3**
17.	Create a VHDL code to realize a half adder using behavioral modeling and structural modeling. **(Nov 2018)**	**BL6**
18.	Draw the circuit of CMOS AND gate and explain it's operation. Also implement it using VHDL. **(Apr 2018)**	**BL4**
19.	(i) Draw the VLSI design flow chart used for IC design and fabrication. (ii) Write down a VHDL code for 8×1 Demultiplexer. **(Apr 2019)**	**BL3**
20.	(i) Illustrate the two approaches used in VHDL coding with full adder design as your example. (ii) What are components in VHDL? Show step-by-step how a NOR gate component can be created and added in the library. **(Apr 2019)**	**BL4**
21.	i) What is a hardware description language? What are the requirements of a good HDL? Briefly describe the salient features of VHDL and Verilog. **(8)** ii) Write the VHDL code for 4-bit adder circuit. **(5)**	**BL4**

22.	i) Explain in detail about ASMD chart for digital system design. **(5)** ii) Explain in detail about ASM block with an example. **(8)**	**BL4**
	Part C	
1.	Write the VHDL code for the given state diagram, using behavioral modeling. Design it using one-hot state assignment and implement it using Programmable Array Logic (PAL).**(Apr 2017)**  	**BL6**
2.	(i) Design a 3 bit magnitude comparator and write the VHDL code to realize it using structural model (ii) Design a 4×4 Array multiplier and write the VHDL code to realise it using structural model. **(Apr 2017)**	**BL6**
3.	Design a 4 bit code converter which converts given binary code into a code in which the adjacent number differs by only 1 by the preceding number. Also, develop VHDL coding for the above mentioned code converter**.(Nov 2016)**	**BL6**